

GPS LOW NOISE AMPLIFIER GaAs MMIC

■ GENERAL DESCRIPTION

NJG1130KA1 is a low noise amplifier GaAs MMIC designed for GPS application at the 1.575GHz. The LNA offers excellent low noise figure, high linearity and low current consumption.

Two stage amplifier and ESD protection circuit are integrated in the IC to achieve very high gain and high ESD tolerance.

An ultra-small and ultra-thin package of FLP6-A1 is adopted.

■ PACKAGE OUTLINE

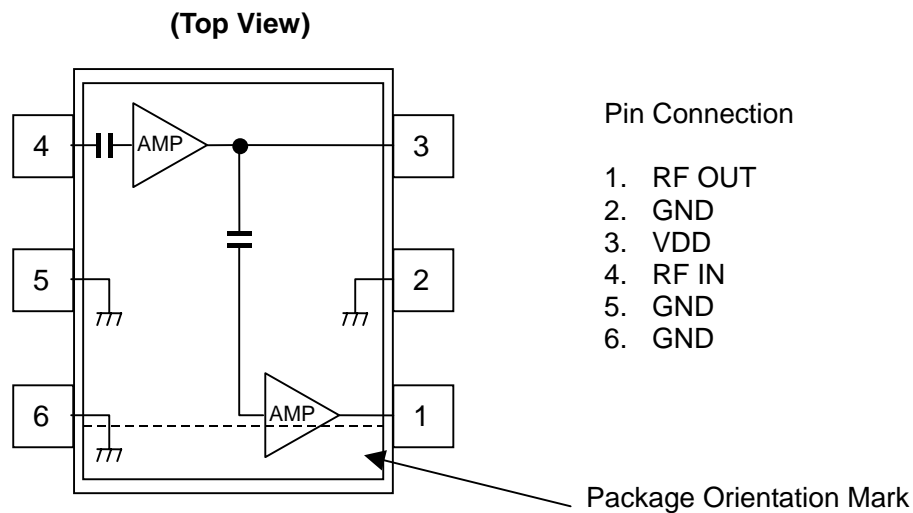


NJG1130KA1

■ FEATURES

- | | |
|-------------------------------------|---|
| ● Low voltage operation | +2.85V typ. |
| ● Low current consumption | 5.0mA typ. |
| ● High gain | 29.0dB typ. @ f=1.575GHz |
| ● Low noise figure | 0.65dB typ. @ f=1.575GHz |
| ● 1dB gain compression output power | +11.0dBm typ. @ f=1.575GHz |
| ● High output IP3 | +14dBm typ. @ f=1.575+1.5751GHz, Pin=-35dBm |
| ● Ultra-small & ultra-thin package | FLP6-A1 (Package size: 1.6x1.6x0.6mm) |

■ PIN CONFIGURATION



Note: Specifications and description listed in this datasheet are subject to change without notice.

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■ ABSOLUTE MAXIMUM RATINGS

$T_a=+25^{\circ}\text{C}$, $Z_s=Z_l=50\text{ohm}$

PARAMETERS	SYMBOL	CONDITIONS	RATINGS	UNITS
Drain Voltage	V_{DD}		5.0	V
Input power	P_{in}	$V_{DD}=2.85\text{V}$	+15	dBm
Power dissipation	P_D	on PCB board, at $T_{jmax}=150^{\circ}\text{C}$	170	mW
Operating temperature	T_{opr}		-40~+85	$^{\circ}\text{C}$
Storage temperature	T_{stg}		-55~+150	$^{\circ}\text{C}$

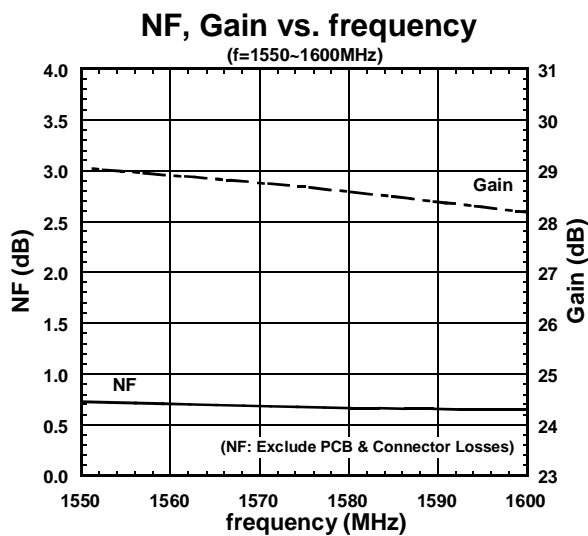
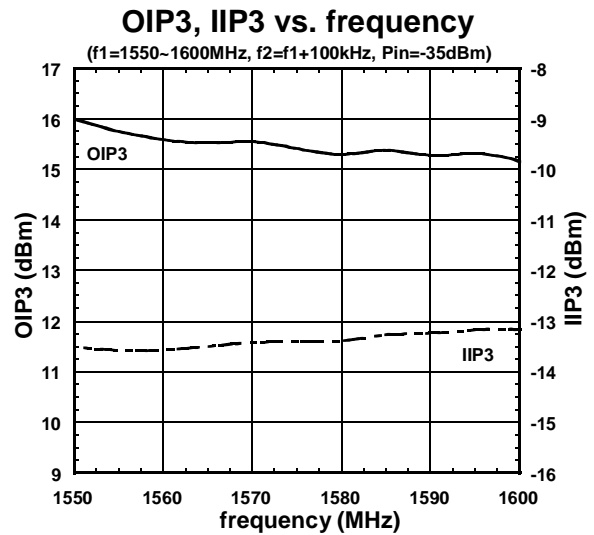
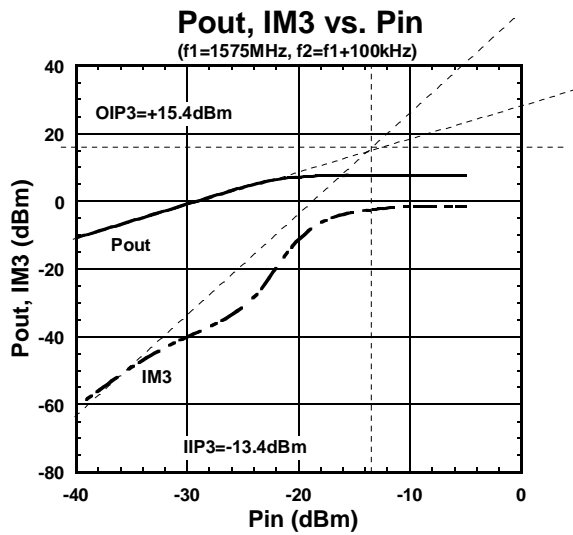
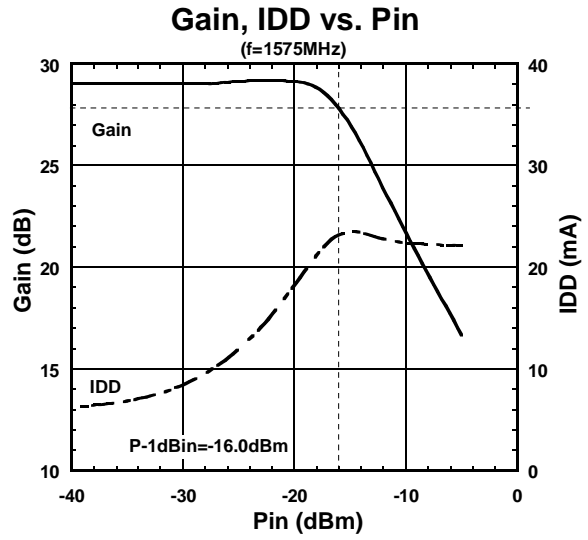
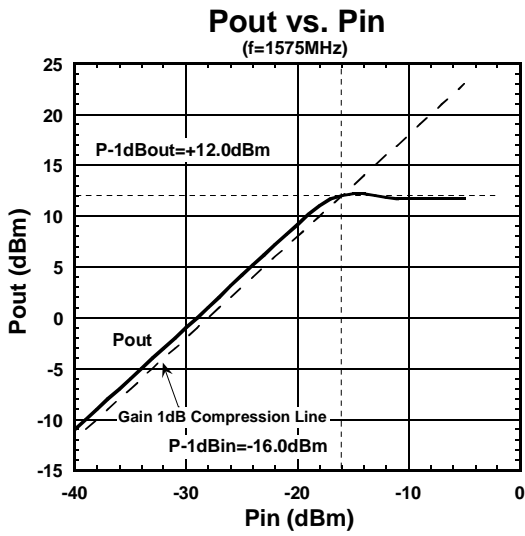
■ ELECTRICAL CHARACTERISTICS

GENERAL CONDITIONS: $V_{DD}=2.85\text{V}$, $\text{freq}=1.575\text{GHz}$, $T_a=+25^{\circ}\text{C}$, $Z_s=Z_l=50\text{ohm}$, with application circuit

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating voltage	V_{DD}		2.5	2.85	3.3	V
Operating current	I_{DD}	RF OFF	-	5.0	8.5	mA
Small signal gain	Gain		26.0	29.0	31.5	dB
Noise figure	NF	Exclude PCB & connector losses (0.10dB)	-	0.65	0.95	dB
1dB gain compression output power	$P_{-1\text{dB}(\text{out})}$		+5.0	+11.0	-	dBm
3rd order output intercept point	OIP3	$f=1.575+1.5751\text{GHz}$, $P_{in}=-35\text{dBm}$	+7.0	+14.0	-	dBm
RF IN VSWR	VSWR _i		-	2.4	2.8	
RF OUT VSWR	VSWR _o		-	1.6	2.0	

ELECTRICAL CHARACTERISTICS

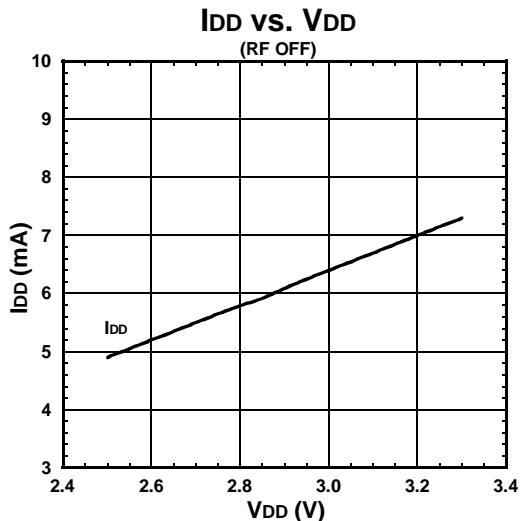
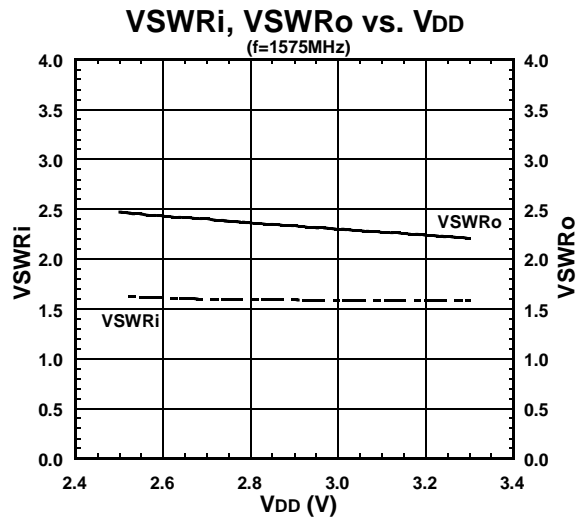
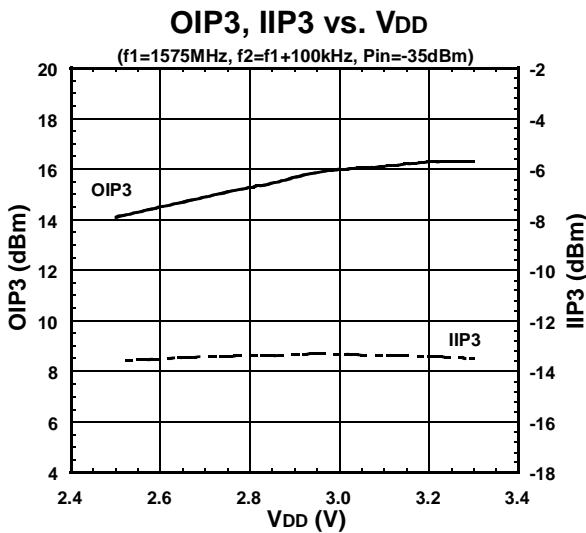
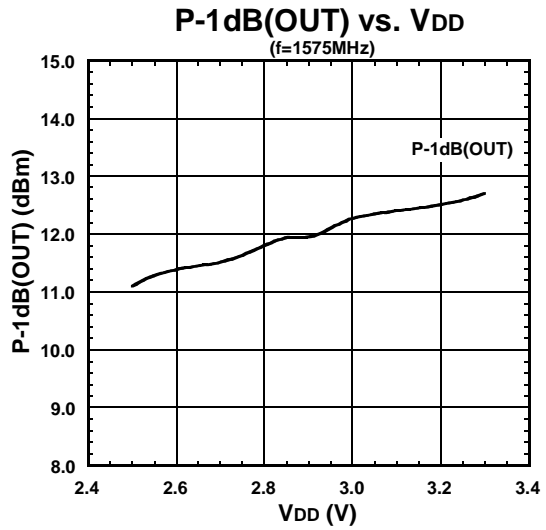
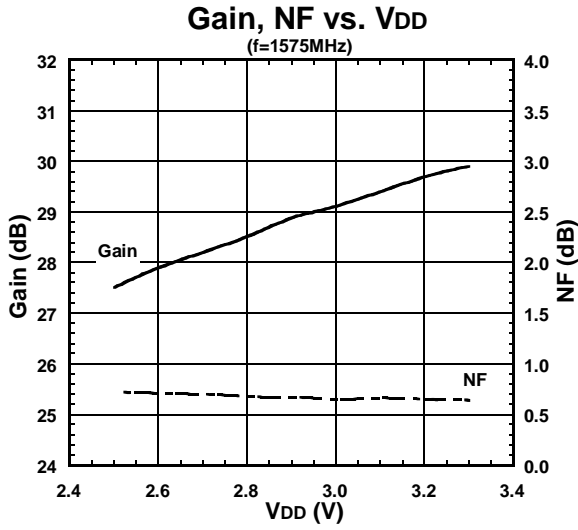
(Condition : $T_a=+25^\circ\text{C}$, $V_{DD}=2.85\text{V}$, $Z_s=Z_l=50\text{ohm}$ with application circuit)



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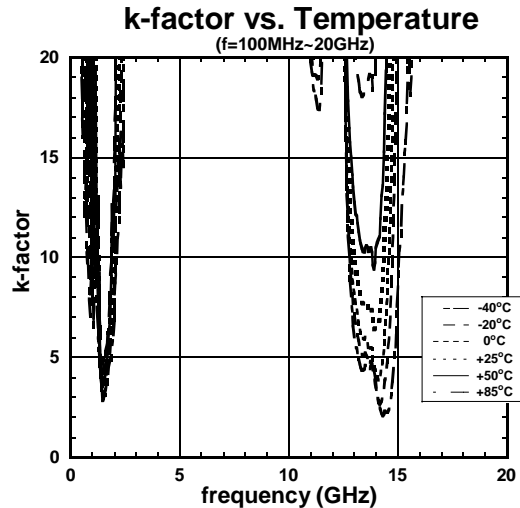
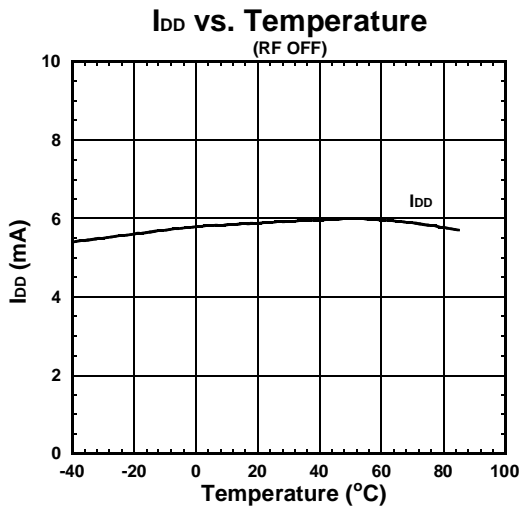
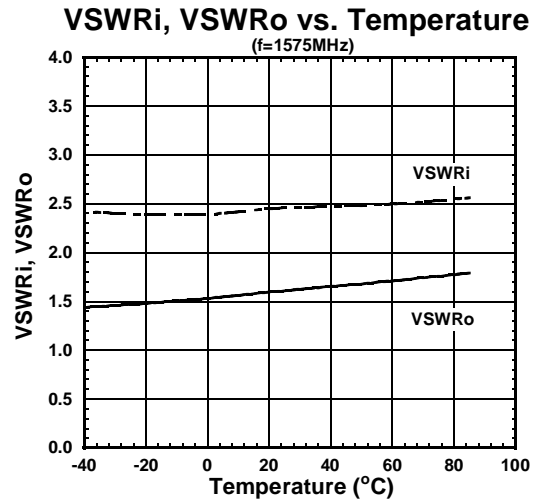
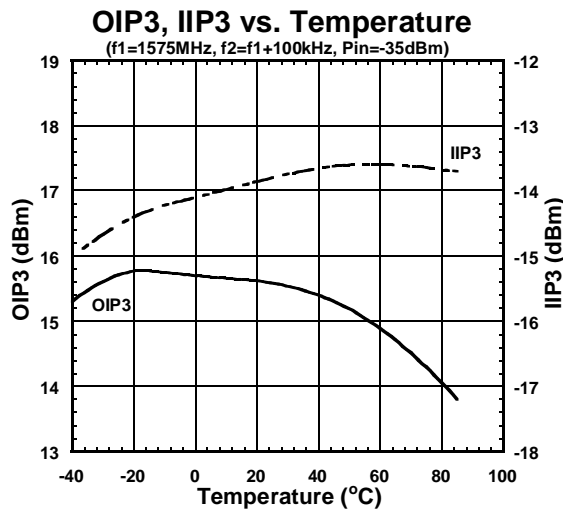
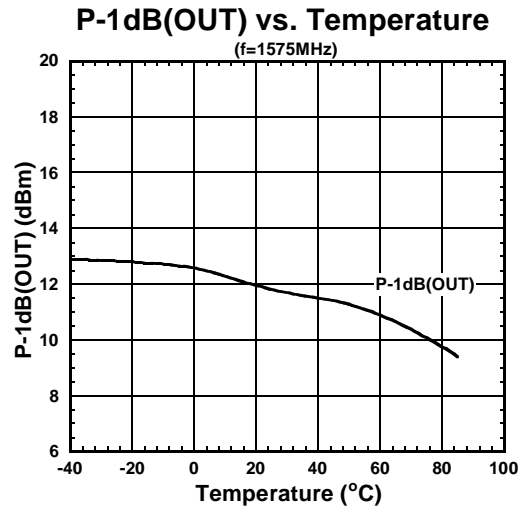
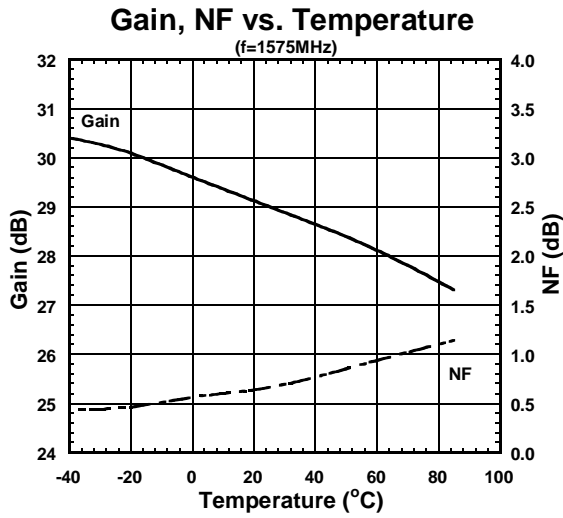
ELECTRICAL CHARACTERISTICS

(Condition : Ta=+25°C, Zs=Zl=50ohm with application circuit)



ELECTRICAL CHARACTERISTICS

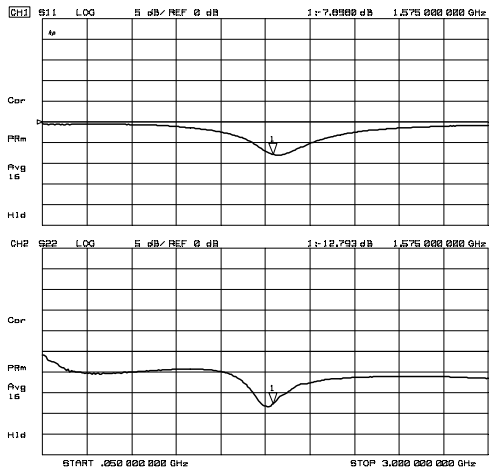
(Condition : $V_{DD}=2.85V, Z_s=Z_l=50\text{ohm}$ with application circuit)



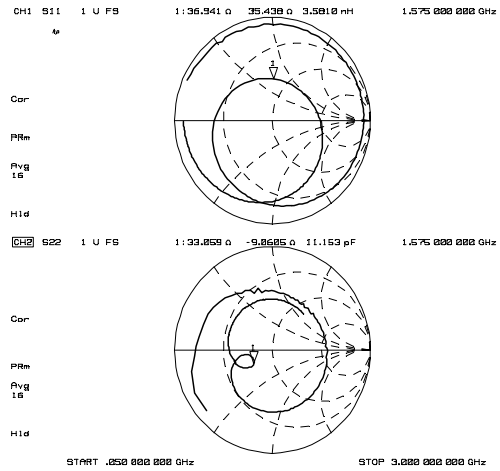
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ELECTRICAL CHARACTERISTICS

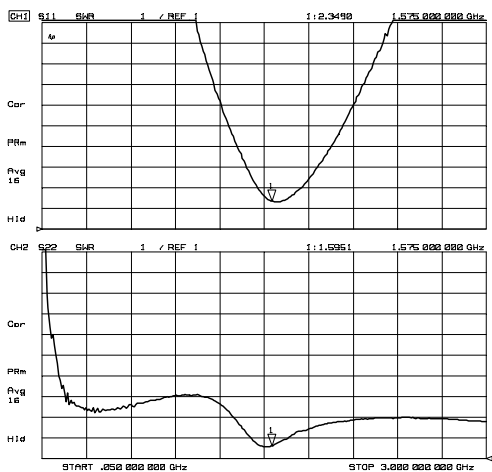
(Condition : $T_a=+25^{\circ}\text{C}$, $V_{DD}=2.85\text{V}$, $Z_S=Z_L=50\text{ohm}$ with application circuit)



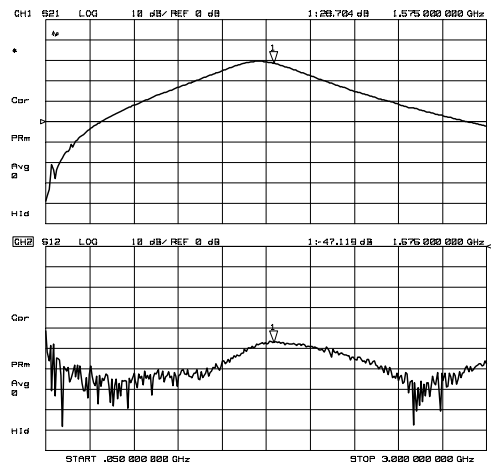
S11, S22



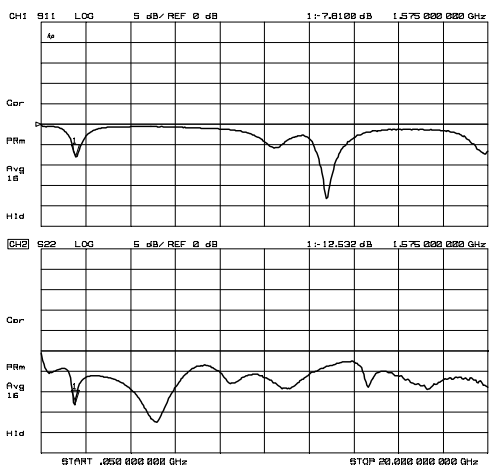
Zin, Zout



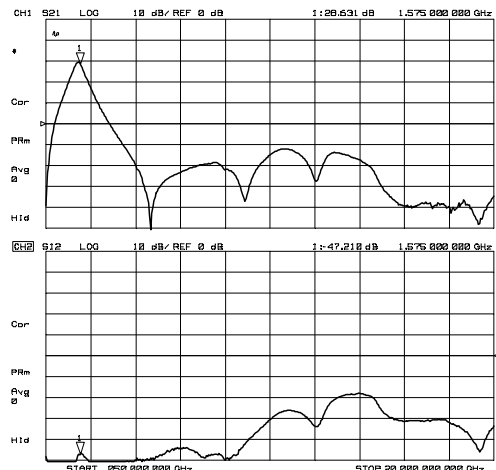
VSWR



S21, S12

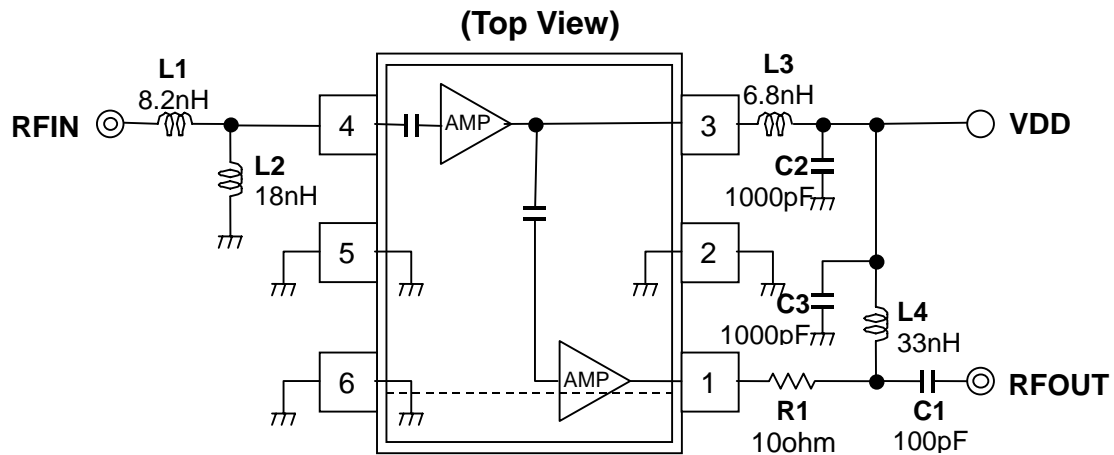


S11, S22 (~20GHz)



S21, S12 (~20GHz)

APPLICATION CIRCUIT



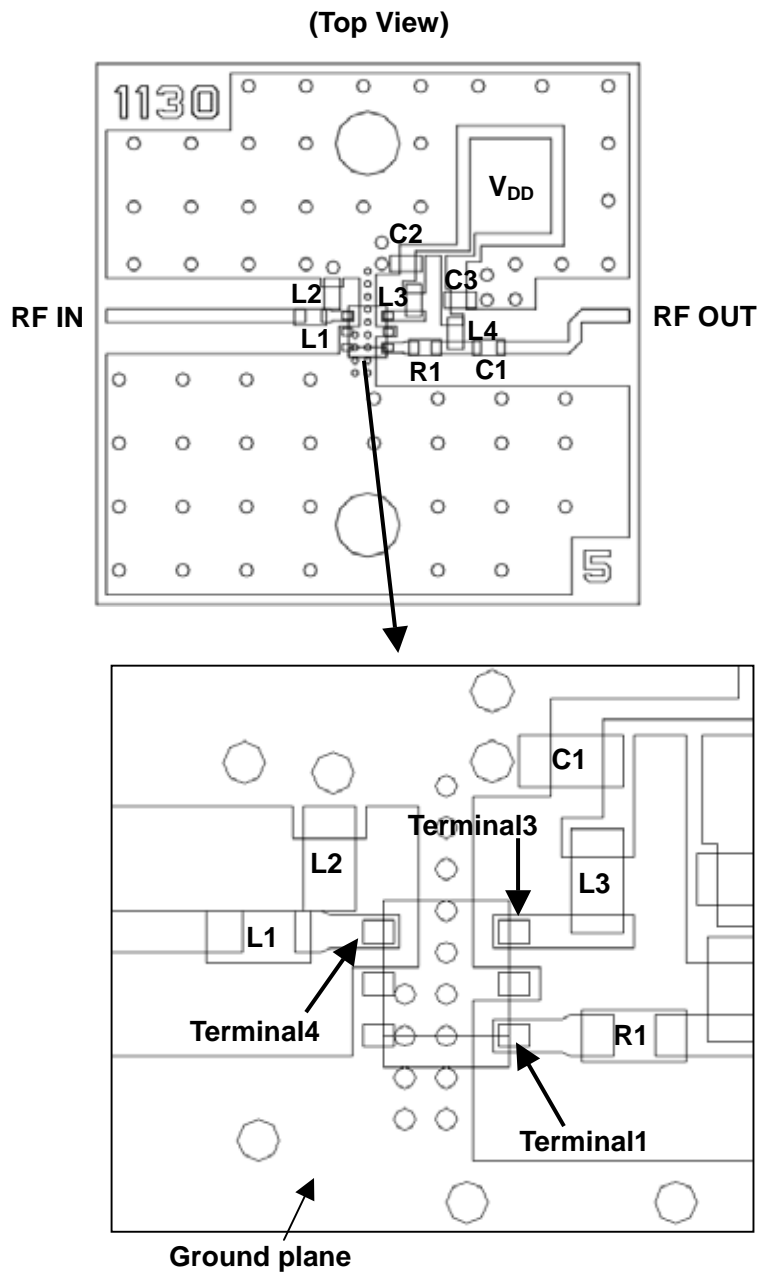
NOTES:

- L1 and L2 form the input matching circuit. The LNA has integrated coupling and DC-blocking capacitor at the input.
- L3 is a matching inductor of the integrated 1st amplifier and 2nd amplifier. It should be connected to the terminal3 as close as possible.
- L4 is an output matching inductor.
- C1 is a coupling and DC-blocking capacitor at the output.
- C2 and C3 are bypass capacitors. They should be connected between L3 and L4. C2 should be placed to the side of L3, and C3 should be placed to the side of L4, and should not be directly connected L3 and L4.
- R1 is a stability resistor at high frequency, and it should be connected to the terminal1.
- Ground terminal (No.2, 5, 6) should be connected to the ground plane as close as possible for good RF performance.
- For good performance, the terminal1,3 and 4 should not be coupled though floating-capacitance which exists between RF transmission lines.

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■ TEST PCB LAYOUT

■ Parts List



Parts ID	Comment
L1~L4	TAIYO-YUDEN HK1005 Series
C1~C3	MURATA GRM15 Series
R1	1005 Size

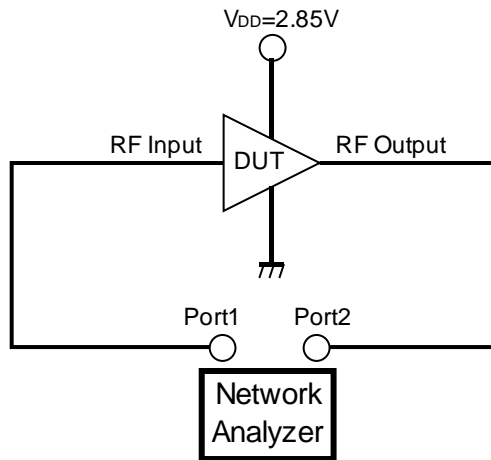
PCB (FR-4) :
 $t=0.2\text{mm}$
 MICROSTRIP LINE WIDTH
 $=0.4\text{mm}$ ($Z_0=50\Omega$)
 PCB SIZE
 $=17.0\text{mm} \times 17.0\text{mm}$

PRECAUTION:

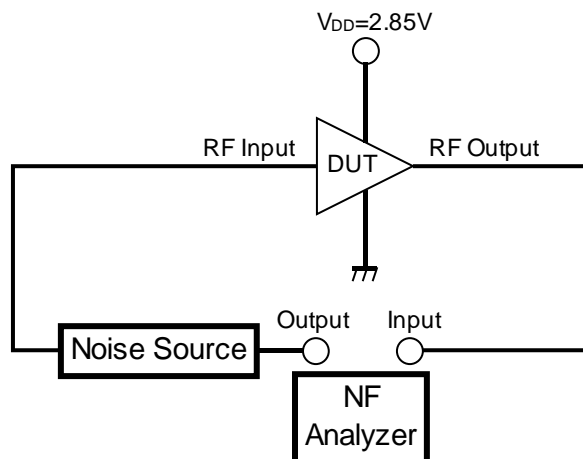
- [1] For good performance, the terminal1, 3 and 4 should not be coupled though floating-capacitance which exists between RF transmission lines.
- [2] In order not to couple with terminal 1, 3 and 4, please layout ground pattern under the IC.
- [3] C2 should be placed to the side of L3, and C3 should be placed the side of L4. They should be connect between L3 and L4, should not be directly connected L3 and L4.

TEST CIRCUITS

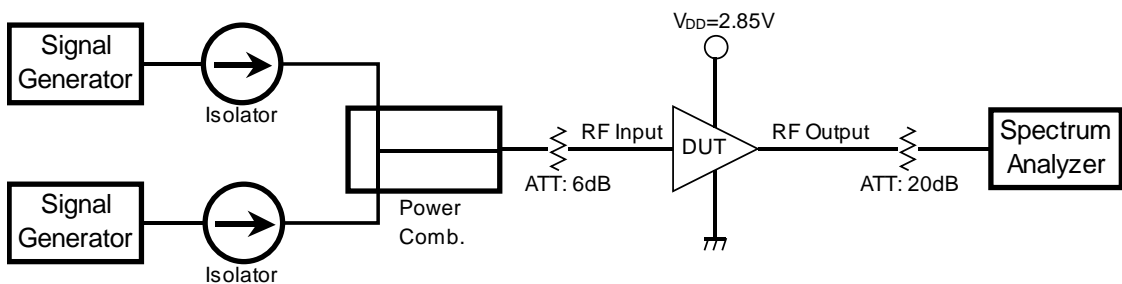
Test Circuits 1 to 3 define the test conditions used in the product electrical characteristics table.



Test Circuit 1. S-Parameter



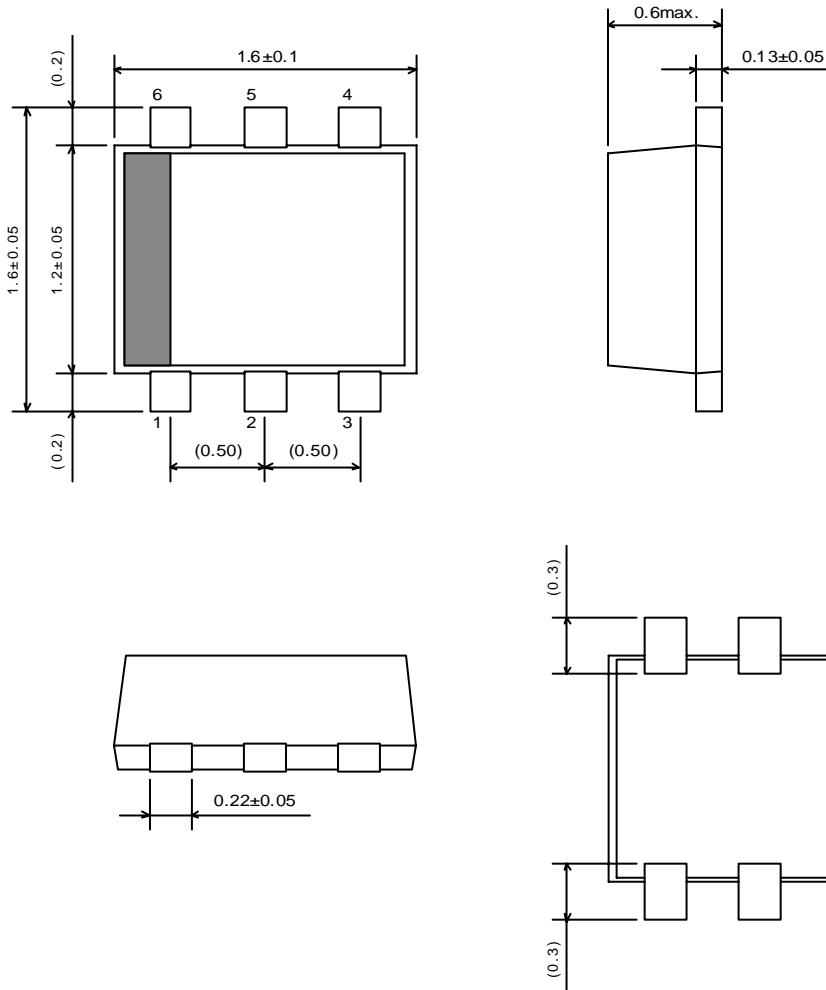
Test Circuit 2. NF



Test Circuit 3. Third order output intercept point

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■ PACKAGE OUTLINE (FLP6-A1)



UNIT: mm

Cautions on using this product

This product contains Gallium-Arsenide (GaAs) which is a harmful material.

- Do NOT eat or put into mouth.
- Do NOT dispose in fire or break up this product.
- Do NOT chemically make gas or powder with this product.
- To waste this product, please obey the relating law of your country.

[CAUTION]

The specifications on this databook are only given for information, without any guarantee as regards either mistakes or omissions. The application circuits in this databook are described only to show representative usages of the product and not intended for the guarantee or permission of any right including the industrial rights.

This product may be damaged with electric static discharge (ESD) or spike voltage. Please handle with care to avoid these damages.

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- Техническую поддержку проекта.
- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.



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