# ISL84051, ISL84052, ISL84053

Low Voltage, Single and Dual Supply, 8-to-1 Multiplexer, Dual 4-to-1 Multiplexer and a Triple SPDT Analog Switch

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The Intersil ISL84051, ISL84052, ISL84053 devices are precision, bidirectional, analog switches configured as a 8-Channel multiplexer/demultiplexer (ISL84051), a dual differential 4-Channel multiplexer/demultiplexer (ISL84052) and a triple single pole/double throw (SPDT) switch (ISL84053) designed to operate from a single +2V to +12V supply or from a ±2V to ±6V supply. All devices have an inhibit pin to simultaneously open all signal paths.

ON-resistance is 60Ω with a ±5V supply and 125Ω with a single +5V supply. Each switch can handle rail to rail analog signals. The off-leakage current is only 5nA at +85°C with a ±5V supply.

All digital inputs have 0.8V to 2.4V logic thresholds, ensuring TTL/CMOS logic compatibility when using a single +3.3V and +5V supply or dual ±5V supplies.

The ISL84051 is a 8-to-1 multiplexer device. The ISL84052 is a dual 4-to-1 multiplexer device. The ISL84053 is a committed triple SPDT, which is perfect for use in 2-to-1 multiplexer applications.

Table 1 summarizes the performance of this family.

**TABLE 1. FEATURES AT A GLANCE**

| | ISL84051 | ISL84052 | ISL84053 |
|---|---|---|---|
| CONFIGURATION | 8:1 Mux | DUAL 4:1 Mux | TRIPLE SPDT |
| ±5V $r_{ON}$ | 60Ω | 60Ω | 60Ω |
| ±5V $t_{ON}/t_{OFF}$ | 50ns/40ns | 50ns/40ns | 50ns/40ns |
| 5V $r_{ON}$ | 125Ω | 125Ω | 125Ω |
| 5V $t_{ON}/t_{OFF}$ | 90ns/60ns | 90ns/60ns | 90ns/60ns |
| 3V $r_{ON}$ | 250Ω | 250Ω | 250Ω |
| 3V $t_{ON}/t_{OFF}$ | 180ns/100ns | 180ns/100ns | 180ns/100ns |
| Packages | 16 Ld SOIC | 16 Ld SOIC | 16 Ld SOIC |
| | 16 Ld QSOP | 16 Ld QSOP | 16 Ld QSOP |
| | 16 Ld TSSOP | 16 Ld TSSOP | 16 Ld TSSOP |

## Related Literature

- Technical Brief TB363 “Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)”
- Application Note AN557 “Recommended Test Procedures for Analog Switches”

## Features

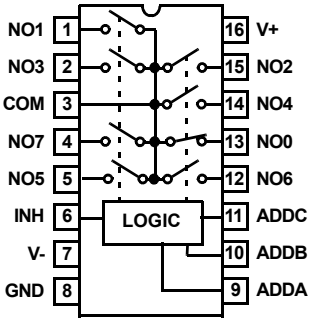
- Drop-in Replacements for MAX4051/MAX4051A, MAX4052/MAX4052A and MAX4053/MAX4053A
- Pin Compatible with MAX4581, MAX4582, MAX4583 and with Industry Standard 74HC4051, 74HC4052 and 74HC4053
- ON-Resistance ($r_{ON}$) Max, $V_S$ = ±5V . . . . . 100Ω
- ON-Resistance ($r_{ON}$) Max, $V_S$ = +5V . . . . . 225Ω
- $r_{ON}$ Matching Between Channels . . . . . <6Ω
- Low Charge Injection . . . . . 2pC
- Single Supply Operation . . . . . +2V to +12V
- Dual Supply Operation . . . . . ±2V to ±6
- Fast Switching Action ($V_S$ = +5V)
  - $t_{ON}$ . . . . . 90ns
  - $t_{OFF}$ . . . . . 60ns
- Guaranteed Max Off-leakage @ $V_S$ = ±5V . . . . . 5nA
- Break-Before-Make
- TTL, CMOS Compatible
- Pb-Free Available (RoHS Compliant)

## Applications

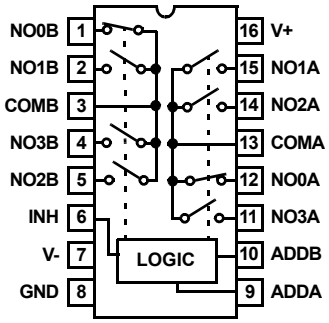
- Portable Equipment
- Communications Systems
  - Radios
  - Telecom Infrastructure
  - ADSL, VDSL Modems
- Test Equipment
  - Medical Ultrasound
  - Magnetic Resonance Image
  - CT and PET Scanners (MRI)
  - ATE
  - Electrocardiograph
- Audio and Video Signal Routing
- Various Circuits
  - +3V/+5V DACs and ADCs
  - Sample and Hold Circuits
  - Operational Amplifier Gain Switching Networks
  - High Frequency Analog Switching
  - High Speed Multiplexing
  - Integrator Reset Circuits

# Pin Configurations

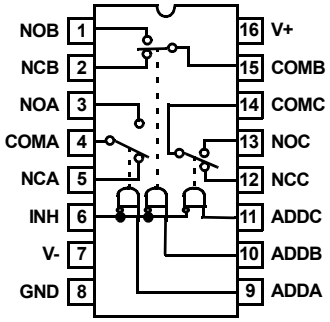
ISL84051
(16 LD SOIC, QSOP, TSSOP)
TOP VIEW




ISL84052
(16 LD SOIC, QSOP, TSSOP)
TOP VIEW




ISL84053
(16 LD SOIC, QSOP, TSSOP)
TOP VIEW




NOTE:

1. Switches Shown for Logic “0” Inputs.

# Pin Description

| PIN NAME | PIN NUMBER | | | FUNCTION |
|---|---|---|---|---|
| | ISL84051 | ISL84052 | ISL84053 | |
| V+ | 16 | 16 | 16 | Positive Power Supply Input |
| V- | 7 | 7 | 7 | Negative Power Supply Input. Connect to GND for Single Supply Configurations. |
| GND | 8 | 8 | 8 | Ground Connection |
| INH | 6 | 6 | 6 | Digital Control Input. Connect to GND for Normal Operation. Connect to V+ to turn all switches off. |
| COM | 3 | - | - | Analog Switch Common Pin |
| COMA | - | 13 | 4 | |
| COMB | - | 3 | 15 | |
| COMC | - | - | 14 | |
| NO1, NO3, NO7, NO5, NO6, NO4, NO2 | 1, 2, 4, 5, 12, 14, 15 | - | - | Analog Switch Normally Open Pin |

## Pin Description (Continued)

| PIN NAME | PIN NUMBER | | | FUNCTION |
|---|---|---|---|---|
| | ISL84051 | ISL84052 | ISL84053 | |
| N00B, N01B, N03B, N02B, N03A, N00A, N02A, N01A | - | 1, 2, 4, 5, 11, 12, 14, 15 | - | Analog Switch Normally Open Pin |
| N0B, N0A, N0C | - | - | 1, 3, 13 | |
| NCB, NCA, NCC | - | - | 2, 5, 12 | Analog Switch Normally Closed Pin |
| ADDA, ADDB, ADDC | 9, 10 11 | 9, 10 - | 9, 10 11 | Address Input Pin |

## Ordering Information

| PART NUMBER | PART MARKING | TEMP. RANGE (°C) | PACKAGE (Pb-free) | PKG. DWG. # |
|---|---|---|---|---|
| ISL84051IAZ | 84051 IAZ | -40 to +85 | 16 Ld QSOP | M16.15A |
| ISL84051IBZ | 84051IBZ | -40 to +85 | 16 Ld SOIC | M16.15 |
| ISL84051IVZ | 84051 IVZ | -40 to +85 | 16 Ld TSSOP | M16.173 |
| ISL84052IAZ | 84052 IAZ | -40 to +85 | 16 Ld QSOP | M16.15A |
| ISL84052IBZ | 84052IBZ | -40 to +85 | 16 Ld SOIC | M16.15 |
| ISL84052IVZ | 84052 IVZ | -40 to +85 | 16 Ld TSSOP | M16.173 |
| ISL84053IAZ | 84053 IAZ | -40 to +85 | 16 Ld QSOP | M16.15A |
| ISL84053IBZ | 84053IBZ | -40 to +85 | 16 Ld SOIC | M16.15 |
| ISL84053IVZ | 84053 IVZ | -40 to +85 | 16 Ld TSSOP | M16.173 |

NOTES:

2. Add “-T*” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
3. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020
4. For Moisture Sensitivity Level (MSL), please see device information page for ISL84051, ISL84052, ISL84053. For more information on MSL please see techbrief TB363.

# Truth Tables

**ISL84051**

| INH | ADDC | ADDB | ADDA | SWITCH ON |
|---|---|---|---|---|
| 1 | X | X | X | None |
| 0 | 0 | 0 | 0 | NO0 |
| 0 | 0 | 0 | 1 | NO1 |
| 0 | 0 | 1 | 0 | NO2 |
| 0 | 0 | 1 | 1 | NO3 |
| 0 | 1 | 0 | 0 | NO4 |
| 0 | 1 | 0 | 1 | NO5 |
| 0 | 1 | 1 | 0 | NO6 |
| 0 | 1 | 1 | 1 | NO7 |

**ISL84052**

| INH | ADDB | ADDA | SWITCH ON |
|---|---|---|---|
| 1 | X | X | None |
| 0 | 0 | 0 | NO0 |
| 0 | 0 | 1 | NO1 |
| 0 | 1 | 0 | NO2 |
| 0 | 1 | 1 | NO3 |

**ISL84053**

| INH | $ADD_C$ | $ADD_B$ | $ADD_A$ | SWITCH ON |
|---|---|---|---|---|
| 1 | X | X | X | None |
| 0 | X | X | 0 | $NC_A$ |
| 0 | X | X | 1 | $NO_A$ |
| 0 | X | 0 | X | $NC_B$ |
| 0 | X | 1 | X | $NO_B$ |
| 0 | 0 | X | X | $NC_C$ |
| 0 | 1 | X | X | $NO_C$ |

NOTE: Logic “0” ≤0.8V. Logic “1” ≥2.4V, with V+ between 2.7V and 10V. X = Don’t Care.

## Absolute Maximum Ratings

V+ to V- . . . . . -0.3V to 15V
V+ to GND . . . . . -0.3V to 15V
V- to GND . . . . . -15V to 0.3V
Input Voltages
INH, NO, NC, ADD (Note 5) . . . . . ((V-) - 0.3) to ((V+) + 0.3V)
Output Voltages
COM (Note 5) . . . . . ((V-) - 0.3) to ((V+) + 0.3V)
Continuous Current (Any Terminal) . . . . . ±30mA
Peak Current NO, NC, or COM
(Pulsed 1ms, 10% Duty Cycle, Max) . . . . . ±100mA
ESD Rating
Human Body Model (Per MIL-STD-883, Method 3015.7) . . . . . >2kV

## Thermal Information

| Thermal Resistance (Typical, Notes 6, 7) | $\theta_{JA}$ (°C/W) | $\theta_{JC}$ (°C/W) |
|---|---|---|
| 16 Ld SOIC Package | 75 | 39 |
| 16 Ld QSOP Package | 95 | 56 |
| 16 Ld TSSOP Package | 110 | 33 |

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

## Operating Conditions

Temperature Range . . . . . -40°C to +85°C

*CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.*

NOTES:

5. Signals on NC, NO, COM, ADD, or INH exceeding V+ or V- are clamped by internal diodes. Limit forward diode current to maximum current ratings.
6. $\theta_{JA}$ is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
7. For $\theta_{JC}$, the "case temp" location is taken at the package top center.

## Electrical Specifications 5V Supply

Test Conditions: $V_{SUPPLY}$ = ±4.5V to ±5.5V, GND = 0V, $V_{INH}$ = 2.4V, $V_{INL}$ = 0.8V (Note 8), Unless Otherwise Specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

| PARAMETER | TEST CONDITIONS | TEMP (°C) | MIN (Notes 9, 10) | TYP | MAX (Notes 9, 10) | UNITS |
|---|---|---|---|---|---|---|
| **ANALOG SWITCH CHARACTERISTICS** | | | | | | |
| Analog Signal Range, $V_{ANALOG}$ | | Full | **V-** | - | **V+** | V |
| ON-Resistance, $r_{ON}$ | $V_S$ = ±5V, $I_{COM}$ = 1mA, $V_{NO}$ or $V_{NC}$ = ±3V (see Figure 5) | +25 | - | 60 | 100 | Ω |
| | | Full | - | - | **125** | Ω |
| $r_{ON}$ Matching Between Channels, $\Delta r_{ON}$ | $V_S$ = ±5V, $I_{COM}$ = 1mA, $V_{NO}$ or $V_{NC}$ = ±3V (Note 11) | +25 | - | - | 6 | Ω |
| | | Full | - | - | **12** | Ω |
| $r_{ON}$ Flatness, $r_{FLAT(ON)}$ | $V_S$ = ±5V, $I_{COM}$ = 1mA, $V_{NO}$ or $V_{NC}$ = ±3V, 0V (Note 12) | +25 | - | - | 10 | Ω |
| | | Full | - | - | **15** | Ω |
| NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$ | $V_S$ = ±5.5V, $V_{COM}$ = ±4.5V, $V_{NO}$ or $V_{NC}$ = ±4.5V (Note 12) | +25 | - | 0.002 | - | nA |
| | | Full | **-5** | - | **5** | nA |
| COM OFF Leakage Current, $I_{COM(OFF)}$, (ISL84051) | $V_S$ = ±5.5V, $V_{COM}$ = ±4.5V, $V_{NO}$ or $V_{NC}$ = ±4.5V (Note 12) | +25 | - | 0.002 | - | nA |
| | | Full | **-5** | - | **5** | nA |
| COM OFF Leakage Current, $I_{COM(OFF)}$, (ISL84052, ISL84053) | $V_S$ = ±5.5V, $V_{COM}$ = ±4.5V, $V_{NO}$ or $V_{NC}$ = ±4.5V (Note 12) | +25 | - | 0.002 | - | nA |
| | | Full | **-2.5** | - | **2.5** | nA |
| COM ON Leakage Current, $I_{COM(ON)}$, (ISL84051) | $V_S$ = ±5.5V, $V_{COM}$ = $V_{NO}$ or $V_{NC}$ = ±4.5V (Note 12) | +25 | - | 0.002 | - | nA |
| | | Full | **-5** | - | **5** | nA |
| COM ON Leakage Current, $I_{COM(ON)}$, (ISL84052, ISL84053) | $V_S$ = ±5.5V, $V_{COM}$ = $V_{NO}$ or $V_{NC}$ = ±4.5V (Note 12) | +25 | - | 0.002 | - | nA |
| | | Full | **-2.5** | - | **2.5** | nA |
| **DIGITAL INPUT CHARACTERISTICS** | | | | | | |
| Input Voltage High, $V_{INH}$, $V_{ADDH}$ | | Full | **2.4** | - | - | V |
| Input Voltage Low, $V_{INL}$, $V_{ADDL}$ | | Full | - | - | **0.8** | V |
| Input Current, $I_{INH}$, $I_{INL}$, $I_{ADDH}$, $I_{ADDL}$ | $V_S$ = ±5.5V, $V_{INH}$, $V_{ADD}$ = 0V or V+ | Full | **-1** | 0.03 | 1 | µA |

## Electrical Specifications 5V Supply

Test Conditions: $V_{SUPPLY}$ = ±4.5V to ±5.5V, GND = 0V, $V_{INH}$ = 2.4V, $V_{INL}$ = 0.8V (Note 8), Unless Otherwise Specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

| PARAMETER | TEST CONDITIONS | | TEMP (°C) | MIN (Notes 9, 10) | TYP | MAX (Notes 9, 10) | UNITS |
|---|---|---|---|---|---|---|---|
| **DYNAMIC CHARACTERISTICS** | | | | | | | |
| Inhibit Turn-ON Time, $t_{ON}$ | $V_S$ = ±4.5V, $V_{NO}$ or $V_{NC}$ = ±3V, $R_L$ = 300Ω, $C_L$ = 35pF, $V_{IN}$ = 0V to 3V (see Figure 1) | | +25 | - | 50 | - | ns |
| | | | Full | - | 60 | - | ns |
| Inhibit Turn-OFF Time, $t_{OFF}$ | $V_S$ = ±4.5V, $V_{NO}$ or $V_{NC}$ = ±3V, $R_L$ = 300Ω, $C_L$ = 35pF, $V_{IN}$ = 0V to 3V (see Figure 1) | | +25 | - | 40 | - | ns |
| | | | Full | - | 50 | - | ns |
| Address Transition Time, $t_{TRANS}$ | $V_S$ = ±4.5V, $V_{NO}$ or $V_{NC}$ = ±3V, $R_L$ = 300Ω, $C_L$ = 35pF, $V_{IN}$ = 0V to 3V (see Figure 1) | | +25 | - | 75 | - | ns |
| Break-Before-Make Time, $t_{BBM}$ | $V_S$ = ±5.5V, $V_{NO}$ or $V_{NC}$ = 3V, $R_L$ = 300Ω, $C_L$ = 35pF, $V_{IN}$ = 0V to 3V (see Figure 3) | | +25 | - | 10 | - | ns |
| Charge Injection, Q | $C_L$ = 1.0nF, $V_G$ = 0V, $R_G$ = 0Ω (see Figure 2) | | +25 | - | 2 | - | pC |
| NO/NC OFF-Capacitance, $C_{OFF}$ | f = 1MHz, $V_{NO}$ or $V_{NC}$ = $V_{COM}$ = 0V (see Figure 7) | | +25 | - | 3 | - | pF |
| COM OFF-Capacitance, $C_{OFF}$ | f = 1MHz, $V_{NO}$ or $V_{NC}$ = $V_{COM}$ = 0V (see Figure 7) | ISL84051 | +25 | - | 21 | - | pF |
| | | ISL84052 | +25 | - | 12 | - | pF |
| | | ISL84053 | +25 | - | 9 | - | pF |
| COM ON-Capacitance, $C_{COM(ON)}$ | f = 1MHz, $V_{NO}$ or $V_{NC}$ = $V_{COM}$ = 0V (see Figure 7) | ISL84051 | +25 | - | 26 | - | pF |
| | | ISL84052 | +25 | - | 18 | - | pF |
| | | ISL84053 | +25 | - | 14 | - | pF |
| OFF Isolation | $R_L$ = 50Ω, $C_L$ = 15pF, f = 100kHz $V_{NO}$ or $V_{NC}$ = $1V_{RMS}$ (see Figures 4 and 6) | | +25 | - | <90 | - | dB |
| Crosstalk, (Note 9) (ISL84052, ISL84053 Only) | | | +25 | - | < -90 | - | dB |
| **POWER SUPPLY CHARACTERISTICS** | | | | | | | |
| Power Supply Range | | | Full | **±2** | - | **±6** | V |
| Positive Supply Current, I+ | $V_S$ = ±5.5V, $V_{INH}$, $V_{ADD}$ = 0V or V+, Switch On or Off | | +25 | -1 | 0.1 | 1 | µA |
| | | | Full | **-10** | - | **10** | µA |
| Negative Supply Current, I- | | | 25 | -1 | 0.1 | 1 | µA |
| | | | Full | **-10** | - | **10** | µA |

## Electrical Specifications 5V Supply

Test Conditions: V+ = +4.5V to +5.5V, V- = GND = 0V, $V_{INH}$ = 2.4V, $V_{INL}$ = 0.8V (Note 8), Unless Otherwise Specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

| PARAMETER | TEST CONDITIONS | TEMP (°C) | MIN (Notes 9, 10) | TYP | MAX (Notes 9, 10) | UNITS |
|---|---|---|---|---|---|---|
| **ANALOG SWITCH CHARACTERISTICS** | | | | | | |
| Analog Signal Range, $V_{ANALOG}$ | | Full | **0** | - | **V+** | V |
| ON-Resistance, $r_{ON}$ | V+ = 5V, $I_{COM}$ = 1.0mA, $V_{NO}$ or $V_{NC}$ = 3.5V (see Figure 5) | +25 | - | 125 | 225 | Ω |
| | | Full | - | - | **280** | Ω |
| NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$ | V+ = 5.5V, $V_{COM}$ = 0V, 4.5V, $V_{NO}$ or $V_{NC}$ = 4.5V, 0V (Note 12) | +25 | - | 0.002 | - | nA |
| | | Full | **-10** | - | **10** | nA |
| COM OFF Leakage Current, $I_{COM(OFF)}$, (ISL84051) | V+ = 5.5V, $V_{COM}$ = 0V, 4.5V, $V_{NO}$ or $V_{NC}$ = 4.5V, 0V (Note 12) | +25 | - | 0.002 | - | nA |
| | | Full | **-10** | - | **10** | nA |
| COM OFF Leakage Current, $I_{COM(OFF)}$, (ISL84052, ISL84053) | V+ = 5.5V, $V_{COM}$ = 0V, 4.5V, $V_{NO}$ or $V_{NC}$ = 4.5V, 0V (Note 12) | +25 | - | 0.002 | - | nA |
| | | Full | **-5** | - | **5** | nA |

## Electrical Specifications 5V Supply

Test Conditions: V+ = +4.5V to +5.5V, V- = GND = 0V, $V_{INH}$ = 2.4V, $V_{INL}$ = 0.8V (Note 8), Unless Otherwise Specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

| PARAMETER | TEST CONDITIONS | TEMP (°C) | MIN (Notes 9, 10) | TYP | MAX (Notes 9, 10) | UNITS |
|---|---|---|---|---|---|---|
| COM ON Leakage Current, $I_{COM(ON)}$ | V+ = 5.5V, $V_{COM}$ = $V_{NO}$ or $V_{NC}$ = 4.5V (Note 12) | +25 | - | 0.002 | - | nA |
| | | Full | **-10** | - | **10** | nA |
| **DIGITAL INPUT CHARACTERISTICS** | | | | | | |
| Input Voltage High, $V_{INH}$, $V_{ADDH}$ | | Full | **2.4** | - | - | V |
| Input Voltage Low, $V_{INL}$, $V_{ADDL}$ | | Full | - | - | **0.8** | V |
| Input Current, $I_{INH}$, $I_{INL}$, $I_{ADDH}$, $I_{ADDL}$ | V+ = 5.5V, $V_{INH}$, $V_{ADD}$ = 0V or V+ | Full | **-1** | 0.03 | **1** | µA |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Inhibit Turn-ON Time, $t_{ON}$ | V+ = 4.5V, $V_{NO}$ or $V_{NC}$ = 3V, $R_L$ = 300Ω, $C_L$ = 35pF, $V_{IN}$ = 0 to 3V (see Figure 1) | +25 | - | 90 | - | ns |
| | | Full | - | 100 | - | ns |
| Inhibit Turn-OFF Time, $t_{OFF}$ | V+ = 4.5V, $V_{NO}$ or $V_{NC}$ = 3V, $R_L$ = 300Ω, $C_L$ = 35pF, $V_{IN}$ = 0V to 3V (see Figure 1) | +25 | - | 60 | - | ns |
| | | Full | - | 70 | - | ns |
| Break-Before-Make Time, $t_{BBM}$ | V+ = 5.5V, $V_{NO}$ or $V_{NC}$ = 3V, $R_L$ = 300Ω, $C_L$ = 35pF, $V_{IN}$ = 0V to 3V (see Figure 3) | +25 | - | 30 | - | ns |
| Charge Injection, Q | $C_L$ = 1.0nF, $V_G$ = 0V, $R_G$ = 0Ω (see Figure 2) | +25 | - | 2 | - | pC |
| OFF Isolation | $R_L$ = 50Ω, $C_L$ = 15pF, f = 100kHz $V_{NO}$ or $V_{NC}$ = $1V_{RMS}$ (see Figures 4 and 6) | +25 | - | <90 | - | dB |
| Crosstalk, (Note 9) (ISL84052, ISL840533 Only) | | +25 | - | <-90 | - | dB |
| **POWER SUPPLY CHARACTERISTICS** | | | | | | |
| Power Supply Range | | Full | **2** | - | **12** | V |
| Positive Supply Current, I+ | V+ = 5.5V, V- = 0V, $V_{INH}$, $V_{ADD}$ = 0V or V+, Switch On or Off | +25 | -1 | - | 1 | µA |
| | | Full | **-10** | - | **10** | µA |

## Electrical Specifications 3.3V Supply

Test Conditions: V+ = +3.0V to +3.6V, V- = GND = 0V, $V_{INH}$ = 2.4V, $V_{INL}$ = 0.8V (Note 8), Unless Otherwise Specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

| PARAMETER | TEST CONDITIONS | TEMP (°C) | MIN (Notes 9, 10) | TYP | MAX (Notes 9, 10) | UNITS |
|---|---|---|---|---|---|---|
| **ANALOG SWITCH CHARACTERISTICS** | | | | | | |
| Analog Signal Range, $V_{ANALOG}$ | | Full | **0** | - | **V+** | V |
| ON-Resistance, $r_{ON}$ | V+ = 3V, $I_{COM}$ = 1.0mA, $V_{NO}$ or $V_{NC}$ = 1.5V | +25 | - | 250 | - | Ω |
| | | Full | - | 270 | - | Ω |
| NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$ | V+ = 3.6V, $V_{COM}$ = 0V, 3V, $V_{NO}$ or $V_{NC}$ = 3V, 0V (Note 12) | +25 | - | 0.002 | - | nA |
| | | Full | **-10** | - | **10** | nA |
| COM OFF Leakage Current, $I_{COM(OFF)}$, (ISL84051) | V+ = 3.6V, $V_{COM}$ = 0V, 3V, $V_{NO}$ or $V_{NC}$ = 3V, 0V (Note 12) | +25 | - | 0.002 | - | nA |
| | | Full | **-10** | - | **10** | nA |
| COM OFF Leakage Current, $I_{COM(OFF)}$, (ISL84052, ISL84053) | V+ = 3.6V, $V_{COM}$ = 0V, 3V, $V_{NO}$ or $V_{NC}$ = 3V, 0V (Note 12) | +25 | - | 0.002 | - | nA |
| | | Full | **-5** | - | **5** | nA |
| COM ON Leakage Current, $I_{COM(ON)}$ | V+ = 3.6V, $V_{COM}$ = $V_{NO}$ or $V_{NC}$ = 3V (Note 12) | +25 | - | 0.002 | - | nA |
| | | Full | **-10** | - | **10** | nA |
| **DIGITAL INPUT CHARACTERISTICS** | | | | | | |
| Input Voltage High, $V_{INH}$, $V_{ADDH}$ | | Full | **2.4** | - | - | V |

## Electrical Specifications 3.3V Supply

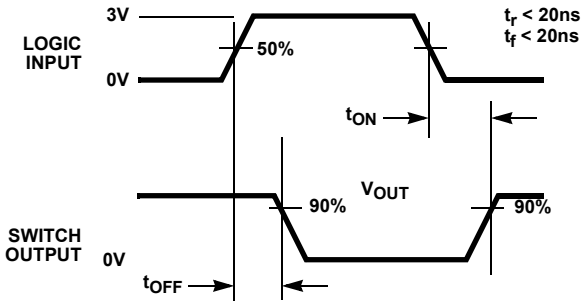
Test Conditions: V+ = +3.0V to +3.6V, V- = GND = 0V, $V_{INH}$ = 2.4V, $V_{INL}$ = 0.8V (Note 8), Unless Otherwise Specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

| PARAMETER | TEST CONDITIONS | TEMP (°C) | MIN (Notes 9, 10) | TYP | MAX (Notes 9, 10) | UNITS |
|---|---|---|---|---|---|---|
| Input Voltage Low, $V_{INL}$, $V_{ADDL}$ | | Full | - | - | **0.8** | V |
| Input Current, $I_{INH}$, $I_{INL}$, $I_{ADDH}$, $I_{ADDL}$ | V+ = 3.6V, $V_{INH}$, $V_{ADD}$ = 0V or V+ | Full | **-1** | 0.03 | **1** | µA |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Inhibit Turn-ON Time, $t_{ON}$ | V+ = 3V, $V_{NO}$ or $V_{NC}$ = 1.5V, $R_L$ = 300Ω, $C_L$ = 35pF, $V_{IN}$ = 0V to 3V (see Figure 1) | +25 | - | 180 | - | ns |
| | | Full | - | 280 | - | ns |
| Inhibit Turn-OFF Time, $t_{OFF}$ | V+ = 3V, $V_{NO}$ or $V_{NC}$ = 1.5V, $R_L$ = 300Ω, $C_L$ = 35pF, $V_{IN}$ = 0V to 3V (see Figure 1) | +25 | - | 100 | - | ns |
| | | Full | - | 200 | - | ns |
| Break-Before-Make Time, $t_{BBM}$ | V+ = 3.6V, $V_{NO}$ or $V_{NC}$ = 1.5V, $R_L$ = 300Ω, $C_L$ = 35pF, $V_{IN}$ = 0V to 3V (see Figure 3) | +25 | - | 90 | - | ns |
| Charge Injection, Q | $C_L$ = 1.0nF, $V_G$ = 0V, $R_G$ = 0Ω (see Figure 2) | +25 | - | 1 | - | pC |
| OFF Isolation | $R_L$ = 50Ω, $C_L$ = 15pF, f = 100kHz $V_{NO}$ or $V_{NC}$ = $1V_{RMS}$, (see Figures 4 and 6) | +25 | - | <90 | - | dB |
| Crosstalk, (Note 9) (ISL84052, ISL84053 Only) | | +25 | - | <-90 | - | dB |
| **POWER SUPPLY CHARACTERISTICS** | | | | | | |
| Power Supply Range | | Full | **2** | - | **12** | V |
| Positive Supply Current, I+ | V+ = 3.6V, V- = 0V, $V_{INH}$, $V_{ADD}$ = 0V or V+ Switch On or Off | +25 | -1 | - | 1 | µA |
| | | Full | **-10** | - | **10** | µA |

NOTES:

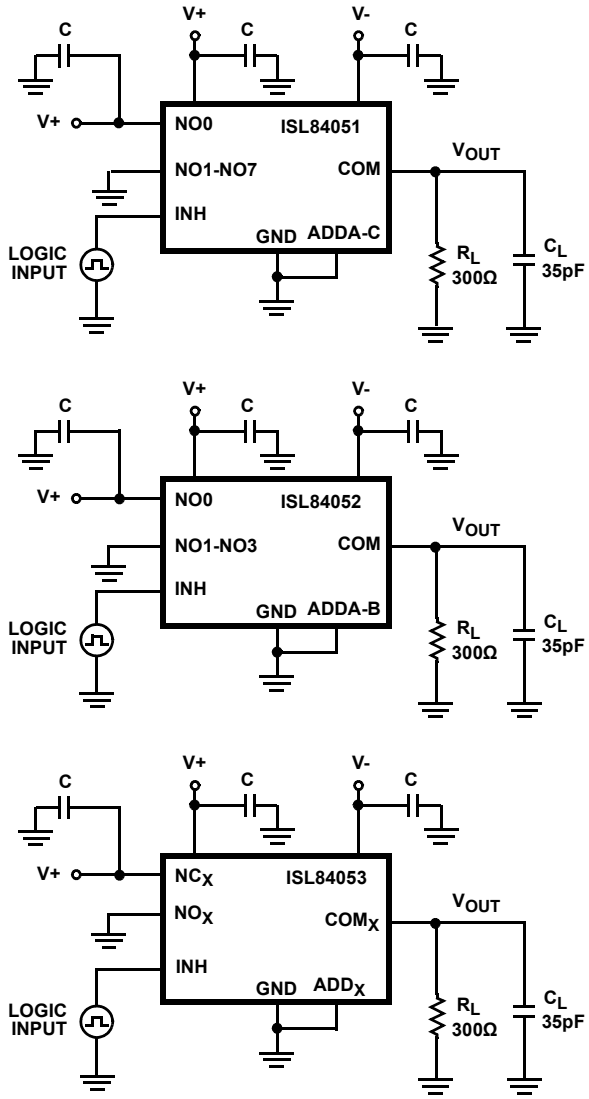
8. $V_{IN}$ = Input voltage to perform proper function.
9. The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
10. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
11. $\Delta r_{ON} = r_{ON}$ (MAX) - $r_{ON}$ (MIN).
12. Flatness is defined as the difference between maximum and minimum value of on-resistance over the specified analog signal range.
13. Between any two switches.

# Test Circuits and Waveforms




Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 1A. INHIBIT $t_{ON}/t_{OFF}$ MEASUREMENT POINTS



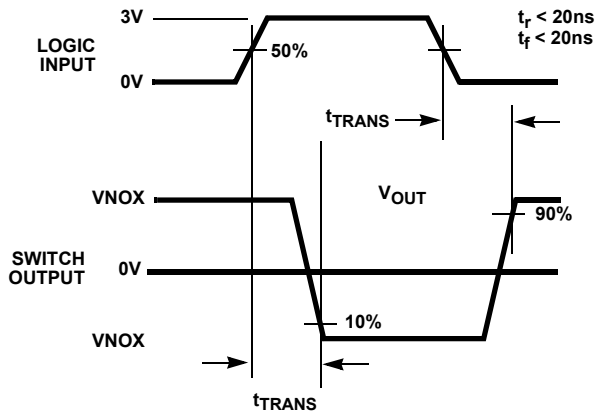

Repeat test for other switches. $C_L$ includes fixture and stray capacitance.

$$V_{OUT} = V_{(NO\ or\ NC)} \frac{R_L}{R_L + r_{ON}}$$

FIGURE 1B. INHIBIT $t_{ON}/t_{OFF}$ TEST CIRCUIT

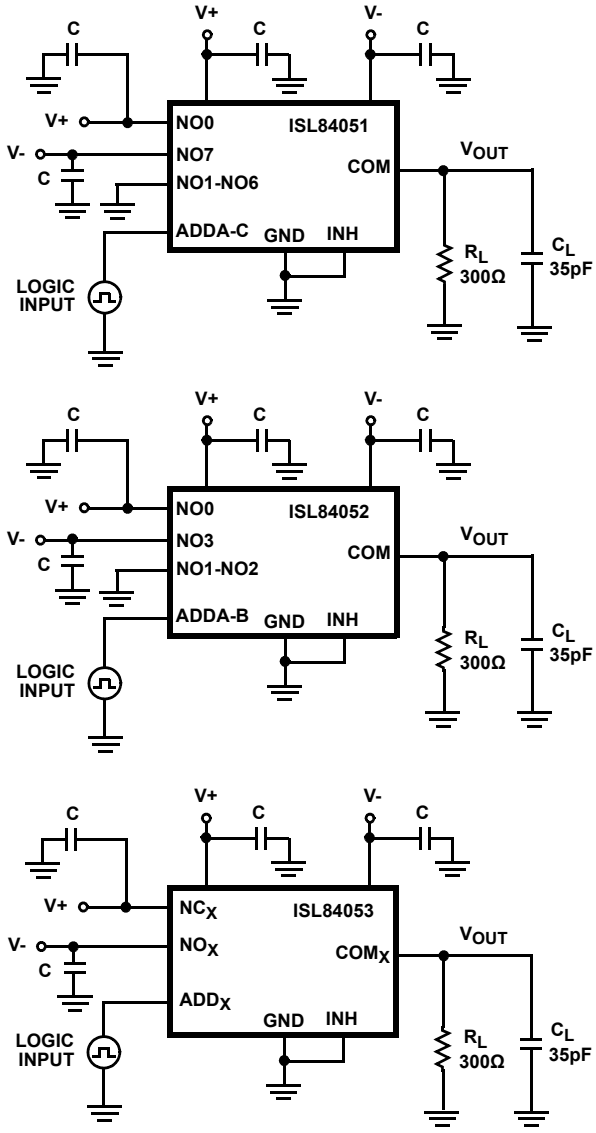
FIGURE 1. SWITCHING TIMES

## Test Circuits and Waveforms (Continued)




Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 1C. ADDRESS $t_{TRANS}$ MEASUREMENT POINTS




Repeat test for other switches. $C_L$ includes fixture and stray capacitance.

$$V_{OUT} = V_{(NO\ or\ NC)} \frac{R_L}{R_L + r_{ON}}$$

FIGURE 1D. ADDRESS $t_{TRANS}$ TEST CIRCUIT

FIGURE 1. SWITCHING TIMES (Continued)

## Test Circuits and Waveforms (Continued)

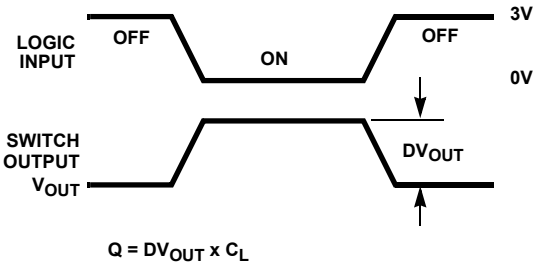
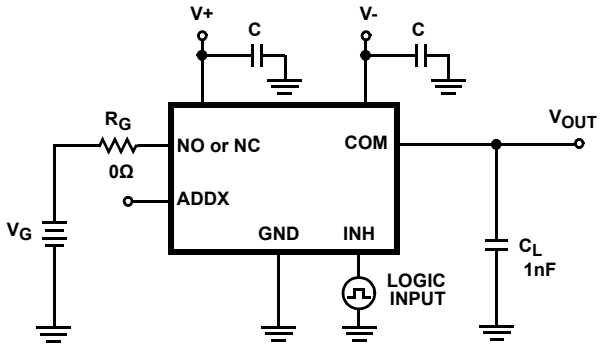



FIGURE 2A. Q MEASUREMENT POINTS




Repeat test for other switches.

FIGURE 2B. Q TEST CIRCUIT

FIGURE 2. CHARGE INJECTION

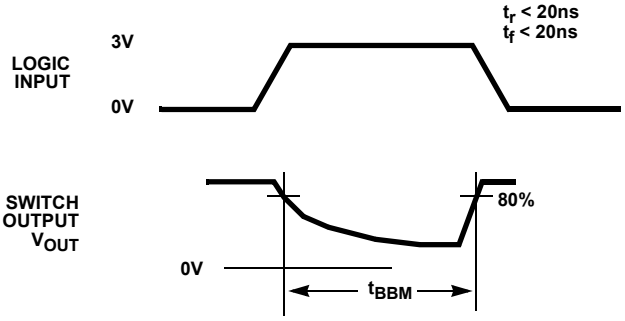
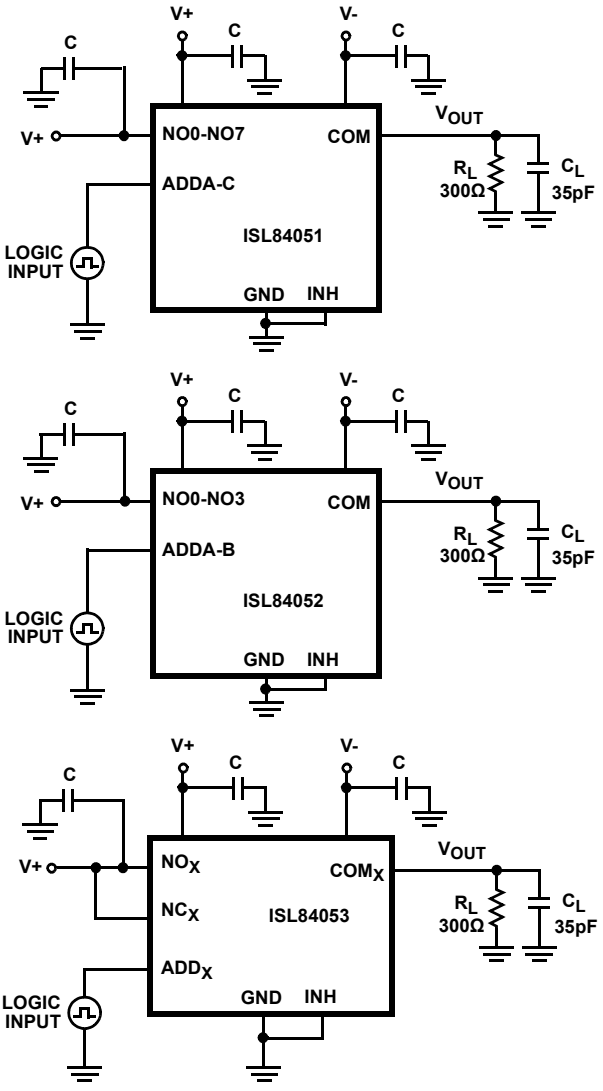



FIGURE 3A. $t_{BBM}$ MEASUREMENT POINTS




Repeat test for other switches. $C_L$ includes fixture and stray capacitance.

FIGURE 3B. $t_{BBM}$ TEST CIRCUIT

FIGURE 3. BREAK-BEFORE-MAKE TIME

## Test Circuits and Waveforms (Continued)

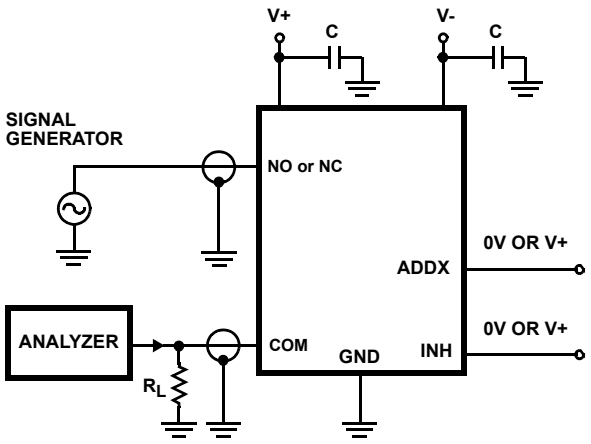



FIGURE 4. OFF ISOLATION TEST CIRCUIT

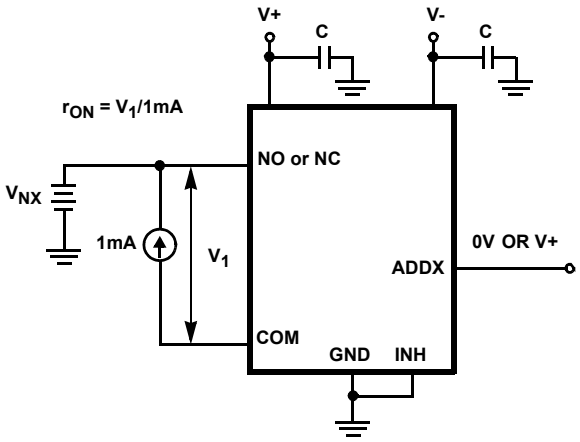



FIGURE 5. $r_{ON}$ TEST CIRCUIT

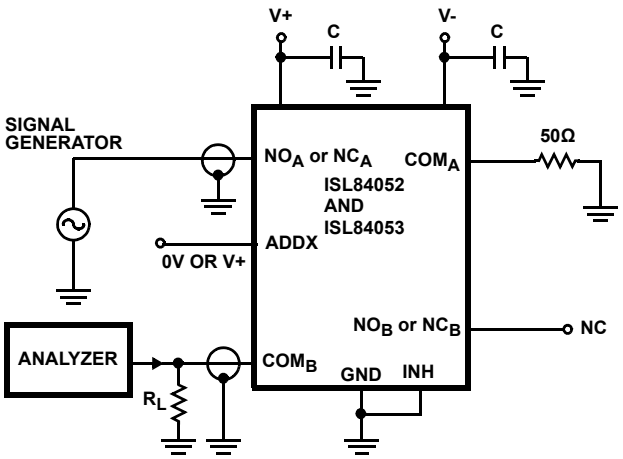



FIGURE 6. CROSSTALK TEST CIRCUIT

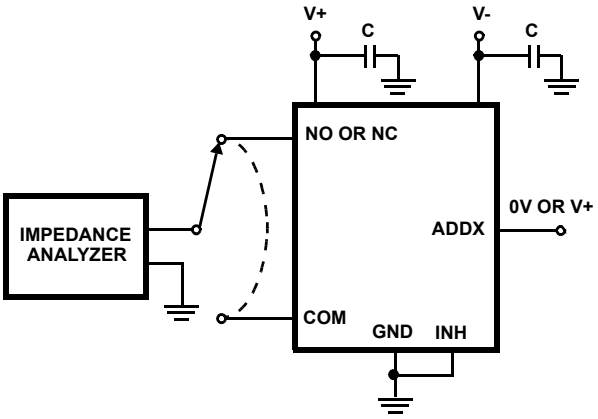



FIGURE 7. CAPACITANCE TEST CIRCUIT

# Detailed Description

The ISL84051, ISL84052, ISL84053 analog switches offer precise switching capability from a bipolar ±2V to ±6V or a single 2V to 12V supply with low on-resistance (60Ω) and high speed operation ($t_{ON}$ = 50ns, $t_{OFF}$ = 40ns). The devices are especially well suited to portable battery powered equipment thanks to the low operating supply voltage (2V), low power consumption (3µW), low leakage currents (5nA max). High frequency applications also benefit from the wide bandwidth, and the very high off isolation and crosstalk rejection.

## Supply Sequencing And Overvoltage Protection

With any CMOS device, proper power supply sequencing is required to protect the device from excessive input currents which might permanently damage the IC. All I/O pins contain ESD protection diodes from the pin to V+ and to V- (see Figure 8). To prevent forward biasing these diodes, V+ and V- must be applied before any input signals, and input signal voltages must remain between V+ and V-. If these conditions cannot be guaranteed, then one of the following two protection methods should be employed.

Logic inputs can easily be protected by adding a 1kΩ resistor in series with the input (see Figure 8). The resistor limits the input current below the threshold that produces permanent damage, and the sub-microamp input current produces an insignificant voltage drop during normal operation.

This method is not applicable for the signal path inputs. Adding a series resistor to the switch input defeats the purpose of using a low $r_{ON}$ switch, so two small signal diodes can be

added in series with the supply pins to provide overvoltage protection for all pins (see Figure 8). These additional diodes limit the analog signal from 1V below V+ to 1V above V-. The low leakage current performance is unaffected by this approach, but the switch resistance may increase, especially at low supply voltages.

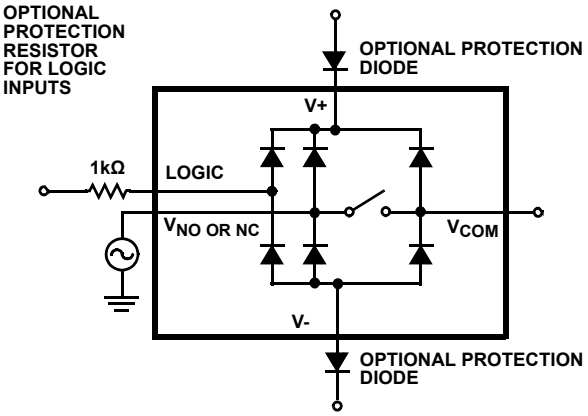



FIGURE 8. INPUT OVERVOLTAGE PROTECTION

## Power-Supply Considerations

The ISL8405x construction is typical of most CMOS analog switches, in that they have three supply pins: V+, V-, and GND. V+ and V- drive the internal CMOS switches and set their analog voltage limits, so there are no connections between the analog signal path and GND. Unlike switches with a 13V maximum supply voltage, the ISL8405x 15V maximum supply voltage provides plenty of room for the 10% tolerance of 12V supplies (±6V or 12V single supply), as well as room for overshoot and noise spikes.

This family of switches performs equally well when operated with bipolar or single voltage supplies. The minimum recommended supply voltage is 2V or ±2V. It is important to note that the input signal range, switching times, and ON-resistance degrade at lower supply voltages. Refer to the "Electrical Specification" tables beginning on page 5 and "Typical Performance Curves" beginning on page 14 for details.

V+ and GND power the internal logic (thus setting the digital switching point) and level shifters. The level shifters convert the logic levels to switched V+ and V- signals to drive the analog switch gate terminals.

## Logic-Level Thresholds

V+ and GND power the internal logic stages, so V- has no affect on logic thresholds. This switch family is TTL compatible (0.8V and 2.4V) over a V+ supply range of 2.7V to 10V. At 12V the $V_{IH}$ level is about 3.5V. This is still below the CMOS guaranteed high output minimum level of 4V, but noise margin is reduced. For best results with a 12V supply, use a logic family that provides a $V_{OH}$ greater than 4V.

The digital input stages draw supply current whenever the digital input voltage is not at one of the supply rails. Driving the digital input signals from GND to V+ with a fast transition time minimizes power dissipation.

## High-Frequency Performance

In 50Ω systems, signal response is reasonably flat even past 100MHz (see Figure 17). Figure 17 also illustrates that the frequency response is very consistent over varying analog signal levels.

An OFF switch acts like a capacitor and passes higher frequencies with less attenuation, resulting in signal feed through from a switch's input to its output. Off isolation is the resistance to this feed through, while crosstalk indicates the amount of feed through from one switch to another. Figure 18 details the high off isolation and crosstalk rejection provided by this family. At 10MHz, off isolation is about 55dB in 50Ω systems, decreasing approximately 20dB per decade as frequency increases. Higher load impedances decrease off isolation and crosstalk rejection due to the voltage divider action of the switch OFF impedance and the load impedance.

## Leakage Considerations

Reverse ESD protection diodes are internally connected between each analog-signal pin and both V+ and V-. One of these diodes conducts if any analog signal exceeds V+ or V-.

Virtually all the analog leakage current comes from the ESD diodes to V+ or V-. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or V- and the analog signal. This means their leakages will vary as the signal varies. The difference in the two diode leakages to the V+ and V- pins constitutes the analog-signal-path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of the same or opposite polarity. There is no connection between the analog signal paths and GND.

## Typical Performance Curves $T_A$ = +25°C, Unless Otherwise Specified

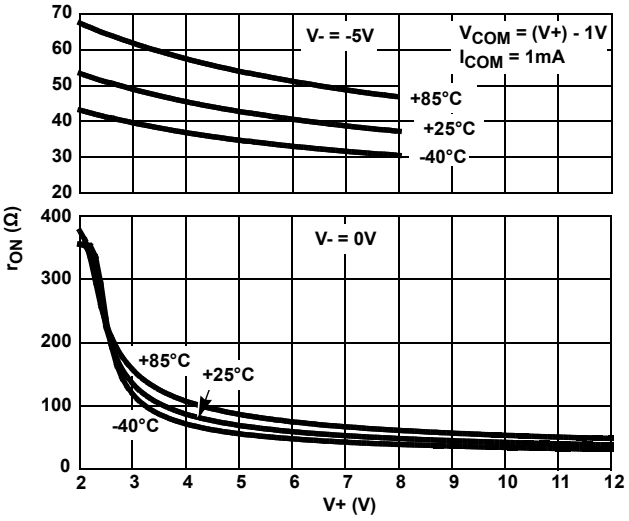



FIGURE 9. ON-RESISTANCE vs SUPPLY VOLTAGE

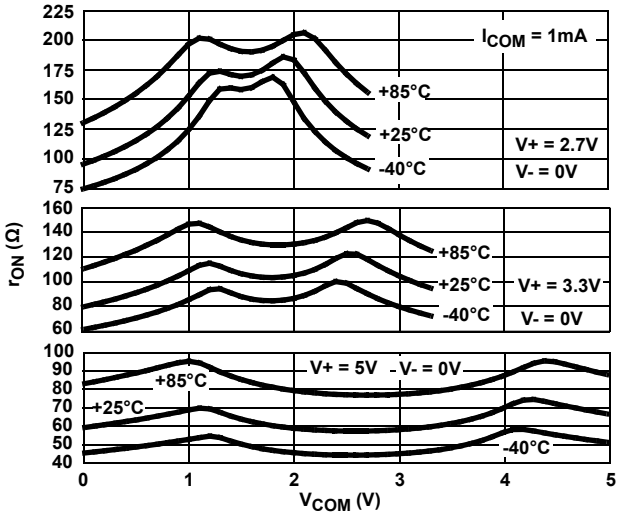



FIGURE 10. ON-RESISTANCE vs SWITCH VOLTAGE

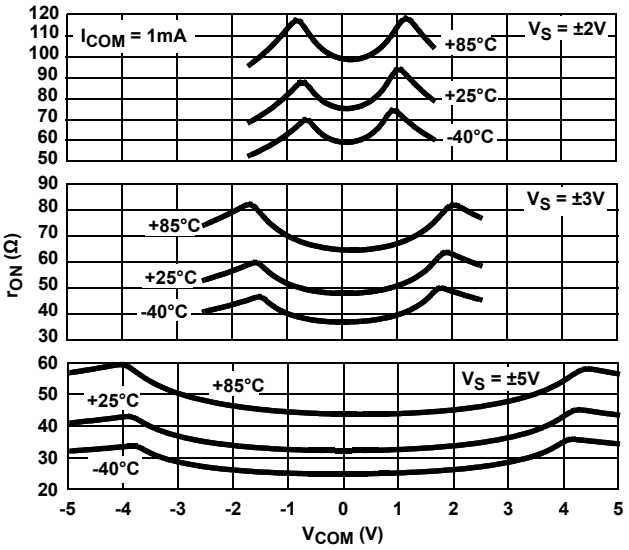



FIGURE 11. ON-RESISTANCE vs SWITCH VOLTAGE

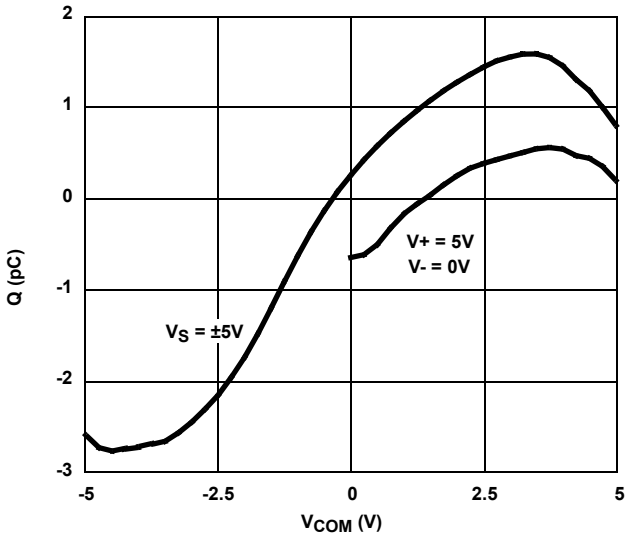



FIGURE 12. CHARGE INJECTION vs SWITCH VOLTAGE

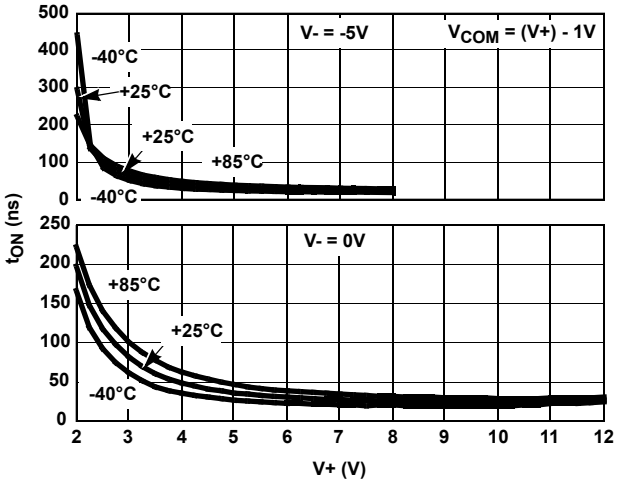



FIGURE 13. INHIBIT TURN-ON TIME vs SUPPLY VOLTAGE

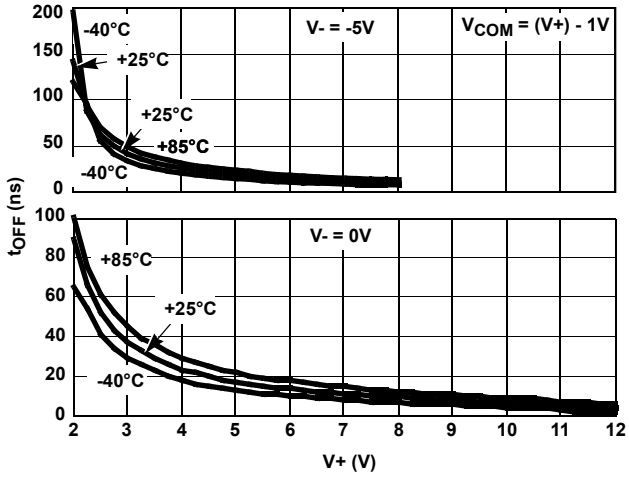



FIGURE 14. INHIBIT TURN-OFF TIME vs SUPPLY VOLTAGE

## Typical Performance Curves $T_A$ = +25°C, Unless Otherwise Specified (Continued)

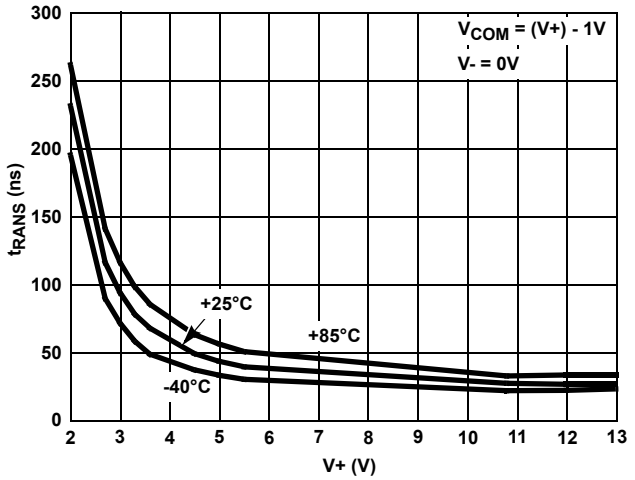



FIGURE 15. ADDRESS TRANS TIME vs SINGLE SUPPLY VOLTAGE

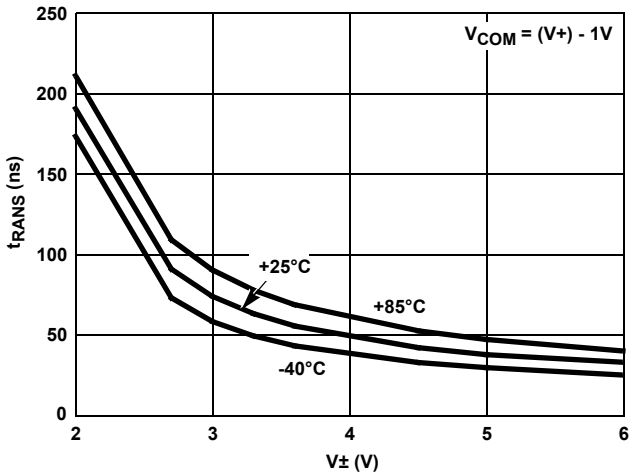



FIGURE 16. ADDRESS TRANS TIME vs DUAL SUPPLY VOLTAGE

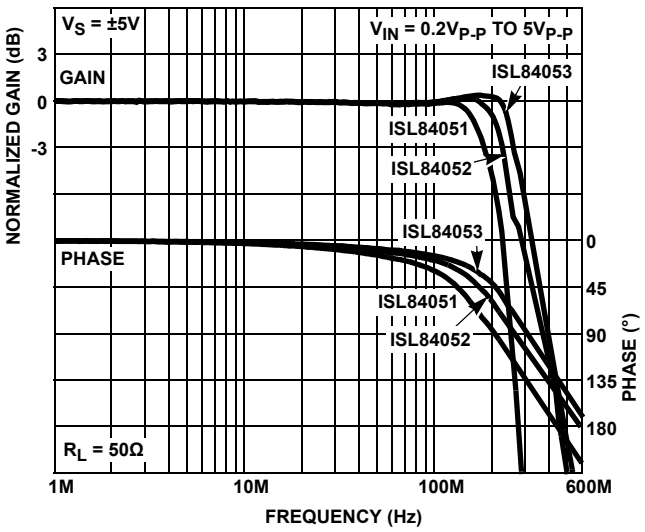



FIGURE 17. FREQUENCY RESPONSE

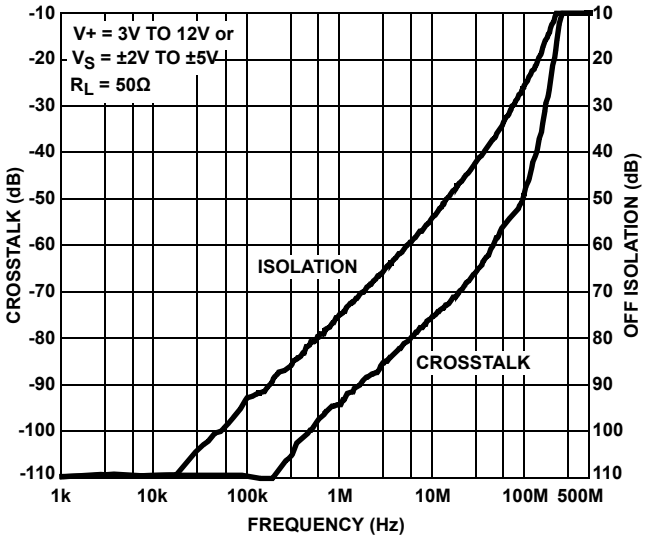



FIGURE 18. CROSSTALK AND OFF ISOLATION

# Die Characteristics

### SUBSTRATE POTENTIAL (POWERED UP):

V-

### TRANSISTOR COUNT:

ISL84051: 193
ISL84052: 193
ISL84053: 193

### PROCESS:

Si Gate CMOS

# Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

| DATE | REVISION | CHANGE |
|---|---|---|
| 05/02/11 | FN6047.10 | -Converted to new datasheet template.<br><br>-Updated Intersil Trademark statement at bottom of page 1 per directive from Legal.<br><br>-Added TSSOP Package option to ISL84053 in Pin Configuration and ordering information.<br><br>-Updated ordering information by removing withdrawn and obsolete non pb-free parts: ISL84051IA, ISL84051IA-T, ISL84051IB, ISL84051IB-T, ISL84052IA, ISL84051IB, ISL84053IA-T<br>Updated notes in ordering information<br><br>-Updated “Parameters...” note in Electrical Specifications tables to new “Compliance...” note according to standards<br><br>-M16.173 - Converted to new POD format by moving dimensions from table onto drawing and adding land pattern. No dimension changes.<br><br>-Added Revision History and Products Information. |

# Products

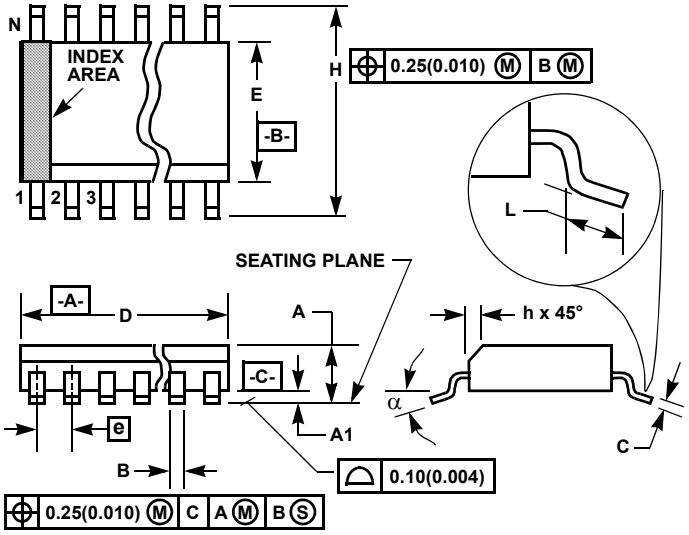
Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

*For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL84051, ISL84052, ISL84053

To report errors or suggestions for this datasheet, please go to: www.intersil.com/askourstaff

FITs are available from our website at: http://rel.intersil.com/reports/search.php

## *Small Outline Plastic Packages (SOIC)*




NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

**M16.15 (JEDEC MS-012-AC ISSUE C)**
**16 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE**

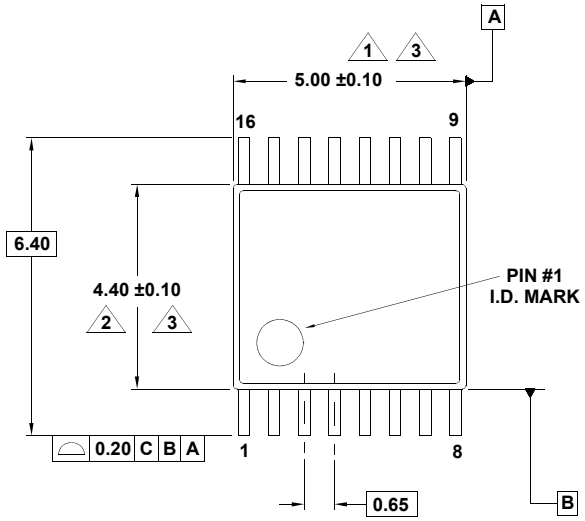
| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | |
| A | 0.0532 | 0.0688 | 1.35 | 1.75 | - |
| A1 | 0.0040 | 0.0098 | 0.10 | 0.25 | - |
| B | 0.013 | 0.020 | 0.33 | 0.51 | 9 |
| C | 0.0075 | 0.0098 | 0.19 | 0.25 | - |
| D | 0.3859 | 0.3937 | 9.80 | 10.00 | 3 |
| E | 0.1497 | 0.1574 | 3.80 | 4.00 | 4 |
| e | 0.050 BSC | | 1.27 BSC | | - |
| H | 0.2284 | 0.2440 | 5.80 | 6.20 | - |
| h | 0.0099 | 0.0196 | 0.25 | 0.50 | 5 |
| L | 0.016 | 0.050 | 0.40 | 1.27 | 6 |
| N | 16 | | 16 | | 7 |
| α | 0° | 8° | 0° | 8° | - |

Rev. 1 6/05

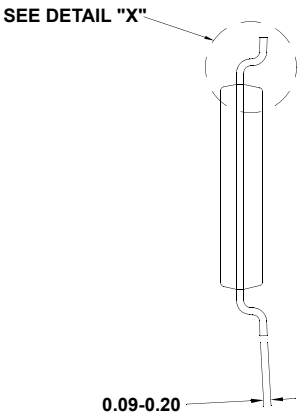
# Package Outline Drawing

## M16.173

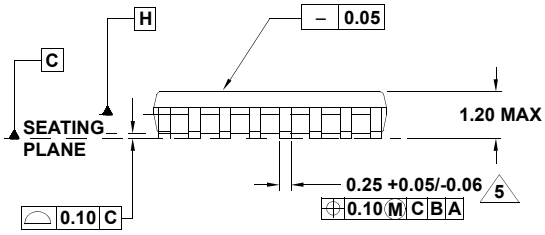
**16 LEAD THIN SHRINK SMALL OUTLINE PACKAGE (TSSOP)**
**Rev 2, 5/10**



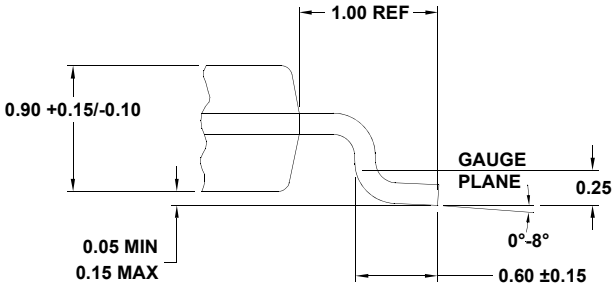

TOP VIEW



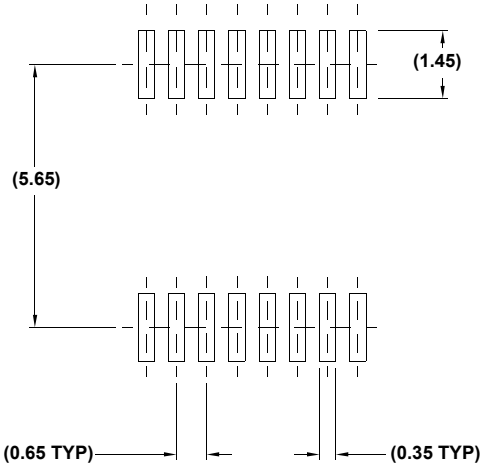

END VIEW




SIDE VIEW




DETAIL "X"

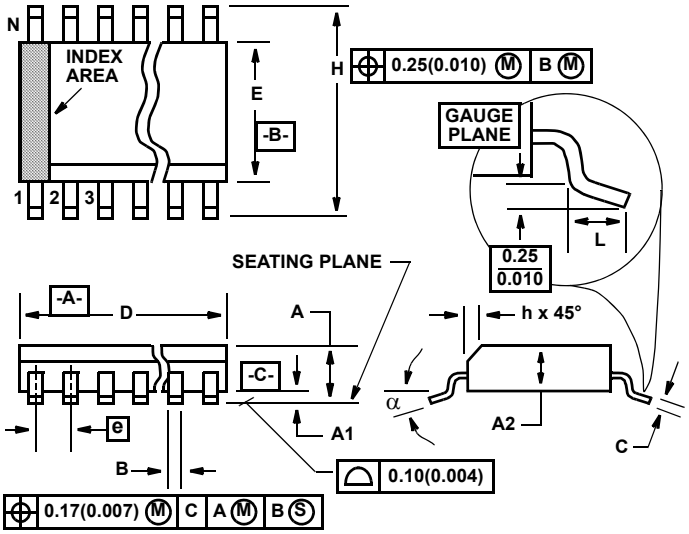



TYPICAL RECOMMENDED LAND PATTERN

**NOTES:**

1. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
2. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
3. Dimensions are measured at datum plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Dimension does not include dambar protrusion. Allowable protrusion shall be 0.08mm total in excess of dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm.
6. Dimension in ( ) are for reference only.
7. Conforms to JEDEC MO-153.

## *Shrink Small Outline Plastic Packages (SSOP)*
## *Quarter Size Outline Plastic Packages (QSOP)*




### M16.15A

**16 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE (0.150" WIDE BODY)**

| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | |
| A | 0.061 | 0.068 | 1.55 | 1.73 | - |
| A1 | 0.004 | 0.0098 | 0.102 | 0.249 | - |
| A2 | 0.055 | 0.061 | 1.40 | 1.55 | - |
| B | 0.008 | 0.012 | 0.20 | 0.31 | 9 |
| C | 0.0075 | 0.0098 | 0.191 | 0.249 | - |
| D | 0.189 | 0.196 | 4.80 | 4.98 | 3 |
| E | 0.150 | 0.157 | 3.81 | 3.99 | 4 |
| e | 0.025 BSC | | 0.635 BSC | | - |
| H | 0.230 | 0.244 | 5.84 | 6.20 | - |
| h | 0.010 | 0.016 | 0.25 | 0.41 | 5 |
| L | 0.016 | 0.035 | 0.41 | 0.89 | 6 |
| N | 16 | | 16 | | 7 |
| α | 0° | 8° | 0° | 8° | - |

Rev. 2 6/04

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension "B" does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm (0.004 inch) total in excess of "B" dimension at maximum material condition.
10. Controlling dimension: INCHES. Converted millimeter dimensions are not necessarily exact.

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