Power management (dual transistors)

UMF9N

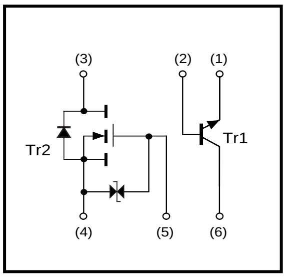
2SC5585 and 2SK3019 are housed independently in a UMT package.

●Application
Power management circuit

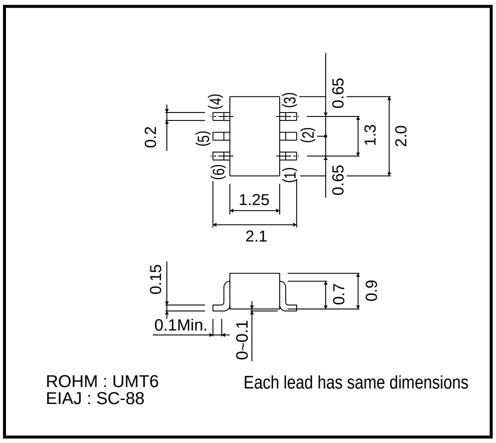
●Features
1) Power switching circuit in a single package.
2) Mounting cost and area can be cut in half.

●Structure
Silicon epitaxial planar transistor

●Equivalent circuits



●Dimensions (Units : mm)



●Packaging specifications

Type	UMF9N
Package	UMT6
Marking	F9
Code	TR
Basic ordering unit (pieces)	3000

●Absolute maximum ratings (Ta=25°C)

Tr1

Parameter	Symbol	Limits	Unit
Collector-base voltage	V_{CBO}	15	V
Collector-emitter voltage	V_{CEO}	12	V
Emitter-base voltage	V_{EBO}	6	V
Collector current	I_C	500	mA
	I_{CP}	1.0	A *1
Power dissipation	P_C	150(TOTAL)	mW *2
Junction temperature	Tj	150	°C
Range of storage temperature	Tstg	−55 to +150	°C

*1 Single pulse P_W=1ms
*2 120mW per element must not be exceeded. Each terminal mounted on a recommended land.

Tr2

Parameter		Symbol	Limits	Unit
Drain-source voltage		V_{DSS}	30	V
Gate-source voltage		V_{GSS}	±20	V
Drain current	Continuous	I_D	100	mA
	Pulsed	I_{DP}	200	mA *1
Reverse drain current	Continuous	I_{DR}	100	mA
	Pulsed	I_{DRP}	200	mA *1
Total power dissipation		P_D	150(TOTAL)	mW *2
Channel temperature		Tch	150	°C
Range of storage temperature		Tstg	−55 to +150	°C

*1 $P_W \leq 10ms$ Duty cycle≤50%
*2 120mW per element must not be exceeded. Each terminal mounted on a recommended land.

●Electrical characteristics (Ta=25°C)

Tr1

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Collector-emitter breakdown voltage	BV_{CEO}	12	–	–	V	I_C=1mA
Collector-base breakdown voltage	BV_{CBO}	15	–	–	V	I_C=10μA
Emitter-base breakdown voltage	BV_{EBO}	6	–	–	V	I_E=10μA
Collector cut-off current	I_{CBO}	–	–	100	nA	V_{CB}=15V
Emitter cut-off current	I_{EBO}	–	–	100	nA	V_{EB}=6V
Collector-emitter saturation voltage	$V_{CE(sat)}$	–	100	250	mV	I_C=200mA, I_B=10mA
DC current gain	h_{FE}	270	–	680	–	V_{CE}=2V, I_C=10mA
Transition frequency	f_T	–	320	–	MHz	V_{CE}=2V, I_E=−10mA, f=100MHz
Collector output capacitance	Cob	–	7.5	–	pF	V_{CB}=10V, I_E=0mA, f=1MHz

Tr2

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	–	–	±1	μA	V_{GS}=±20V, V_{DS}=0V
Drain-source breakdown voltage	$V_{(BR)DSS}$	30	–	–	V	I_D=10μA, V_{GS}=0V
Zero gate voltage drain current	I_{DSS}	–	–	1.0	μA	V_{DS}=30V, V_{GS}=0V
Gate-threshold voltage	$V_{GS(th)}$	0.8	–	1.5	V	V_{DS}=3V, I_D=100μA
Static drain-source on-state resistance	$R_{DS(on)}$	–	5	8	Ω	I_D=10mA, V_{GS}=4V
		–	7	13	Ω	I_D=1mA, V_{GS}=2.5V
Forward transfer admittance	$\lvert Y_{fs} \rvert$	20	–	–	ms	V_{DS}=3V, I_D=10mA
Input capacitance	C_{iss}	–	13	–	pF	V_{DS}=5V, V_{GS}=0V, f=1MHz
Output capacitance	C_{oss}	–	9	–	pF	
Reverce transfer capacitance	C_{rss}	–	4	–	pF	
Turn-on delay time	$t_{d(on)}$	–	15	–	ns	I_D=10mA, V_{DD} ≒5V, V_{GS}=5V, R_L=500Ω, R_{GS}=10Ω
Rise time	t_r	–	35	–	ns	
Turn-off delay time	$t_{d(off)}$	–	80	–	ns	
Fall time	t_f	–	80	–	ns	

● **Electrical characteristic curves**

Tr1

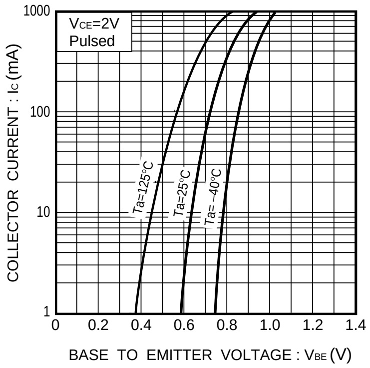


Fig.1 Grounded emitter propagation characteristics

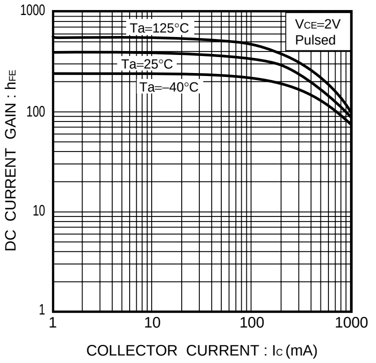


Fig.2 DC current gain vs. collector current

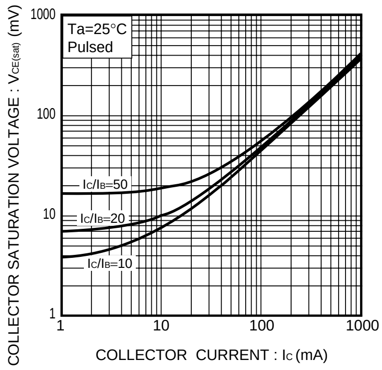


Fig.3 Collector-emitter saturation voltage vs. collector current (I)

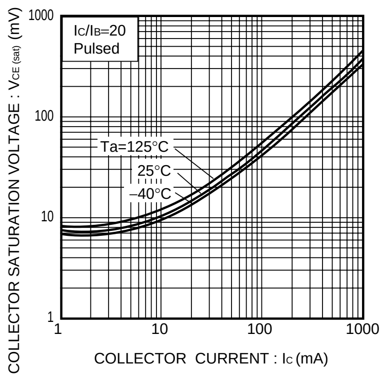


Fig.4 Collector-emitter saturation voltage vs. collector current (II)

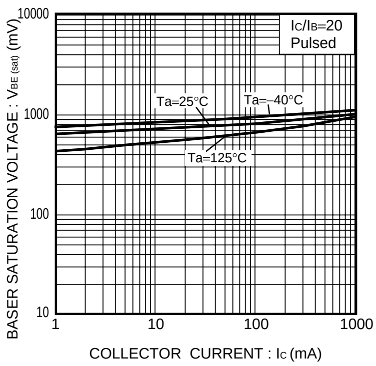


Fig.5 Base-emitter saturation voltage vs. collector current

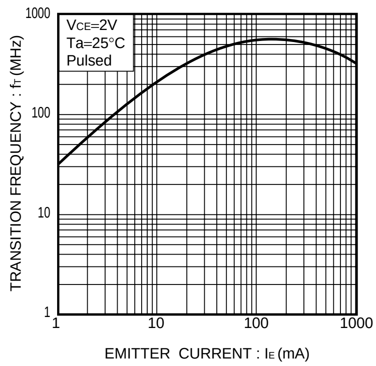


Fig.6 Gain bandwidth product vs. emitter current

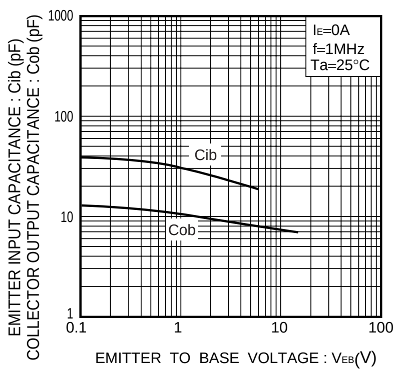


Fig.7 Collector output capacitance vs. collector-base voltage
Emitter input capacitance vs. emitter-base voltage

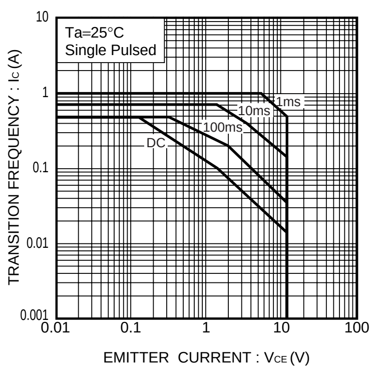


Fig.8 Safe operation area

Tr2

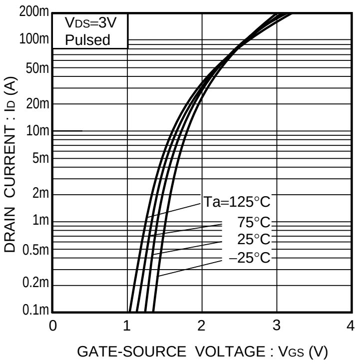


Fig.9 Typical transfer characteristics

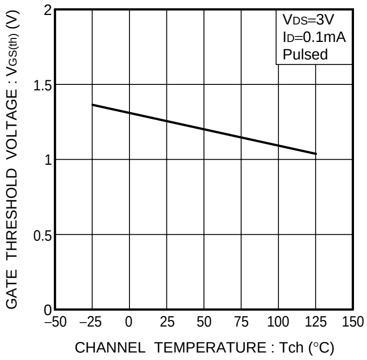


Fig.10 Gate threshold voltage vs. channel temperature

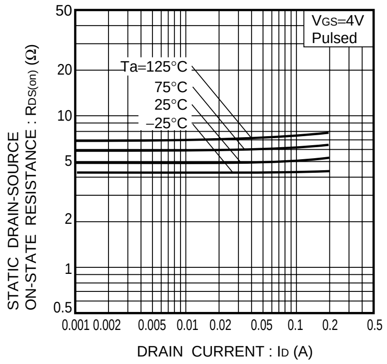


Fig.11 Static drain-source on-state resistance vs. drain current (I)

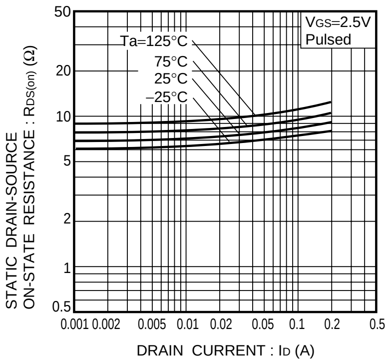


Fig.12 Static drain-source on-state resistance vs. drain current (II)

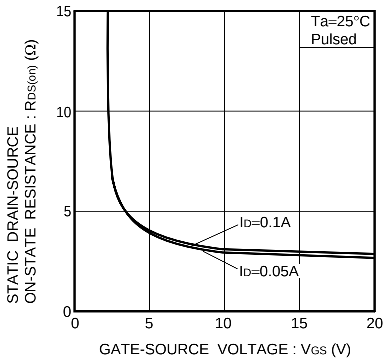


Fig.13 Static drain-source on-state resistance vs. gate-source voltage

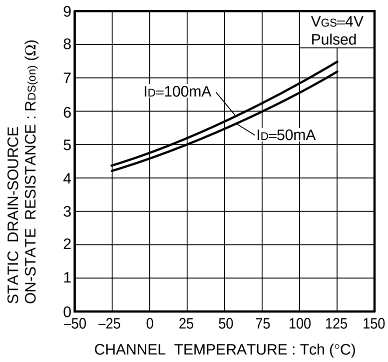


Fig.14 Static drain-source on-state resistance vs. channel temperature

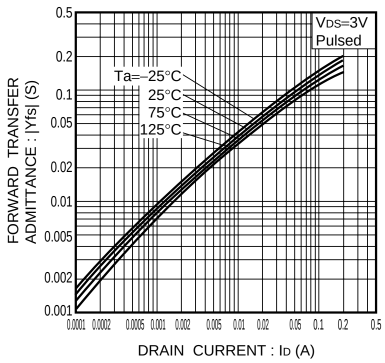


Fig.15 Forward transfer admittance vs. drain current

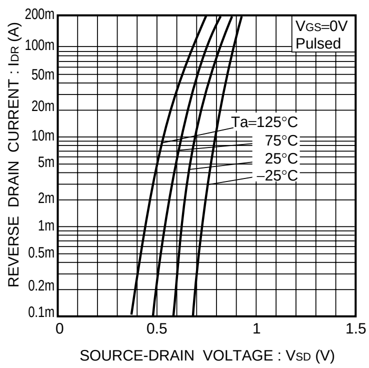


Fig.16 Reverse drain current vs. source-drain voltage (I)

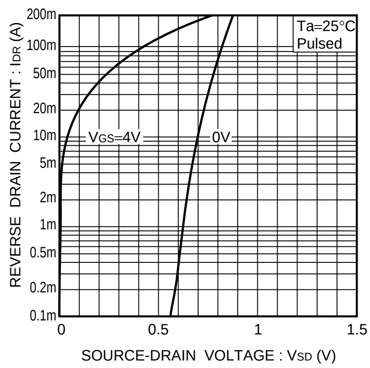


Fig.17 Reverse drain current vs. source-drain voltage (II)

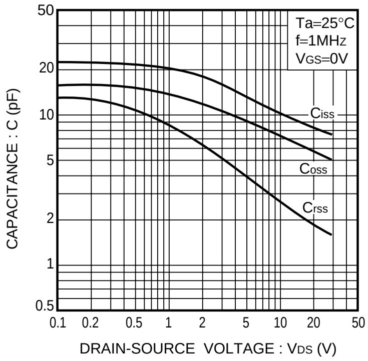


Fig.18 Typical capacitance vs. drain-source voltage

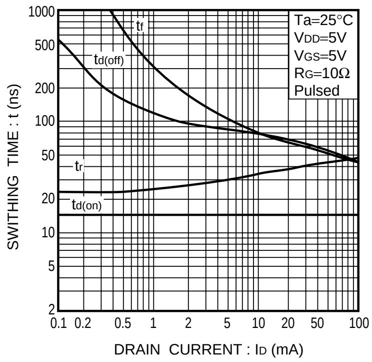


Fig.19 Switching characteristics

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