

IS61NLF12836A/IS61NVF12836A IS61NLF25618A/IS61NVF25618A



128K x 36 and 256K x 18 4Mb, FLOW THROUGH 'NO WAIT' STATE BUS SRAM

AUGUST 2011

FEATURES

- 100 percent bus utilization
- No wait cycles between Read and Write
- Internal self-timed write cycle
- Individual Byte Write Control
- Single Read/Write control pin
- Clock controlled, registered address, data and control
- Interleaved or linear burst sequence control using MODE input
- Three chip enables for simple depth expansion and address pipelining
- Power Down mode
- Common data inputs and data outputs
- $\overline{\text{CKE}}$ pin to enable clock and suspend operation
- JEDEC 100-pin TQFP, 119-ball PBGA, and 165-ball PBGA packages
- Power supply:
NVF: V_{DD} 2.5V ($\pm 5\%$), V_{DDQ} 2.5V ($\pm 5\%$)
NLF: V_{DD} 3.3V ($\pm 5\%$), V_{DDQ} 3.3V/2.5V ($\pm 5\%$)
- Industrial temperature available
- Lead-free available

DESCRIPTION

The 4 Meg 'NLF/NVF' product family feature high-speed, low-power synchronous static RAMs designed to provide a burstable, high-performance, 'no wait' state, device for networking and communications applications. They are organized as 128K words by 36 bits and 256K words by 18 bits, fabricated with ISSI's advanced CMOS technology.

Incorporating a 'no wait' state feature, wait cycles are eliminated when the bus switches from read to write, or write to read. This device integrates a 2-bit burst counter, high-speed SRAM core, and high-drive capability outputs into a single monolithic circuit.

All synchronous inputs pass through registers are controlled by a positive-edge-triggered single clock input. Operations may be suspended and all synchronous inputs ignored when Clock Enable, $\overline{\text{CKE}}$ is HIGH. In this state the internal device will hold their previous values.

All Read, Write and Deselect cycles are initiated by the ADV input. When the ADV is HIGH the internal burst counter is incremented. New external addresses can be loaded when ADV is LOW.

Write cycles are internally self-timed and are initiated by the rising edge of the clock inputs and when $\overline{\text{WE}}$ is LOW. Separate byte enables allow individual bytes to be written.

A burst mode pin (MODE) defines the order of the burst sequence. When tied HIGH, the interleaved burst sequence is selected. When tied LOW, the linear burst sequence is selected.

FAST ACCESS TIME

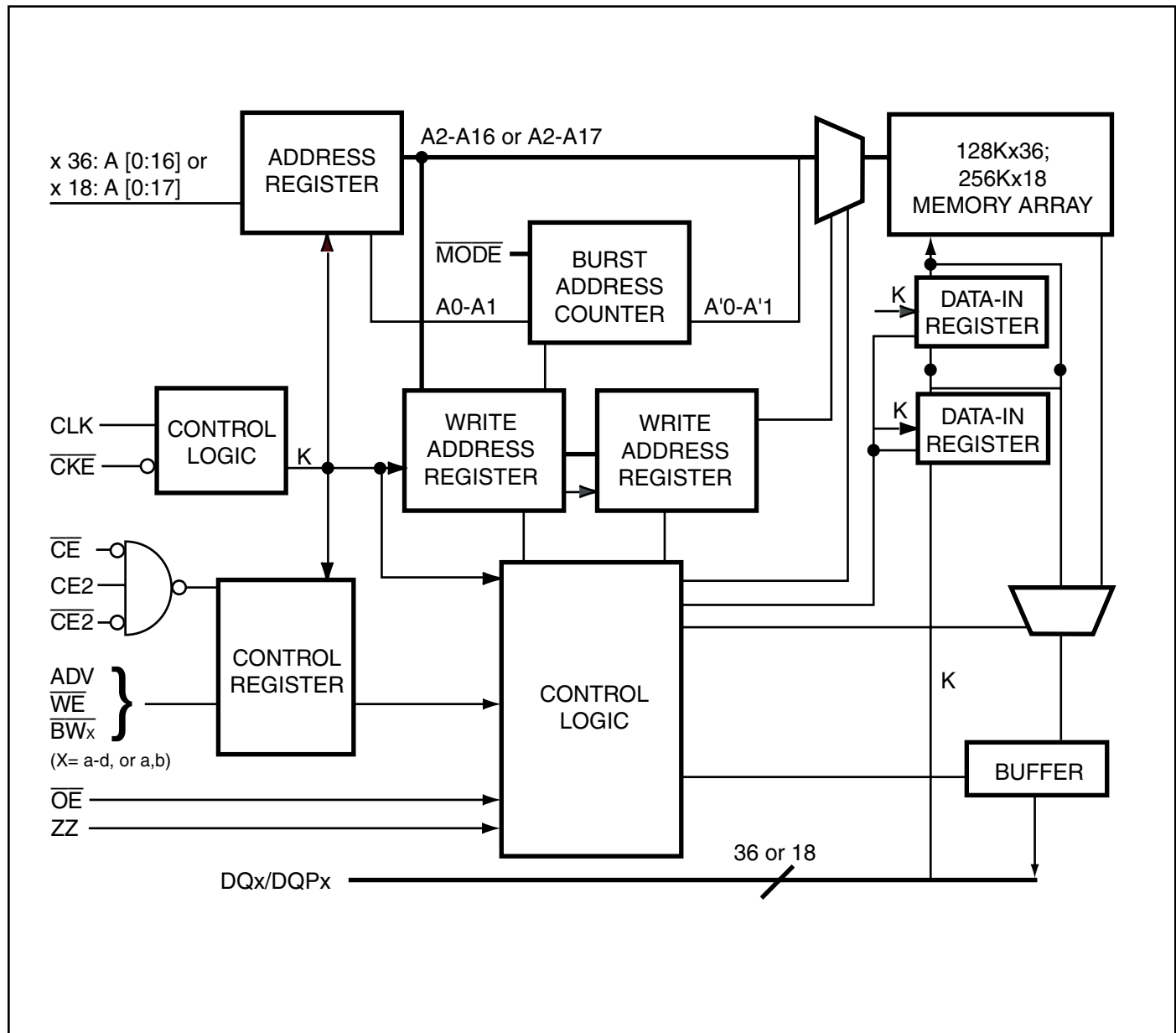
Symbol	Parameter	6.5	7.5	Units
t_{KQ}	Clock Access Time	6.5	7.5	ns
t_{KC}	Cycle Time	7.5	8.5	ns
	Frequency	133	117	MHz

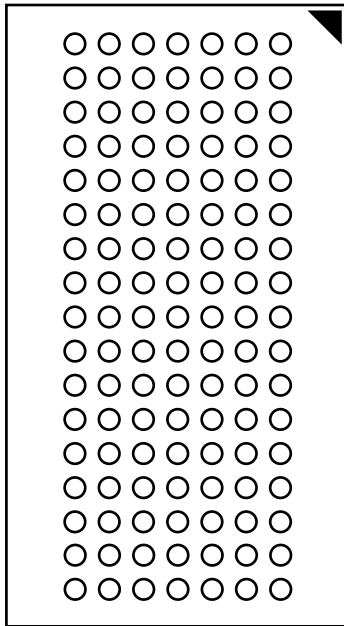
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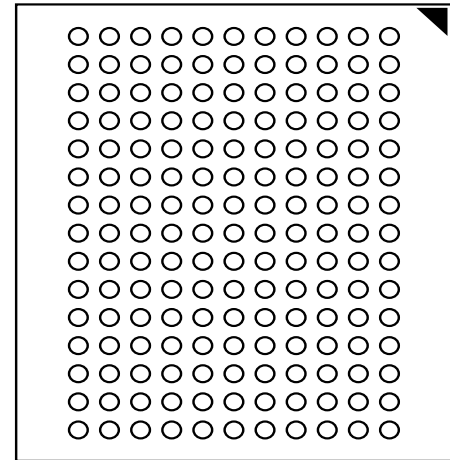
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- b.) the user assume all such risks; and
- c.) potential liability of Integrated Silicon Solution, Inc is adequately protected under the circumstances

BLOCK DIAGRAM





Bottom View
119-Ball, 14 mm x 22 mm BGA



Bottom View
165-Ball, 13 mm x 15mm BGA

PIN CONFIGURATION — 128K x 36, 165-Ball PBGA (TOP VIEW)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A	$\overline{CE}$	$\overline{BWc}$	$\overline{BWb}$	$\overline{CE2}$	$\overline{CKE}$	ADV	NC	A	NC
B	NC	A	CE2	$\overline{BWd}$	$\overline{BWa}$	CLK	$\overline{WE}$	$\overline{OE}$	NC	A	NC
C	DQPc	NC	VDDQ	VSS	VSS	VSS	VSS	VSS	VDDQ	NC	DQPb
D	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
E	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
F	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
G	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
H	NC	NC	NC	VDD	VSS	VSS	VSS	VDD	NC	NC	ZZ
J	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
K	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
L	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
M	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
N	DQPd	NC	VDDQ	VSS	NC	NC	NC	VSS	VDDQ	NC	DQPa
P	NC	NC	A	A	NC	A1*	NC	A	A	A	NC
R	MODE	NC	A	A	NC	A0*	NC	A	A	A	A

Note: A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.

PIN DESCRIPTIONS

Symbol	Pin Name
A	Address Inputs
A0, A1	Synchronous Burst Address Inputs
ADV	Synchronous Burst Address Advance/Load
$\overline{WE}$	Synchronous Read/Write Control Input
CLK	Synchronous Clock
$\overline{CKE}$	Clock Enable
$\overline{CE}$, $\overline{CE2}$, CE2	Synchronous Chip Enable
$\overline{BWx}$ (x=a-d)	Synchronous Byte Write Inputs
$\overline{OE}$	Output Enable
ZZ	Power Sleep Mode

MODE	Burst Sequence Selection
VDD	3.3V/2.5V Power Supply
NC	No Connect
DQx	Data Inputs/Outputs
DQPx	Parity Data I/O
VDDQ	Isolated output Power Supply 3.3V/2.5V
VSS	Ground

119-PIN PBGA PACKAGE CONFIGURATION —128K x 36 (TOP VIEW)

	1	2	3	4	5	6	7
A	V _{DDQ}	A	A	NC	A	A	V _{DDQ}
B	NC	CE2	A	ADV	A	$\overline{\text{CE2}}$	NC
C	NC	A	A	V _{DD}	A	A	NC
D	DQc	DQPc	V _{SS}	NC	V _{SS}	DQPb	DQb
E	DQc	DQc	V _{SS}	$\overline{\text{CE}}$	V _{SS}	DQb	DQb
F	V _{DDQ}	DQc	V _{SS}	$\overline{\text{OE}}$	V _{SS}	DQb	V _{DDQ}
G	DQc	DQc	$\overline{\text{BWc}}$	NC	$\overline{\text{BWb}}$	DQb	DQb
H	DQc	DQc	V _{SS}	$\overline{\text{WE}}$	V _{SS}	DQb	DQb
J	V _{DDQ}	V _{DD}	NC	V _{DD}	NC	V _{DD}	V _{DDQ}
K	DQd	DQd	V _{SS}	CLK	V _{SS}	DQa	DQa
L	DQd	DQd	$\overline{\text{BWd}}$	NC	$\overline{\text{BWa}}$	DQa	DQa
M	V _{DDQ}	DQd	V _{SS}	$\overline{\text{CKE}}$	V _{SS}	DQa	V _{DDQ}
N	DQd	DQd	V _{SS}	A ₁ *	V _{SS}	DQa	DQa
P	DQd	DQPd	V _{SS}	A ₀ *	V _{SS}	DQPa	DQa
R	NC	A	MODE	V _{DD}	NC	A	NC
T	NC	NC	A	A	A	NC	ZZ
U	V _{DDQ}	NC	NC	NC	NC	NC	V _{DDQ}

Note: A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.

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A0, A1	Synchronous Burst Address Inputs
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$\overline{\text{WE}}$	Synchronous Read/Write Control Input
CLK	Synchronous Clock
$\overline{\text{CKE}}$	Clock Enable
$\overline{\text{CE}}$	Synchronous Chip Select
$\overline{\text{CE2}}$	Synchronous Chip Select
CE2	Synchronous Chip Select
$\overline{\text{BWx}}$ (x=a-d)	Synchronous Byte Write Inputs

$\overline{\text{OE}}$	Output Enable
ZZ	Power Sleep Mode
MODE	Burst Sequence Selection
V _{DD}	Power Supply
V _{SS}	Ground
NC	No Connect
DQa-DQd	Data Inputs/Outputs
DQPa-Pd	Parity Data I/O
V _{DDQ}	Output Power Supply

165-PIN PBGA PACKAGE CONFIGURATION —256K x 18 (TOP VIEW)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A	$\overline{CE}$	$\overline{BWb}$	NC	$\overline{CE2}$	$\overline{CKE}$	ADV	NC	A	A
B	NC	A	CE2	NC	$\overline{BWa}$	CLK	$\overline{WE}$	$\overline{OE}$	NC	A	NC
C	NC	NC	VDDQ	Vss	Vss	Vss	Vss	Vss	VDDQ	NC	DQPa
D	NC	DQb	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	NC	DQa
E	NC	DQb	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	NC	DQa
F	NC	DQb	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	NC	DQa
G	NC	DQb	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	NC	DQa
H	NC	NC	NC	VDD	Vss	Vss	Vss	VDD	NC	NC	ZZ
J	DQb	NC	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	DQa	NC
K	DQb	NC	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	DQa	NC
L	DQb	NC	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	DQa	NC
M	DQb	NC	VDDQ	VDD	Vss	Vss	Vss	VDD	VDDQ	DQa	NC
N	DQPb	NC	VDDQ	Vss	NC	NC	NC	Vss	VDDQ	NC	NC
P	NC	NC	A	A	NC	A1*	NC	A	A	A	NC
R	MODE	NC	A	A	NC	A0*	NC	A	A	A	A

Note: A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.

PIN DESCRIPTIONS

Symbol	Pin Name
A	Address Inputs
A0, A1	Synchronous Burst Address Inputs
ADV	Synchronous Burst Address Advance/Load
$\overline{WE}$	Synchronous Read/Write Control Input
CLK	Synchronous Clock
$\overline{CKE}$	Clock Enable
$\overline{CE}$, $\overline{CE2}$, CE2	Synchronous Chip Enable
$\overline{BWx}$ (x=a,b)	Synchronous Byte Write Inputs
$\overline{OE}$	Output Enable
ZZ	Power Sleep Mode

MODE	Burst Sequence Selection
VDD	3.3V/2.5V Power Supply
NC	No Connect
DQx	Data Inputs/Outputs
DQPx	Parity Data I/O
VDDQ	Isolated output Power Supply 3.3V/2.5V
Vss	Ground

119-PIN PBGA PACKAGE CONFIGURATION —256K x 18 (TOP VIEW)

	1	2	3	4	5	6	7
A	V _{DDQ}	A	A	NC	A	A	V _{DDQ}
B	NC	CE2	A	ADV	A	$\overline{\text{CE}}2$	NC
C	NC	A	A	V _{DD}	A	A	NC
D	DQb	NC	V _{SS}	NC	V _{SS}	DQPa	NC
E	NC	DQb	V _{SS}	$\overline{\text{CE}}$	V _{SS}	NC	DQa
F	V _{DDQ}	NC	V _{SS}	$\overline{\text{OE}}$	V _{SS}	DQa	V _{DDQ}
G	NC	DQb	$\overline{\text{BW}}b$	NC	NC	NC	DQa
H	DQb	NC	V _{SS}	$\overline{\text{WE}}$	V _{SS}	DQa	NC
J	V _{DDQ}	V _{DD}	NC	V _{DD}	NC	V _{DD}	V _{DDQ}
K	NC	DQb	V _{SS}	CLK	V _{SS}	NC	DQa
L	DQb	NC	NC	NC	$\overline{\text{BW}}a$	DQa	NC
M	V _{DDQ}	DQb	V _{SS}	$\overline{\text{CKE}}$	V _{SS}	NC	V _{DDQ}
N	DQb	NC	V _{SS}	A ₁ *	V _{SS}	DQa	NC
P	NC	DQPb	V _{SS}	A ₀ *	V _{SS}	NC	DQa
R	NC	A	MODE	V _{DD}	NC	A	NC
T	NC	A	A	NC	A	A	ZZ
U	V _{DDQ}	NC	NC	NC	NC	NC	V _{DDQ}

Note: A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.

PIN DESCRIPTIONS

Symbol	Pin Name
A	Address Inputs
A0, A1	Synchronous Burst Address Inputs
ADV	Synchronous Burst Address Advance/Load
$\overline{\text{WE}}$	Synchronous Read/Write Control Input
CLK	Synchronous Clock
$\overline{\text{CKE}}$	Clock Enable
$\overline{\text{CE}}$	Synchronous Chip Select
$\overline{\text{CE}}2$	Synchronous Chip Select
CE2	Synchronous Chip Select
$\overline{\text{BW}}x$ (x=a,b)	Synchronous Byte Write Inputs

$\overline{\text{OE}}$	Output Enable
ZZ	Power Sleep Mode
MODE	Burst Sequence Selection
V _{DD}	Power Supply
V _{SS}	Ground
NC	No Connect
DQa-DQb	Data Inputs/Outputs
DQPa-Pb	Parity Data I/O
V _{DDQ}	Output Power Supply

The image displays two pin diagrams for memory modules. The left diagram is for a 128K x 36 module, showing a 30-pin connector with pins 1-30 on the left and 80-51 on the right. The right diagram is for a 256K x 18 module, showing a 30-pin connector with pins 1-30 on the left and 80-51 on the right. Both diagrams include a table of pin functions and a table of pin numbers.

128K x 36 Pin Diagram:

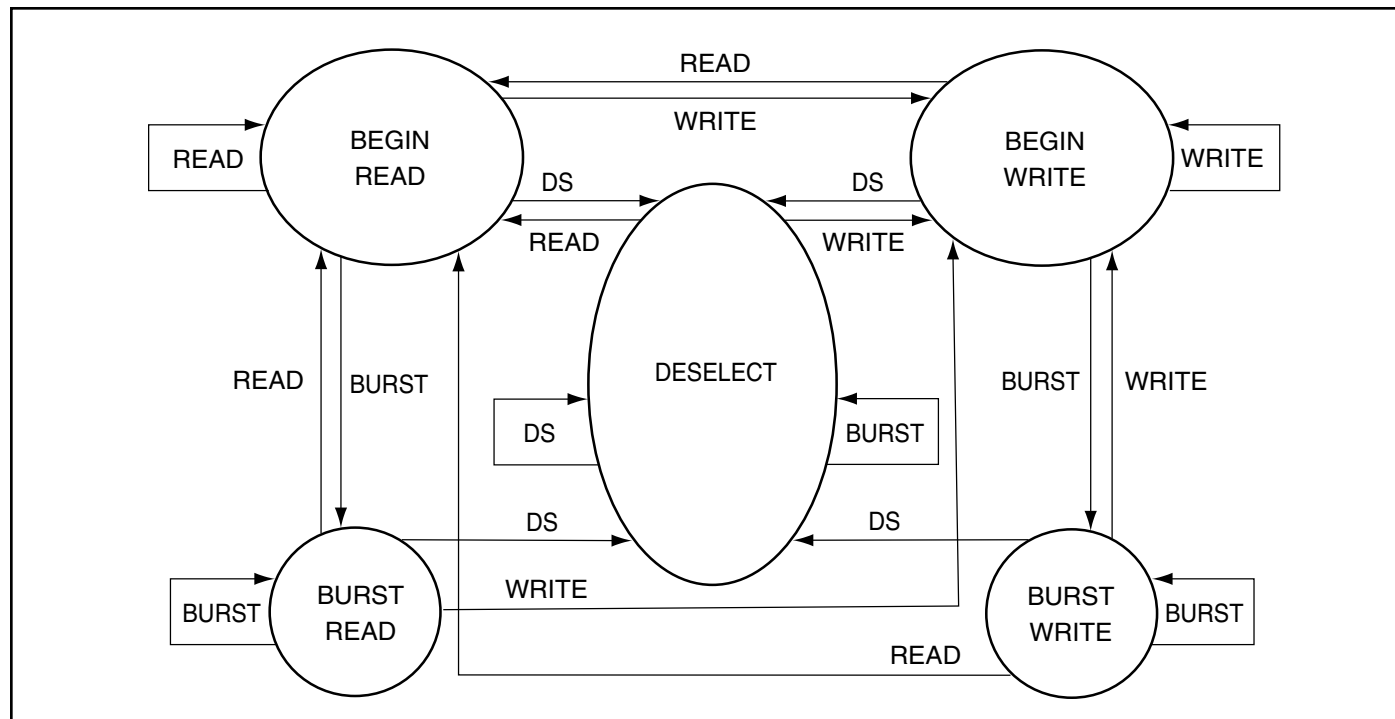
Pin	Function	Pin	Function
1	DQPC	80	DQPb
2	DQc	79	DQb
3	DQc	78	DQb
4	VDDQ	77	VDDQ
5	VSS	76	VSS
6	DQc	75	DQb
7	DQc	74	DQb
8	DQc	73	DQb
9	DQc	72	DQb
10	VSS	71	VSS
11	VDDQ	70	VDDQ
12	DQc	69	DQb
13	DQc	68	DQb
14	NC	67	VSS
15	VDD	66	NC
16	NC	65	VDD
17	VSS	64	ZZ
18	DQd	63	DQa
19	DQd	62	DQa
20	VDDQ	61	VDDQ
21	VSS	60	VSS
22	DQd	59	DQa
23	DQd	58	DQa
24	DQd	57	DQa
25	DQd	56	DQa
26	VSS	55	VSS
27	VDDQ	54	VDDQ
28	DQd	53	DQa
29	DQd	52	DQa
30	DQPd	51	DQPa

256K x 18 Pin Diagram:

Pin	Function	Pin	Function
1	NC	80	A
2	NC	79	NC
3	NC	78	NC
4	VDDQ	77	VDDQ
5	VSS	76	VSS
6	NC	75	NC
7	NC	74	DQPa
8	DQb	73	DQa
9	DQb	72	DQa
10	VSS	71	VSS
11	VDDQ	70	VDDQ
12	DQb	69	DQa
13	DQb	68	DQa
14	NC	67	VSS
15	VDD	66	NC
16	NC	65	VDD
17	VSS	64	ZZ
18	DQb	63	DQa
19	DQb	62	DQa
20	VDDQ	61	VDDQ
21	VSS	60	VSS
22	DQb	59	DQa
23	DQb	58	DQa
24	DQPB	57	NC
25	NC	56	NC
26	VSS	55	VSS
27	VDDQ	54	VDDQ
28	NC	53	NC
29	NC	52	NC
30	NC	51	NC

$\overline{CE}$, CE2, $\overline{CE2}$	Synchronous Chip Enable
$\overline{OE}$	Output Enable
DQa-DQd	Synchronous Data Input/Output
DQPa-DQPd	Parity Data I/O
MODE	Burst Sequence Selection
V _{DD}	+3.3V/2.5V Power Supply
V _{SS}	Ground for output Buffer
V _{DDQ}	Isolated Output Buffer Supply: +3.3V/2.5V
ZZ	Snooze Enable

STATE DIAGRAM



SYNCHRONOUS TRUTH TABLE⁽¹⁾

Operation	Address Used	$\overline{CE}$	CE2	$\overline{CE2}$	ADV	$\overline{WE}$	$\overline{BWx}$	$\overline{OE}$	$\overline{CKE}$	CLK
Not Selected	N/A	H	X	X	L	X	X	X	L	↑
Not Selected	N/A	X	L	X	L	X	X	X	L	↑
Not Selected	N/A	X	X	H	L	X	X	X	L	↑
Not Selected Continue	N/A	X	X	X	H	X	X	X	L	↑
Begin Burst Read	External Address	L	H	L	L	H	X	L	L	↑
Continue Burst Read	Next Address	X	X	X	H	X	X	L	L	↑
NOP/Dummy Read	External Address	L	H	L	L	H	X	H	L	↑
Dummy Read	Next Address	X	X	X	H	X	X	H	L	↑
Begin Burst Write	External Address	L	H	L	L	L	L	X	L	↑
Continue Burst Write	Next Address	X	X	X	H	X	L	X	L	↑
NOP/Write Abort	N/A	L	H	L	L	L	H	X	L	↑
Write Abort	Next Address	X	X	X	H	X	H	X	L	↑
Ignore Clock	Current Address	X	X	X	X	X	X	X	H	↑

Notes:

1. "X" means don't care.
2. The rising edge of clock is symbolized by ↑
3. A continue deselect cycle can only be entered if a deselect cycle is executed first.
4. $\overline{WE} = L$ means Write operation in Write Truth Table.
 $\overline{WE} = H$ means Read operation in Write Truth Table.
5. Operation finally depends on status of asynchronous pins ($\overline{ZZ}$ and $\overline{OE}$).

ASYNCHRONOUS TRUTH TABLE⁽¹⁾

Operation	ZZ	$\overline{OE}$	I/O STATUS
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

Notes:

1. X means "Don't Care".
2. For write cycles following read cycles, the output buffers must be disabled with $\overline{OE}$, otherwise data bus contention will occur.
3. Sleep Mode means power Sleep Mode where stand-by current does not depend on cycle time.
4. Deselected means power Sleep Mode where stand-by current depends on cycle time.

WRITE TRUTH TABLE (x18)

Operation	$\overline{WE}$	$\overline{Bw}a$	$\overline{Bw}b$
READ	H	X	X
WRITE BYTE a	L	L	H
WRITE BYTE b	L	H	L
WRITE ALL BYTES	L	L	L
WRITE ABORT/NOP	L	H	H

Notes:

1. X means "Don't Care".
2. All inputs in this table must be setup and hold time around the rising edge of CLK.

WRITE TRUTH TABLE (x36)

Operation	$\overline{WE}$	$\overline{BWa}$	$\overline{BWb}$	$\overline{BWc}$	$\overline{BWd}$
READ	H	X	X	X	X
WRITE BYTE a	L	L	H	H	H
WRITE BYTE b	L	H	L	H	H
WRITE BYTE c	L	H	H	L	H
WRITE BYTE d	L	H	H	H	L
WRITE ALL BYTEs	L	L	L	L	L
WRITE ABORT/NOP	L	H	H	H	H

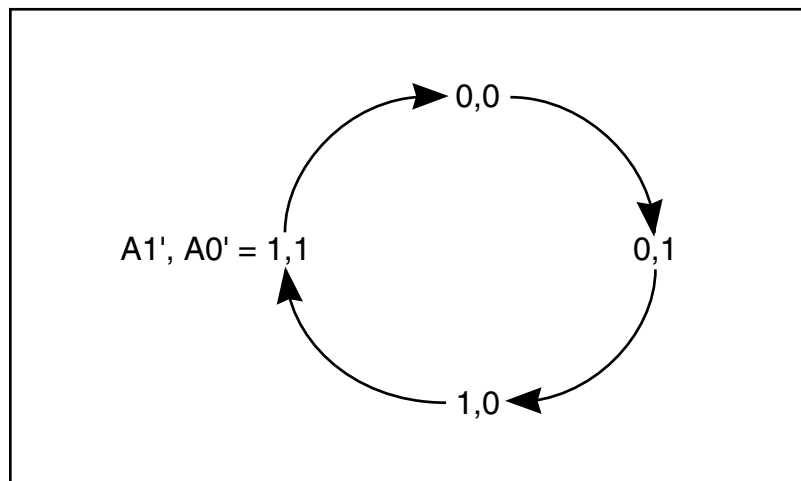
Notes:

1. X means "Don't Care".
2. All inputs in this table must meet setup and hold time around the rising edge of CLK.

INTERLEAVED BURST ADDRESS TABLE (MODE = V_{DD} or NC)

External Address A1 A0	1st Burst Address A1 A0	2nd Burst Address A1 A0	3rd Burst Address A1 A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

LINEAR BURST ADDRESS TABLE (MODE = V_{SS})



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Parameter	Value	Unit
T _{STG}	Storage Temperature	−65 to +150	°C
P _D	Power Dissipation	1.6	W
I _{OUT}	Output Current (per I/O)	100	mA
V _{IN} , V _{OUT}	Voltage Relative to V _{SS} for I/O Pins	−0.5 to V _{DDQ} + 0.3	V
V _{IN}	Voltage Relative to V _{SS} for for Address and Control Inputs	−0.3 to 4.6	V

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, precautions may be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.
3. This device contains circuitry that will ensure the output devices are in High-Z at power up.

OPERATING RANGE (IS61NLFx)

Range	Ambient Temperature	V _{DD}	V _{DDQ}
Commercial	0°C to +70°C	3.3V ± 5%	3.3V / 2.5V ± 5%
Industrial	−40°C to +85°C	3.3V ± 5%	3.3V / 2.5V ± 5%

OPERATING RANGE (IS61NVFx)

Range	Ambient Temperature	V _{DD}	V _{DDQ}
Commercial	0°C to +70°C	2.5V ± 5%	2.5V ± 5%
Industrial	-40°C to +85°C	2.5V ± 5%	2.5V ± 5%

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions	3.3V		2.5V		Unit
			Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	I _{OH} = -4.0 mA (3.3V) I _{OH} = -1.0 mA (2.5V)	2.4	—	2.0	—	V
V _{OL}	Output LOW Voltage	I _{OL} = 8.0 mA (3.3V) I _{OL} = 1.0 mA (2.5V)	—	0.4	—	0.4	V
V _{IH}	Input HIGH Voltage		2.0	V _{DD} + 0.3	1.7	V _{DD} + 0.3	V
V _{IL}	Input LOW Voltage		-0.3	0.8	-0.3	0.7	V
I _{LI}	Input Leakage Current	V _{SS} ≤ V _{IN} ≤ V _{DD} ⁽¹⁾	-5	5	-5	5	μA
I _{LO}	Output Leakage Current	V _{SS} ≤ V _{OUT} ≤ V _{DDQ} , OE = V _{IH}	-5	5	-5	5	μA

POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	Test Conditions	Temp. range	6.5 MAX		7.5 MAX		Unit
				x18	x36	x18	x36	
I _{CC}	AC Operating Supply Current	Device Selected, OE = V _{IH} , ZZ ≤ V _{IL} , All Inputs ≤ 0.2V or ≥ V _{DD} - 0.2V, Cycle Time ≥ t _{kc} min.	Com. Ind. typ. ⁽²⁾	175 180	175 180	155 160	155 160	mA
I _{SB}	Standby Current TTL Input	Device Deselected, V _{DD} = Max., All Inputs ≤ V _{IL} or ≥ V _{IH} , ZZ ≤ V _{IL} , f = Max.	Com. Ind.	90 100	90 100	90 100	90 100	mA
I _{SB1}	Standby Current CMOS Input	Device Deselected, V _{DD} = Max., V _{IN} ≤ V _{SS} + 0.2V or ≥ V _{DD} - 0.2V f = 0	Com. Ind. typ. ⁽²⁾	70 75	70 75	70 75	70 75	mA
I _{SB2}	Sleep Mode	ZZ > V _{IH}	Com. Ind. typ. ⁽²⁾	30 35 20	30 35	30 35 20	30 35	mA

Note:

- MODE pin has an internal pullup and should be tied to V_{DD} or V_{SS}. It exhibits ±100 μA maximum leakage current when tied to ≤ V_{SS} + 0.2V or ≥ V_{DD} - 0.2V.
- Typical values are measured at V_{DD} = 3.3V, T_A = 25°C and not 100% tested.

CAPACITANCE^(1,2)

Symbol	Parameter	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6	pF
C _{OUT}	Input/Output Capacitance	V _{OUT} = 0V	8	pF

Notes:

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{DD} = 3.3V.

3.3V I/O AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	1.5 ns
Input and Output Timing and Reference Level	1.5V
Output Load	See Figures 1 and 2

3.3V I/O OUTPUT LOAD EQUIVALENT

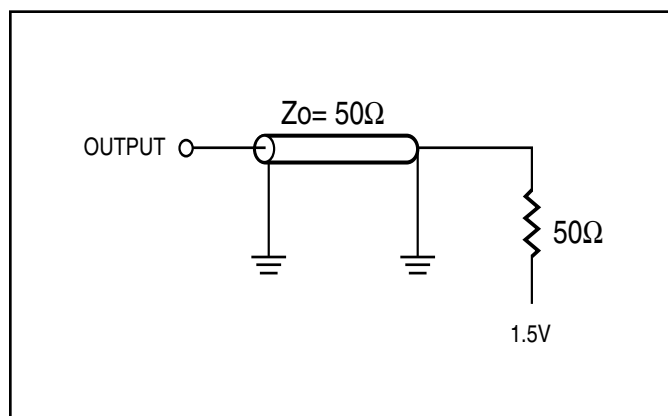


Figure 1

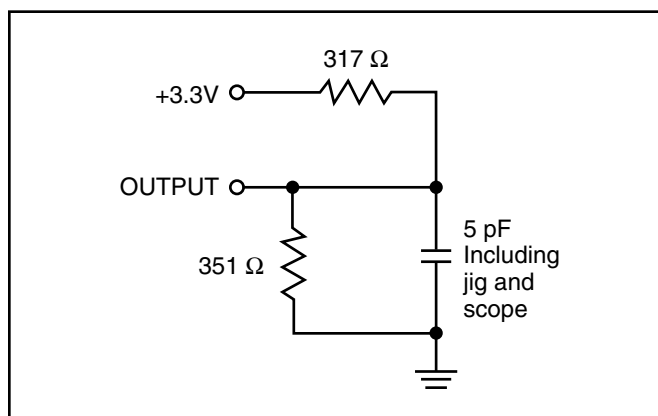


Figure 2

2.5V I/O AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 2.5V
Input Rise and Fall Times	1.5 ns
Input and Output Timing and Reference Level	1.25V
Output Load	See Figures 3 and 4

2.5V I/O OUTPUT LOAD EQUIVALENT

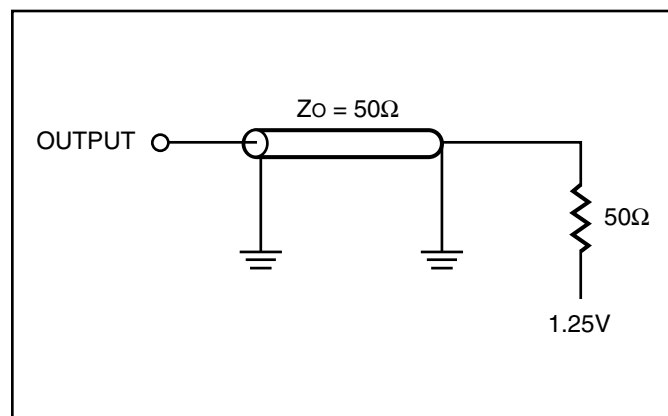


Figure 3

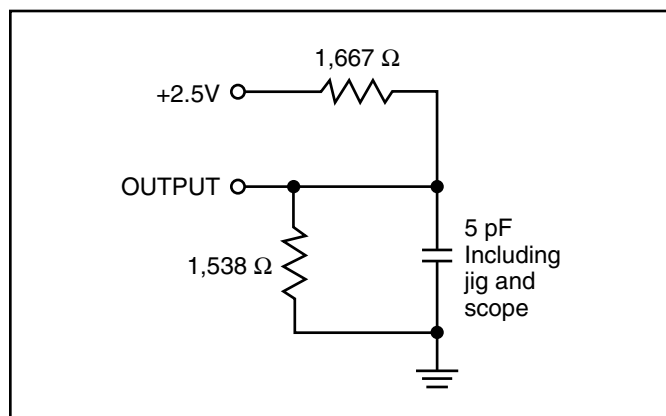


Figure 4

READ/WRITE CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

Symbol	Parameter	6.5		7.5		Unit
		Min.	Max.	Min.	Max.	
fmax	Clock Frequency	—	133	—	117	MHz
t _{KC}	Cycle Time	7.5	—	8.5	—	ns
t _{KH}	Clock High Time	2.2	—	2.5	—	ns
t _{KL}	Clock Low Time	2.2	—	2.5	—	ns
t _{KQ}	Clock Access Time	—	6.5	—	7.5	ns
t _{KQX} ⁽²⁾	Clock High to Output Invalid	2.5	—	2.5	—	ns
t _{KQLZ} ^(2,3)	Clock High to Output Low-Z	2.5	—	2.5	—	ns
t _{KQHZ} ^(2,3)	Clock High to Output High-Z	—	3.8	—	4.0	ns
t _{OEQ}	Output Enable to Output Valid	—	3.2	—	3.4	ns
t _{OELZ} ^(2,3)	Output Enable to Output Low-Z	0	—	0	—	ns
t _{OEHZ} ^(2,3)	Output Disable to Output High-Z	—	3.5	—	3.5	ns
t _{AS}	Address Setup Time	1.5	—	1.5	—	ns
t _{WS}	Read/Write Setup Time	1.5	—	1.5	—	ns
t _{CES}	Chip Enable Setup Time	1.5	—	1.5	—	ns
t _{SE}	Clock Enable Setup Time	1.5	—	1.5	—	ns
t _{ADVS}	Address Advance Setup Time	1.5	—	1.5	—	ns
t _{DS}	Data Setup Time	1.5	—	1.5	—	ns
t _{AH}	Address Hold Time	0.5	—	0.5	—	ns
t _{HE}	Clock Enable Hold Time	0.5	—	0.5	—	ns
t _{WH}	Write Hold Time	0.5	—	0.5	—	ns
t _{CEH}	Chip Enable Hold Time	0.5	—	0.5	—	ns
t _{ADVH}	Address Advance Hold Time	0.5	—	0.5	—	ns
t _{DH}	Data Hold Time	0.5	—	0.5	—	ns
t _{PDS}	ZZ High to Power Down	—	2	—	2	cyc
t _{PUS}	ZZ Low to Power Down	—	2	—	2	cyc

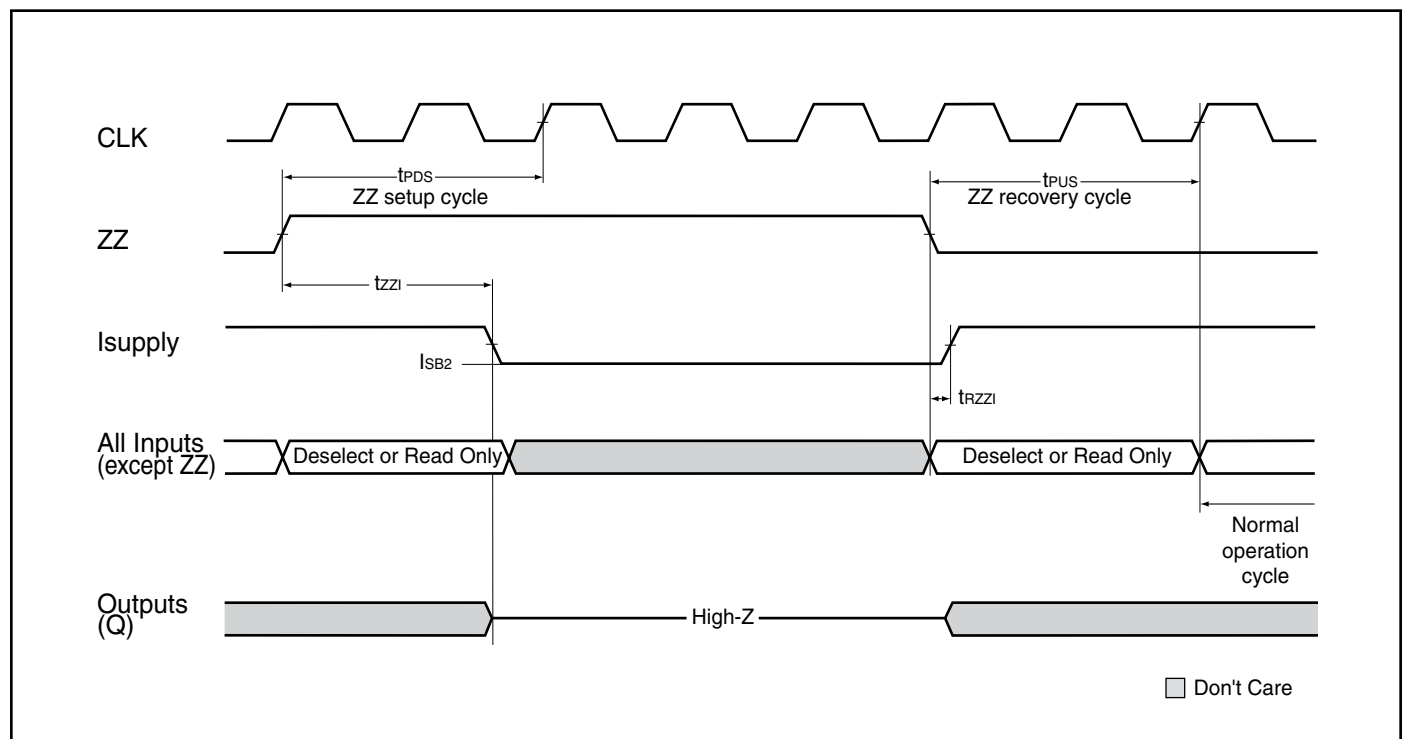
Notes:

1. Configuration signal MODE is static and must not change during normal operation.
2. Guaranteed but not 100% tested. This parameter is periodically sampled.
3. Tested with load in Figure 2.

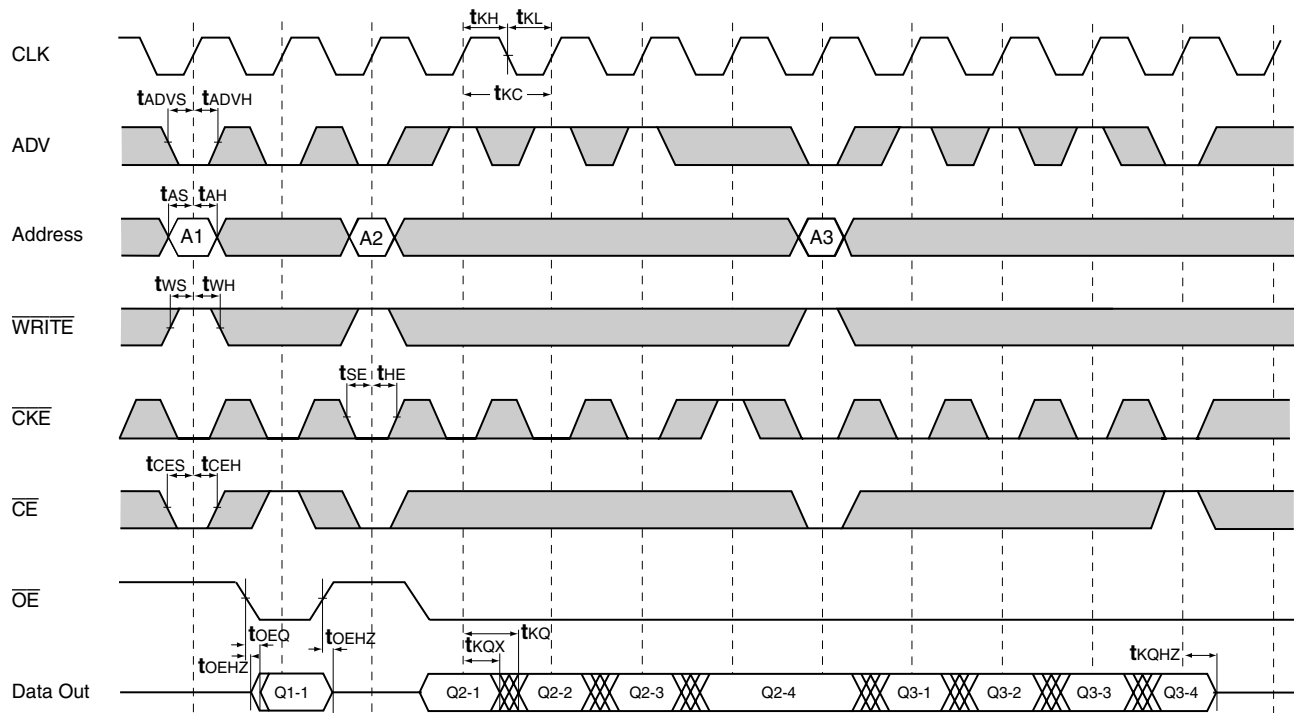
SLEEP MODE ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Min.	Max.	Unit
I _{SB2}	Current during SLEEP MODE	ZZ ≥ V _{IH}		35	mA
t _{PDS}	ZZ active to input ignored			2	cycle
t _{PUS}	ZZ inactive to input sampled		2		cycle
t _{ZZI}	ZZ active to SLEEP current		2		cycle
t _{ZZI}	ZZ inactive to exit SLEEP current		0		ns

SLEEP MODE TIMING



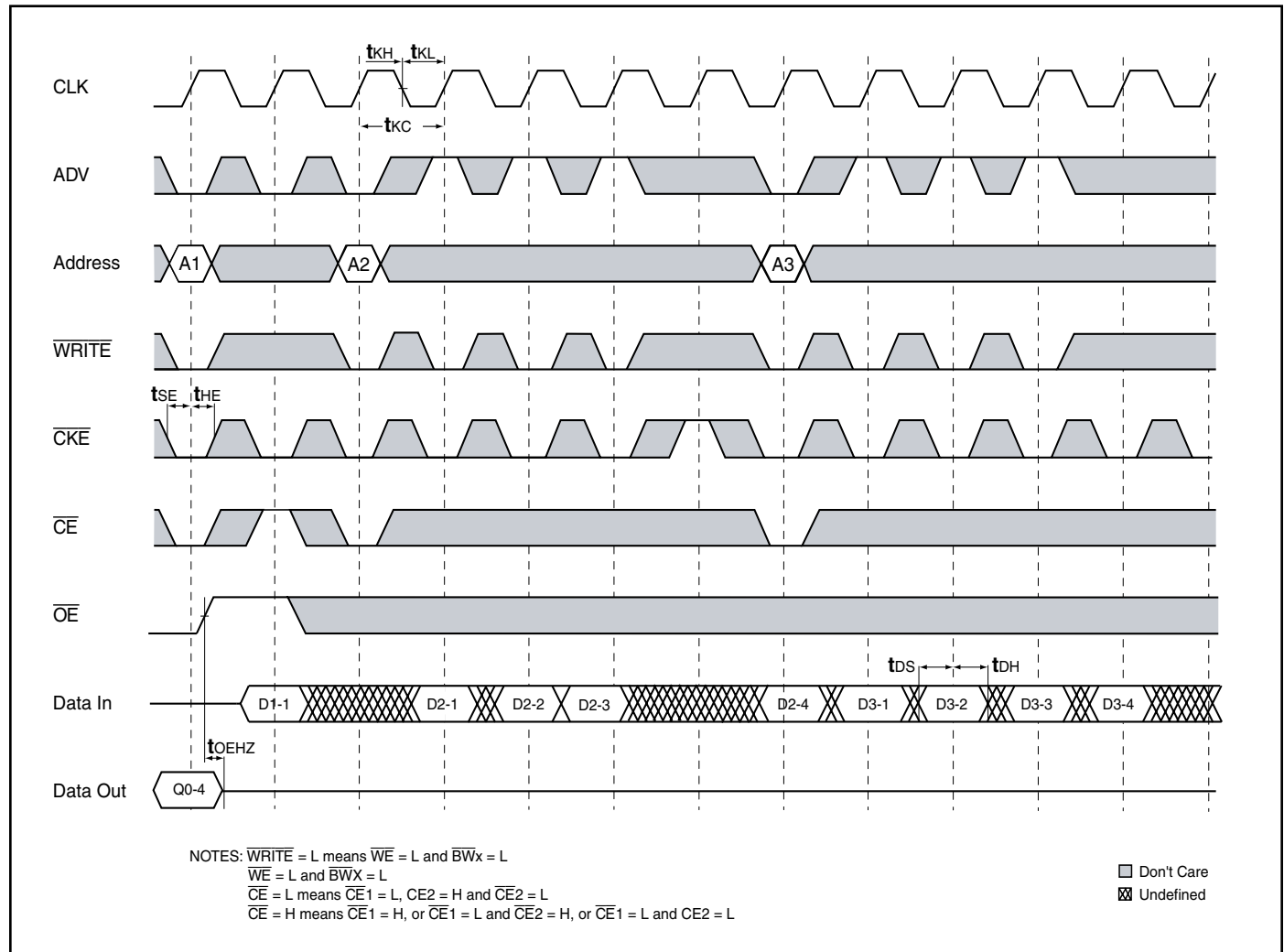
READ CYCLE TIMING



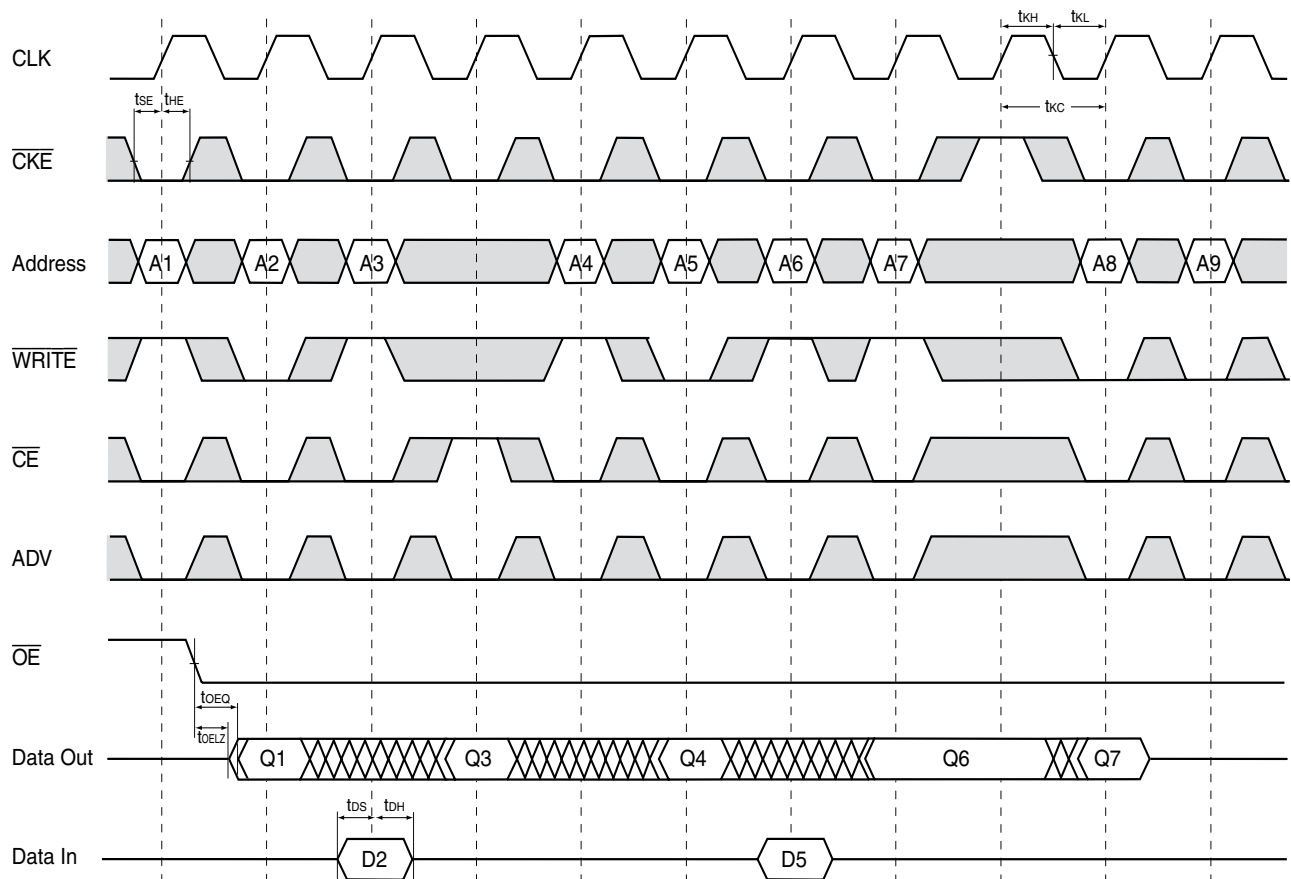
NOTES: WRITE = L means $\overline{WE}$ = L and $\overline{BWx}$ = L
 $\overline{WE}$ = L and $\overline{BWx}$ = L
 CE = L means $\overline{CE1}$ = L, $\overline{CE2}$ = H and $\overline{CE2}$ = L
 CE = H means $\overline{CE1}$ = H, or $\overline{CE1}$ = L and $\overline{CE2}$ = H, or $\overline{CE1}$ = L and $\overline{CE2}$ = L

□ Don't Care
 ⊗ Undefined

WRITE CYCLE TIMING



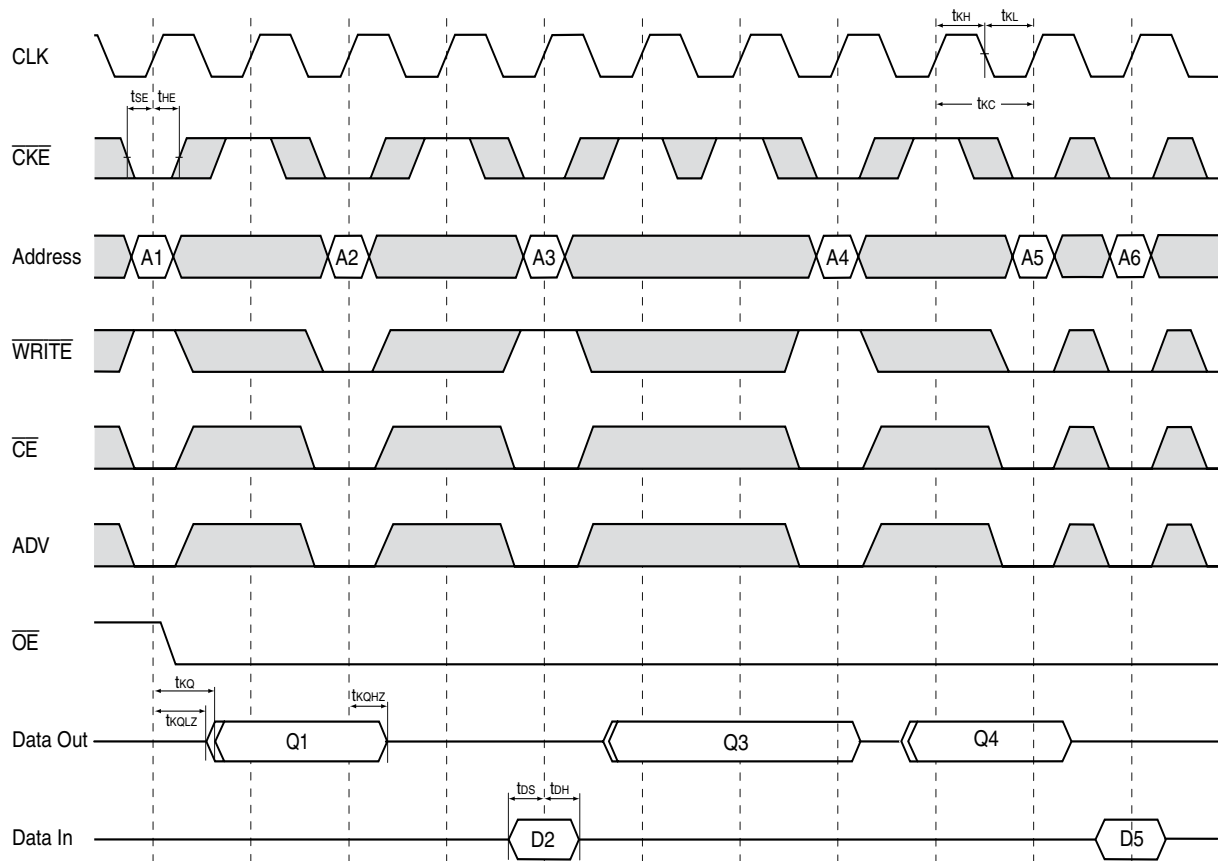
SINGLE READ/WRITE CYCLE TIMING



NOTES: $\overline{WRITE} = L$ means $\overline{WE} = L$ and $\overline{BWx} = L$
 $\overline{CE} = L$ means $\overline{CE1} = L$, $\overline{CE2} = H$ and $\overline{CE2} = L$
 $\overline{CE} = H$ means $\overline{CE1} = H$, or $\overline{CE1} = L$ and $\overline{CE2} = H$, or $\overline{CE1} = L$ and $\overline{CE2} = L$

□ Don't Care
 ▤ Undefined

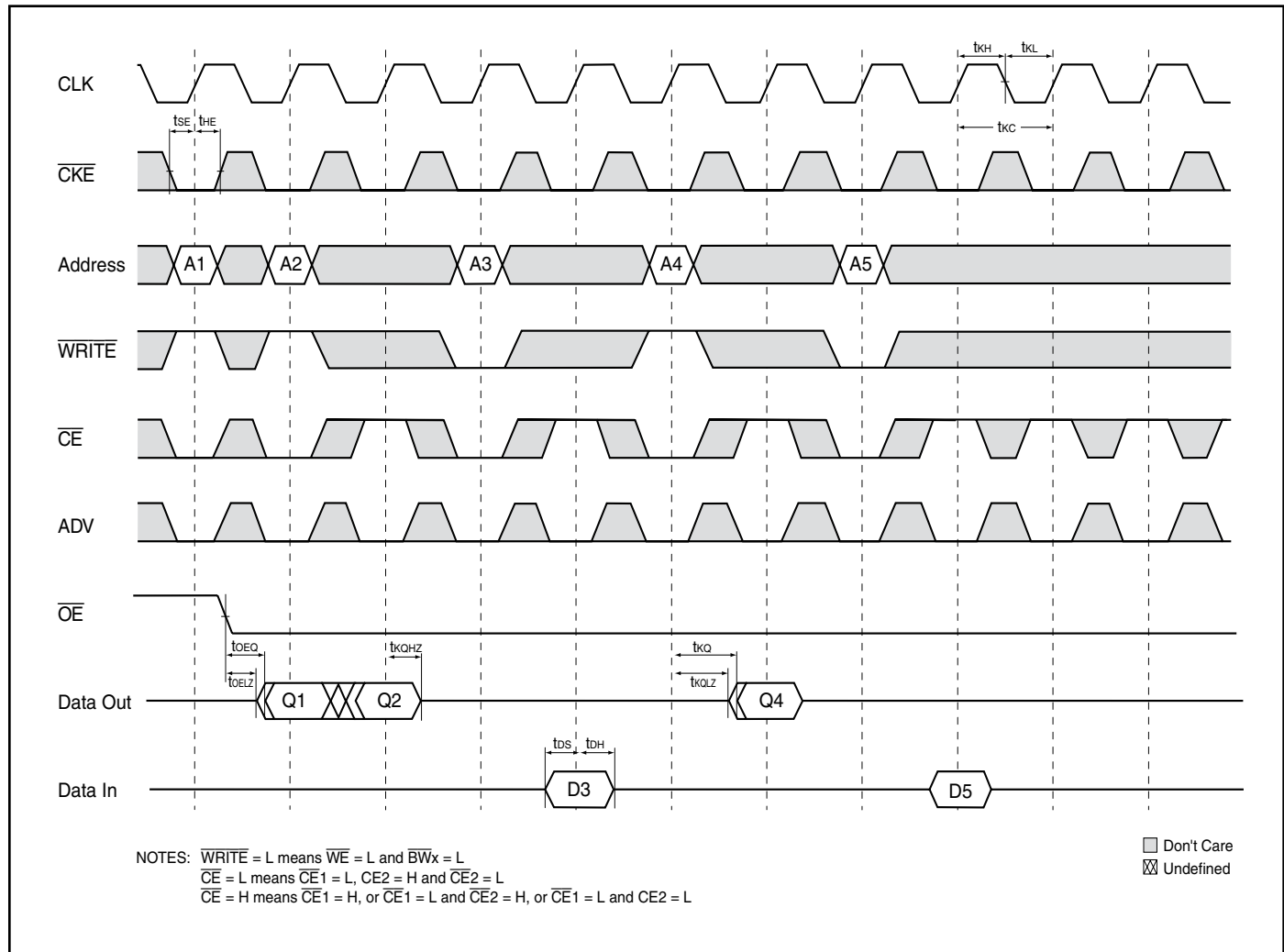
CKE OPERATION TIMING



NOTES: $\overline{\text{WRITE}} = \text{L}$ means $\overline{\text{WE}} = \text{L}$ and $\overline{\text{BWx}} = \text{L}$
 $\overline{\text{CE}} = \text{L}$ means $\overline{\text{CE1}} = \text{L}$, $\text{CE2} = \text{H}$ and $\overline{\text{CE2}} = \text{L}$
 $\overline{\text{CE}} = \text{H}$ means $\overline{\text{CE1}} = \text{H}$, or $\overline{\text{CE1}} = \text{L}$ and $\overline{\text{CE2}} = \text{H}$, or $\overline{\text{CE1}} = \text{L}$ and $\text{CE2} = \text{L}$

□ Don't Care
 ▨ Undefined

CE OPERATION TIMING



ORDERING INFORMATION ($V_{DD} = 3.3V/V_{DDQ} = 2.5V/3.3V$)

Commercial Range: 0°C to +70°C

Access Time	Order Part Number	Package
128Kx36		
6.5	IS61NLF12836A-6.5TQ	100 TQFP
	IS61NLF12836A-6.5B2	119 PBGA
	IS61NLF12836A-6.5B3	165 PBGA
7.5	IS61NLF12836A-7.5TQ	100 TQFP
	IS61NLF12836A-7.5B2	119 PBGA
	IS61NLF12836A-7.5B3	165 PBGA
256Kx18		
6.5	IS61NLF25618A-6.5TQ	100 TQFP
	IS61NLF25618A-6.5B2	119 PBGA
	IS61NLF25618A-6.5B3	165 PBGA
7.5	IS61NLF25618A-7.5TQ	100 TQFP
	IS61NLF25618A-7.5B2	119 PBGA
	IS61NLF25618A-7.5B3	165 PBGA

Industrial Range: -40°C to +85°C

Access Time	Order Part Number	Package
128Kx36		
6.5	IS61NLF12836A-6.5TQI	100 TQFP
	IS61NLF12836A-6.5B2I	119 PBGA
	IS61NLF12836A-6.5B3I	165 PBGA
7.5	IS61NLF12836A-7.5TQI	100 TQFP
	IS61NLF12836A-7.5TQLI	100 TQFP, Lead-free
	IS61NLF12836A-7.5B2I	119 PBGA
	IS61NLF12836A-7.5B3I	165 PBGA
	IS61NLF12836A-7.5B3LI	165 PBGA, Lead-free
256Kx18		
6.5	IS61NLF25618A-6.5TQI	100 TQFP
	IS61NLF25618A-6.5B2I	119 PBGA
	IS61NLF25618A-6.5B3I	165 PBGA
7.5	IS61NLF25618A-7.5TQI	100 TQFP
	IS61NLF25618A-7.5TQLI	100 TQFP, Lead-free
	IS61NLF25618A-7.5B2I	119 PBGA
	IS61NLF25618A-7.5B3I	165 PBGA

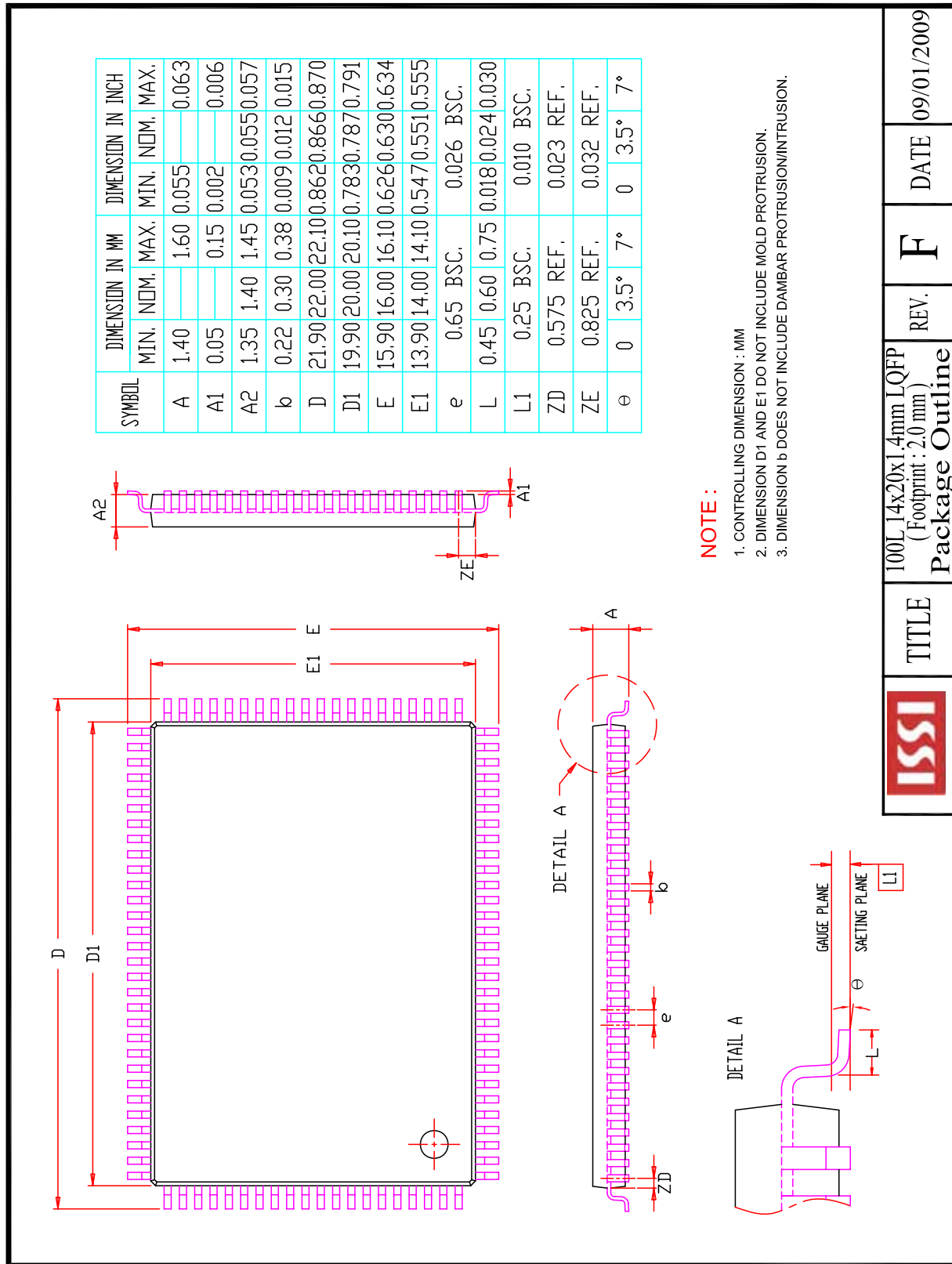
ORDERING INFORMATION ($V_{DD} = 2.5V/V_{DDQ} = 2.5V$)

Commercial Range: 0°C to +70°C

Access Time	Order Part Number	Package
128Kx36		
6.5	IS61NVF12836A-6.5TQ	100 TQFP
	IS61NVF12836A-6.5B2	119 PBGA
	IS61NVF12836A-6.5B3	165 PBGA
7.5	IS61NVF12836A-7.5TQ	100 TQFP
	IS61NVF12836A-7.5B2	119 PBGA
	IS61NVF12836A-7.5B3	165 PBGA
256Kx18		
6.5	IS61NVF25618A-6.5TQ	100 TQFP
	IS61NVF25618A-6.5B2	119 PBGA
	IS61NVF25618A-6.5B3	165 PBGA
7.5	IS61NVF25618A-7.5TQ	100 TQFP
	IS61NVF25618A-7.5B2	119 PBGA
	IS61NVF25618A-7.5B3	165 PBGA

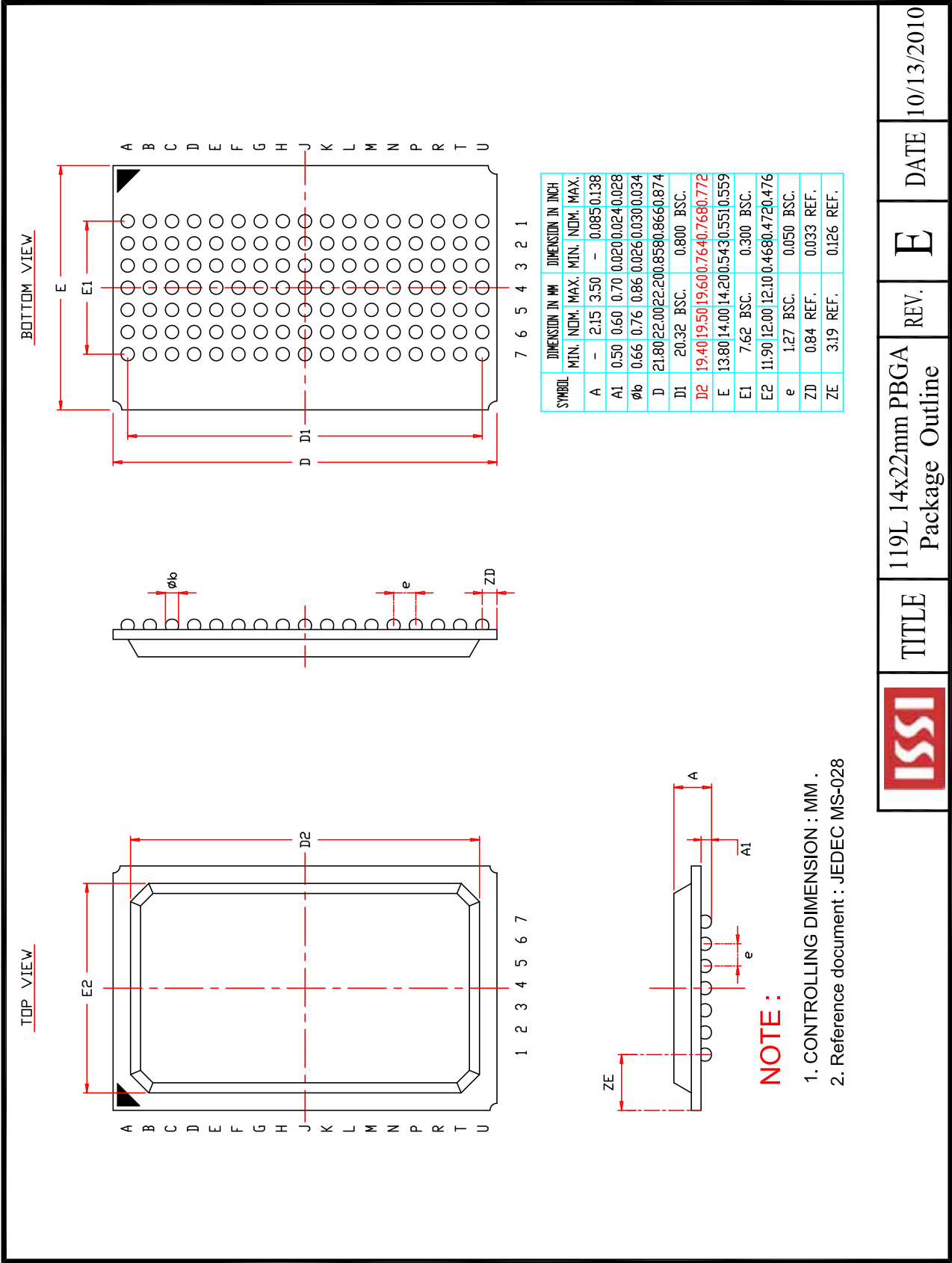
Industrial Range: -40°C to +85°C

Access Time	Order Part Number	Package
128Kx36		
6.5	IS61NVF12836A-6.5TQI	100 TQFP
	IS61NVF12836A-6.5B2I	119 PBGA
	IS61NVF12836A-6.5B3I	165 PBGA
7.5	IS61NVF12836A-7.5TQI	100 TQFP
	IS61NVF12836A-7.5B2I	119 PBGA
	IS61NVF12836A-7.5B3I	165 PBGA
256Kx18		
6.5	IS61NVF25618A-6.5TQI	100 TQFP
	IS61NVF25618A-6.5B2I	119 PBGA
	IS61NVF25618A-6.5B3I	165 PBGA
7.5	IS61NVF25618A-7.5TQI	100 TQFP
	IS61NVF25618A-7.5B2I	119 PBGA
	IS61NVF25618A-7.5B3I	165 PBGA



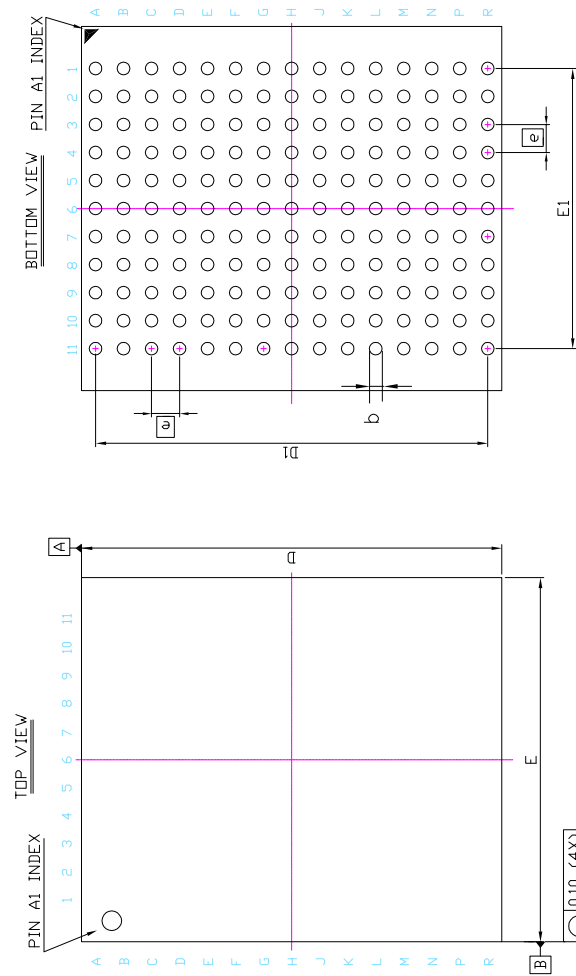
ISSI	TITLE	100L14x20x1.4mm LQFP (Footprint : 2.0 mm) Package Outline	REV.	F	DATE	09/01/2009

280-600-011 REV. A



IS61NLF12836A/IS61NVF12836A

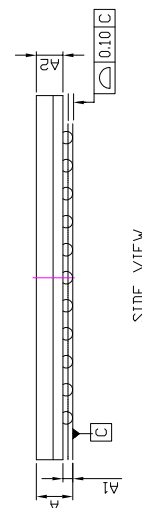
IS61NLF25618A/IS61NVF25618A



SYM.	DIMENSION (mm)			DIMENSION (inch)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A1	0.25	0.35	0.40	0.010	0.014	0.016
A2	—	0.79	—	—	0.031	—
b	0.40	0.45	0.50	0.016	0.018	0.020
D	14.90	15.00	15.10	0.587	0.591	0.594
D1	13.90	14.00	14.10	0.547	0.551	0.555
E	12.90	13.00	13.10	0.508	0.512	0.516
E1	9.90	10.00	10.10	0.390	0.394	0.398
$\bar{E}$	1.00 BSC			0.039 BSC		

NOTE :

1. CONTROLLING DIMENSION : MM .



	TITLE	165L 13x15mm TF-BGA Package Outline	REV. B	DATE 08/28/2008
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Компания «Life Electronics» занимается поставками электронных компонентов импортного и отечественного производства от производителей и со складов крупных дистрибьюторов Европы, Америки и Азии.

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- Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.
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- Работу по проектам и поставку образцов.
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- Тестирование поставляемой продукции.
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- Входной контроль качества.
- Наличие сертификата ISO.

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- Техническую поддержку проекта.
- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.



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