microelectronics group

Lucent Technologies
Bell Labs Innovations

W3000 PLL Dual-Band Frequency Synthesizer

Features

- 2.2 GHz operational
- Dual-band optimized
- Low supply current (5.1 mA)
- Surface-mount 14-pin TSSOP package
- Scaled PD gain for dual-band operation
- Programmable phase-detector polarity
- Synchronous or forced counter update loading
- Powerdown mode via external pin or serial bus
- Low-load capacitance on reference input buffer

Applications

- GSM900/1800/1900
- North American IS-136/137
- Personal Digital Cellular (Japan RCR-27)
- Personal Handy Phone (Japan RCR-28)
- CDMA (IS-95)

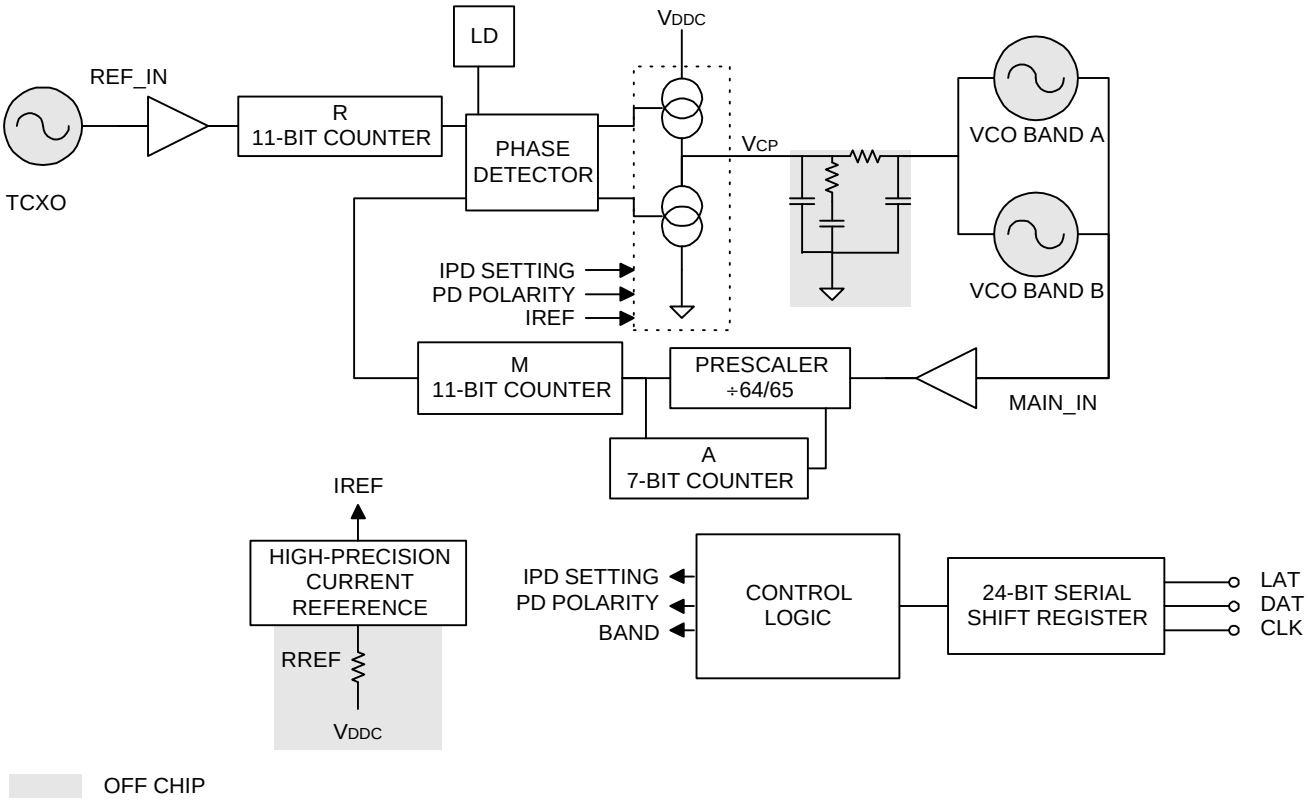


Figure 1. Block Diagram with Pinout

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Description

The W3000 is a high-performance UHF RF PLL synthesizer, designed for use in digital wireless communication applications. Particular emphasis in the design has been placed on dual-band applications, with near-seamless switching between operational bands without the need for external loop-filter circuitry other than that required for single band applications. In combination with a suitable reference crystal, UHF VCO, and associated loop-filter components, the W3000 offers a very low-noise oscillator solution.

The reference signal is divided by a programmable 11-bit counter to provide a wide range of comparison frequencies, allowing compliance with the various standards. The reference input is rising-edge triggered, and we recommend that an inverting buffer be used when the W3000 is interfaced to a commercial TCXO.

The MAIN_IN signal normally associated with the UHF VCO is fed into a dual modulus prescaler (64/65) and is then divided by the 11-bit main counter to be compared to the output of the reference counter in a digital phase detector.

The W3000 is implemented with programmable charge-pump currents to allow fast switching between bands for dual-band applications, without changing the loop filter. The charge pump can be programmed internally, or externally with a resistor (recommended). Charge pump outputs can be disabled, thereby allowing open-loop VCO modulation schemes.

With synchronous reloading, the counter reloads a new programmed value when the counter reaches zero. With forced counter reloading, the reloading occurs when the programmed word is latched in. These techniques can improve lock time when performing a dual-band hop or in start-up conditions.

The W3000 uses a standard 3-wire programming bus (data, enable, clock) that operates up to 10 MHz. This serial interface is via a 24-bit word that incorporates both register addressing and device addressing allowing two chips to share the bus.

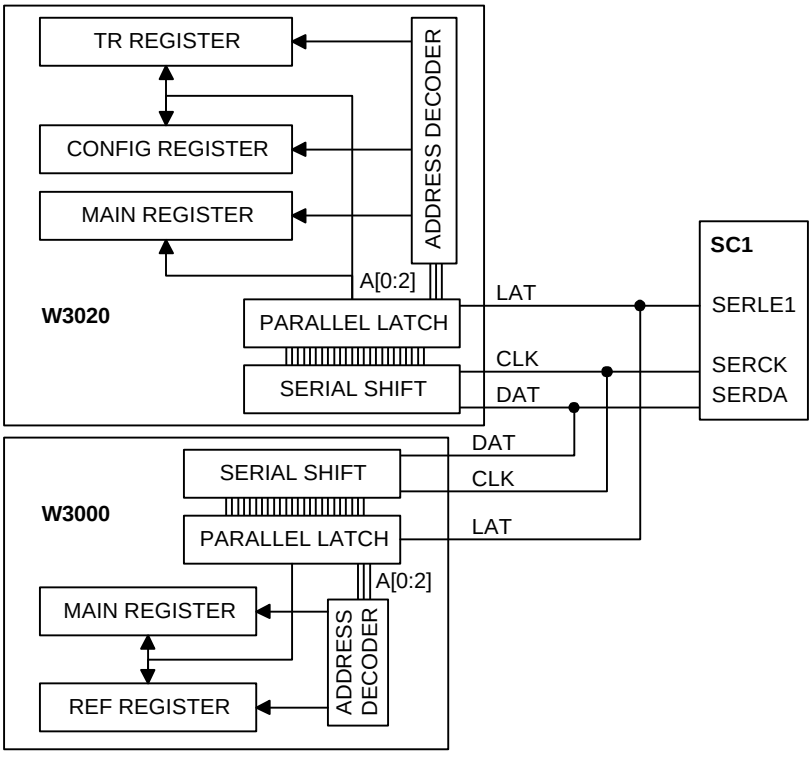


Figure 2. Serial Bus Programming

Pin Information

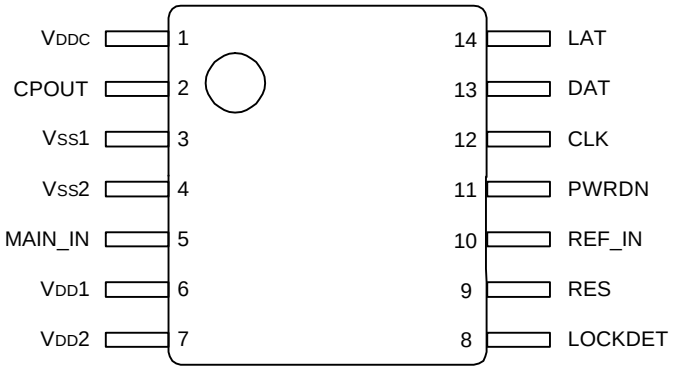


Figure 3. Pin Diagram

Table 1. Pin Descriptions

Pin	Symbol	Function	Name/Description
1	V_{DDC}	Supply	**Charge Pump Positive Supply Voltage**. Must be ≥V_{DD}. (V_{DD} = V_{DD}1 = V_{DD}2).
2	CPOUT	Output	**Charge Pump Output**.
3	V_{SS}1	Ground	**Ground 1**. Charge pump and logic ground.
4	V_{SS}2	Ground	**Ground 2**. Prescaler and reference ground.
5	MAIN_IN	Input	**VCO Signal Input**. Must be ac-coupled.
6	V_{DD}1	Supply	**Voltage Supply 1**. Prescaler supply voltage.
7	V_{DD}2	Supply	**Voltage Supply 2**. Logic and reference supply (must be equal to V_{DD}1).
8	LOCKDET	Output	**Lock Detect Output.**
9	RES	Input	**External Resistor Input**. Add resistor to V_{DDC} if required (>10 kΩ).
10	REF_IN	Input	**Reference Frequency Input**. Connection from reference oscillator. Must be ac-coupled.
11	PWRDN	Input	**Powerdown**. For low current operation. (Low is powerdown mode.)
12	CLK	Input	**Serial Input**. Programming clock line.
13	DAT	Input	**Serial Input**. Programming data line.
14	LAT	Input	**Serial Input**. Programming latch line.

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operations sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Max	Unit
Ambient Operating Temperature	T_A	–30	85	°C
Storage Temperature	T_{stg}	–65	150	°C
Lead Temperature (soldering, 10 s)	T_L	—	300	°C
Positive Supply Voltage	V_{DD}	0	4.5	Vdc
Positive Charge Pump Supply Voltage	V_{DDC}	0	4.5	Vdc
Power Dissipation	P_D	—	250	mW
ac Input Voltage	—	0	V_{DD}	Vp-p
Digital Voltages	—	Vss – 0.3	V_{DD} + 0.3	Vdc

Electrostatic Discharge Caution

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. Lucent Technologies Microelectronics Group employs a human-body model (HBM) and a charged-device model (CDM) for ESD-susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used to define the model. No industry-wide standard has been adopted for CDM. However, a standard HBM (resistance = 1500 Ω, capacitance = 100 pF) is widely used and, therefore, can be used for comparison purposes.

Parameter	Model	Min	Max	Unit
ESD Threshold Voltage	HBM	1000	—	V
ESD Threshold Voltage (corner pins)	CDM	1000	—	V
ESD Threshold Voltage (noncorner pins)	CDM	1500	—	V

Electrical Characteristics

Table 2. General Specifications

Conditions (unless otherwise specified): V_{DD} = 2.7 V; T_A = 25 °C ± 3 °C; V_{REF} = 0.25 Vp-p, V_{DDC} = 2.85 V.

Parameters	Symbol	Min	Typ	Max	Unit
Ambient Operating Temperature	T_A	–30	25	85	°C
Nominal Operating Voltage	V_{DD}	2.7	2.85	3.6	V
Nominal Charge Pump Operating Voltage	V_{DDC}	V_{DD}	2.85	3.6	V
Power Supply Current†	I_{DD}	—	5.1	8.0	mA
Powerdown Current‡	I_{DD}	—	0.1	20	µA
Digital Inputs:					
Logic High Voltage	V_{IH}	0.7 * V_{DD}	V_{DD}	V_{DD} + 0.15	V
Logic Low Voltage	V_{IL}	– 0.3	GND	0.3 * V_{DD}	V
Logic High Current (V_{IH} = V_{DD} + 0.15 V)	$\|I_{IH}\|$	—	—	10	µA
Logic Low Current (V_{IL} = –0.3 V)	$\|I_{IL}\|$	—	—	10	µA
Digital Outputs:					
Logic High Voltage ($\|I_{OH}\|$ = 2 mA)	V_{OH}	V_{DD} – 0.4	—	—	V
Logic Low Voltage ($\|I_{OL}\|$ = 2 mA)	V_{OL}	—	—	0.4	V

† ($I_{DD}1$ + $I_{DD}2$ + $I_{DD}C$) under locked condition, V_{DDC} = 2.85 V; f_{VCO}.= 1200 MHz; f_{REF} = 13 MHz.
‡ ($I_{DD}1$ + $I_{DD}2$ + $I_{DD}C$) V_{IL} = 0 Vdc on all logic input pins.

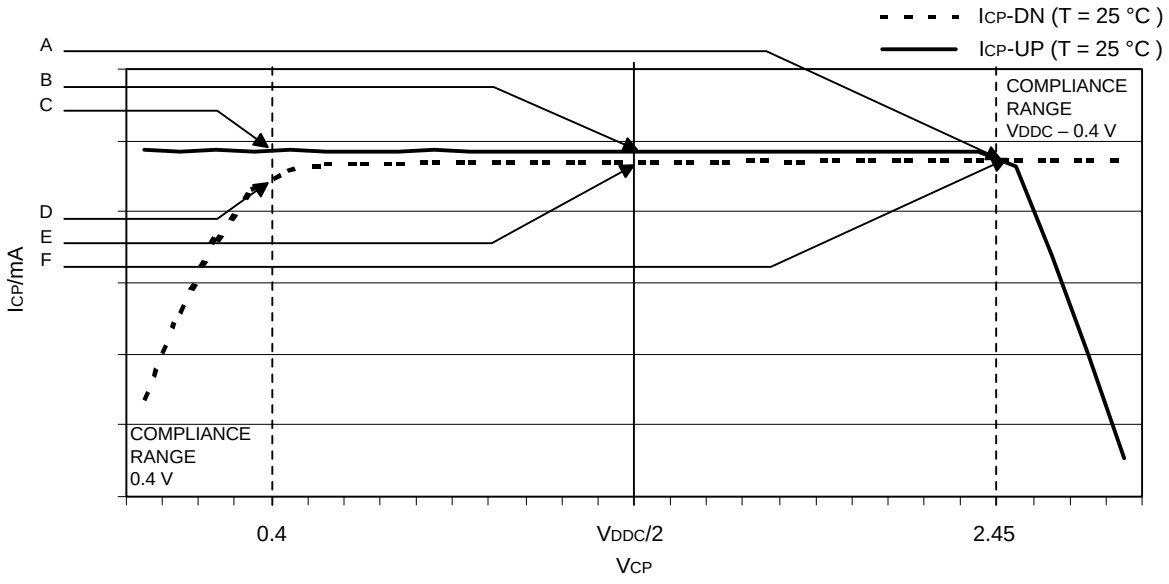
Table 3. Electrical Specifications

Conditions (unless otherwise specified): V_{DD} = 2.7 V; T_A = 25 °C ± 3 °C; V_{REF} = 0.25 Vp-p, V_{DDC} = 2.85 V.

Parameter	Symbol	Min	Typ	Max	Unit
Main Input Frequency Range	f_{VCO}	0.5	—	2.2	GHz
Main Input Level (1100 MHz—1750 MHz)	V_{MAIN}	–20	—	6	dBm/50 Ω*
Main Input Level†	V_{MAIN}	–10	—	6	dBm/50 Ω*
Reference Input Frequency Range	f_{REF}	8	—	30	MHz
Reference Input Shunt Resistance	—	20	30	—	kΩ
Reference Input Shunt Capacitance	—	—	1.2	3	pF
Reference Input Slew Rate	—	41	60	—	mV/ns
Reference Input Level	V_{REF}	0.25	—	2.00	Vp-p
Phase Detector Comparison Frequency	f_{COMP}	0.025	—	2	MHz
External Resistor Value (pin 9 to V_{DDC})	—	10	18	—	kΩ
Phase Detector Range	—	–2 π	—	2 π	rad.
Phase Detector Noise Floor, ±150 Hz offset (25 kHz comparison frequency) ‡	—	—	–167	—	dBc/Hz

*Equivalent voltage of a 50 Ω terminated source.
† Frequencies outside the 1100 MHz—1750 MHz range and up to and including 2200 MHz.
‡ f_{VCO} = 1190 MHz; V_{REF} = 1.4 Vp-p.

Charge Pump Current



A: CP UP CURRENT AT $V_{CP} = V_{DDC} – 0.4$.
B: CP UP CURRENT AT $V_{CP} = V_{DDC}/2$.
C: CP UP CURRENT AT $V_{CP} = 0.4$.
D: CP DOWN CURRENT AT $V_{CP} = 0.4$ V.
E: CP DOWN CURRENT AT $V_{CP} = V_{DDC}/2$.
F: CP DOWN CURRENT AT $V_{CP} = V_{DDC} – 0.4$.

Figure 4. Charge Pump Current vs. Voltage

Table 4. Charge Pump Specifications

Conditions (unless otherwise specified): V_{DD} = 2.7 V; T_A = 25 °C ± 3 °C; V_{DDC} = 2.85 V; $V_{CP} = V_{DDC}/2$; R_{REF} = 18 kΩ.

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Charge Pump Output Current	I_{CP} = 0.7 mA	I_{UP}	0.6	0.7	0.8	mA
	I_{CP}= 0.7 mA	I_{DN}	–0.8	–0.7	–0.6	mA
	I_{CP} = 0.9 mA	I_{UP}	0.8	0.9	1.0	mA
	I_{CP} = 0.9 mA	I_{DN}	–1.0	–0.9	–0.8	mA
	I_{CP} = 1.9 mA	I_{UP}	1.6	1.9	2.2	mA
	I_{CP} = 1.9 mA	I_{DN}	–2.2	–1.9	–1.6	mA
	I_{CP} = 2.5 mA	I_{UP}	2.1	2.5	2.9	mA
	I_{CP} = 2.5 mA	I_{DN}	–2.9	–2.5	–2.1	mA
CP High-Impedance State Current	0.4 ≤ V_{CP} ≤ V_{DDC} – 0.4 V, –30 °C < T_A < +85 °C	I_{TRI}	—	0.1	20	nA
CP Sink vs. Source Mismatch[1]	T_A = 25 °C	—	—	3	15	%
CP Current vs. Voltage[2]	0.4 ≤ V_{CP} ≤ V_{DDC} – 0.4 V, T_A = 25 °C	—	—	2	8.5	%
CP Current vs Temperature[3]	–30 °C < T_A < +85 °C	—	—	8	10	%

Notes (refer to Figure 4 for definitions):
1. ICP-DN vs ICP-UP = charge pump output current up vs down mismatch = [|E| – |B|]/[1/2 * {|E| + |B|}] * 100%.
2. ICP vs VCP = charge pump output current magnitude variation vs voltage = [1/2 * {|F| – |D|}]/[1/2 * {|F| +|D|}] * 100% and [1/2 * {|A| - |C|}]/[1/2 *{|A| + |C|}] * 100%.
3. ICP vs TA = charge pump output current magnitude variation vs. temperature = [|E @ temp| – |E @ 25 °C|]/|E @ 25 °C| * 100% and [|B @ temp| – |B @ 25 °C|]/|B @ 25°C| * 100%.

PLL Programming Information

The oscillator frequency is selected according to the following expression:

$$f_{VCO} = \frac{[(P * M) + A] * f_{REF}}{R}$$

where:

f_{VCO} = VCO frequency

P/(P + 1) = Dual modulus prescaler

M = Programmable counter ratio (2 to 2047), M > A

A = Swallow counter ratio (0 to M – 1 or 127)

f_{REF} = External reference oscillator frequency

R = Reference counter ratio (2 to 2047)

Example

You wish to have a VCO operating at 1172 MHz, ability to step the frequency in 200 kHz steps, and a reference clock at 13 MHz.

Step 1:

Calculate the reference counter ratio R

$$R = \frac{13\ \text{MHz}}{200\ \text{kHz}} = 65$$

Step 2: Calculate M & A

$$f_{VCO} = \frac{[(P * M) + A] * f_{REF}}{R}$$

$$1172 = \frac{[(64 * M) + A] * 13}{65}$$

$$(64 * M + A) = \frac{1172 * 65}{13} = 5860$$

$$\frac{5860}{64} = 91\frac{36}{64}$$

M is an integer, and so is A; therefore, M = 91, and A = 36.

Serial Data Input

The PLL is programmed via a 3-wire serial bus, utilizing a data pin (DAT), a clock pin (CLK), and a latch pin (LAT).

Serial Bus Timing Information

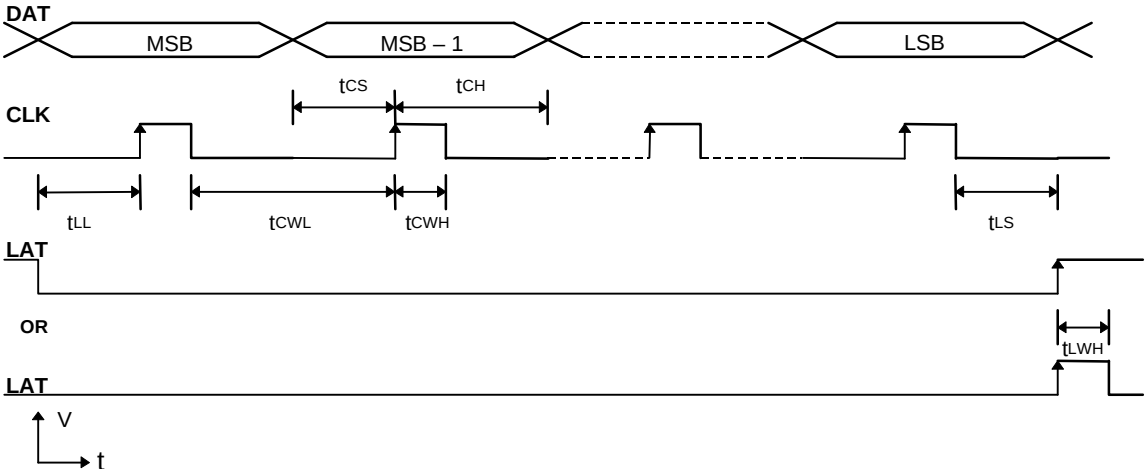


Figure 5. Serial Bus Timing Diagram

Table 5. Serial Bus Timing Information

Symbol	Parameter	Min	Typ	Max	Unit
t_{CS}	Data to Clock Setup Time	33	—	—	ns
t_{CH}	Data to Clock Hold Time	10	—	—	ns
t_{CWH}	Clock Pulse Width High	33	—	—	ns
t_{CWL}	Clock Pulse Width Low	33	—	—	ns
t_{LS}	Clock Falling Edge to Latch High Setup Time	0	—	—	ns
t_{LWH}	Latch Pulse Width	50	—	—	ns
t_{LL}	Latch to Clock Setup Time	33	—	—	ns
f_{CLK}	Clock Input Frequency	—	—	10	MHz

Functional Descriptions

The W3000 contains a reference register (REF) and a main register (MAIN). The REF register is used for programming the division ratio of the reference clock and for initial setup of the operation modes. The MAIN register is intended for programming that can occur frequently, e.g., dynamic channel switching and putting the W3000 into power-saving mode.

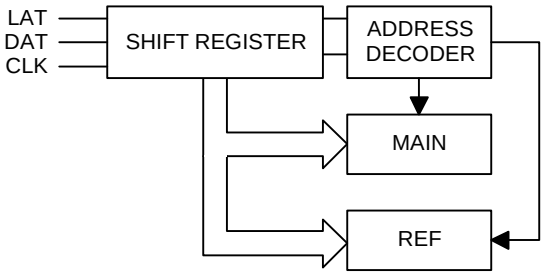


Figure 6. Register Programming Diagram

Both REF and MAIN registers are programmed separately, each with a 24-bit data sequence. The last bit is that which immediately precedes a low-to-high latch input transition occurring while the CLOCK input is low. Bit 24 is loaded first, and bit 1 is loaded last. The last bit in the serial sequence is C0. This bit is used to direct the 24-bit sequence to the MAIN or REF registers.

Table 6. C0:C1: MAIN and REF Register Addressing (Destination of Serial Data) (Bits 1 and 24)

C1	C0	Addressed Register
0	0	MAIN
0	1	REF
1	0	Secondary Address
1	1	Secondary Address

The first bit, C1, allows the W3000 to share the serial bus. When C1 is a logic high, the W3000 ignores the data sent on the serial bus.

REF Register

This section describes each bit of the reference register. The REF register is used for programming the division ratio of the reference clock and for initial setup of the operation modes.

Table 7. REF Register Bit Description (C0 = 1, C1 = 0)

Bit	Name	Description
1	C0 = 1	Register address bit. C0 = 1 for REF (last bit in serial sequence).
2:12	R[1:11]	Reference frequency divide ratio.
13	D1	Forced counter reload programming (synchronous/asynchronous).
14	D2	Charge pump disable function.
15:16	D3, D4	Programable charge pump current for frequency band 2.
17	D5	Phase detector polarity.
18:19	D6, D7	Programable charge pump current for frequency band 1.
20	RE	Reset for first programming after powerup (1 = reset).
21	ERES	Enables external resistor (on RES pin) to set charge pump current.
22	EN1	Enable W3000. (0 is powerdown.)
23	LD	Lock detect output enable.
24	C1 = 0	Secondary address bit (first bit in serial sequence).

Table 8. REF Register

Last bit in serial sequence ↙ ↘ First bit in serial sequence

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
C0 = 1	R 1	R 2	R 3	R 4	R 5	R 6	R 7	R 8	R 9	R 10	R 11	D 1	D 2	D 3	D 4	D 5	D 6	D 7	RE	ERES	EN	LD	C1 = 0

Table 9. R1:R11: Reference Divider Ratio (Bits 2 to 12)

R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	Divide Ratio R
—	—	—	—	—	—	—	—	—	—	—	—*
0	0	0	0	0	0	0	0	0	1	0	2
0	0	0	0	0	0	0	0	0	1	1	3
. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .
1	1	1	1	1	1	1	1	1	1	1	2047

*The reference counter cannot operate with division numbers less than 2.

REF Register (continued)

Table 10. D1: Forced Counter Reload (Bit 13)

D1	Response
0	Synchronous counter reloading update
1	Forced counter reload (M, R, A)

With synchronous reloading, the counter reloads a new programmed value when the counter reaches zero. With forced counter reloading, the reloading occurs when the programmed word is latched in. This can improve lock time when performing a dual-band hop.

Table 11. D2: Charge Pump Off Mode (Bit 14)

D2	Response
0	Charge pump enabled
1	Charge pump off (high impedance)

This allows the disabling of the charge pump for systems that directly modulate an open-loop VCO.

Table 12. Band and Charge Pump Current (Band 1, Bits 18 and 19; Band 2, Bits 15 and 16)

Band	D3 Bit 15	D4 Bit 16	D6 Bit 18	D7 Bit 19	Charge Pump Current I_{SET}
1	x	x	0	0	0.7 mA
1	x	x	1	0	0.9 mA
1	x	x	0	1	1.9 mA
1	x	x	1	1	2.5 mA
2	0	0	x	x	0.7 mA
2	1	0	x	x	0.9 mA
2	0	1	x	x	1.9 mA
2	1	1	x	x	2.5 mA

The charge pump current is selected by bit 23 of the MAIN register. Setting bit 23 to a 0 will select band 1, which is established with bits 18 and 19 of the REF register. Likewise, setting bit 23 to a 1 will select band 2, which is established with bits 15 and 16 of the REF register. This allows the charge pump current to be dynamically changed along with the VCO frequency.

The PLL loop natural frequency is proportional to charge pump current and inversely proportional to the N count. Therefore, when the ratio of charge pump current and VCO frequency is the same, the loop natural frequency does not change. This allows the same loop filter to be used for two different VCO frequencies. For example, in a GSM900/1800 system with VCOs running at 1190 MHz/1570 MHz, the current could be set to 1.9 mA for GSM900 and 2.5 mA for GSM 1800 to compensate for the change in division ratios. The current setting may also be determined by an external resistor. (See Table 15.) In that case, the ratio between the currents programmed will stay the same, but the absolute level will be resistor-dependent.

REF Register (continued)

Table 13. D5: Phase Detector Polarity (Bit 17)

D5	Phase Detector Polarity
0	Negative slope
1	Positive slope

The phase detector can be programmed for either a negative or positive slope to accommodate the VCO and low-pass filter characteristics. (See Figure 7.)

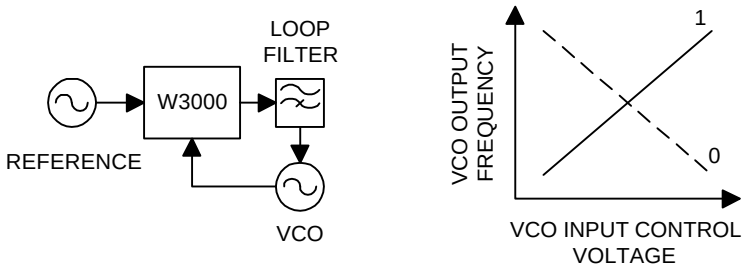


Figure 7. Programming the Phase Detector Slope

Table 14. RE: Reset (Bit 20)

RE	Response
0	Operation mode
1	Reset MAIN and secondary registers

After the power supply is turned on, the REF register must be programmed with a reset. This must be followed by a programming of the MAIN register before or at the enabling of the PLL circuit.

The RE bit will clear itself, and is required to ensure correct initialization of the IC. This results in the following conditions:

- The RE bit is cleared back to 0.
- The device is in powerdown mode, since the EN[1:2] bits are also cleared.
- Previous reference and main counter values are maintained.

REF Register (continued)

Table 15. ERES: External Resistor Setting for Charge Pump Current (Bit 21)

ERES	External Resistor Status
0	Use internal charge pump current setting (not tested in production)
1	Use external resistor to set charge pump current (recommended)

If bit 21 is set to 0, the W3000 uses its internal current source to set the charge pump currents, with the values shown in Table 12. If bit 21 is set to 1, the charge pump current is set by an external resistor between pin 9 (RES) and V_{DDC}. In this case, the charge pump current is given by the following formula:

$$I_{CP} = I_{SET} * \frac{V_{DDC} - 1.05}{100\,\mu A * R_{REF}}$$

where

I_{CP} = Nominal charge pump current.

I_{SET} = Current setting as in Table 12.

RREF = Value of external current reference resistor. See Table 3 for appropriate value.

A tight-tolerance R_{REF} resistor is recommended.

Table 16. EN1: Synthesizer Enable (Bit 22)

PWRDN (Input Pin 11)	EN1	Mode
High	0	Powerdown
High	1	Enable
Low	0	Powerdown
Low	1	Powerdown

The MAIN register also contains an enable bit, EN2. The W3000 is enabled and powered down with either the REF or the MAIN register, whichever was programmed more recently. The contents of the MAIN and REF registers are maintained in powerdown mode, providing supply voltages are maintained.

Table 17. LD: Lock Detect Enable (Bit 23)

LD (Bit 23)	Mode	PLL Condition	Output Level on Pin 8 LockDet
0	Disabled	Locked	High
0	Disabled	Unlocked	High
1	Enabled	Locked	High
1	Enabled	Unlocked	Low

MAIN Register

The MAIN register is intended for programming that can occur frequently for dynamic channel switching and putting the W3000 into power-saving mode.

Table 18. MAIN Register Bit Description (C0 = 0, C1 = 0)

Bit	Name	Description
1	C0 = 0	Register address bit. C0 = 0 for MAIN (last bit in serial sequence).
2:8	A[1:7]	Swallow counter for prescaler modulus control.
9:19	M[1:11]	Main counter.
20	Reserved	—
21	Reserved	—
22	EN2	Enable all PLL circuits (0 = powerdown mode).
23	B	Band select for charge pump current control (band 1 = 0, band 2 = 1).
24	C1 = 0	Secondary address bit.

Table 19. MAIN Register

Last bit in serial sequence ← → First bit in serial sequence

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
C0 = 0	A 1	A 2	A 3	A 4	A 5	A 6	A 7	M 1	M 2	M 3	M 4	M 5	M 6	M 7	M 8	M 9	M 10	M 11	X	X	EN	B	C1 = 0

Note: X bits are don't care bits.

Table 20. A1:A7: Swallow Counter Count (Bits 2 to 8)

A7 Bit 8	A6 Bit 7	A5 Bit 6	A4 Bit 5	A3 Bit 4	A2 Bit 3	A1 Bit 2	Counter Ratio
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
0	0	0	0	0	1	0	2
. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .
0	1	1	1	1	1	1	63
. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .
1	1	1	1	1	1	1	127

MAIN Register (continued)

Table 21. M1:M11: Programmable Main Counter Divide Ratio (Bits 9 to 19)

M11 Bit 19	M10 Bit 18	M9 Bit 17	M8 Bit 16	M7 Bit 15	M6 Bit 14	M5 Bit 13	M4 Bit 12	M3 Bit 11	M2 Bit 10	M1 Bit 9	Divide Ratio M
0	0	0	0	0	0	0	0	0	1	0	2
0	0	0	0	0	0	0	0	0	1	1	3
. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .
0	0	0	1	1	1	1	1	1	1	1	255
. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .	. . .
1	1	1	1	1	1	1	1	1	1	1	2047

The main counter divides the frequency of the prescaler output signal and sources the divided signal to the phase comparator.

Table 22. EN2: Synthesizer Enable (Bit 22)

PWRDN	EN2	Mode
H	0	Powerdown
H	1	Enable
L	0	Powerdown
L	1	Powerdown

The REF register also contains an enable bit, EN1 (see Table 16). The W3000 is enabled or powered down with either the REF or MAIN register, whichever was programmed more recently. The contents of the MAIN and REF registers are maintained in powerdown mode, providing supply voltages are maintained.

Table 23. B: Band Select (Bit 23)

B	Band
0	Band 1
1	Band 2

In dual-band operation, this bit allows the use of one loop filter by setting the charge pump current to correspond to the frequency of the band selected. See Table 12 for the available charge pump current settings.

PLL Lock-Detect Function

The W3000 provides a basic lock-detect function for fault finding or for system specification requirements.

Inside the W3000, the length of the up or down pulses applied to the loop filter is compared with a reference clock period. If the current pulses are shorter than a reference clock period for 15 consecutive comparison periods, the LD line is asserted. If a current pulse is detected that is longer than a reference clock period, the LD line is unset.

The LD line gives a signal to indicate a PLL fault condition. It does not provide a true loop-locked output. For example, in a GSM system with a reference clock of 13 MHz and a comparison frequency of 200 kHz, the current pulses only have to be less than 1/65 of a cycle for 15 consecutive times for the LD line to be asserted. This equates to ~0.4º of phase. In the worst case, if the phase stays inside this limit, moving from one extreme to the other, the frequency will only be within 0.2%, i.e., 4 MHz on a 2 GHz VCO.

The LD output from the W3000 is a standard logic signal and requires no external comparison or R-C filters.

Typical Performance Characteristics

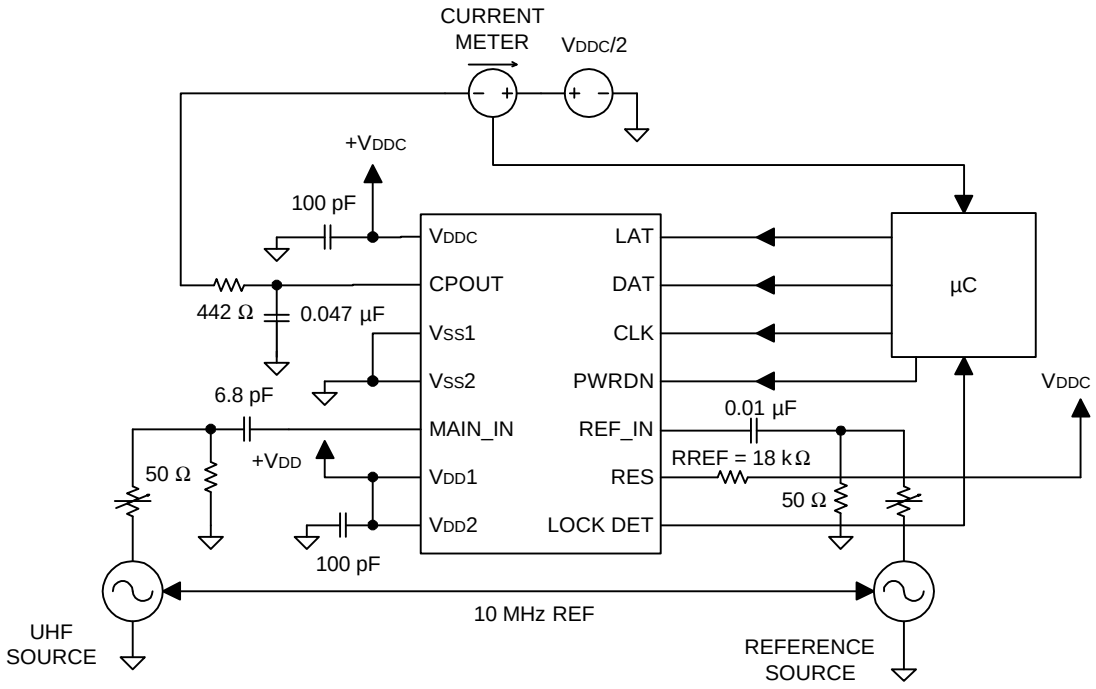


Figure 8. MAIN_IN and REF_IN Sensitivity Test Circuit Diagram

MAIN_IN and REF_IN are set to cause a small beat frequency at the phase detector input. This generates a sawtooth signal at the charge pump output of known slope. The amplitude of the UHF source is decreased. The sensitivity limit is reached when the slope of this waveform deviates from the calculated value. This is then repeated for the reference source.

MAIN_IN Input Parallel Equivalent Circuit

The input impedance is high, and can best be represented by the model shown in Figure 9.

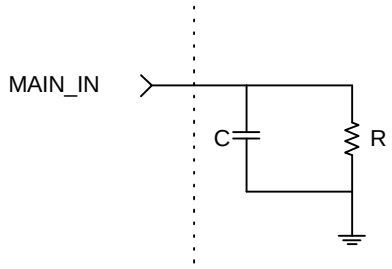


Figure 9. MAIN_IN Parallel Equivalent Circuit

Table 24. MAIN_IN Input Parallel Equivalent Circuit Values

Frequency (MHz)	C (pF)	R (Ω)
600	0.88	3680
800	0.87	2650
1000	0.85	2370
1200	0.85	1970
1400	0.86	1580
1600	0.92	1230
1800	1.00	740
2000	1.10	590
2200	1.20	480

Application Example

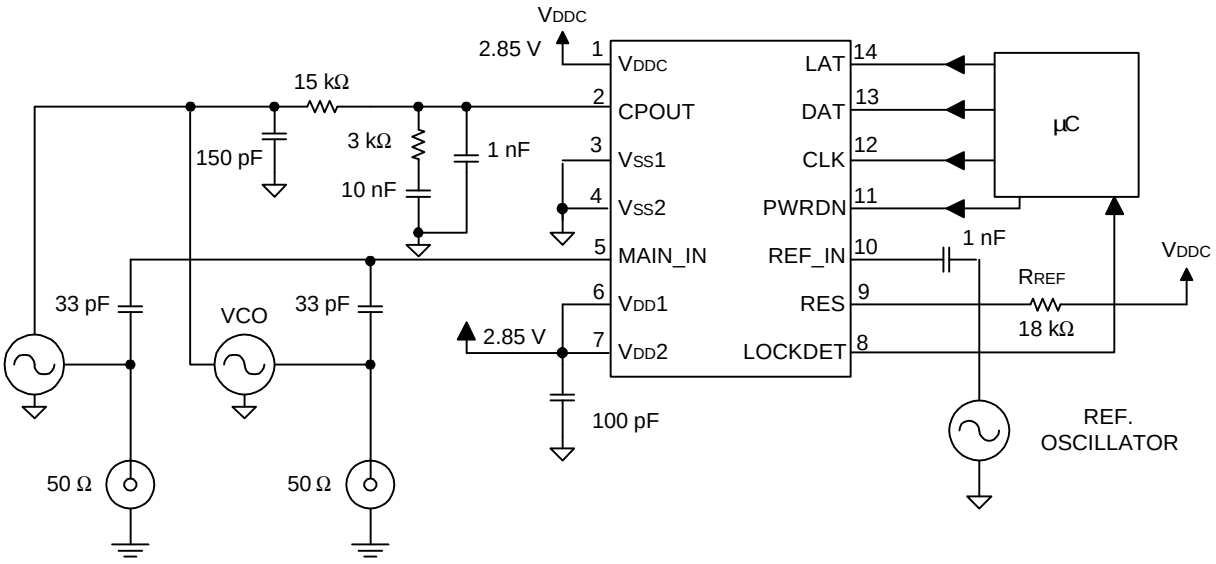


Figure 10. Application Circuit Diagram

Application Information

A typical PLL system can be modeled as follows:

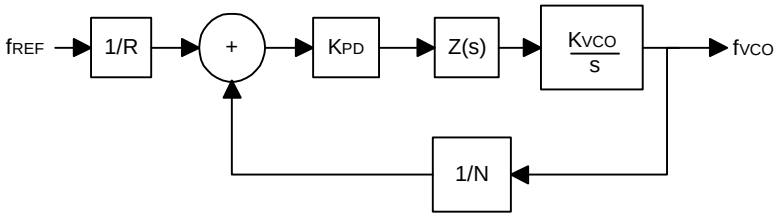


Figure 11. Typical PLL Model

K_{PD} = Phase detector in mA/2π rad

Z(s) = Loop filter

K_{VCO} = VCO gain in MHz/V

N = Total divide ratio

R = Reference divide ratio

Where the open loop gain is:

$$G(s)_{OPEN} = \frac{K_{PD} * Z(s) * Kvco}{Ns}$$

Where

$s = j\omega$

The circuit shown in Figure 12 uses a passive third-order loop filter for the element Z(s), defined by the network:

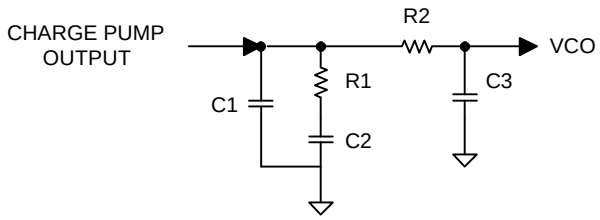


Figure 12. Third-Order Loop Filter

The purpose of the loop filter is to provide response with bandwidth sufficient not only to allow a quick lock time but also to meet phase-noise and reference sideband requirements. Addition of a third pole formed by R2 and C3 will improve reference sideband performance with little overall impact on the loop performance. A reasonable practical limit is that the f comparison is greater than 5 times loop bandwidth.

Application Information (continued)

General rules for the values of these components have been derived many times[1], and are quoted here merely for reference. If:

$$T1 = \frac{\sec\phi - \tan\phi}{\omega_p}$$

$$T2 = \frac{1}{\omega_c^2 * (T1 + T3)}$$

$$T3 = \sqrt{\frac{10^{attn/20} - 1}{(2\pi * F_{REF})^2}}$$

where

ϕ = Phase margin required, normally 45° for a critically damped response.

ω_p = Loop bandwidth.

ω_c = Loop bandwidth modified for extra pole of R3 and C3, as described by:

$$\omega_c = \frac{\tan\phi * (T1 + T3)}{(T1 + T3)^2 + (T1 * T3)} * \left[\sqrt{1 + \frac{(T1 + T3)^2 + (T1 * T3)}{[\tan\phi * (T1 + T3)]^2}} - 1\right]$$

f_{REF} = Reference frequency.

atten = Attenuation provided by the third pole at the reference frequency.

The loop filter values can then be derived as:

$$C1 = \frac{T1}{T2} * \frac{K_{PD} * K_{VCO}}{\omega_c{}^2 * N} * \left[\frac{(1 + \omega_c^2 * T2^2)}{(1 + \omega_c{}^2 * T1^2)(1 + \omega_c{}^2 * T3^2)}\right]^{1/2}$$

$$C2 = C1 * \left(\frac{T2}{T1} - 1\right)$$

$$R1 = \frac{T2}{C2}$$

The final pole, consisting of R2 and C3, should be chosen such that the following guidelines are followed:

$$C3 \le \frac{C1}{10} \text{ and } R2 \ge 2 * R1$$

1. Rohde, Ulrich L., *Digital PLL Frequency Synthesizers Theory and Design*, Prentice-Hall, 1983.

Application Information (continued)

For example, take a GSM application where a loop bandwidth of 22 kHz is required.

Other parameters specified by the system are listed below:

Parameter	Value
VCO Gain (K_{VCO})	88 MHz/V
Charge Pump Current (I_{CP})	2.5 mA
Divider Ratio (value of midband frequency used) (N)	7850
Required Phase Margin	45°
Reference Frequency Attenuation from Additional Pole	20 dB

Using the formulas above, the three time constants can be calculated as follows:

$T1 = 2.63697E - 10^{-6}$ s

$T2 = 3.14484E - 10^{-5}$ s

$T3 = 2.38732E - 10^{-6}$ s

From these values, we can derive the initial component values as follows:

$R1 = 2992\ \Omega$

C1 = 0.96 nF

C2 = 10.5 nF

If we choose R2 = 15 kΩ, then

C3 = 159 pF

From these initial values, the loop filter components used in the application circuit can be derived through practical optimization.

Typical Performance Data

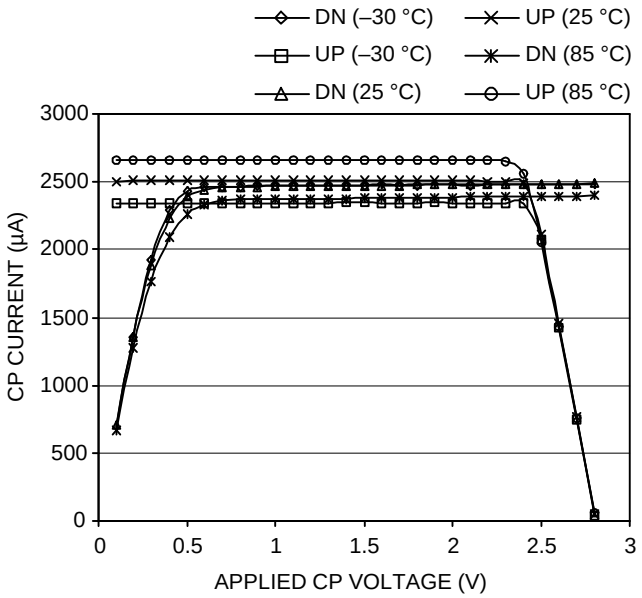


Figure 13. Charge Pump Current vs. Voltage and Temperature (2.5 mA)

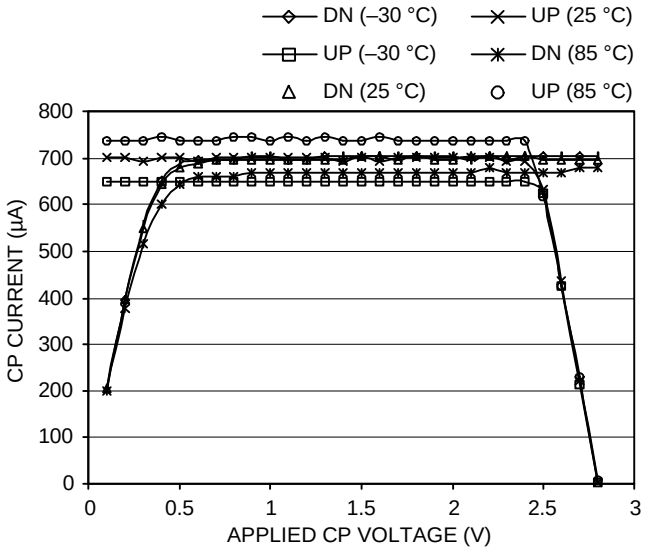


Figure 14. Charge Pump Current vs. Voltage and Temperature (0.7 mA)

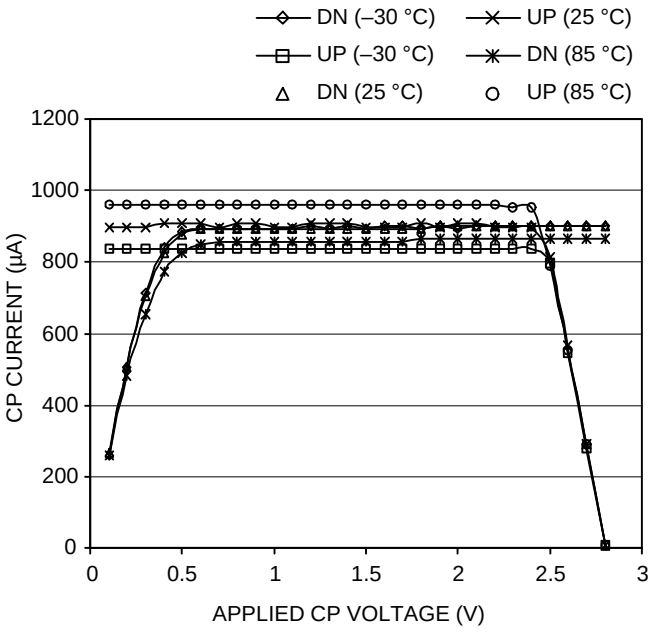


Figure 15. Charge Pump Current vs. Voltage and Temperature (0.9 mA)

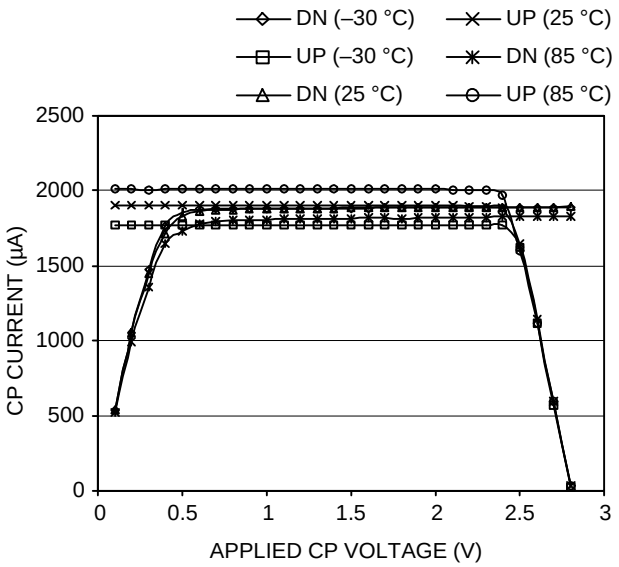


Figure 16. Charge Pump Current vs. Voltage and Temperature (1.9 mA)

Typical Performance Data (continued)

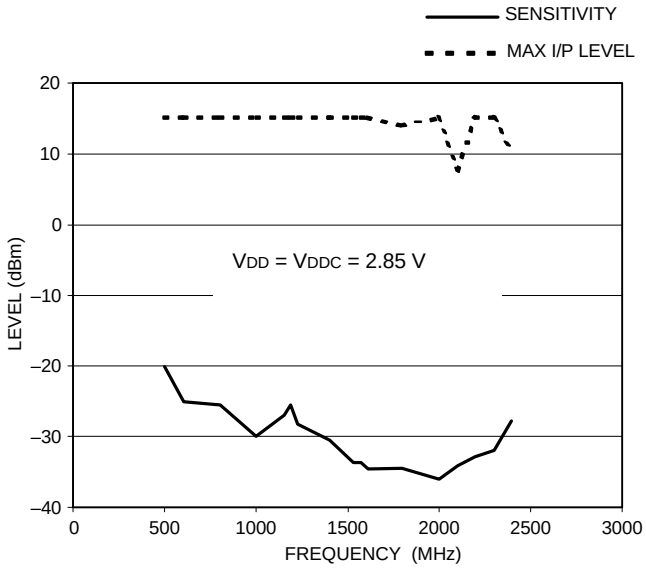


Figure 17. Prescaler Sensitivity and Maximum Input Level

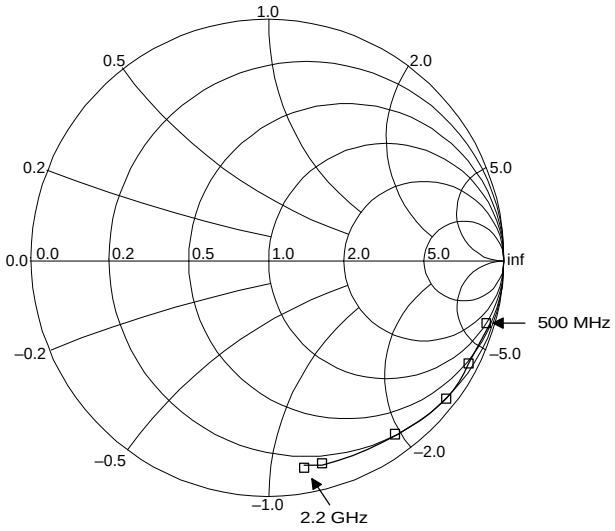


Figure 18. Input Impedance Smith Chart: 0.5 GHz to 2.2 GHz Frequency

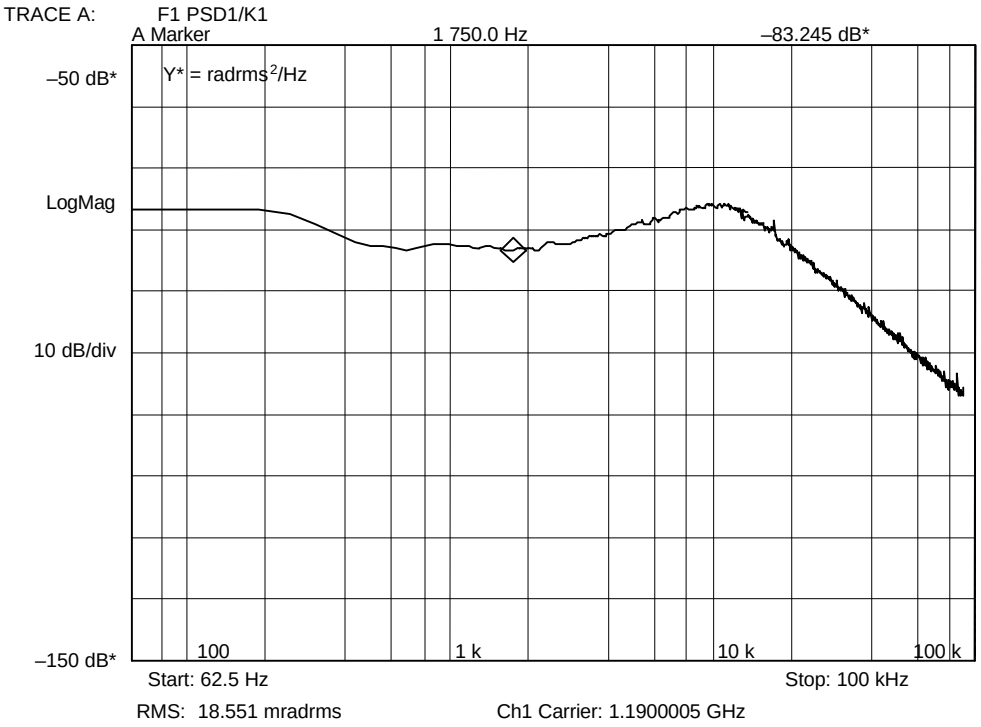


Figure 19. Phase Noise 1190 MHz, Fcomp = 200 kHz

Typical Performance Data (continued)

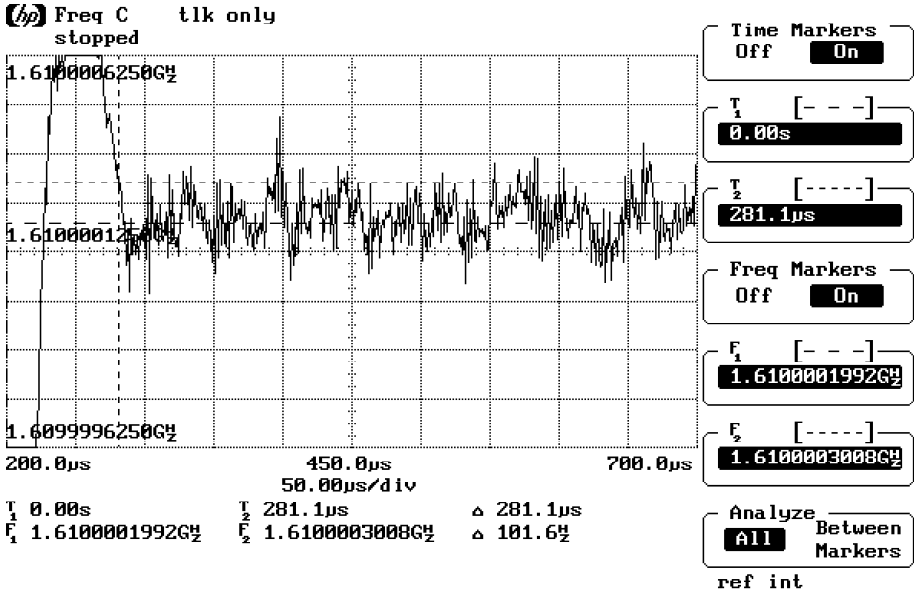


Figure 20. Settling Time from 1150 MHz to 1230 MHz ± 50 Hz

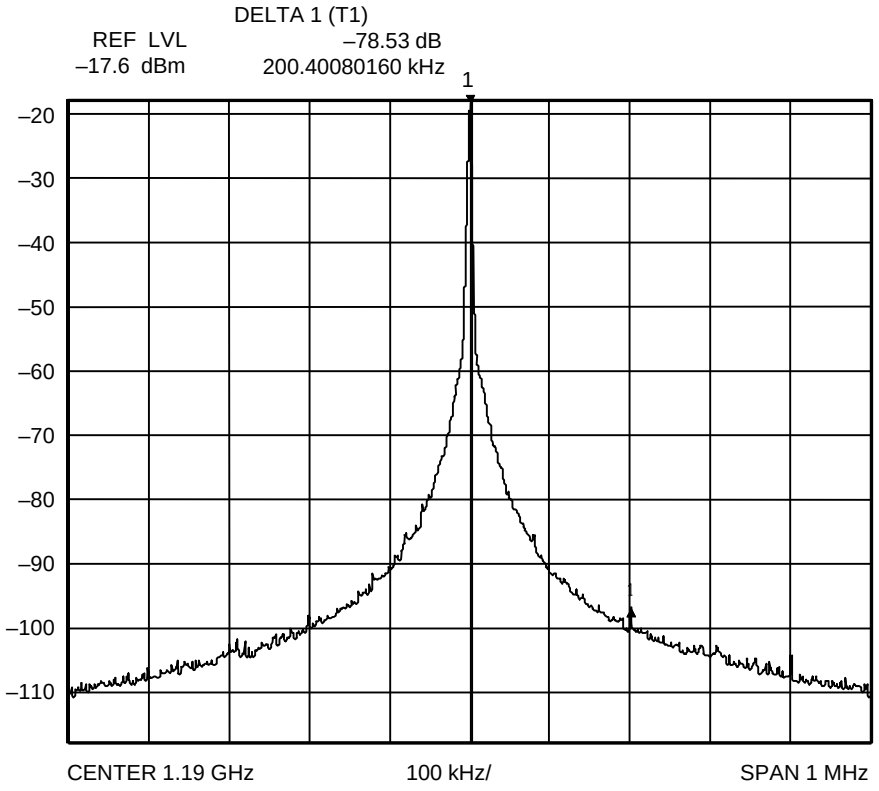


Figure 21. PLL Reference Spurs

Typical Performance Data (continued)

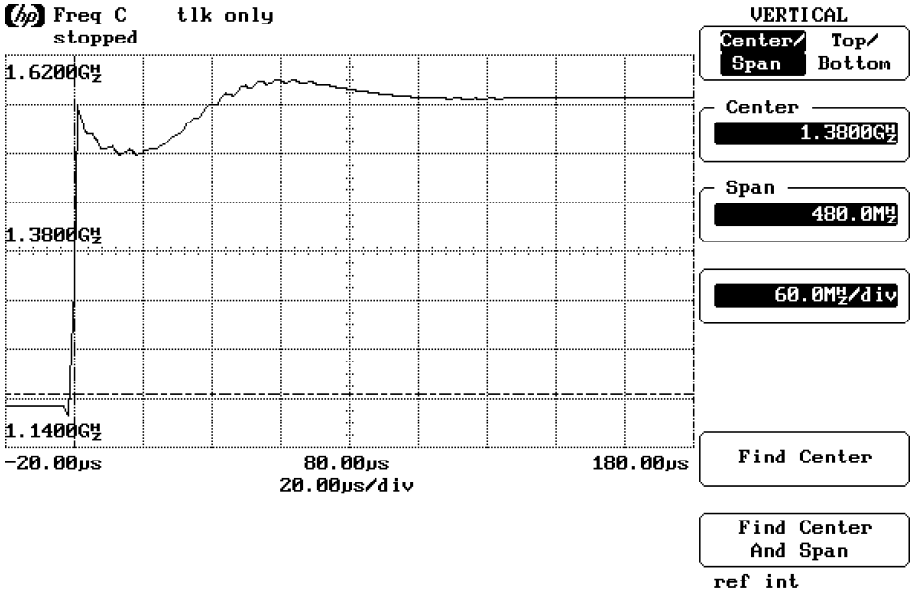
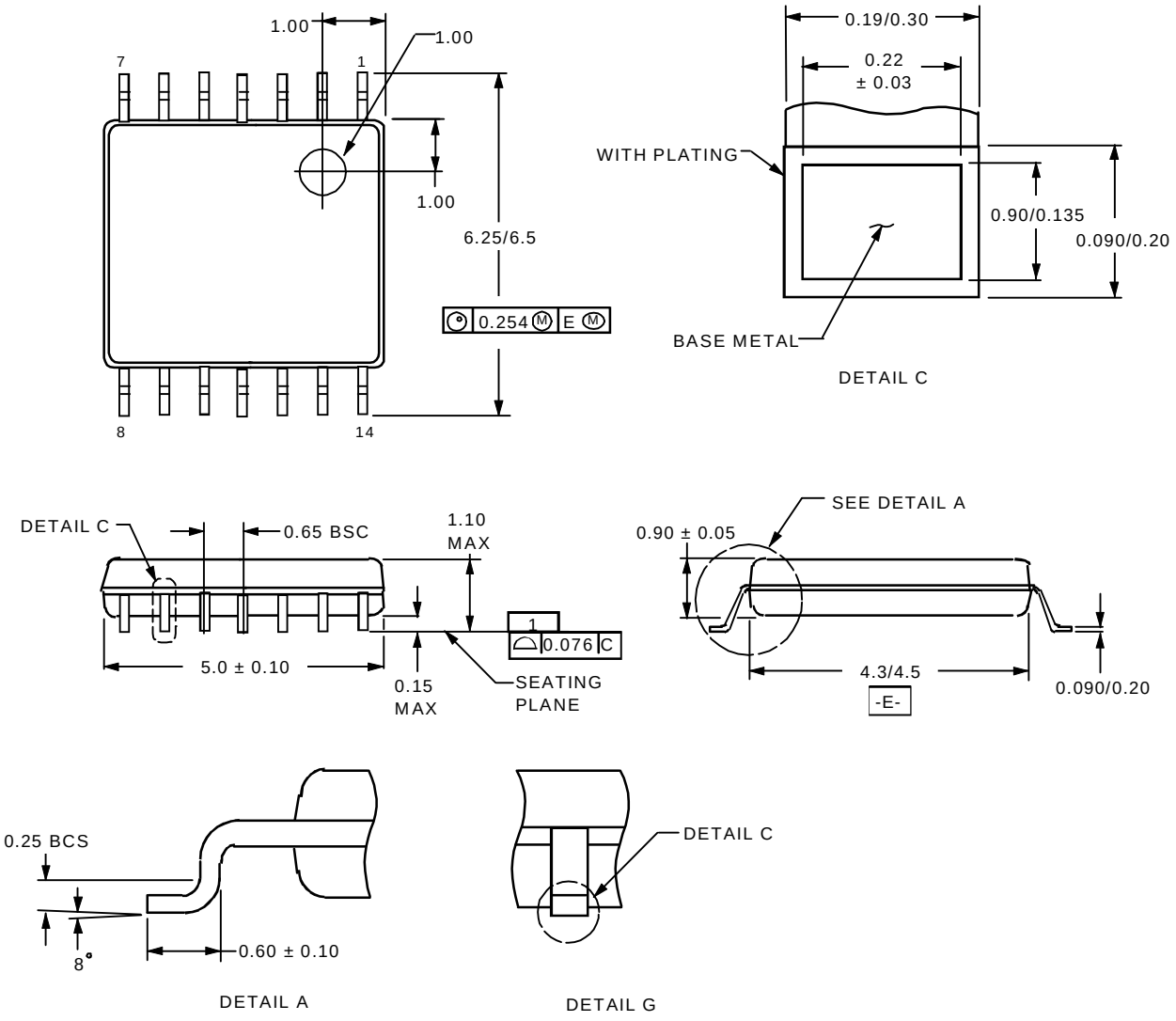


Figure 22. Dual-Band Locking

Outline Diagram

14-Pin TSSOP

Dimensions are in millimeters.



5-5462 C

Manufacturing Information

This device will be assembled in multiple locations, which include assembly codes P, M, and T.

Ordering Information

Device Code	Description	Package	Comcode
LUCW3000CCN	W3000 PLL Frequency Synthesizer Sticks	14-pin TSSOP	108417601
LUCW3000CCN-TR	W3000 PLL Frequency Synthesizer Tape and Reel	14-pin TSSOP	108417619

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