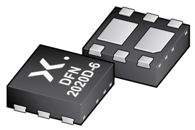


PBSS4160PANPS

60 V, 1 A NPN/NPN low VCEsat (BISS) transistor

11 February 2015 | Product data sheet

1. General description

NPN/PNP low V_{CEsat} Breakthrough In Small Signal (BISS) transistor in a leadless medium power DFN2020D-6 (SOT1118D) Surface-Mounted Device (SMD) plastic package with visible and solderable side pads.

NPN/NPN complement: PBSS4160PANS. PNP/PNP complement: PBSS5160PAPS.

2. Features and benefits

- Very low collector-emitter saturation voltage V_{CEsat}
- High collector current capability I_C and I_{CM}
- High collector current gain h_{FE} at high I_C
- Reduced Printed-Circuit Board (PCB) requirements
- Exposed heat sink for excellent thermal and electrical conductivity
- High energy efficiency due to less heat generation
- Suitable for Automatic Optical Inspection (AOI) of solder joints
- AEC-Q101 qualified

3. Applications

- Load switch
- Battery-driven devices
- Power management
- Charging circuits
- LED lighting
- Power switches (e.g. motors, fans)

4. Quick reference data

Table 1. Quick reference data

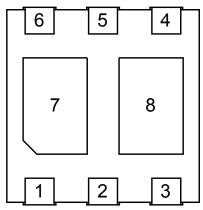
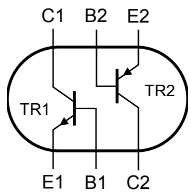
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor; for the PNP transistor with negative polarity							
V_{CEO}	collector-emitter voltage	open base		-	-	60	V
I_C	collector current			-	-	1	A
I_{CM}	peak collector current	single pulse; $t_p \leq 1$ ms		-	-	1.5	A

nexperia

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
TR1 (NPN)							
R_{CEsat}	collector-emitter saturation resistance	I_C = 0.5 A; I_B = 50 mA; pulsed; $t_p \leq 300$ µs; $\delta \leq 0.02$; T_{amb} = 25 °C		-	-	240	mΩ
TR2 (PNP)							
R_{CEsat}	collector-emitter saturation resistance	I_C = -0.5 A; I_B = -50 mA; pulsed; $t_p \leq 300$ µs; $\delta \leq 0.02$; T_{amb} = 25 °C		-	-	360	mΩ

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	E1	emitter TR1	 Transparent top view **DFN2020D-6 (SOT1118D)**	 *sym139*
2	B1	base TR1		
3	C2	collector TR2		
4	E2	emitter TR2		
5	B2	base TR2		
6	C1	collector TR1		
7	C1	collector TR1		
8	C2	collector TR2		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PBSS4160PANPS	DFN2020D-6	DFN2020D-6: plastic, thermally enhanced ultra thin and small outline package; no leads; 6 terminals; body 2 x 2 x 0.65 mm	SOT1118D

7. Marking

Table 4. Marking codes

Type number	Marking code
PBSS4160PANPS	3G

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transistor; for the PNP transistor with negative polarity						
V_{CBO}	collector-base voltage	open emitter		-	60	V
V_{CEO}	collector-emitter voltage	open base		-	60	V
V_{EBO}	emitter-base voltage	open collector		-	7	V
I_C	collector current			-	1	A
I_{CM}	peak collector current	single pulse; $t_p \leq 1$ ms		-	1.5	A
I_B	base current			-	0.3	A
I_{BM}	peak base current	single pulse; $t_p \leq 1$ ms		-	1	A
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	[1]	-	370	mW
			[2]	-	570	mW
			[3]	-	530	mW
			[4]	-	700	mW
			[5]	-	450	mW
			[6]	-	760	mW
			[7]	-	700	mW
			[8]	-	1450	mW
Per device						
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	[1]	-	510	mW
			[2]	-	780	mW
			[3]	-	730	mW
			[4]	-	960	mW
			[5]	-	620	mW
			[6]	-	1040	mW
			[7]	-	960	mW
			[8]	-	2000	mW
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			-55	150	°C
T_{stg}	storage temperature			-65	150	°C

[1] Device mounted on an FR4 PCB, single-sided 35 µm copper strip line, tin-plated and standard footprint.

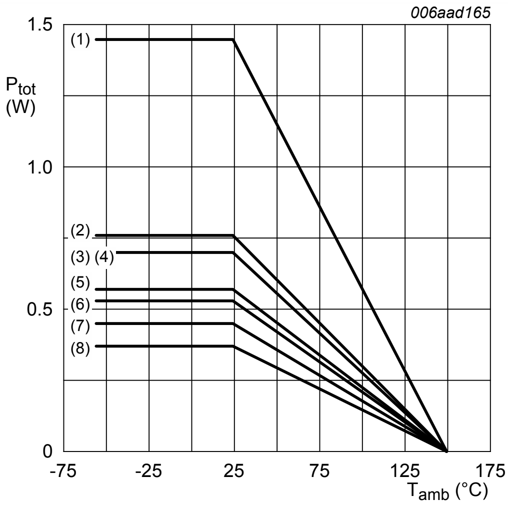
[2] Device mounted on an FR4 PCB, single-sided 35 µm copper strip line, tin-plated, mounting pad for collector 1 cm^2.

[3] Device mounted on 4-layer PCB 35 µm copper strip line, tin-plated and standard footprint.

[4] Device mounted on 4-layer PCB 35 µm copper strip line, tin-plated, mounting pad for collector 1 cm^2.

[5] Device mounted on an FR4 PCB, single-sided 70 µm copper strip line, tin-plated and standard footprint.

[6] Device mounted on an FR4 PCB, single-sided 70 µm copper strip line, tin-plated, mounting pad for collector 1 cm^2.
[7] Device mounted on 4-layer PCB 70 µm copper strip line, tin-plated and standard footprint.
[8] Device mounted on 4-layer PCB 70 µm copper strip line, tin-plated, mounting pad for collector 1 cm^2.



(1) 4-layer PCB 70 µm, mounting pad for collector 1 cm^2
(2) FR4 PCB 70 µm, mounting pad for collector 1 cm^2
(3) 4-layer PCB 70 µm, standard footprint
(4) 4-layer PCB 35 µm, mounting pad for collector 1 cm^2
(5) FR4 PCB 35 µm, mounting pad for collector 1 cm^2
(6) 4-layer PCB 35 µm, standard footprint
(7) FR4 PCB 70 µm, standard footprint
(8) FR4 PCB 35 µm, standard footprint

Fig. 1. Per transistor: power derating curves

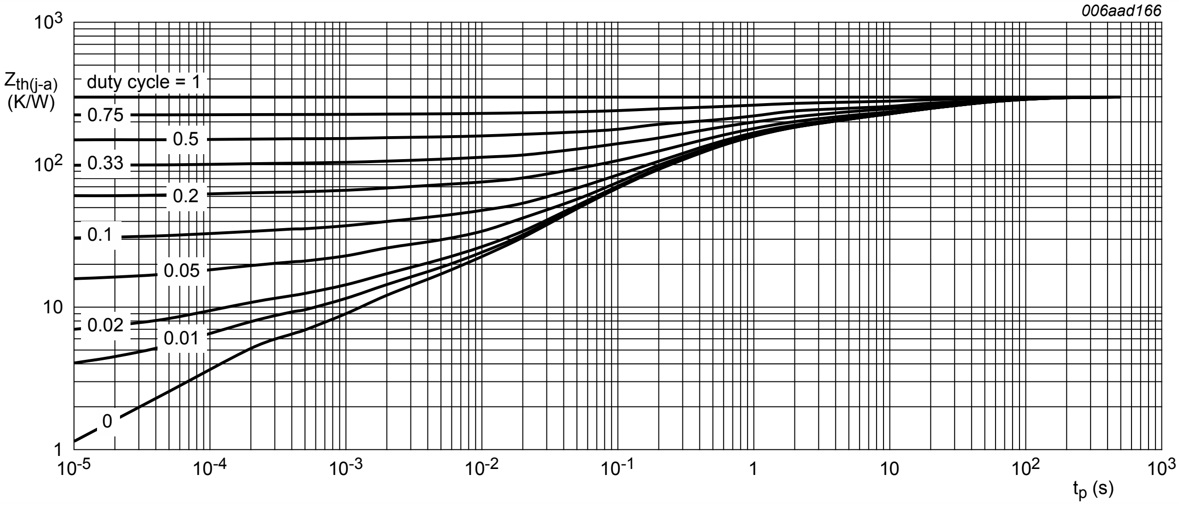
9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	338	K/W
			[2]	-	-	219	K/W
			[3]	-	-	236	K/W
			[4]	-	-	179	K/W
			[5]	-	-	278	K/W
			[6]	-	-	164	K/W
			[7]	-	-	179	K/W
			[8]	-	-	86	K/W

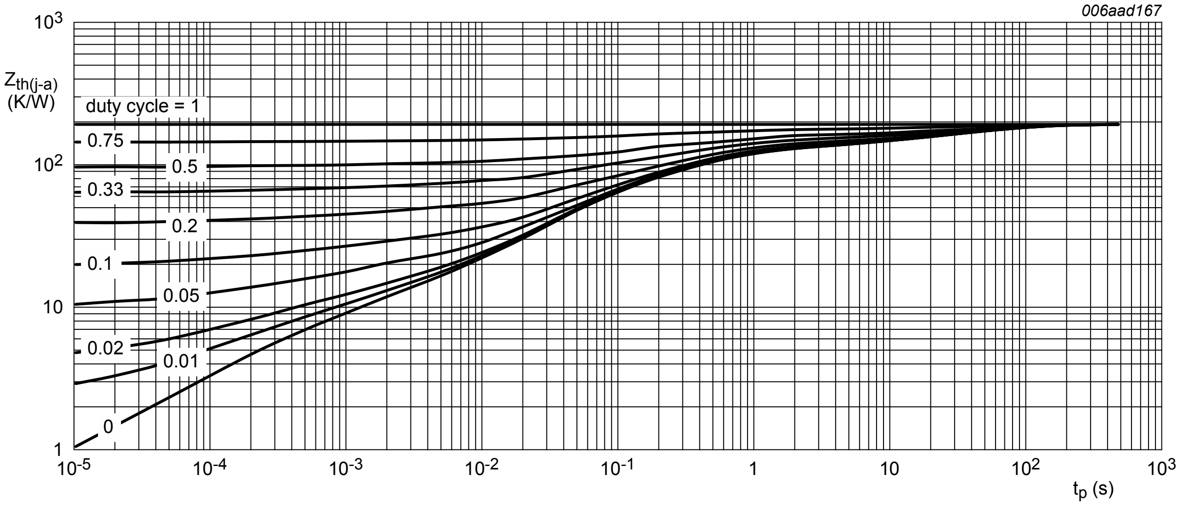
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j\text{-}sp)}$	thermal resistance from junction to solder point			-	-	30	K/W
Per device							
$R_{th(j\text{-}a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	245	K/W
			[2]	-	-	160	K/W
			[3]	-	-	171	K/W
			[4]	-	-	130	K/W
			[5]	-	-	202	K/W
			[6]	-	-	120	K/W
			[7]	-	-	130	K/W
			[8]	-	-	63	K/W

[1] Device mounted on an FR4 PCB, single-sided 35 µm copper strip line, tin-plated and standard footprint.
[2] Device mounted on an FR4 PCB, single-sided 35 µm copper strip line, tin-plated, mounting pad for collector 1 cm^2.
[3] Device mounted on 4-layer PCB 35 µm copper strip line, tin-plated and standard footprint.
[4] Device mounted on 4-layer PCB 35 µm copper strip line, tin-plated, mounting pad for collector 1 cm^2.
[5] Device mounted on an FR4 PCB, single-sided 70 µm copper strip line, tin-plated and standard footprint.
[6] Device mounted on an FR4 PCB, single-sided 70 µm copper strip line, tin-plated, mounting pad for collector 1 cm^2.
[7] Device mounted on 4-layer PCB 70 µm copper strip line, tin-plated and standard footprint.
[8] Device mounted on 4-layer PCB 70 µm copper strip line, tin-plated, mounting pad for collector 1 cm^2.



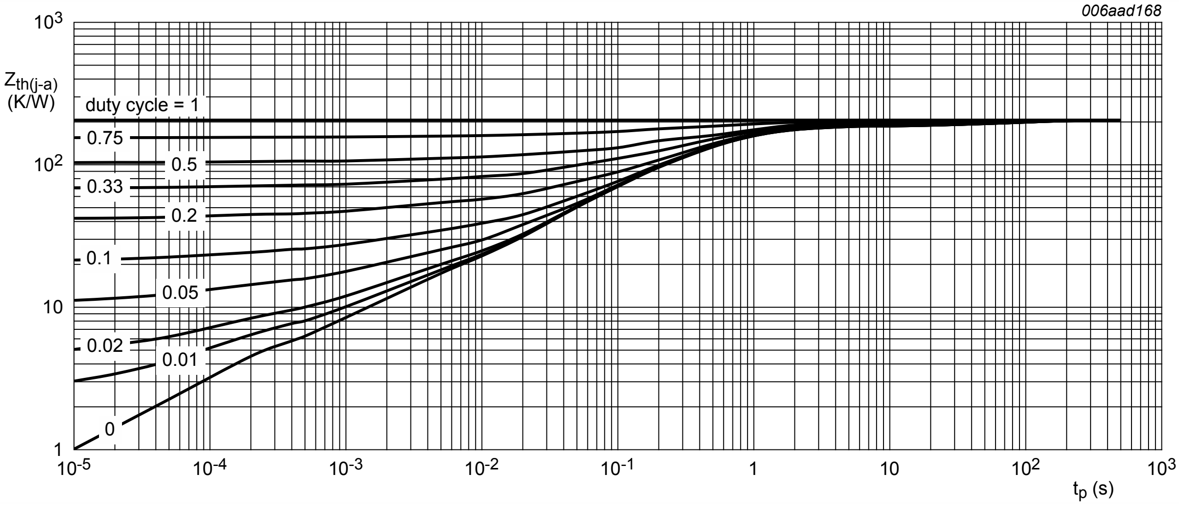
FR4 PCB 35 µm, standard footprint

Fig. 2. Per transistor: transient thermal impedance from junction to ambient as a function of pulse duration; typical values



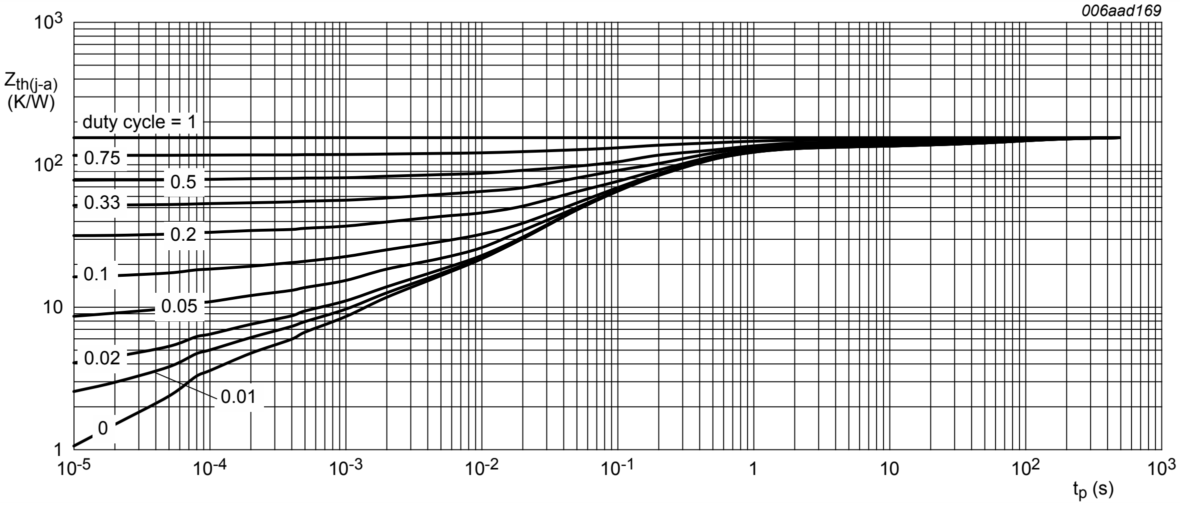
FR4 PCB 35 µm, mounting pad for collector 1 cm^2

Fig. 3. Per transistor: transient thermal impedance from junction to ambient as a function of pulse duration; typical values



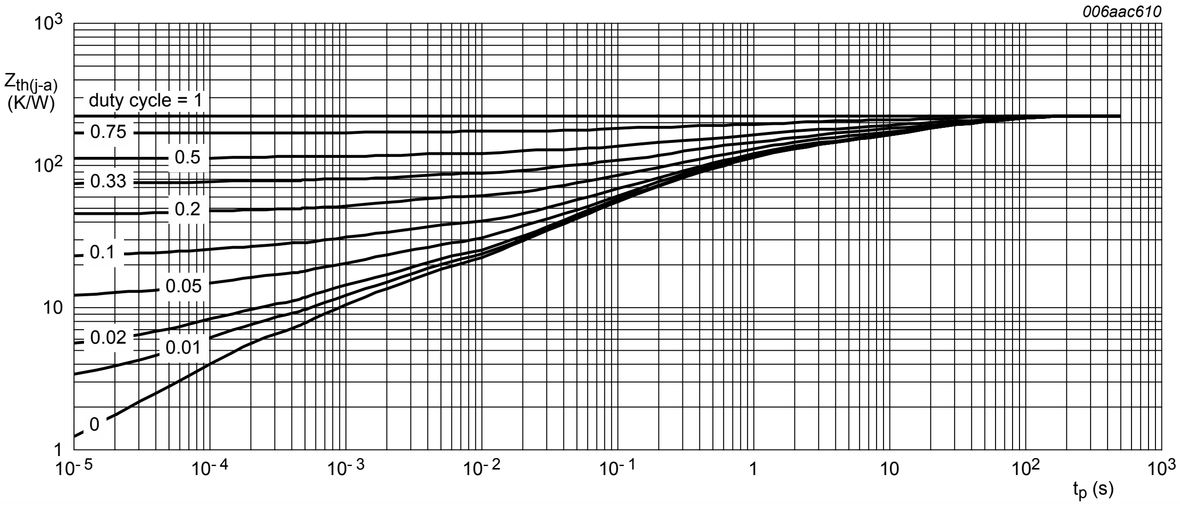
4-layer PCB 35 µm, standard footprint

Fig. 4. Per transistor: transient thermal impedance from junction to ambient as a function of pulse duration; typical values



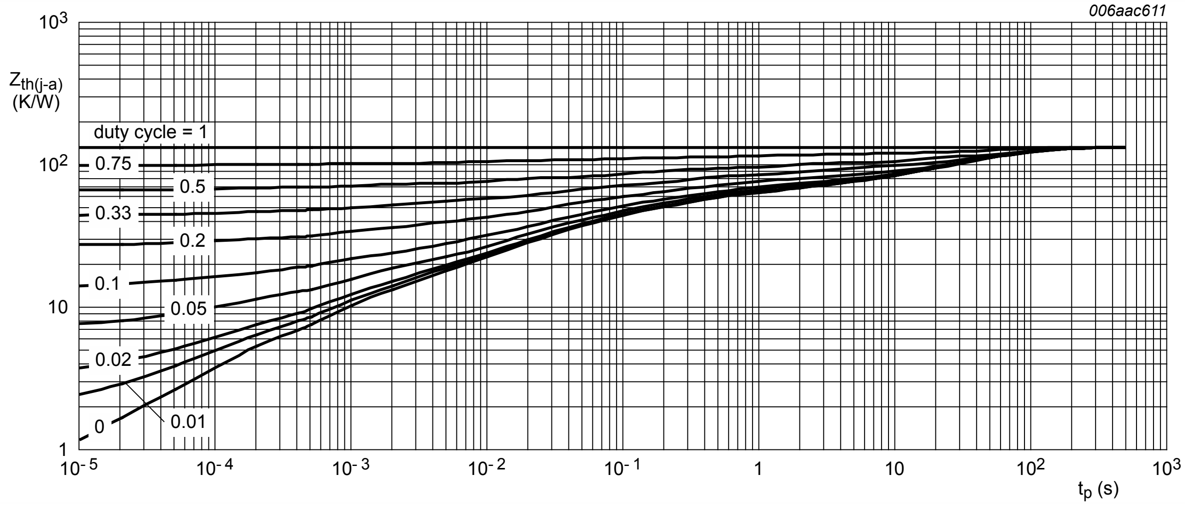
4-layer PCB 35 μm, mounting pad for collector 1 cm^2

Fig. 5. Per transistor: transient thermal impedance from junction to ambient as a function of pulse duration; typical values



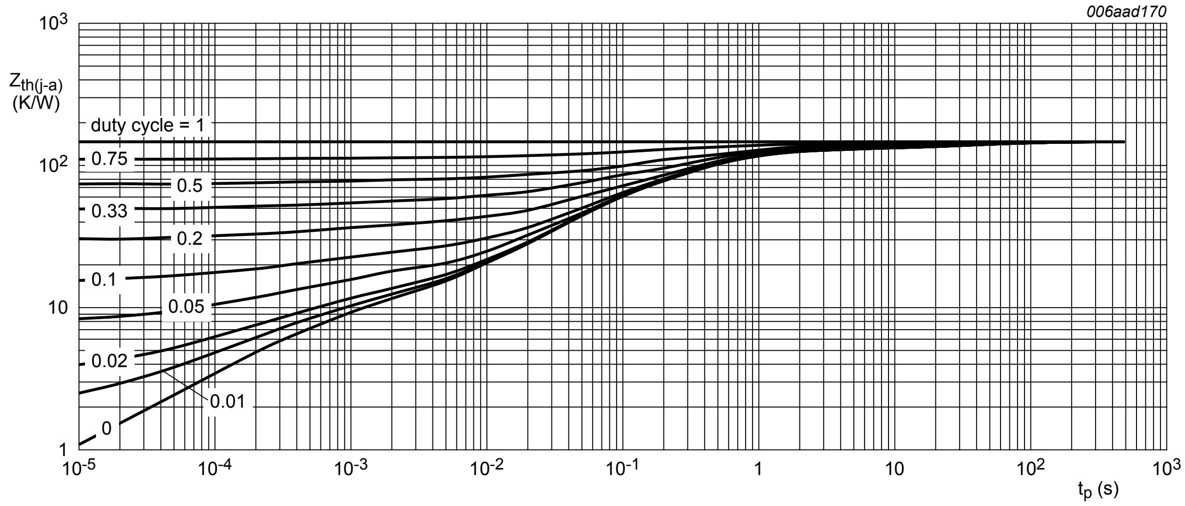
FR4 PCB 70 μm, standard footprint

Fig. 6. Per transistor: transient thermal impedance from junction to ambient as a function of pulse duration; typical values



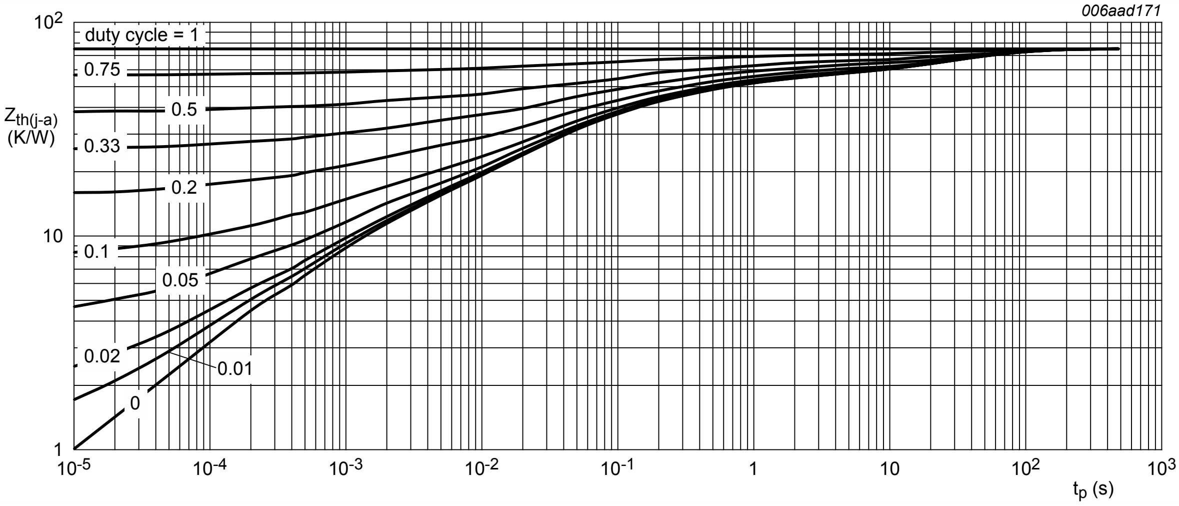
FR4 PCB 70 µm, mounting pad for collector 1 cm^2

Fig. 7. Per transistor: transient thermal impedance from junction to ambient as a function of pulse duration; typical values



4-layer PCB 70 µm, standard footprint

Fig. 8. Per transistor: transient thermal impedance from junction to ambient as a function of pulse duration; typical values



4-layer PCB 70 µm, mounting pad for collector 1 cm^2

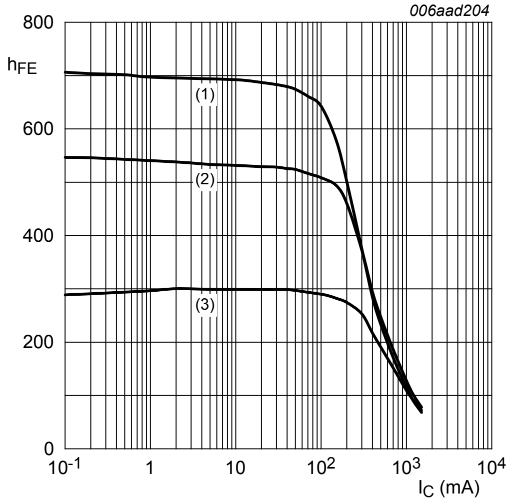
Fig. 9. Per transistor: transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

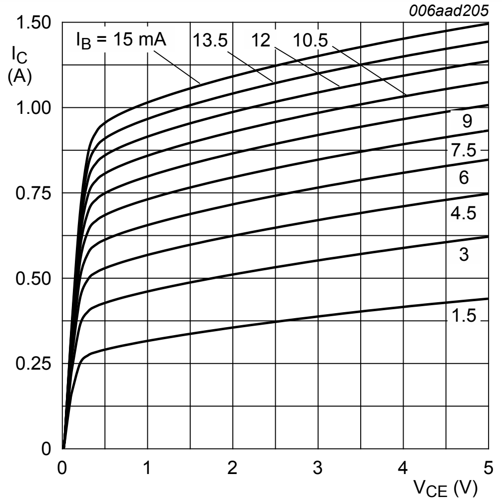
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
TR1 (NPN)							
I_{CBO}	collector-base cut-off current	V_{CB} = 48 V; I_E = 0 A; T_{amb} = 25 °C		-	-	100	nA
		V_{CB} = 48 V; I_E = 0 A; T_j = 150 °C		-	-	50	µA
I_{EBO}	emitter-base cut-off current	V_{EB} = 5 V; I_C = 0 A; T_{amb} = 25 °C		-	-	100	nA
h_{FE}	DC current gain	V_{CE} = 2 V; I_C = 100 mA; pulsed; t_p ≤ 300 µs; δ ≤ 0.02; T_{amb} = 25 °C		290	430	-	
		V_{CE} = 2 V; I_C = 500 mA; pulsed; t_p ≤ 300 µs; δ ≤ 0.02; T_{amb} = 25 °C		150	220	-	
		V_{CE} = 2 V; I_C = 1 A; pulsed; t_p ≤ 300 µs; δ ≤ 0.02; T_{amb} = 25 °C		70	110	-	
V_{CEsat}	collector-emitter saturation voltage	I_C = 500 mA; I_B = 50 mA; T_{amb} = 25 °C		-	90	120	mV
		I_C = 1 A; I_B = 50 mA; pulsed; t_p ≤ 300 µs; δ ≤ 0.02; T_{amb} = 25 °C		-	185	240	mV
		I_C = 1 A; I_B = 100 mA; pulsed; t_p ≤ 300 µs; δ ≤ 0.02; T_{amb} = 25 °C		-	175	220	mV
R_{CEsat}	collector-emitter saturation resistance	I_C = 0.5 A; I_B = 50 mA; pulsed; t_p ≤ 300 µs; δ ≤ 0.02; T_{amb} = 25 °C		-	-	240	mΩ
V_{BEsat}	base-emitter saturation voltage	I_C = 500 mA; I_B = 50 mA; T_{amb} = 25 °C		-	-	1	V
		I_C = 1 A; I_B = 50 mA; pulsed; t_p ≤ 300 µs; δ ≤ 0.02; T_{amb} = 25 °C		-	-	1.1	V
		I_C = 1 A; I_B = 100 mA; pulsed; t_p ≤ 300 µs; δ ≤ 0.02; T_{amb} = 25 °C		-	-	1.1	V
V_{BEon}	base-emitter turn-on voltage	V_{CE} = 2 V; I_C = 0.5 A; pulsed; t_p ≤ 300 µs; δ ≤ 0.02; T_{amb} = 25 °C		-	-	0.9	V
t_d	delay time	V_{CC} = 10 V; I_C = 0.5 A; I_{Bon} = 25 mA; I_{Boff} = -25 mA; T_{amb} = 25 °C		-	15	-	ns
t_r	rise time			-	90	-	ns
t_{on}	turn-on time			-	105	-	ns
t_s	storage time			-	410	-	ns
t_f	fall time			-	130	-	ns
t_{off}	turn-off time			-	540	-	ns
f_T	transition frequency	V_{CE} = 10 V; I_C = 50 mA; f = 100 MHz; T_{amb} = 25 °C		90	175	-	MHz
C_c	collector capacitance	V_{CB} = 10 V; I_E = 0 A; i_e = 0 A; f = 1 MHz; T_{amb} = 25 °C		-	4	6	pF

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
TR2 (PNP)							
I_{CBO}	collector-base cut-off current	V_{CB} = -48 V; I_E = 0 A		-	-	-100	nA
		V_{CB} = -48 V; I_E = 0 A; T_j = 150 °C		-	-	-50	μA
I_{EBO}	emitter-base cut-off current	V_{EB} = -5 V; I_C = 0 A		-	-	-100	nA
h_{FE}	DC current gain	V_{CE} = -2 V; I_C = -100 mA; pulsed; t_p ≤ 300 μs; δ ≤ 0.02; T_{amb} = 25 °C		170	245	-	
		V_{CE} = -2 V; I_C = -500 mA; pulsed; t_p ≤ 300 μs; δ ≤ 0.02; T_{amb} = 25 °C		120	170	-	
		V_{CE} = -2 V; I_C = -1 A; pulsed; t_p ≤ 300 μs; δ ≤ 0.02; T_{amb} = 25 °C		70	100	-	
V_{CEsat}	collector-emitter saturation voltage	I_C = -500 mA; I_B = -50 mA; pulsed; t_p ≤ 300 μs; δ ≤ 0.02; T_{amb} = 25 °C		-	-125	-180	mV
		I_C = -1 A; I_B = -50 mA; pulsed; t_p ≤ 300 μs; δ ≤ 0.02; T_{amb} = 25 °C		-	-390	-550	mV
		I_C = -1 A; I_B = -100 mA; pulsed; t_p ≤ 300 μs; δ ≤ 0.02; T_{amb} = 25 °C		-	-240	-340	mV
R_{CEsat}	collector-emitter saturation resistance	I_C = -0.5 A; I_B = -50 mA; pulsed; t_p ≤ 300 μs; δ ≤ 0.02; T_{amb} = 25 °C		-	-	360	mΩ
V_{BEsat}	base-emitter saturation voltage	I_C = -500 mA; I_B = -50 mA; pulsed; t_p ≤ 300 μs; δ ≤ 0.02; T_{amb} = 25 °C		-	-	-1	V
		I_C = -1 A; I_B = -50 mA; pulsed; t_p ≤ 300 μs; δ ≤ 0.02; T_{amb} = 25 °C		-	-	-1	V
		I_C = -1 A; I_B = -100 mA; pulsed; t_p ≤ 300 μs; δ ≤ 0.02; T_{amb} = 25 °C		-	-	-1.1	V
V_{BEon}	base-emitter turn-on voltage	V_{CE} = -2 V; I_C = -0.5 A; pulsed; t_p ≤ 300 μs; δ ≤ 0.02; T_{amb} = 25 °C		-	-	-0.9	V
t_d	delay time	V_{CC} = -10 V; I_C = -0.5 A; I_{Bon} = -25 mA; I_{Boff} = 25 mA; T_{amb} = 25 °C		-	15	-	ns
t_r	rise time			-	40	-	ns
t_{on}	turn-on time			-	55	-	ns
t_s	storage time			-	95	-	ns
t_f	fall time			-	40	-	ns
t_{off}	turn-off time			-	135	-	ns
f_T	transition frequency	V_{CE} = -10 V; I_C = -50 mA; f = 100 MHz; T_{amb} = 25 °C		65	125	-	MHz
C_c	collector capacitance	V_{CB} = -10 V; I_E = 0 A; i_e = 0 A; f = 1 MHz; T_{amb} = 25 °C		-	9.5	13	pF



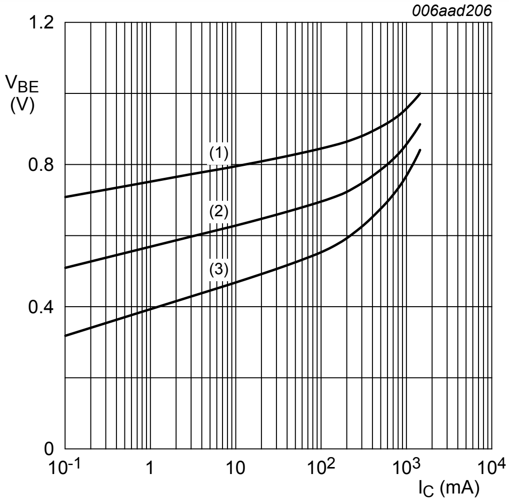
V_{CE} = 2 V
(1) T_{amb} = 100 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = −55 °C

Fig. 10. TR1 (NPN): DC current gain as a function of collector current; typical values



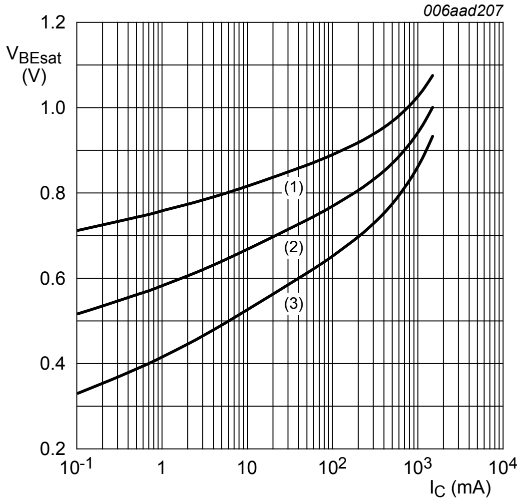
T_{amb} = 25 °C

Fig. 11. TR1 (NPN): Collector current as a function of collector-emitter voltage; typical values



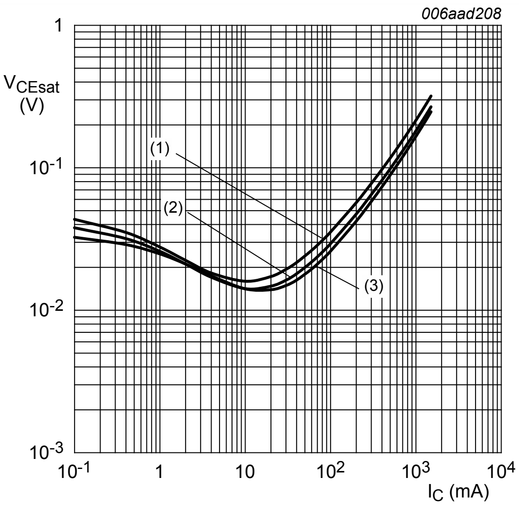
V_{CE} = 2 V
(1) T_{amb} = −55 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 100 °C

Fig. 12. TR1 (NPN): Base-emitter voltage as a function of collector current; typical values



I_C/I_B = 20
(1) T_{amb} = −55 °C
(2) T_{amb} = 25 °C
(3) T_{amb}= 100 °C

Fig. 13. TR1 (NPN): Base-emitter saturation voltage as a function of collector current; typical values



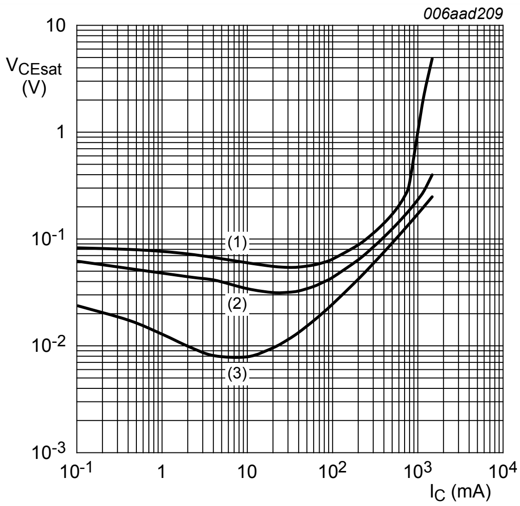
$I_C/I_B = 20$

(1) T_{amb} = 100 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = −55 °C

Fig. 14. TR1 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values



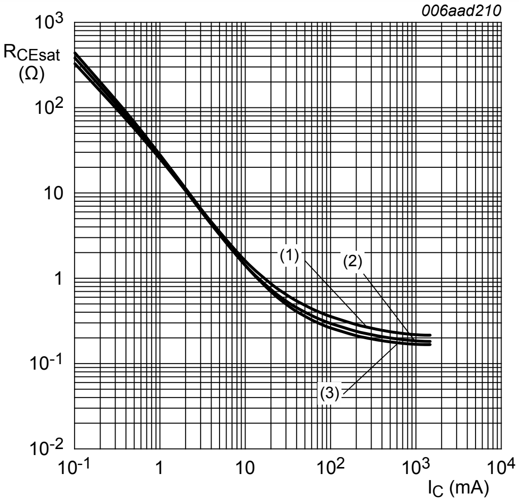
T_{amb} = 25 °C

(1) $I_C/I_B = 100$

(2) $I_C/I_B = 50$

(3) $I_C/I_B = 10$

Fig. 15. TR1 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values



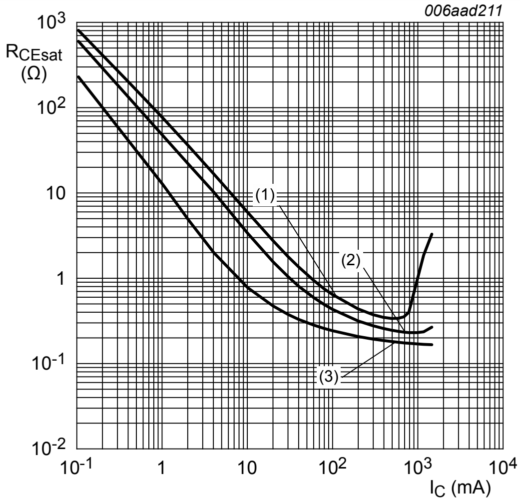
$I_C/I_B = 20$

(1) T_{amb} = 100 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = −55 °C

Fig. 16. TR1 (NPN): Collector-emitter saturation resistance as a function of collector current; typical values



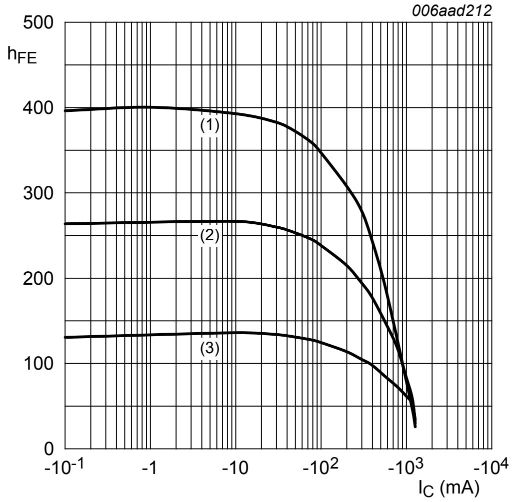
T_{amb} = 25 °C

(1) $I_C/I_B = 100$

(2) $I_C/I_B = 50$

(3) $I_C/I_B = 10$

Fig. 17. TR1 (NPN): Collector-emitter saturation resistance as a function of collector current; typical values



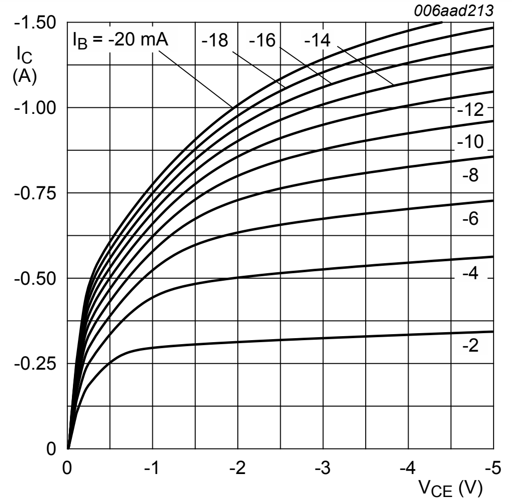
$V_{CE} = -2$ V

(1) $T_{amb} = 100$ °C

(2) $T_{amb} = 25$ °C

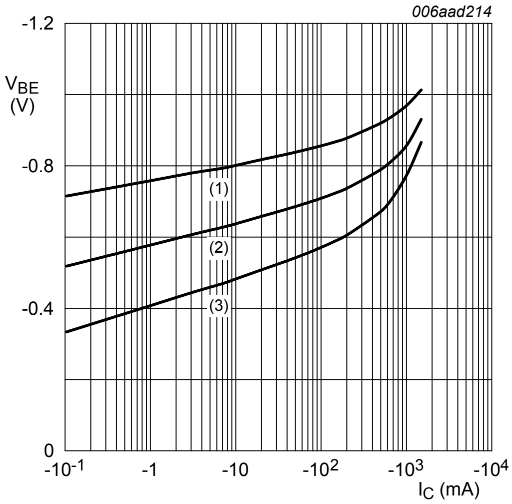
(3) $T_{amb} = -55$ °C

Fig. 18. TR2 (PNP): DC current gain as a function of collector current; typical values



$T_{amb} = 25$ °C

Fig. 19. TR2 (PNP): Collector current as a function of collector-emitter voltage; typical values



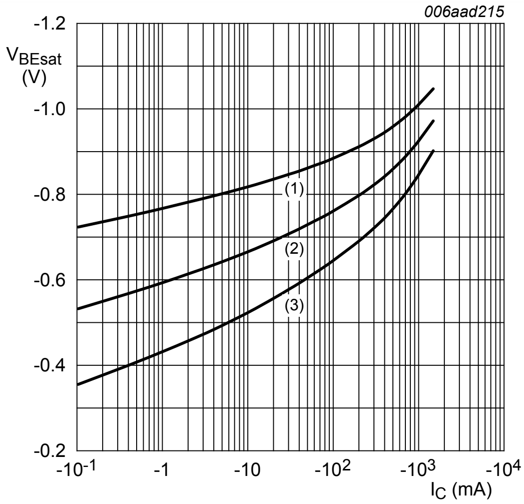
$V_{CE} = -2$ V

(1) $T_{amb} = -55$ °C

(2) $T_{amb} = 25$ °C

(3) $T_{amb} = 100$ °C

Fig. 20. TR2 (PNP): Base-emitter voltage as a function of collector current; typical values



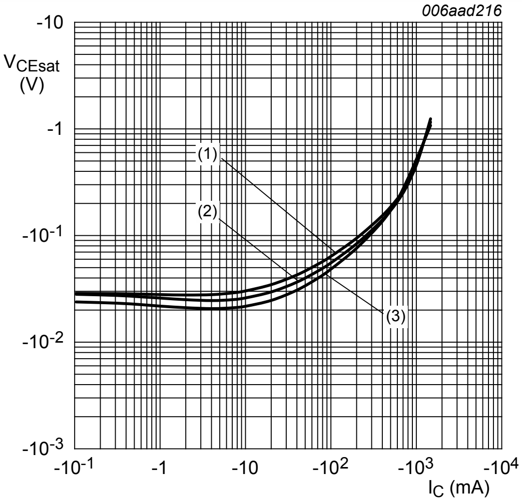
$I_C/I_B = 20$

(1) $T_{amb} = -55$ °C

(2) $T_{amb} = 25$ °C

(3) $T_{amb} = 100$ °C

Fig. 21. TR2 (PNP): Base-emitter saturation voltage as a function of collector current; typical values



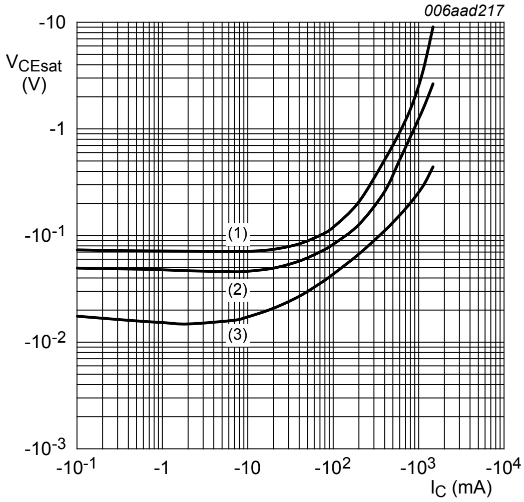
I_C/I_B = 20

(1) T_{amb} = 100 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = −55 °C

Fig. 22. TR2 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values



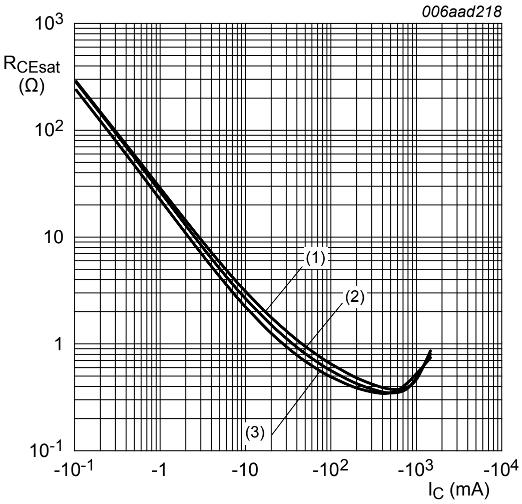
T_{amb} = 25 °C

(1) I_C/I_B = 100

(2) I_C/I_B = 50

(3) I_C/I_B = 10

Fig. 23. TR2 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values



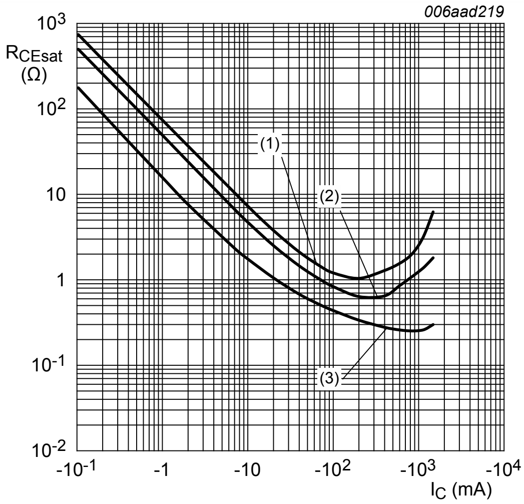
I_C/I_B = 20

(1) T_{amb} = 100 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = −55 °C

Fig. 24. TR2 (PNP): Collector-emitter saturation resistance as a function of collector current; typical values



T_{amb} = 25 °C

(1) I_C/I_B = 100

(2) I_C/I_B = 50

(3) I_C/I_B= 10

Fig. 25. TR2 (PNP): Collector-emitter saturation resistance as a function of collector current; typical values

11. Test information

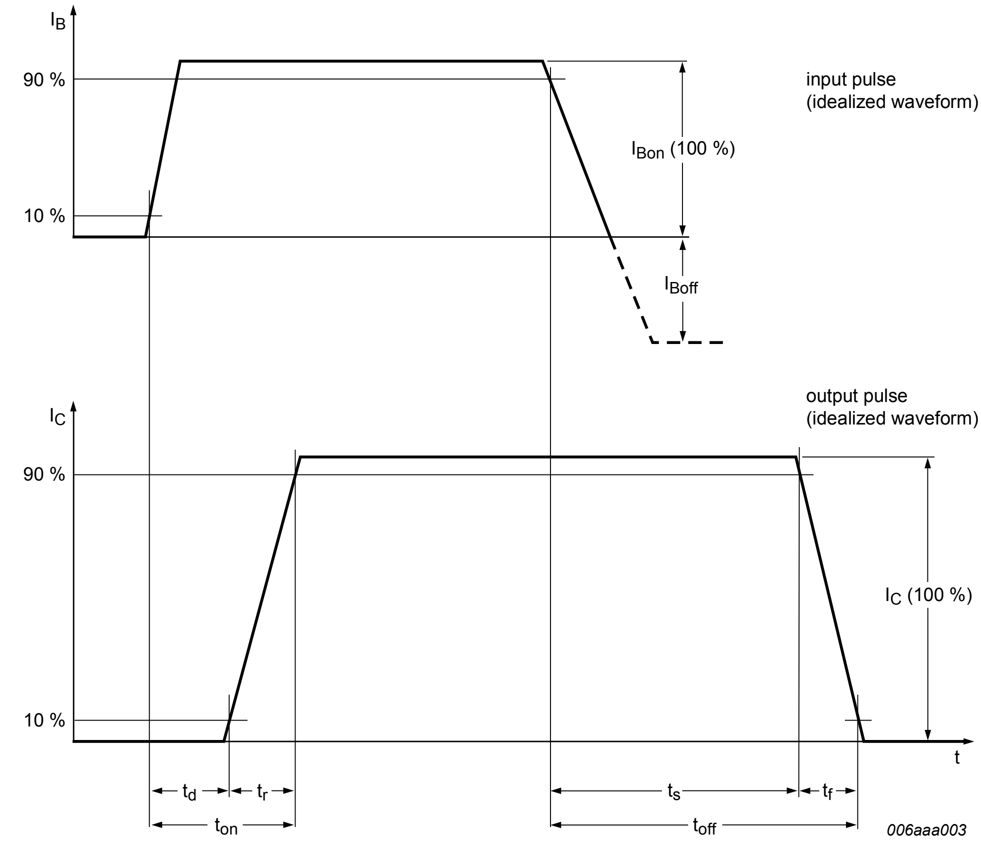


Fig. 26. TR1 (NPN): BISS transistor switching time definition

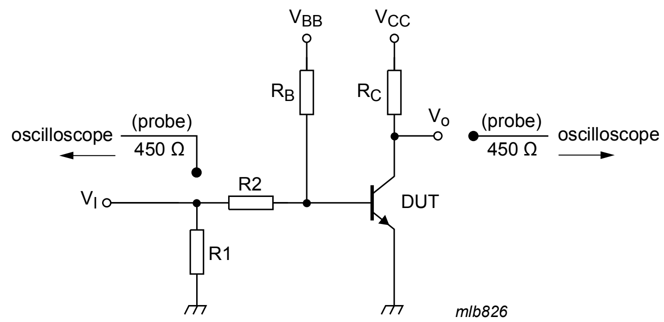


Fig. 27. TR1 (NPN): Test circuit for switching times

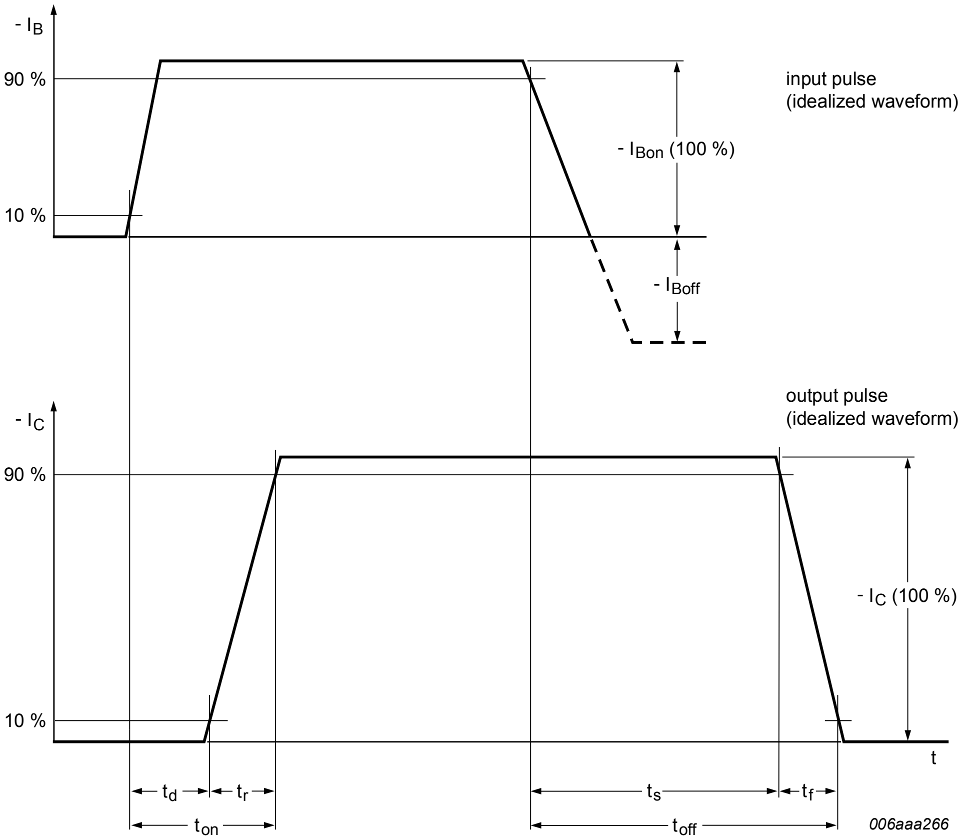


Fig. 28. TR2 (PNP): BISS transistor switching time definition

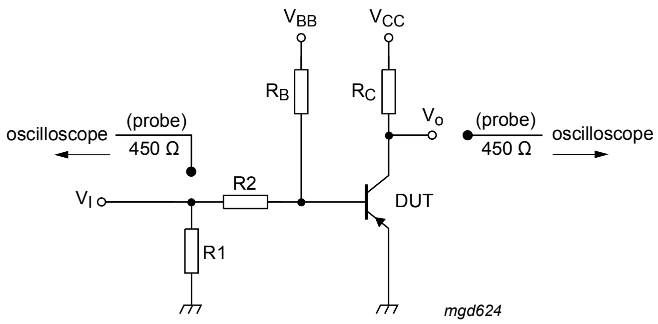


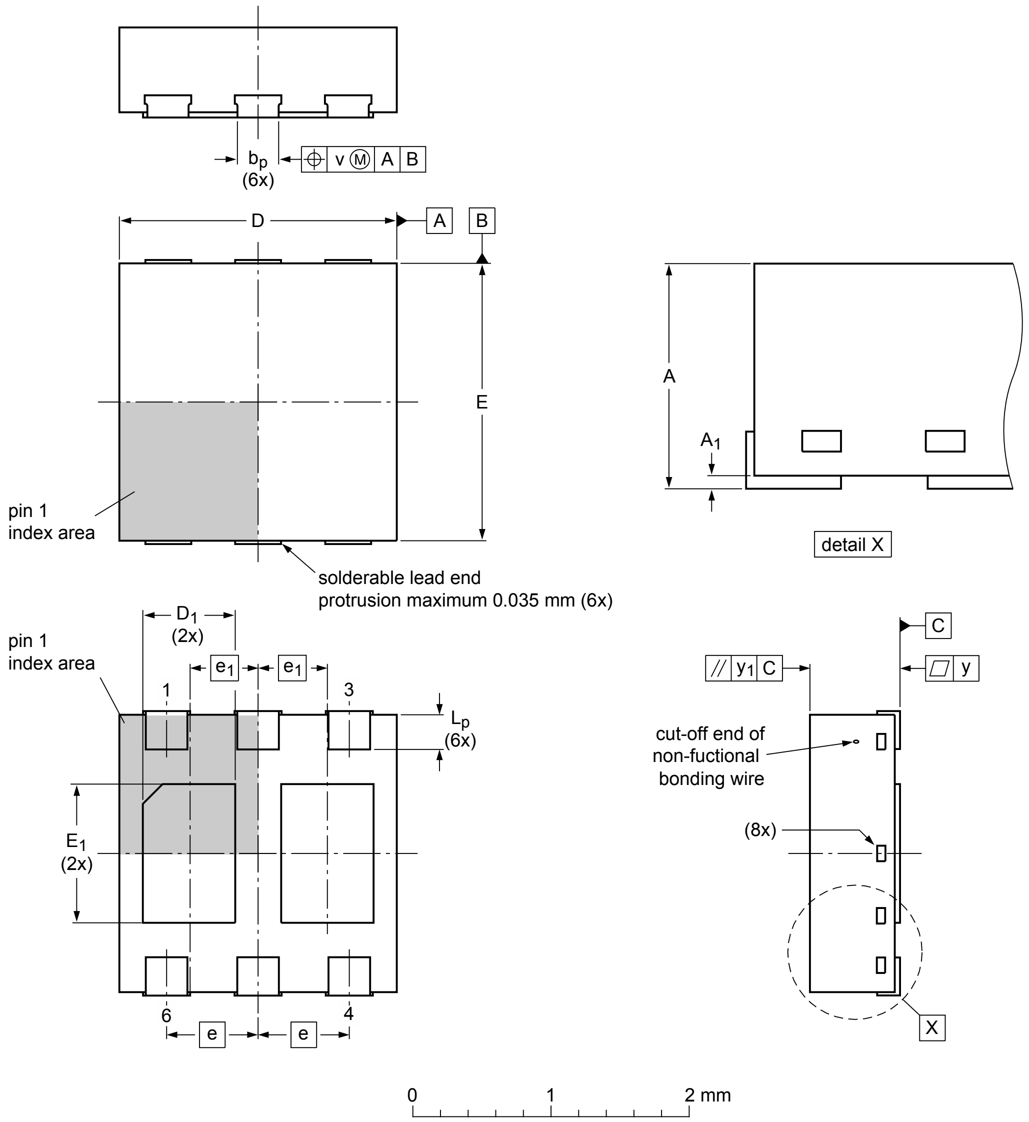
Fig. 29. TR2 (PNP): Test circuit for switching times

11.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q101 - Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline

DFN2020D-6: plastic, thermally enhanced ultra thin and small outline package; no leads; 6 terminals; body 2 x 2 x 0.65 mm **SOT1118D**



Dimensions (mm are the original dimensions)

Unit		A	A_1	b_p	D	D_1	E	E_1	e	e_1	L_p	v	y	y_1
mm	max	0.65	0.04	0.35	2.1	0.77	2.1	1.0		0.54	0.30			
	nom	0.62		0.30	2.0	0.67	2.0	0.9	0.65	0.49	0.25	0.1	0.05	0.05
	min	0.59		0.25	1.9	0.57	1.9	0.8		0.44	0.20			

Note

1. Dimension A is including plating thickness.

sot1118d_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1118D		- - -				~~14-07-16~~ 14-10-16

Fig. 30. Package outline DFN2020D-6 (SOT1118D)

13. Soldering

SOT1118D

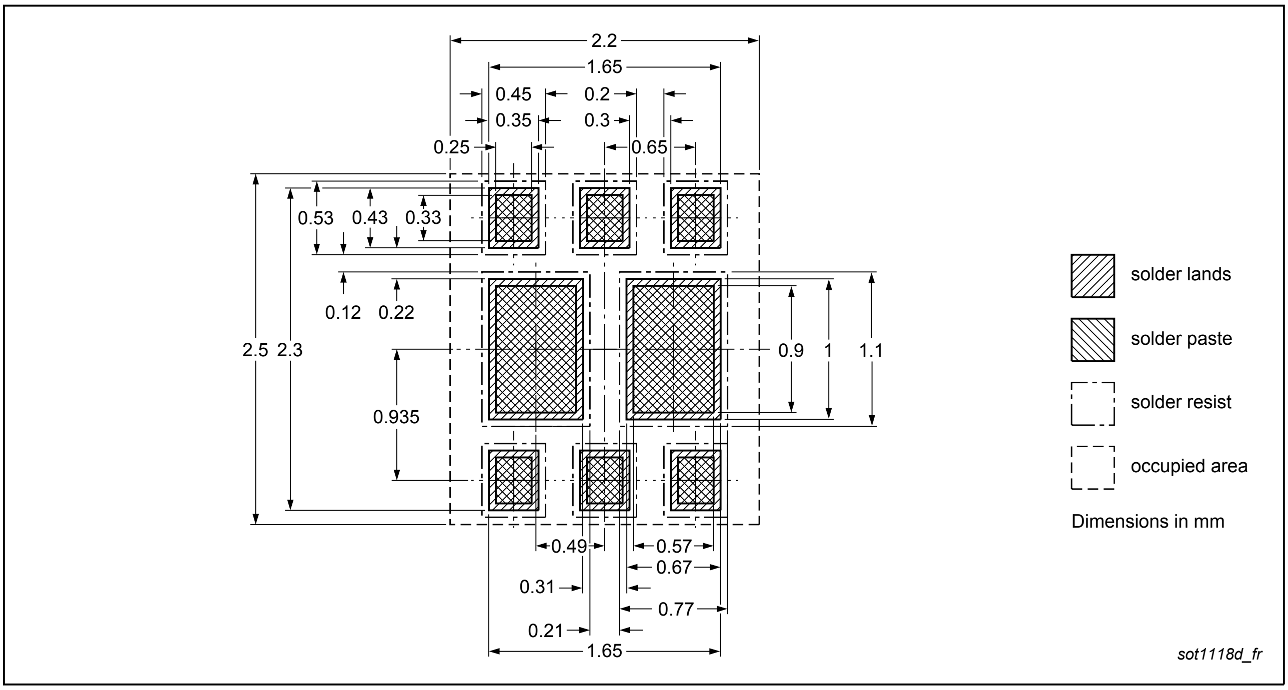


Fig. 31. Reflow soldering footprint for DFN2020D-6 (SOT1118D)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PBSS4160PANPS v.1	20150211	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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16. Contents

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