119- and 209-Pin BGA
Commercial Temp
Industrial Temp

2M x 18, 1M x 36, 512K x 72 36Mb Sync NBT SRAMs

250 MHz–133MHz
2.5 V or 3.3 V V_{DD}
2.5 V or 3.3 V I/O

Features

- NBT (No Bus Turn Around) functionality allows zero wait Read-Write-Read bus utilization; fully pin-compatible with both pipelined and flow through NtRAM™, NoBL™ and ZBT™ SRAMs
- FT pin for user-configurable flow through or pipeline operation
- IEEE 1149.1 JTAG-compatible Boundary Scan
- ZQ mode pin for user-selectable high/low output drive
- 2.5 V or 3.3 V +10%/–5% core power supply
- 2.5 V or 3.3 V I/O supply
- LBO pin for Linear or Interleaved Burst mode
- Byte Write (BW) and/or Global Write (GW) operation
- Internal self-timed write cycle
- Automatic power-down for portable applications
- JEDEC-standard 119- and 209-bump BGA package

		-250	-225	-200	-166	-150	-133	Unit
Pipeline 3-1-1-1	t_{KQ}	2.3	2.5	3.0	3.5	3.8	4.0	ns
	tCycle	4.0	4.4	5.0	6.0	6.6	7.5	ns
3.3 V	Curr (x18)	365	335	305	265	245	215	mA
	Curr (x36)	560	510	460	400	370	330	mA
	Curr (x72)	660	600	540	460	430	380	mA
2.5 V	Curr (x18)	360	330	305	260	240	215	mA
	Curr (x36)	550	500	460	390	360	330	mA
	Curr (x72)	640	590	530	450	420	370	mA
Flow Through 2-1-1-1	t_{KQ}	6.0	6.5	7.5	8.5	10	11	ns
	tCycle	7.0	7.5	8.5	10	10	15	ns
3.3 V	Curr (x18)	235	230	210	200	195	150	mA
	Curr (x36)	300	300	270	270	270	200	mA
	Curr (x72)	350	350	300	300	300	220	mA
2.5 V	Curr (x18)	235	230	210	200	195	145	mA
	Curr (x36)	300	300	270	270	270	190	mA
	Curr (x72)	340	340	300	300	300	220	mA

Functional Description

Applications

The GS8324Z18/36/72 is a 37,748,736-bit high performance 2-die synchronous SRAM module with a 2-bit burst address counter. Although of a type originally developed for Level 2 Cache applications supporting high performance CPUs, the device now finds application in synchronous SRAM applications, ranging from DSP main store to networking chip set support.

Controls

Addresses, data I/Os, chip enable (E1), address burst control inputs (ADSP, ADSC, ADV), and write control inputs (Bx, BW, GW) are synchronous and are controlled by a positive-edge-triggered clock input (CK). Output enable (G) and power down control (ZZ) are asynchronous inputs. Burst cycles can be initiated with either ADSP or ADSC inputs. In Burst mode, subsequent burst addresses are generated internally and are controlled by ADV. The burst address counter may be configured to count in either linear or interleave order with the Linear Burst Order (LBO) input. The Burst function need not be used. New addresses can be loaded on every cycle with no degradation of chip performance.

Flow Through/Pipeline Reads

The function of the Data Output register can be controlled by the user via the FT mode . Holding the FT mode pin low places the RAM in Flow Through mode, causing output data to bypass the Data Output Register. Holding FT high places the RAM in Pipeline mode, activating the rising-edge-triggered Data Output Register.

Byte Write and Global Write

Byte write operation is performed by using Byte Write enable (BW) input combined with one or more individual byte write signals (Bx). In addition, Global Write (GW) is available for writing all bytes at one time, regardless of the Byte Write control inputs.

FLXDrive™

The ZQ pin allows selection between high drive strength (ZQ low) for multi-drop bus applications and normal drive strength (ZQ floating or high) point-to-point applications. See the Output Driver Characteristics chart for details.

Sleep Mode

Low power (Sleep mode) is attained through the assertion (High) of the ZZ signal, or by stopping the clock (CK). Memory data is retained during Sleep mode.

Core and Interface Voltages

The GS8324Z18/36/72 operates on a 2.5 V or 3.3 V power supply. All input are 3.3 V and 2.5 V compatible. Separate output power (V_{DDQ}) pins are used to decouple output noise from the internal circuits and are 3.3 V and 2.5 V compatible.

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NoBL is a trademark of Cypress Semiconductor Corp.. NtRAM is a trademark of Samsung Electronics Co.. ZBT is a trademark of Integrated Device Technology, Inc.

GS8324Z72B Pad Out
209-Bump BGA—Top View

	1	2	3	4	5	6	7	8	9	10	11	
A	DQ_{G5}	DQ_{G1}	A13	E2	A14	ADV	A15	$\overline{E3}$	A17	DQ_{B1}	DQ_{B5}	A
B	DQ_{G6}	DQ_{G2}	$\overline{BC}$	$\overline{BG}$	NC	$\overline{W}$	A16	$\overline{BB}$	$\overline{BF}$	DQ_{B2}	DQ_{B6}	B
C	DQ_{G7}	DQ_{G3}	$\overline{BH}$	$\overline{BD}$	NC	$\overline{E1}$	NC	$\overline{BE}$	$\overline{BA}$	DQ_{B3}	DQ_{B7}	C
D	DQ_{G8}	DQ_{G4}	V_{SS}	NC	NC	$\overline{G}$	NC	NC	V_{SS}	DQ_{B4}	DQ_{B8}	D
E	DQP_{G9}	DQP_{C9}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{DD}	V_{DD}	V_{DDQ}	V_{DDQ}	DQP_{F9}	DQP_{B9}	E
F	DQ_{C4}	DQ_{C8}	V_{SS}	V_{SS}	V_{SS}	ZQ	V_{SS}	V_{SS}	V_{SS}	DQ_{F8}	DQ_{F4}	F
G	DQ_{C3}	DQ_{C7}	V_{DDQ}	V_{DDQ}	V_{DD}	MCH	V_{DD}	V_{DDQ}	V_{DDQ}	DQ_{F7}	DQ_{F3}	G
H	DQ_{C2}	DQ_{C6}	V_{SS}	V_{SS}	V_{SS}	MCL	V_{SS}	V_{SS}	V_{SS}	DQ_{F6}	DQ_{F2}	H
J	DQ_{C1}	DQ_{C5}	V_{DDQ}	V_{DDQ}	V_{DD}	MCH	V_{DD}	V_{DDQ}	V_{DDQ}	DQ_{F5}	DQ_{F1}	J
K	NC	NC	CK	NC	V_{SS}	MCL	V_{SS}	NC	NC	NC	NC	K
L	DQ_{H1}	DQ_{H5}	V_{DDQ}	V_{DDQ}	V_{DD}	$\overline{FT}$	V_{DD}	V_{DDQ}	V_{DDQ}	DQ_{A5}	DQ_{A1}	L
M	DQ_{H2}	DQ_{H6}	V_{SS}	V_{SS}	V_{SS}	MCL	V_{SS}	V_{SS}	V_{SS}	DQ_{A6}	DQ_{A2}	M
N	DQ_{H3}	DQ_{H7}	V_{DDQ}	V_{DDQ}	V_{DD}	MCH	V_{DD}	V_{DDQ}	V_{DDQ}	DQ_{A7}	DQ_{A3}	N
P	DQ_{H4}	DQ_{H8}	V_{SS}	V_{SS}	V_{SS}	ZZ	V_{SS}	V_{SS}	V_{SS}	DQ_{A8}	DQ_{A4}	P
R	DQP_{D9}	DQP_{H9}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{DD}	V_{DD}	V_{DDQ}	V_{DDQ}	DQP_{A9}	DQP_{E9}	R
T	DQ_{D8}	DQ_{D4}	V_{SS}	NC	NC	$\overline{LBO}$	$\overline{PE}$	NC	V_{SS}	DQ_{E4}	DQ_{E8}	T
U	DQ_{D7}	DQ_{D3}	NC	A12	NC	A11	**A18**	A10	NC	DQ_{E3}	DQ_{E7}	U
V	DQ_{D6}	DQ_{D2}	A9	A8	A7	A1	A6	A5	A4	DQ_{E2}	DQ_{E6}	V
W	DQ_{D5}	DQ_{D1}	TMS	TDI	A3	A0	A2	TDO	TCK	DQ_{E1}	DQ_{E5}	W

11 x 19 Bump BGA—14 x 22 mm^2 Body—1 mm Bump Pitch

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GS8324Z36C Pad Out
209-Bump BGA—Top View

	1	2	3	4	5	6	7	8	9	10	11	
A	NC	NC	A13	E2	A14	ADV	A15	$\overline{E3}$	A17	DQ_{B1}	DQ_{B5}	A
B	NC	NC	$\overline{BC}$	NC	**A19**	$\overline{W}$	A16	$\overline{BB}$	NC	DQ_{B2}	DQ_{B6}	B
C	NC	NC	NC	$\overline{BD}$	NC	$\overline{E1}$	NC	NC	$\overline{BA}$	DQ_{B3}	DQ_{B7}	C
D	NC	NC	V_{SS}	NC	NC	$\overline{G}$	NC	NC	V_{SS}	DQ_{B4}	DQ_{B8}	D
E	NC	DQP_{C9}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{DD}	V_{DD}	V_{DDQ}	V_{DDQ}	NC	DQP_{B9}	E
F	DQ_{C4}	DQ_{C8}	V_{SS}	V_{SS}	V_{SS}	ZQ	V_{SS}	V_{SS}	V_{SS}	NC	NC	F
G	DQ_{C3}	DQ_{C7}	V_{DDQ}	V_{DDQ}	V_{DD}	MCH	V_{DD}	V_{DDQ}	V_{DDQ}	NC	NC	G
H	DQ_{C2}	DQ_{C6}	V_{SS}	V_{SS}	V_{SS}	MCL	V_{SS}	V_{SS}	V_{SS}	NC	NC	H
J	DQ_{C1}	DQ_{C5}	V_{DDQ}	V_{DDQ}	V_{DD}	MCH	V_{DD}	V_{DDQ}	V_{DDQ}	NC	NC	J
K	NC	NC	CK	NC	V_{SS}	MCL	V_{SS}	NC	NC	NC	NC	K
L	NC	NC	V_{DDQ}	V_{DDQ}	V_{DD}	$\overline{FT}$	V_{DD}	V_{DDQ}	V_{DDQ}	DQ_{A5}	DQ_{A1}	L
M	NC	NC	V_{SS}	V_{SS}	V_{SS}	MCL	V_{SS}	V_{SS}	V_{SS}	DQ_{A6}	DQ_{A2}	M
N	NC	NC	V_{DDQ}	V_{DDQ}	V_{DD}	MCH	V_{DD}	V_{DDQ}	V_{DDQ}	DQ_{A7}	DQ_{A3}	N
P	NC	NC	V_{SS}	V_{SS}	V_{SS}	ZZ	V_{SS}	V_{SS}	V_{SS}	DQ_{A8}	DQ_{A4}	P
R	DQP_{D9}	NC	V_{DDQ}	V_{DDQ}	V_{DD}	V_{DD}	V_{DD}	V_{DDQ}	V_{DDQ}	DQP_{A9}	NC	R
T	DQ_{D8}	DQ_{D4}	V_{SS}	NC	NC	$\overline{LBO}$	$\overline{PE}$	NC	V_{SS}	NC	NC	T
U	DQ_{D7}	DQ_{D3}	NC	A12	NC	A11	**A18**	A10	NC	NC	NC	U
V	DQ_{D6}	DQ_{D2}	A9	A8	A7	A1	A6	A5	A4	NC	NC	V
W	DQ_{D5}	DQ_{D1}	TMS	TDI	A3	A0	A2	TDO	TCK	NC	NC	W

11 x 19 Bump BGA—14 x 22 mm^2 Body—1 mm Bump Pitch

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GS8324Z18C Pad Out
209-Bump BGA—Top View

	1	2	3	4	5	6	7	8	9	10	11	
A	NC	NC	A13	**VDD**	A14	ADV	A15	**VSS**	A17	NC	NC	A
B	NC	NC	$\overline{BB}$	NC	**A19**	$\overline{W}$	A16	NC	NC	NC	NC	B
C	NC	NC	NC	NC	NC	$\overline{E1}$	**A20**	NC	$\overline{BA}$	NC	NC	C
D	NC	NC	V_{SS}	NC	NC	$\overline{G}$	NC	NC	V_{SS}	NC	NC	D
E	NC	*DQP*$_{B9}$	V_{DDQ}	V_{DDQ}	V_{DD}	V_{DD}	V_{DD}	V_{DDQ}	V_{DDQ}	NC	NC	E
F	DQ$_{B4}$	DQ$_{B8}$	V_{SS}	V_{SS}	V_{SS}	ZQ	V_{SS}	V_{SS}	V_{SS}	NC	NC	F
G	DQ$_{B3}$	DQ$_{B7}$	V_{DDQ}	V_{DDQ}	V_{DD}	MCH	V_{DD}	V_{DDQ}	V_{DDQ}	NC	NC	G
H	DQ$_{B2}$	DQ$_{B6}$	V_{SS}	V_{SS}	V_{SS}	MCL	V_{SS}	V_{SS}	V_{SS}	NC	NC	H
J	DQ$_{B1}$	DQ$_{B5}$	V_{DDQ}	V_{DDQ}	V_{DD}	MCH	V_{DD}	V_{DDQ}	V_{DDQ}	NC	NC	J
K	NC	NC	CK	NC	V_{SS}	MCL	V_{SS}	NC	NC	NC	NC	K
L	NC	NC	V_{DDQ}	V_{DDQ}	V_{DD}	$\overline{FT}$	V_{DD}	V_{DDQ}	V_{DDQ}	DQ$_{A5}$	DQ$_{A1}$	L
M	NC	NC	V_{SS}	V_{SS}	V_{SS}	MCL	V_{SS}	V_{SS}	V_{SS}	DQ$_{A6}$	DQ$_{A2}$	M
N	NC	NC	V_{DDQ}	V_{DDQ}	V_{DD}	**VDD**	V_{DD}	V_{DDQ}	V_{DDQ}	DQ$_{A7}$	DQ$_{A3}$	N
P	NC	NC	V_{SS}	V_{SS}	V_{SS}	ZZ	V_{SS}	V_{SS}	V_{SS}	DQ$_{A8}$	DQ$_{A4}$	P
R	NC	NC	V_{DDQ}	V_{DDQ}	V_{DD}	V_{DD}	V_{DD}	V_{DDQ}	V_{DDQ}	*DQP*$_{A9}$	NC	R
T	NC	NC	V_{SS}	NC	NC	$\overline{LBO}$	$\overline{PE}$	NC	V_{SS}	NC	NC	T
U	NC	NC	NC	A12	NC	A11	**A18**	A10	NC	NC	NC	U
V	NC	NC	A9	A8	A7	A1	A6	A5	A4	NC	NC	V
W	NC	NC	TMS	TDI	A3	A0	A2	TDO	TCK	NC	NC	W

11 x 19 Bump BGA—14 x 22 mm^2 Body—1 mm Bump Pitch

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GS8324Z18/36/72 209-Bump BGA Pin Description

Pin Location	Symbol	Type	Description
W6, V6	A_0, A_1	I	Address field LSBs and Address Counter Preset Inputs.
W7, W5, V9, V8, V7, V5, V4, V3, U8, U6, U4, A3, A5, A7, B7, A9, U7	An	I	Address Inputs
B5	A_{19}	I	Address Inputs (x36/x18 Versions)
C7	A_{20}	I	Address Inputs (x18 Version)
L11, M11, N11, P11, L10, M10, N10, P10, R10 A10, B10, C10, D10, A11, B11, C11, D11, E11 J1, H1, G1, F1, J2, H2, G2, F2, E2 W2, V2, U2, T2, W1, V1, U1, T1, R1 W10, V10, U10, T10, W11, V11, U11, T11, R11 J11, H11, G11, F11, J10, H10, G10, F10, E10 A2, B2, C2, D2, A1, B1, C1, D1, E1 L1, M1, N1, P1, L2, M2, N2, P2, R2	DQ_{A1}–DQ_{A9} DQ_{B1}–DQ_{B9} DQ_{C1}–DQ_{C9} DQ_{D1}–DQ_{D9} DQ_{E1}–DQ_{E9} DQ_{F1}–DQ_{F9} DQ_{G1}–DQ_{G9} DQ_{H1}–DQ_{H9}	I/O	Data Input and Output pins (x72 Version)
L11, M11, N11, P11, L10, M10, N10, P10, R10 A10, B10, C10, D10, A11, B11, C11, D11, E11 J1, H1, G1, F1, J2, H2, G2, F2, E2 W2, V2, U2, T2, W1, V1, U1, T1, R1	DQ_{A1}–DQ_{A9} DQ_{B1}–DQ_{B9} DQ_{C1}–DQ_{C9} DQ_{D1}–DQ_{D9}	I/O	Data Input and Output pins (x36 Version)
L11, M11, N11, P11, L10, M10, N10, P10, R10 J1, H1, G1, F1, J2, H2, G2, F2, E2	DQ_{A1}–DQ_{A9} DQ_{B1}–DQ_{B9}	I/O	Data Input and Output pins (x18 Version)
C9, B8	$\overline{B}_A$, $\overline{B}_B$	I	Byte Write Enable for DQ_A, DQ_B I/Os; active low
B3, C4	$\overline{B}_C$,$\overline{B}_D$	I	Byte Write Enable for DQ_C, DQ_D I/Os; active low (x72/x36 Versions)
C8, B9, B4, C3	$\overline{B}_E$, $\overline{B}_F$, $\overline{B}_G$,$\overline{B}_H$	I	Byte Write Enable for DQ_E, DQ_F, DQ_G, DQ_H I/Os; active low (x72 Version)
B5	NC	—	No Connect (x72 Version)
C7	NC	—	No Connect (x72/x36 Versions)
W10, V10, U10, T10, W11, V11, U11, T11, R11 J11, H11, G11, F11, J10, H10, G10, F10, E10 A2, B2, C2, D2, A1, B1, C1, D1, E1 L1, M1, N1, P1, L2, M2, N2, P2, R2, C8, B9, B4, C3	NC	—	No Connect (x36/x18 Versions)
B3, C4	NC	—	No Connect (x18 Version)
C5, D4, D5, D7, D8, K1, K2, K4, K8, K9, K10, K11, T4, T5, T7, T8, U3, U5, U9	NC	—	No Connect
K3	CK	I	Clock Input Signal; active high
C6	$\overline{E}_1$	I	Chip Enable; active low
A8	$\overline{E}_3$	I	Chip Enable; active low (x72/x36 Versions)
A4	E_2	I	Chip Enable; active high (x72/x36 Versions)
D6	$\overline{G}$	I	Output Enable; active low
A6	ADV	I	Burst address counter advance enable

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GS8324Z18/36/72 209-Bump BGA Pin Description

Pin Location	Symbol	Type	Description
P6	ZZ	I	Sleep Mode control; active high
L6	$\overline{FT}$	I	Flow Through or Pipeline mode; active low
T6	$\overline{LBO}$	I	Linear Burst Order mode; active low
G6, J6	MCH	I	Must Connect High
N6	MCH	I	Must Connect High (x72 and x36 versions)
H6, J6, K6, M6	MCL		Must Connect Low
A8, N6	MCL		Must Connect Low (x18 version)
B6	$\overline{W}$	I	Write Enable; active low
T7	$\overline{PE}$	I	Parity Bit Enable; active low (High = x16/32 Mode, Low = x18/36 Mode)
F6	ZQ	I	FLXDrive Output Impedance Control (Low = Low Impedance [High Drive], High = High Impedance [Low Drive])
W3	TMS	I	Scan Test Mode Select
W4	TDI	I	Scan Test Data In
W8	TDO	O	Scan Test Data Out
W9	TCK	I	Scan Test Clock
A4, N6	V_{DD}	I	Core power supply (x18 version)
E5, E6, E7, G5, G7, J5, J7, L5, L7, N5, N7, R5, R6, R7	V_{DD}	I	Core power supply
D3, D9, F3, F4, F5, F7, F8, F9, H3, H4, H5, H7, H8, H9, K5, K7, M3, M4, M5, M7, M8, M9, P3, P4, P5, P7, P8, P9, T3, T9	V_{SS}	I	I/O and Core Ground
E3, E4, E8, E9, G3, G4, G8, G9, J3, J4, J8, J9, L3, L4, L8, L9, N3, N4, N8, N9, R3, R4, R8, R9	V_{DDQ}	I	Output driver power supply

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GS8324Z36B Pad Out

119-Bump BGA—Top View

	1	2	3	4	5	6	7	
A	V_{DDQ}	A6	A7	A18	A8	A9	V_{DDQ}	A
B	NC	E2	A4	ADV	A15	$\overline{E3}$	NC	B
C	NC	A5	A3	V_{DD}	A14	A16	NC	C
D	DQC	*DQPC*	V_{SS}	ZQ	V_{SS}	*DQPB*	DQB	D
E	DQC	DQC	V_{SS}	$\overline{E1}$	V_{SS}	DQB	DQB	E
F	V_{DDQ}	DQC	V_{SS}	$\overline{G}$	V_{SS}	DQB	V_{DDQ}	F
G	DQC	DQC	$\overline{BC}$	A17	$\overline{BB}$	DQB	DQB	G
H	DQC	DQC	V_{SS}	$\overline{W}$	V_{SS}	DQB	DQB	H
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}	J
K	DQD	DQD	V_{SS}	CK	V_{SS}	DQA	DQA	K
L	DQD	DQD	$\overline{BD}$	NC	$\overline{BA}$	DQA	DQA	L
M	V_{DDQ}	DQD	V_{SS}	$\overline{CKE}$	V_{SS}	DQA	V_{DDQ}	M
N	DQD	DQD	V_{SS}	A1	V_{SS}	DQA	DQA	N
P	DQD	*DQPD*	V_{SS}	A0	V_{SS}	*DQPA*	DQA	P
R	NC	A2	$\overline{LBO}$	V_{DD}	$\overline{FT}$	A13	$\overline{PE}$	R
T	NC	NC	A10	A11	A12	**A19**	ZZ	T
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}	U

7 x 17 Bump BGA—14 x 22 mm^2 Body—1.27 mm Bump Pitch

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GS8324Z18B Pad Out

119-Bump BGA—Top View

	1	2	3	4	5	6	7	
A	V_{DDQ}	A6	A7	A18	A8	A9	V_{DDQ}	A
B	NC	**VDD**	A4	ADV	A15	**VSS**	NC	B
C	NC	A5	A3	V_{DD}	A14	A16	NC	C
D	DQB	NC	V_{SS}	ZQ	V_{SS}	*DQPA*	NC	D
E	NC	DQB	V_{SS}	$\overline{E1}$	V_{SS}	NC	DQA	E
F	V_{DDQ}	NC	V_{SS}	$\overline{G}$	V_{SS}	DQA	V_{DDQ}	F
G	NC	DQB	$\overline{BB}$	A17	NC	NC	DQA	G
H	DQB	NC	V_{SS}	$\overline{W}$	V_{SS}	DQA	NC	H
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}	J
K	NC	DQB	V_{SS}	CK	V_{SS}	NC	DQA	K
L	DQB	NC	NC	**VDD**	$\overline{BA}$	DQA	NC	L
M	V_{DDQ}	DQB	V_{SS}	$\overline{CKE}$	V_{SS}	NC	V_{DDQ}	M
N	DQB	NC	V_{SS}	A1	V_{SS}	DQA	NC	N
P	NC	*DQPB*	V_{SS}	A0	V_{SS}	NC	DQA	P
R	NC	A2	$\overline{LBO}$	V_{DD}	$\overline{FT}$	A13	$\overline{PE}$	R
T	NC	A10	A11	**A20**	A12	A19	ZZ	T
U	V_{DDQ}	TMS	TDI	TCK	TDO	NC	V_{DDQ}	U

7 x 17 Bump BGA—14 x 22 mm^2 Body—1.27 mm Bump Pitch

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GS8324Z18/36 119-Bump BGA Pin Description

Pin Location	Symbol	Type	Description
P4, N4	A_0, A_1	I	Address field LSBs and Address Counter Preset Inputs
R2, C3, B3, C2, A2, A3, A5, A6, T3, T5, R6, C5, B5, C6, G4, A4	An	I	Address Inputs
T4, T6	An		Address Input (x36 Version)
T2	NC	—	No Connect (x36 Version)
T2, T6, T4	An	I	Address Input (x18 Version)
K7, L7, N7, P7, K6, L6, M6, N6 H7, G7, E7, D7, H6, G6, F6, E6 H1, G1, E1, D1, H2, G2, F2, E2 K1, L1, N1, P1, K2, L2, M2, N2	DQ_{A1}–DQ_{A8} DQ_{B1}–DQ_{B8} DQ_{C1}–DQ_{C8} DQ_{D1}–DQ_{D8}	I/O	Data Input and Output pins. (x36 Version)
P6, D6, D2, P2	DQ_{A9}, DQ_{B9}, DQ_{C9}, DQ_{D9}	I/O	Data Input and Output pins. (x36 Version)
L5, G5, G3, L3	$\overline{B}_A$, $\overline{B}_B$, $\overline{B}_C$, $\overline{B}_D$	I	Byte Write Enable for DQ_A, DQ_B, DQ_C, DQ_D I/Os; active low (x36 Version)
P7, N6, L6, K7, H6, G7, F6, E7, D6 D1, E2, G2, H1, K2, L1, M2, N1, P2	DQ_{A1}–DQ_{A9} DQ_{B1}–DQ_{B9}	I/O	Data Input and Output pins (x18 Version)
L5, G3	$\overline{B}_A$, $\overline{B}_B$	I	Byte Write Enable for DQ_A, DQ_B I/Os; active low (x18 Version)
B1, C1, R1, T1, U6, B7, C7, J3, J5	NC	—	No Connect
P6, N7, M6, L7, K6, H7, G6, E6, D7, D2, E1, F2, G1, H2, K1, L2, N2, P1, G5, L3	NC	—	No Connect (x18 Version)
L4	NC	—	No Connect (x36 Version)
K4	CK	I	Clock Input Signal; active high
M4	$\overline{CKE}$	I	Clock Enable; active low
H4	$\overline{W}$	I	Write Enable; active low
E4	$\overline{E}_1$	I	Chip Enable; active low
B6	$\overline{E}_3$	I	Chip Enable; active low (x36 version)
B2	E_2	I	Chip Enable; active high (x36 version)
F4	$\overline{G}$	I	Output Enable; active low
B4	ADV	I	Burst address counter advance enable
T7	ZZ	I	Sleep mode control; active high
R5	$\overline{FT}$	I	Flow Through or Pipeline mode; active low
R3	$\overline{LBO}$	I	Linear Burst Order mode; active low
D4	ZQ	I	FLXDrive Output Impedance Control (Low = Low Impedance [High Drive], High = High Impedance [Low Drive])
R7	$\overline{PE}$	I	Parity Bit Enable; active low
U2	TMS	I	Scan Test Mode Select
U3	TDI	I	Scan Test Data In

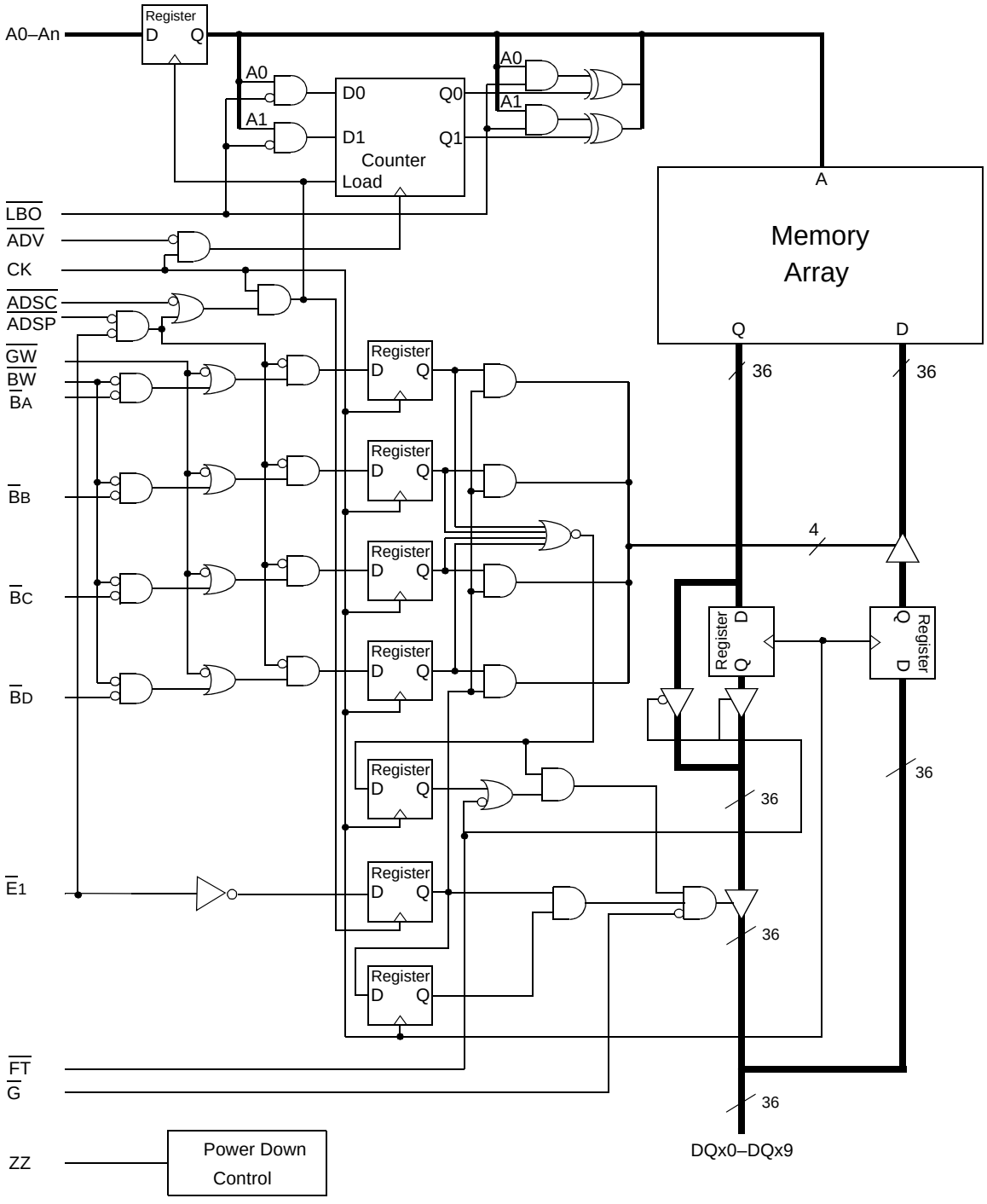
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GS8324Z18/36 119-Bump BGA Pin Description

Pin Location	Symbol	Type	Description
U5	TDO	O	Scan Test Data Out
U4	TCK	I	Scan Test Clock
J2, C4, J4, R4, J6	V_{DD}	I	Core power supply
B2, L4	V_{DD}	I	Core power supply (x18 version)
D3, E3, F3, H3, K3, M3, N3, P3, D5, E5, F5, H5, K5, M5, N5, P5	V_{SS}	I	I/O and Core Ground
B6	V_{SS}	I	I/O and Core Ground (x18 version)
A1, F1, J1, M1, U1, A7, F7, J7, M7, U7	V_{DDQ}	I	Output driver power supply

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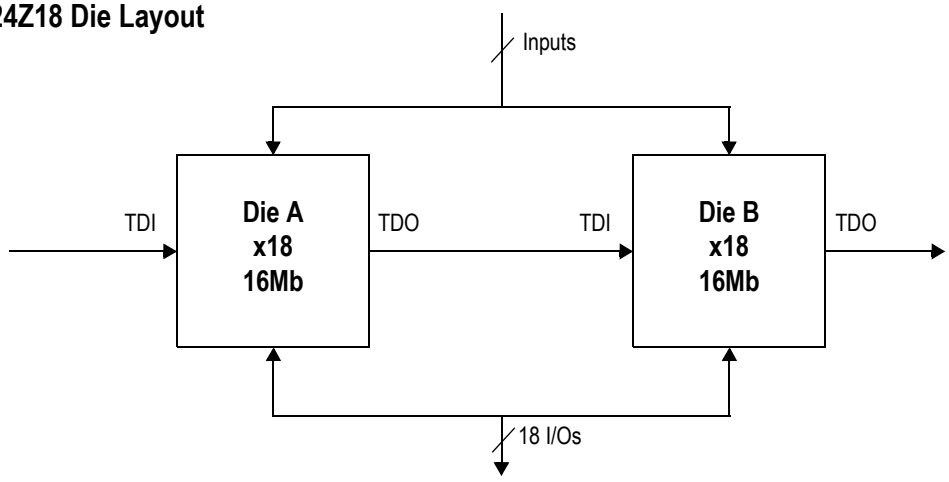
GS8324Z18/36/72 Block Diagram



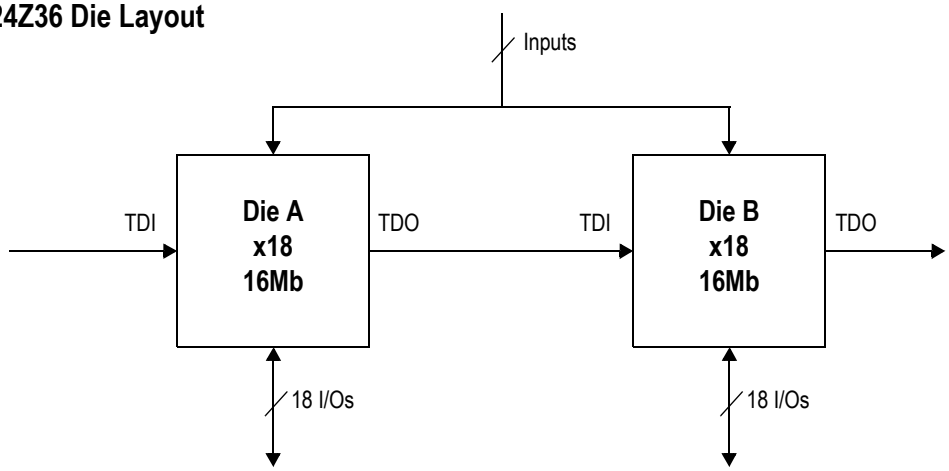
Note: Only x36 version shown for simplicity.

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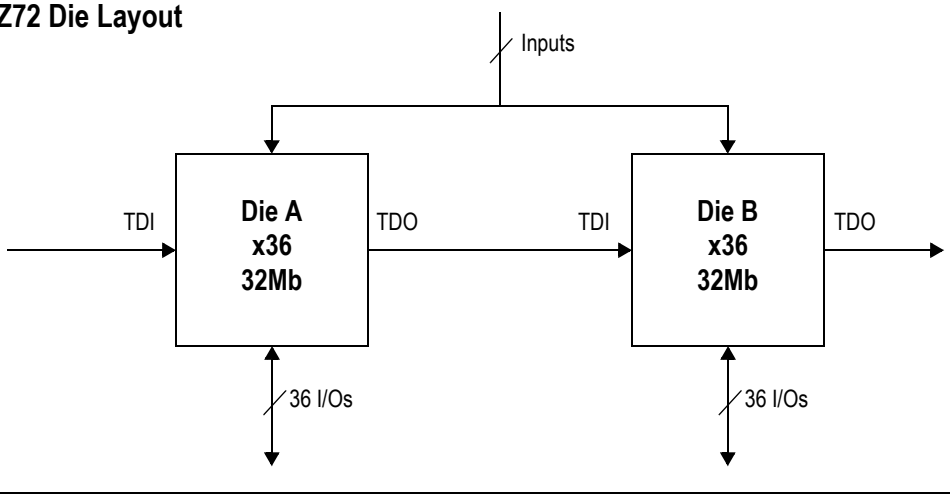
GS8324Z18 Die Layout



GS8324Z36 Die Layout



GS8324Z72 Die Layout



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Functional Details

Clocking

Deassertion of the Clock Enable ($\overline{CKE}$) input blocks the Clock input from reaching the RAM's internal circuits. It may be used to suspend RAM operations. Failure to observe Clock Enable set-up or hold requirements will result in erratic operation.

Pipeline Mode Read and Write Operations

All inputs (with the exception of Output Enable, Linear Burst Order and Sleep) are synchronized to rising clock edges. Single cycle read and write operations must be initiated with the Advance/Load pin (ADV) held low, in order to load the new address. Device activation is accomplished by asserting all three of the Chip Enable inputs ($\overline{E}_1$, E_2, and $\overline{E}_3$). Deassertion of any one of the Enable inputs will deactivate the device.

Function	$\overline{W}$	$\overline{B}_A$	$\overline{B}_B$	$\overline{B}_C$	$\overline{B}_D$
Read	H	X	X	X	X
Write Byte “a”	L	L	H	H	H
Write Byte “b”	L	H	L	H	H
Write Byte “c”	L	H	H	L	H
Write Byte “d”	L	H	H	H	L
Write all Bytes	L	L	L	L	L
Write Abort/NOP	L	H	H	H	H

Read operation is initiated when the following conditions are satisfied at the rising edge of clock: $\overline{CKE}$ is asserted low, all three chip enables ($\overline{E}_1$, E_2, and $\overline{E}_3$) are active, the write enable input signals $\overline{W}$ is deasserted high, and ADV is asserted low. The address presented to the address inputs is latched into the address register and presented to the memory core and control logic. The control logic determines that a read access is in progress and allows the requested data to propagate to the input of the output register. At the next rising edge of clock the read data is allowed to propagate through the output register and onto the output pins.

Write operation occurs when the RAM is selected, CKE is active, and the Write input is sampled low at the rising edge of clock. The Byte Write Enable inputs ($\overline{B}_A$, $\overline{B}_B$, $\overline{B}_C$, and $\overline{B}_D$) determine which bytes will be written. All or none may be activated. A write cycle with no Byte Write inputs active is a no-op cycle. The pipelined NBT SRAM provides double late write functionality, matching the write command versus data pipeline length (2 cycles) to the read command versus data pipeline length (2 cycles). At the first rising edge of clock, Enable, Write, Byte Write(s), and Address are registered. The Data In associated with that address is required at the third rising edge of clock.

Flow Through Mode Read and Write Operations

Operation of the RAM in Flow Through mode is very similar to operations in Pipeline mode. Activation of a Read Cycle and the use of the Burst Address Counter is identical. In Flow Through mode the device may begin driving out new data immediately after new address are clocked into the RAM, rather than holding new data until the following (second) clock edge. Therefore, in Flow Through mode the read pipeline is one cycle shorter than in Pipeline mode.

Write operations are initiated in the same way, but differ in that the write pipeline is one cycle shorter as well, preserving the ability to turn the bus from reads to writes without inserting any dead cycles. While the pipelined NBT RAMs implement a double late write protocol in Flow Through mode a single late write protocol mode is observed. Therefore, in Flow Through mode, address and control are registered on the first rising edge of clock and data in is required at the data input pins at the second rising edge of clock.

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Byte Write Truth Table

Function	$\overline{GW}$	$\overline{BW}$	$\overline{B}_A$	$\overline{B}_B$	$\overline{B}_C$	$\overline{B}_D$	Notes
Read	H	H	X	X	X	X	1
Read	H	L	H	H	H	H	1
Write byte a	H	L	L	H	H	H	2, 3
Write byte b	H	L	H	L	H	H	2, 3
Write byte c	H	L	H	H	L	H	2, 3, 4
Write byte d	H	L	H	H	H	L	2, 3, 4
Write all bytes	H	L	L	L	L	L	2, 3, 4
Write all bytes	L	X	X	X	X	X	

Notes:
1. All byte outputs are active in read cycles regardless of the state of Byte Write Enable inputs.
2. Byte Write Enable inputs $\overline{B}_A$, $\overline{B}_B$, $\overline{B}_C$, and/or $\overline{B}_D$ may be used in any combination with $\overline{BW}$ to write single or multiple bytes.
3. All byte I/Os remain High-Z during all write operations regardless of the state of Byte Write Enable inputs.
4. Bytes "C" and "D" are only available on the x36 version.

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Synchronous Truth Table (x72 and x36 209-Bump BGA)

Operation	Type	Address	$\overline{E}_1$	E_2	$\overline{E}_3$	ZZ	ADV	$\overline{W}$	$\overline{Bx}$	$\overline{G}$	$\overline{CKE}$	CK	DQ	Notes
Deselect Cycle, Power Down	D	None	H	X	X	L	L	X	X	X	L	L-H	High-Z	
Deselect Cycle, Power Down	D	None	X	X	H	L	L	X	X	X	L	L-H	High-Z	
Deselect Cycle, Power Down	D	None	X	L	X	L	L	X	X	X	L	L-H	High-Z	
Deselect Cycle, Continue	D	None	X	X	X	L	H	X	X	X	L	L-H	High-Z	1
Read Cycle, Begin Burst	R	External	L	H	L	L	L	H	X	L	L	L-H	Q	
Read Cycle, Continue Burst	B	Next	X	X	X	L	H	X	X	L	L	L-H	Q	1,10
NOP/Read, Begin Burst	R	External	L	H	L	L	L	H	X	H	L	L-H	High-Z	2
Dummy Read, Continue Burst	B	Next	X	X	X	L	H	X	X	H	L	L-H	High-Z	1,2,10
Write Cycle, Begin Burst	W	External	L	H	L	L	L	L	L	X	L	L-H	D	3
Write Cycle, Continue Burst	B	Next	X	X	X	L	H	X	L	X	L	L-H	D	1,3,10
NOP/Write Abort, Begin Burst	W	None	L	H	L	L	L	L	H	X	L	L-H	High-Z	2,3
Write Abort, Continue Burst	B	Next	X	X	X	L	H	X	H	X	L	L-H	High-Z	1,2,3,10
Clock Edge Ignore, Stall		Current	X	X	X	L	X	X	X	X	H	L-H	-	4
Sleep Mode		None	X	X	X	H	X	X	X	X	X	X	High-Z	

Notes:
1. Continue Burst cycles, whether Read or Write, use the same control inputs. A Deselect continue cycle can only be entered into if a Deselect cycle is executed first.
2. Dummy Read and Write abort can be considered NOPs because the SRAM performs no operation. A Write abort occurs when the $\overline{W}$ pin is sampled low but no Byte Write pins are active, so no write operation is performed.
3. $\overline{G}$ can be wired low to minimize the number of control signals provided to the SRAM. Output drivers will automatically turn off during write cycles.
4. If $\overline{CKE}$ High occurs during a pipelined read cycle, the DQ bus will remain active (Low Z). If $\overline{CKE}$ High occurs during a write cycle, the bus will remain in High Z.
5. X = Don't Care; H = Logic High; L = Logic Low; $\overline{Bx}$ = High = All Byte Write signals are high; $\overline{Bx}$ = Low = One or more Byte/Write signals are Low
6. All inputs, except $\overline{G}$ and ZZ must meet setup and hold times of rising clock edge.
7. Wait states can be inserted by setting $\overline{CKE}$ high.
8. This device contains circuitry that ensures all outputs are in High Z during power-up.
9. A 2-bit burst counter is incorporated.
10. The address counter is incriminated for all Burst continue cycles.

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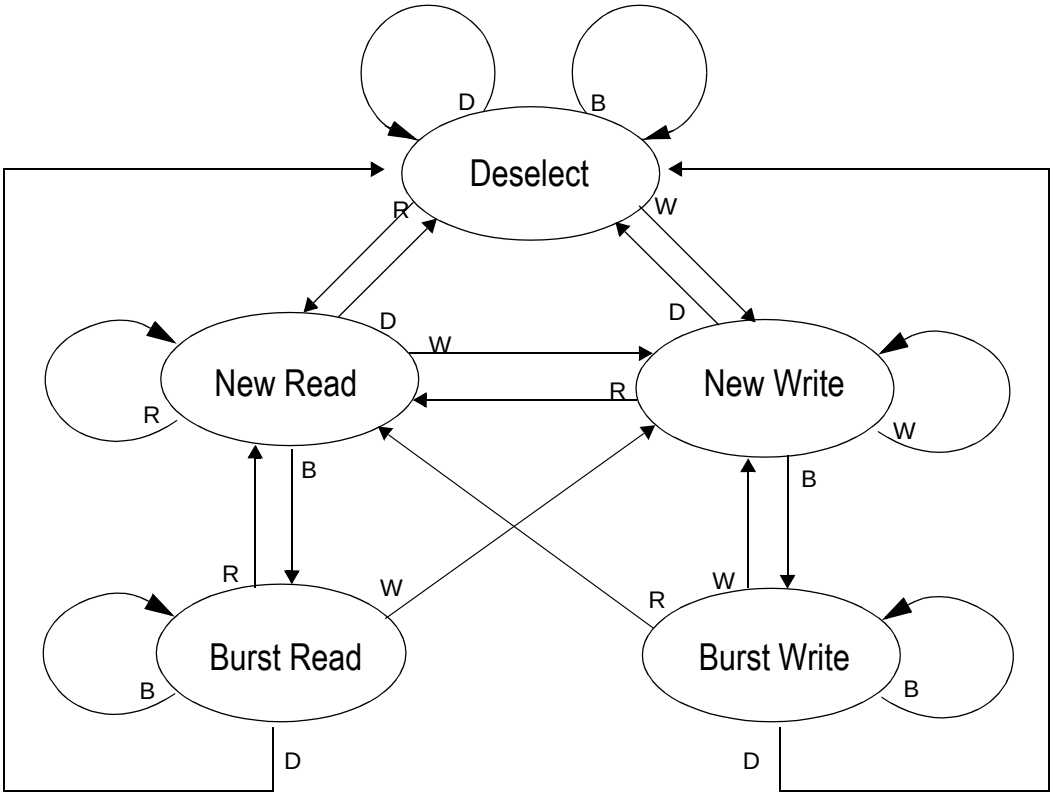
Synchronous Truth Table (x18 209-Bump BGA and x36/x18 119-Bump BGA)

Operation	Type	Address	$\overline{E}_1$	ZZ	ADV	$\overline{W}$	$\overline{Bx}$	$\overline{G}$	$\overline{CKE}$	CK	DQ	Notes
Deselect Cycle, Power Down	D	None	H	L	L	X	X	X	L	L-H	High-Z	
Deselect Cycle, Power Down	D	None	X	L	L	X	X	X	L	L-H	High-Z	
Deselect Cycle, Power Down	D	None	X	L	L	X	X	X	L	L-H	High-Z	
Deselect Cycle, Continue	D	None	X	L	H	X	X	X	L	L-H	High-Z	1
Read Cycle, Begin Burst	R	External	L	L	L	H	X	L	L	L-H	Q	
Read Cycle, Continue Burst	B	Next	X	L	H	X	X	L	L	L-H	Q	1,10
NOP/Read, Begin Burst	R	External	L	L	L	H	X	H	L	L-H	High-Z	2
Dummy Read, Continue Burst	B	Next	X	L	H	X	X	H	L	L-H	High-Z	1,2,10
Write Cycle, Begin Burst	W	External	L	L	L	L	L	X	L	L-H	D	3
Write Cycle, Continue Burst	B	Next	X	L	H	X	L	X	L	L-H	D	1,3,10
NOP/Write Abort, Begin Burst	W	None	L	L	L	L	H	X	L	L-H	High-Z	2,3
Write Abort, Continue Burst	B	Next	X	L	H	X	H	X	L	L-H	High-Z	1,2,3,10
Clock Edge Ignore, Stall		Current	X	L	X	X	X	X	H	L-H	-	4
Sleep Mode		None	X	H	X	X	X	X	X	X	High-Z	

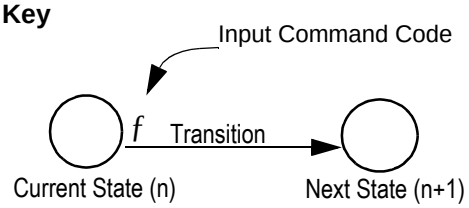
Notes:
1. Continue Burst cycles, whether Read or Write, use the same control inputs. A Deselect continue cycle can only be entered into if a Deselect cycle is executed first.
2. Dummy Read and Write abort can be considered NOPs because the SRAM performs no operation. A Write abort occurs when the $\overline{W}$ pin is sampled low but no Byte Write pins are active, so no write operation is performed.
3. $\overline{G}$ can be wired low to minimize the number of control signals provided to the SRAM. Output drivers will automatically turn off during write cycles.
4. If $\overline{CKE}$ High occurs during a pipelined read cycle, the DQ bus will remain active (Low Z). If $\overline{CKE}$ High occurs during a write cycle, the bus will remain in High Z.
5. X = Don't Care; H = Logic High; L = Logic Low; $\overline{Bx}$ = High = All Byte Write signals are high; $\overline{Bx}$ = Low = One or more Byte/ Write signals are Low
6. All inputs, except $\overline{G}$ and ZZ must meet setup and hold times of rising clock edge.
7. Wait states can be inserted by setting $\overline{CKE}$ high.
8. This device contains circuitry that ensures all outputs are in High Z during power-up.
9. A 2-bit burst counter is incorporated.
10. The address counter is incriminated for all Burst continue cycles.

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Pipelined and Flow Through Read Write Control State Diagram

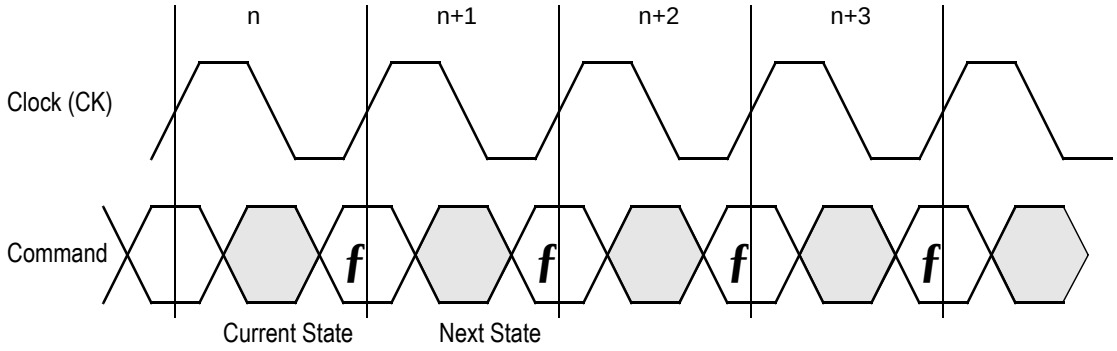


Key



Notes

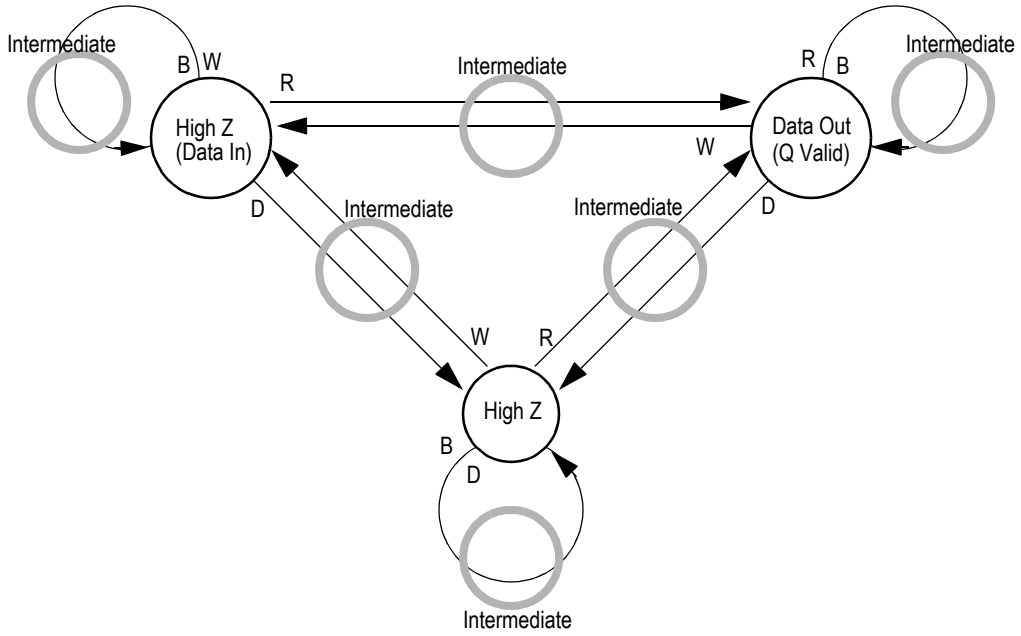
1. The Hold command ($\overline{CKE}$ Low) is not shown because it prevents any state change.
2. W, R, B, and D represent input command codes as indicated in the Synchronous Truth Table.



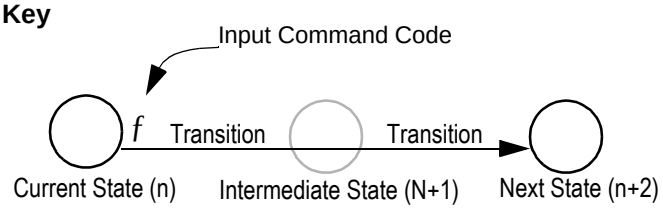
Current State and Next State Definition for Pipelined and Flow through Read/Write Control State Diagram

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Pipeline Mode Data I/O State Diagram

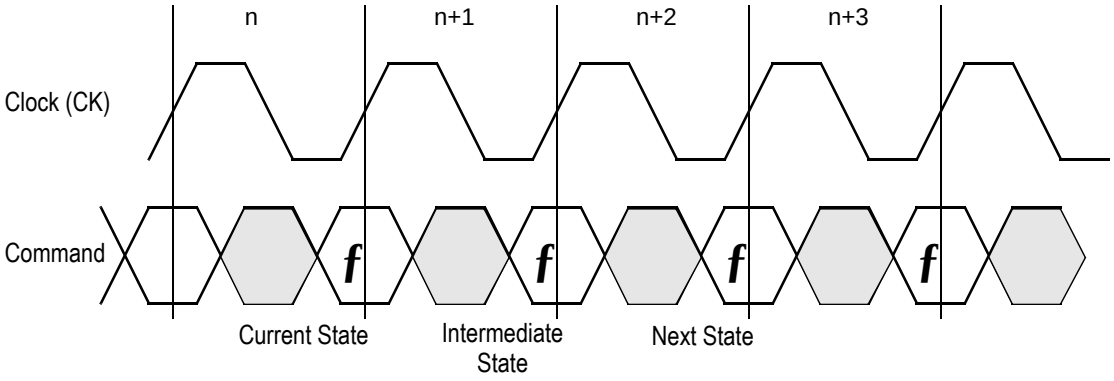


Key



Notes

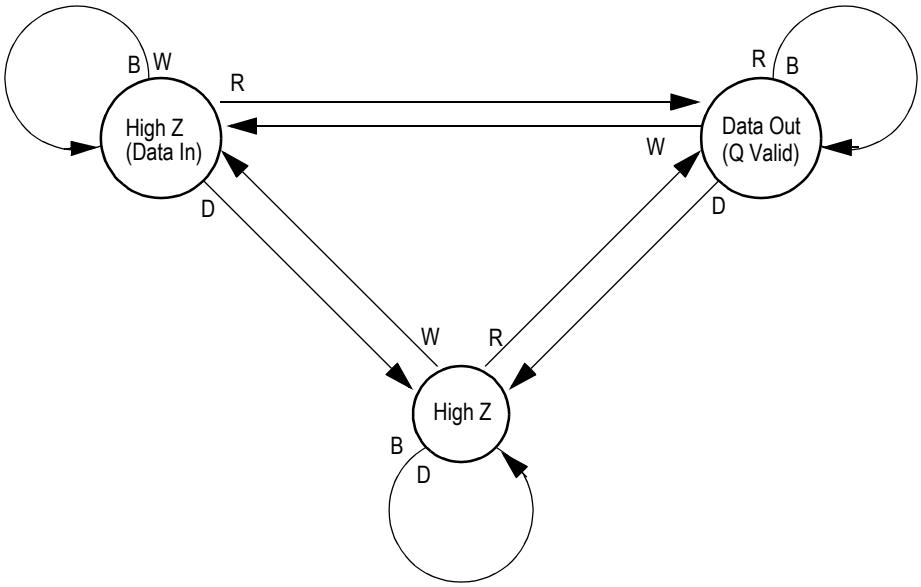
1. The Hold command ($\overline{\text{CKE}}$ Low) is not shown because it prevents any state change.
2. W, R, B, and D represent input command codes as indicated in the Truth Tables.



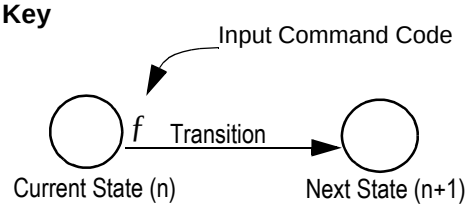
Current State and Next State Definition for Pipeline Mode Data I/O State Diagram

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Flow Through Mode Data I/O State Diagram

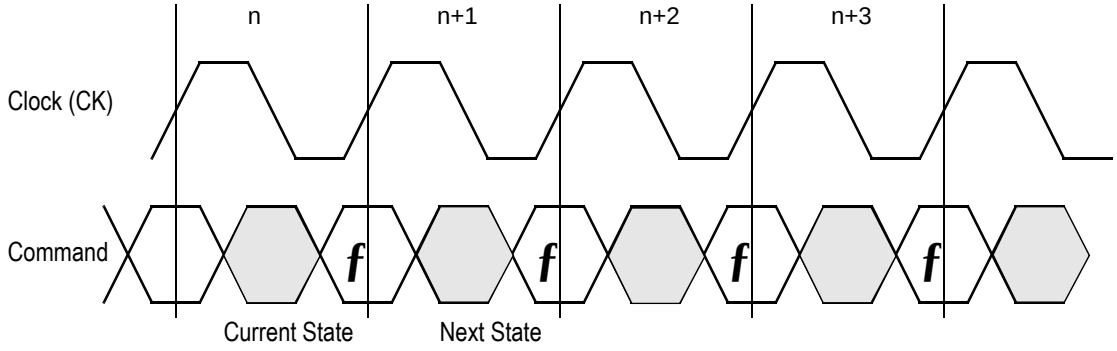


Key



Notes

1. The Hold command ($\overline{CKE}$ Low) is not shown because it prevents any state change.
2. W, R, B, and D represent input command codes as indicated in the Truth Tables.



Current State and Next State Definition for: Pipeline and Flow Through Read Write Control State Diagram

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Burst Cycles

Although NBT RAMs are designed to sustain 100% bus bandwidth by eliminating turnaround cycle when there is transition from read to write, multiple back-to-back reads or writes may also be performed. NBT SRAMs provide an on-chip burst address generator that can be utilized, if desired, to further simplify burst read or write implementations. The ADV control pin, when driven high, commands the SRAM to advance the internal address counter and use the counter generated address to read or write the SRAM. The starting address for the first cycle in a burst cycle series is loaded into the SRAM by driving the ADV pin low, into Load mode.

Burst Order

The burst address counter wraps around to its initial state after four addresses (the loaded address and three more) have been accessed. The burst sequence is determined by the state of the Linear Burst Order pin ($\overline{LBO}$). When this pin is Low, a linear burst sequence is selected. When the RAM is installed with the LBO pin tied high, Interleaved burst sequence is selected. See the tables below for details.

Mode Pin Functions

Mode Name	Pin Name	State	Function
Burst Order Control	$\overline{LBO}$	L	Linear Burst
		H	Interleaved Burst
Output Register Control	$\overline{FT}$	L	Flow Through
		H or NC	Pipeline
Power Down Control	ZZ	L or NC	Active
		H	Standby, $I_{DD} = I_{SB}$
Parity Enable	$\overline{PE}$	L or NC	Activate 9th I/O's (x18/36 Mode)
		H	Deactivate 9th I/O's (x16/32 Mode)
FLXDrive Output Impedance Control	ZQ	L	High Drive (Low Impedance)
		H or NC	Low Drive (High Impedance)

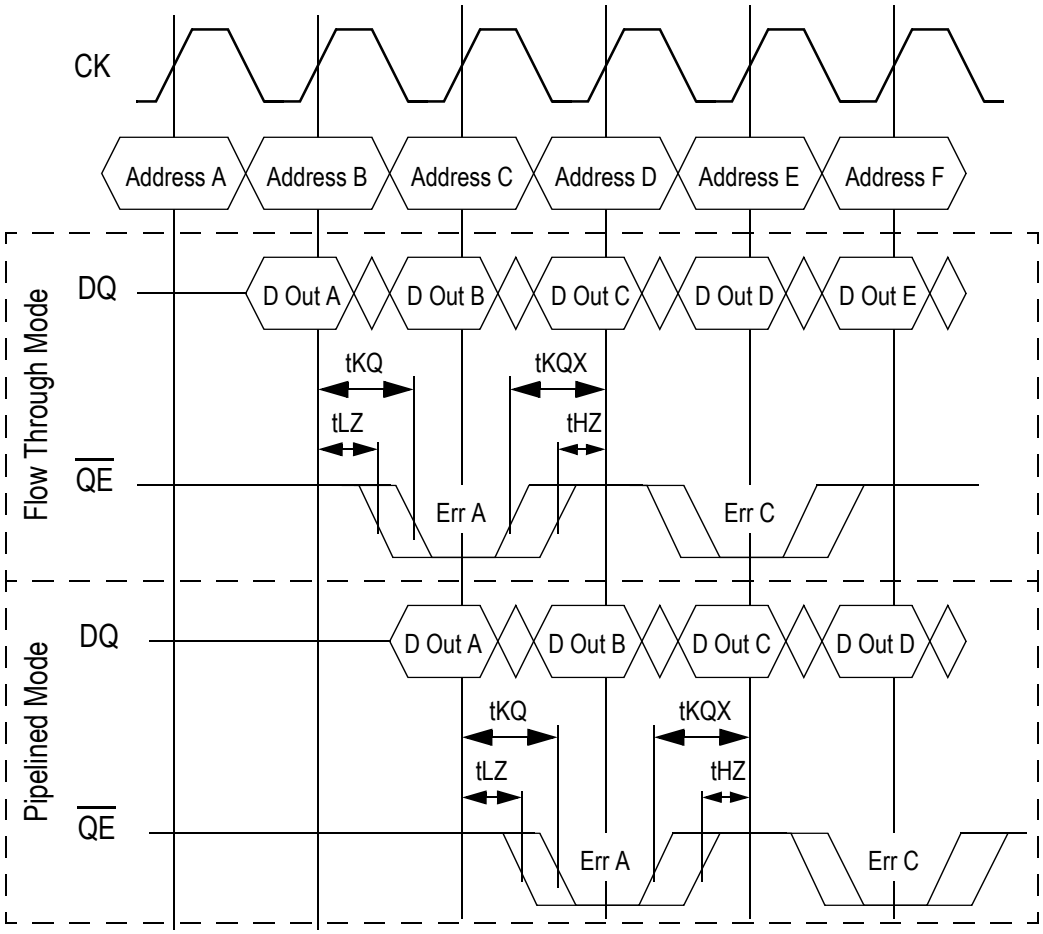
Note:
There are pull-up devices on the ZQ, SCD DP, and $\overline{FT}$ pins and a pull-down devices on the $\overline{PE}$ and ZZ pins, so those input pins can be unconnected and the chip will operate in the default states as specified in the above tables.

Enable/Disable Parity I/O Pins

This SRAM allows the user to configure the device to operate in Parity I/O active (x18, x36, or x72) or in Parity I/O inactive (x16, x32, or x64) mode. Holding the $\overline{PE}$ bump low or letting it float will activate the 9th I/O on each byte of the RAM. Grounding $\overline{PE}$ deactivates the 9th I/O of each byte, although the bit in each byte of the memory array remains active to store and recall parity bits generated and read into the ByteSafe parity circuits.

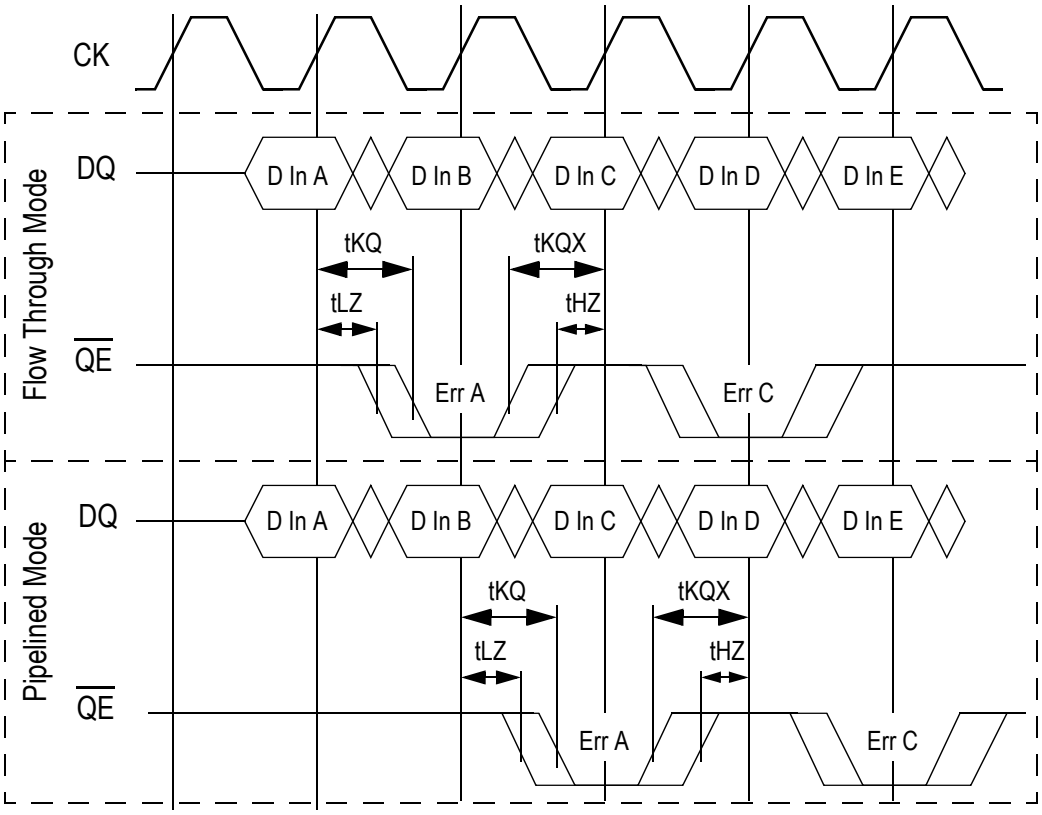
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x16/32/64 Mode ($\overline{PE}$ = 0) Read Parity Error Output Timing Diagram



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x18/x36 Mode ($\overline{PE}$ = 1) Write Parity Error Output Timing Diagram



BPR 1999.05.18

Burst Counter Sequences

Linear Burst Sequence

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1st address	00	01	10	11
2nd address	01	10	11	00
3rd address	10	11	00	01
4th address	11	00	01	10

Note: The burst counter wraps to initial state on the 5th clock.

Interleaved Burst Sequence

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1st address	00	01	10	11
2nd address	01	00	11	10
3rd address	10	11	00	01
4th address	11	10	01	00

Note: The burst counter wraps to initial state on the 5th clock.

BPR 1999.05.18

Sleep Mode

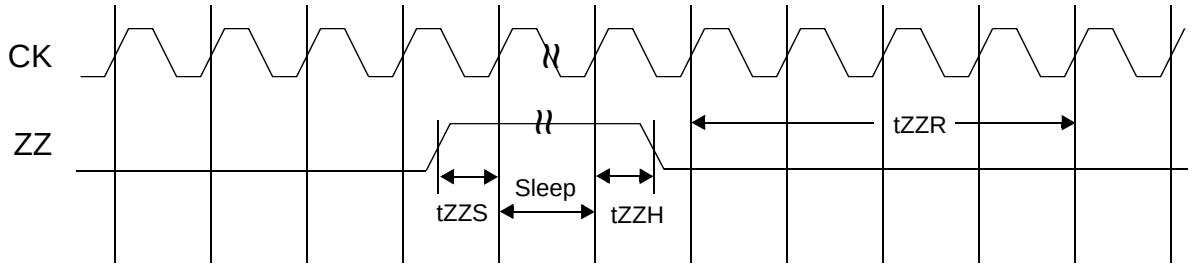
During normal operation, ZZ must be pulled low, either by the user or by its internal pull down resistor. When ZZ is pulled high, the SRAM will enter a Power Sleep mode after 2 cycles. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM operates normally after 2 cycles of wake up time.

Sleep mode is a low current, power-down mode in which the device is deselected and current is reduced to $I_{SB}2$. The duration of

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Sleep mode is dictated by the length of time the ZZ is in a High state. After entering Sleep mode, all inputs except ZZ become disabled and all outputs go to High-Z The ZZ pin is an asynchronous, active high input that causes the device to enter Sleep mode. When the ZZ pin is driven high, $I_{SB}2$ is guaranteed after the time tZZI is met. Because ZZ is an asynchronous input, pending operations or operations in progress may not be properly completed if ZZ is asserted. Therefore, Sleep mode must not be initiated until valid pending operations are completed. Similarly, when exiting Sleep mode during tZZR, only a Deselect or Read commands may be applied while the SRAM is recovering from Sleep mode.

Sleep Mode Timing Diagram



Designing for Compatibility

The GSI NBT SRAMs offer users a configurable selection between Flow Through mode and Pipeline mode via the $\overline{FT}$ signal found on . Not all vendors offer this option, however most mark as V_{DD} or V_{DDQ} on pipelined parts and V_{SS} on flow through parts. GSI NBT SRAMs are fully compatible with these sockets.

Absolute Maximum Ratings

(All voltages reference to V_{SS})

Symbol	Description	Value	Unit
V_{DD}	Voltage on V_{DD} Pins	–0.5 to 4.6	V
V_{DDQ}	Voltage in V_{DDQ} Pins	–0.5 to 4.6	V
V_{CK}	Voltage on Clock Input Pin	–0.5 to 6	V
$V_{I/O}$	Voltage on I/O Pins	–0.5 to V_{DDQ} +0.5 (≤ 4.6 V max.)	V
V_{IN}	Voltage on Other Input Pins	–0.5 to V_{DD} +0.5 (≤ 4.6 V max.)	V
I_{IN}	Input Current on Any Pin	+/–20	mA
I_{OUT}	Output Current on Any I/O Pin	+/–20	mA
P_D	Package Power Dissipation	1.5	W
T_{STG}	Storage Temperature	–55 to 125	°C
T_{BIAS}	Temperature Under Bias	–55 to 125	°C

Note:

Permanent damage to the device may occur if the Absolute Maximum Ratings are exceeded. Operation should be restricted to Recommended Operating Conditions. Exposure to conditions exceeding the Absolute Maximum Ratings, for an extended period of time, may affect reliability of this component.

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Power Supply Voltage Ranges

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
3.3 V Supply Voltage	V_{DD3}	3.0	3.3	3.6	V	
2.5 V Supply Voltage	V_{DD2}	2.3	2.5	2.7	V	
3.3 V V_{DDQ} I/O Supply Voltage	V_{DDQ3}	3.0	3.3	3.6	V	
2.5 V V_{DDQ} I/O Supply Voltage	V_{DDQ2}	2.4	2.5	2.7	V	

Notes:
1. The part numbers of Industrial Temperature Range versions end the character "I". Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.
2. Input Under/overshoot voltage must be –2 V > Vi < V_{DDn}+2 V not to exceed 4.6 V maximum, with a pulse width not to exceed 20% tKC.

V_{DDQ3} Range Logic Levels

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
V_{DD} Input High Voltage	V_{IH}	1.7	—	V_{DD} + 0.3	V	1
V_{DD} Input Low Voltage	V_{IL}	–0.3	—	0.8	V	1
V_{DDQ} I/O Input High Voltage	V_{IHQ}	1.7	—	V_{DDQ} + 0.3	V	1,3
V_{DDQ} I/O Input Low Voltage	V_{ILQ}	–0.3	—	0.8	V	1,3

Notes:
1. The part numbers of Industrial Temperature Range versions end the character "I". Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.
2. Input Under/overshoot voltage must be –2 V > Vi < V_{DDn}+2 V not to exceed 4.6 V maximum, with a pulse width not to exceed 20% tKC.
3. V_{IHQ} (max) is voltage on V_{DDQ} pins plus 0.3 V.

V_{DDQ2} Range Logic Levels

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
V_{DD} Input High Voltage	V_{IH}	0.6*V_{DD}	—	V_{DD} + 0.3	V	1
V_{DD} Input Low Voltage	V_{IL}	–0.3	—	0.3*V_{DD}	V	1
V_{DDQ} I/O Input High Voltage	V_{IHQ}	0.6*V_{DD}	—	V_{DDQ} + 0.3	V	1,3
V_{DDQ} I/O Input Low Voltage	V_{ILQ}	–0.3	—	0.3*V_{DD}	V	1,3

Notes:
1. The part numbers of Industrial Temperature Range versions end the character "I". Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.
2. Input Under/overshoot voltage must be –2 V > Vi < V_{DDn}+2 V not to exceed 4.6 V maximum, with a pulse width not to exceed 20% tKC.
3. V_{IHQ} (max) is voltage on V_{DDQ} pins plus 0.3 V.

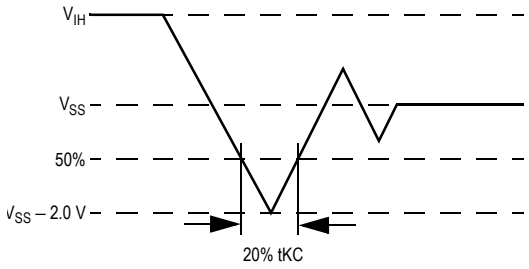
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Recommended Operating Temperatures

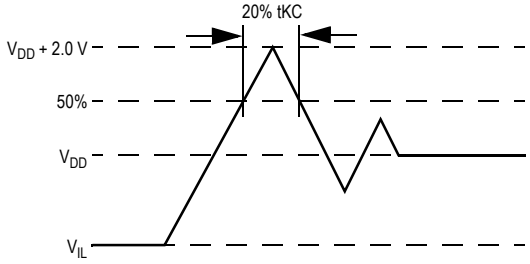
Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Ambient Temperature (Commercial Range Versions)	T_A	0	25	70	°C	2
Ambient Temperature (Industrial Range Versions)	T_A	–40	25	85	°C	2

Note:
1. The part numbers of Industrial Temperature Range versions end the character "I". Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.
2. Input Under/overshoot voltage must be –2 V > Vi < V_{DDn}+2 V not to exceed 4.6 V maximum, with a pulse width not to exceed 20% tKC.

Undershoot Measurement and Timing



Overshoot Measurement and Timing



Capacitance

(T_A = 25°C, f = 1 MHz, V_{DD} = 2.5 V)

Parameter	Symbol	Test conditions	Typ.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN} = 0 V	6.5	7.5	pF
Input/Output Capacitance (x36/x72)	$C_{I/O}$	V_{OUT} = 0 V	6	7	pF
Input/Output Capacitance (x18)	$C_{I/O}$	V_{OUT} = 0 V	8.5	9.5	pF

Note: These parameters are sample tested.

Package Thermal Characteristics

Rating	Layer Board	Symbol	Max	Unit	Notes
Junction to Ambient (at 200 lfm)	single	$R_{\Theta JA}$	40	°C/W	1,2
Junction to Ambient (at 200 lfm)	four	$R_{\Theta JA}$	24	°C/W	1,2
Junction to Case (TOP)	—	$R_{\Theta JC}$	9	°C/W	3

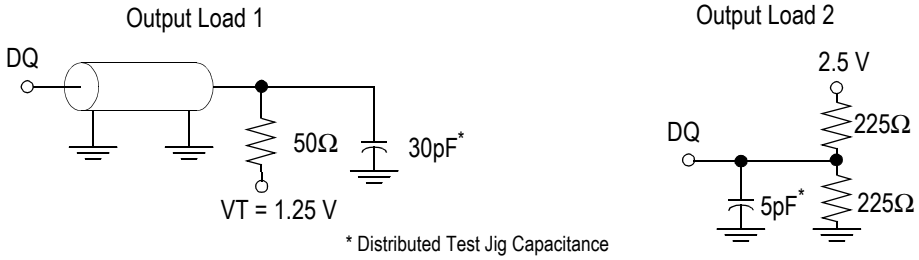
Notes:
1. Junction temperature is a function of SRAM power dissipation, package thermal resistance, mounting board temperature, ambient. Temperature air flow, board density, and PCB thermal resistance.
2. SCMI G-38-87
3. Average thermal resistance between die and top surface, MIL SPEC-883, Method 1012.1

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AC Test Conditions

Parameter	Conditions
Input high level	2.3 V
Input low level	0.2 V
Input slew rate	1 V/ns
Input reference level	1.25 V
Output reference level	1.25 V
Output load	**Fig. 1& 2**

Notes:
1. Include scope and jig capacitance.
2. Test conditions as specified with output loading as shown in **Fig. 1** unless otherwise noted.
3. Output Load 2 for t_{LZ}, t_{HZ}, t_{OLZ} and t_{OHZ}
4. Device is deselected as defined by the Truth Table.



DC Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Max
Input Leakage Current (except mode pins)	I_{IL}	V_{IN} = 0 to V_{DD}	–2 uA	2 uA
ZZ and $\overline{PE}$ Input Current	I_{IN1}	$V_{DD} \geq V_{IN} \geq V_{IH}$ 0 V ≤ $V_{IN} \leq V_{IH}$	–1 uA –1 uA	1 uA 100 uA
$\overline{FT}$, SCD, ZQ, DP Input Current	I_{IN2}	$V_{DD} \geq V_{IN} \geq V_{IL}$ 0 V ≤ $V_{IN} \leq V_{IL}$	–100 uA –1 uA	1 uA 1 uA
Output Leakage Current (x36/x72)	I_{OL}	Output Disable, V_{OUT} = 0 to V_{DD}	–1 uA	1 uA
Output Leakage Current (x18)	I_{OL}	Output Disable, V_{OUT} = 0 to V_{DD}	–2 uA	2 uA
Output High Voltage	V_{OH2}	I_{OH} = –8 mA, V_{DDQ} = 2.375 V	1.7 V	—
Output High Voltage	V_{OH3}	I_{OH} = –8 mA, V_{DDQ} = 3.135 V	2.4 V	—
Output Low Voltage	V_{OL}	I_{OL} = 8 mA	—	0.4 V

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Operating Currents

Parameter	Test Conditions	Mode		Symbol	-250		-225		-200		-166		-150		-133		Unit
					0 to 70°C	–40 to 85°C	0 to 70°C	–40 to 85°C	0 to 70°C	–40 to 85°C	0 to 70°C	–40 to 85°C	0 to 70°C	–40 to 85°C	0 to 70°C	–40 to 85°C	
Operating Current **3.3 V**	Device Selected; All other inputs ≥V_{IH} or ≤ V_{IL} Output open	**(x72)**	Pipeline	I_{DD} I_{DDQ}	580 80	560 80	530 70	550 70	480 60	500 60	410 50	430 50	380 50	400 50	340 40	360 40	mA
			Flow Through	I_{DD} I_{DDQ}	310 40	330 40	340 40	330 40	270 30	290 30	270 30	290 30	270 30	290 30	200 20	220 20	mA
		(x36)	Pipeline	I_{DD} I_{DDQ}	520 40	540 40	470 40	490 40	430 30	450 30	370 30	390 30	340 30	360 30	310 20	330 20	mA
			Flow Through	I_{DD} I_{DDQ}	280 20	300 20	280 20	300 20	250 20	270 20	350 20	270 20	250 20	270 20	180 20	200 20	mA
		(x18)	Pipeline	I_{DD} I_{DDQ}	345 20	360 20	315 20	330 20	290 15	305 15	250 15	265 15	230 15	245 15	205 10	220 10	mA
			Flow Through	I_{DD} I_{DDQ}	200 10	215 10	200 10	215 10	175 10	190 10	175 10	190 10	175 10	190 10	135 10	150 10	mA
Operating Current **2.5 V**	Device Selected; All other inputs ≥V_{IH} or ≤ V_{IL} Output open	**(x72)**	Pipeline	I_{DD} I_{DDQ}	580 60	600 60	530 60	550 60	480 50	500 50	410 40	430 40	380 40	400 40	340 30	360 30	mA
			Flow Through	I_{DD} I_{DDQ}	310 30	330 30	310 30	330 30	270 30	290 30	270 30	290 30	270 30	290 30	200 20	220 20	mA
		(x36)	Pipeline	I_{DD} I_{DDQ}	520 30	540 30	470 30	490 30	430 30	450 30	370 20	390 20	340 20	360 20	310 20	330 20	mA
			Flow Through	I_{DD} I_{DDQ}	280 20	300 20	280 20	300 20	250 20	270 20	250 20	270 20	250 20	270 20	180 10	200 10	mA
		(x18)	Pipeline	I_{DD} I_{DDQ}	345 15	360 15	315 15	330 15	290 15	305 15	250 10	265 10	230 10	245 10	205 10	220 10	mA
			Flow Through	I_{DD} I_{DDQ}	200 10	215 10	200 10	215 10	175 10	190 10	175 10	190 10	175 10	190 10	135 5	150 5	mA
Standby Current	ZZ ≥ V_{DD} – 0.2 V	—	Pipeline	I_{SB}	40	60	40	60	40	60	40	60	40	60	40	60	mA
			Flow Through	I_{SB}	40	60	40	60	40	60	40	60	40	60	40	60	mA
Deselect Current	Device Deselected; All other inputs ≥ V_{IH} or ≤ V_{IL}	—	Pipeline	I_{DD}	170	180	160	170	150	160	130	140	120	130	100	110	mA
			Flow Through	I_{DD}	120	130	120	130	100	110	100	110	100	110	90	100	mA

Notes:
1. I_{DD} and I_{DDQ} apply to any combination of V_{DD3}, V_{DD2}, V_{DDQ3}, and V_{DDQ2} operation.
2. All parameters listed are worst case scenario.

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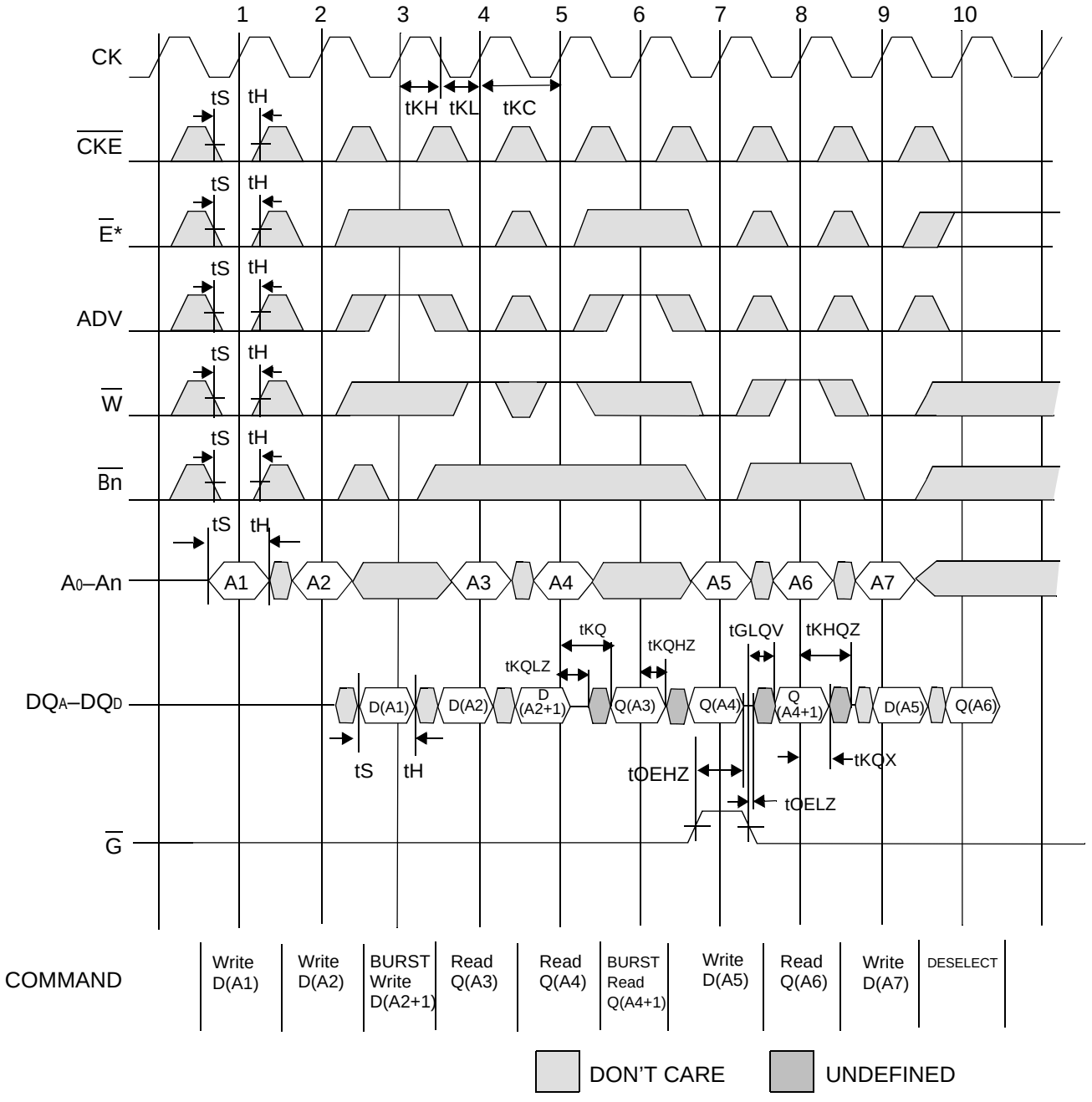
AC Electrical Characteristics

	Parameter	Symbol	-250		-225		-200		-166		-150		-133		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Pipeline	Clock Cycle Time	tKC	4.0	—	4.4	—	5.0	—	6.0	—	6.7	—	7.5	—	ns
	Clock to Output Valid	tKQ	—	2.3	—	2.5	—	3.0	—	3.4	—	3.8	—	4.0	ns
	Clock to Output Invalid	tKQX	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
	Clock to Output in Low-Z	tLZ[1]	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
Flow Through	Clock Cycle Time	tKC	7.0	—	7.5	—	8.5	—	10.0	—	10.0	—	15.0	—	ns
	Clock to Output Valid	tKQ	—	6.0	—	6.0	—	7.5	—	8.5	—	10.0	—	10.0	ns
	Clock to Output Invalid	tKQX	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns
	Clock to Output in Low-Z	tLZ[1]	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns
	Clock HIGH Time	tKH	1.3	—	1.3	—	1.3	—	1.3	—	1.5	—	1.7	—	ns
	Clock LOW Time	tKL	1.5	—	1.5	—	1.5	—	1.5	—	1.7	—	2	—	ns
	Clock to Output in High-Z	tHZ[1]	1.5	2.3	1.5	2.5	1.5	3.0	1.5	3.5	1.5	3.8	1.5	4.0	ns
	$\overline{G}$ to Output Valid	tOE	—	2.3	—	2.5	—	3.2	—	3.5	—	3.8	—	4.0	ns
	$\overline{G}$ to output in Low-Z	tOLZ[1]	0	—	0	—	0	—	0	—	0	—	0	—	ns
	$\overline{G}$ to output in High-Z	tOHZ[1]	—	2.3	—	2.5	—	3.0	—	3.5	—	3.8	—	4.0	ns
	Setup time	tS	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
	Hold time	tH	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	ns
	ZZ setup time	tZZS[2]	5	—	5	—	5	—	5	—	5	—	5	—	ns
	ZZ hold time	tZZH[2]	1	—	1	—	1	—	1	—	1	—	1	—	ns
	ZZ recovery	tZZR	100	—	100	—	100	—	100	—	100	—	100	—	ns

Notes:
1. These parameters are sampled and are not 100% tested.
2. ZZ is an asynchronous signal. However, in order to be recognized on any given clock cycle, ZZ must meet the specified setup and hold times as specified above.

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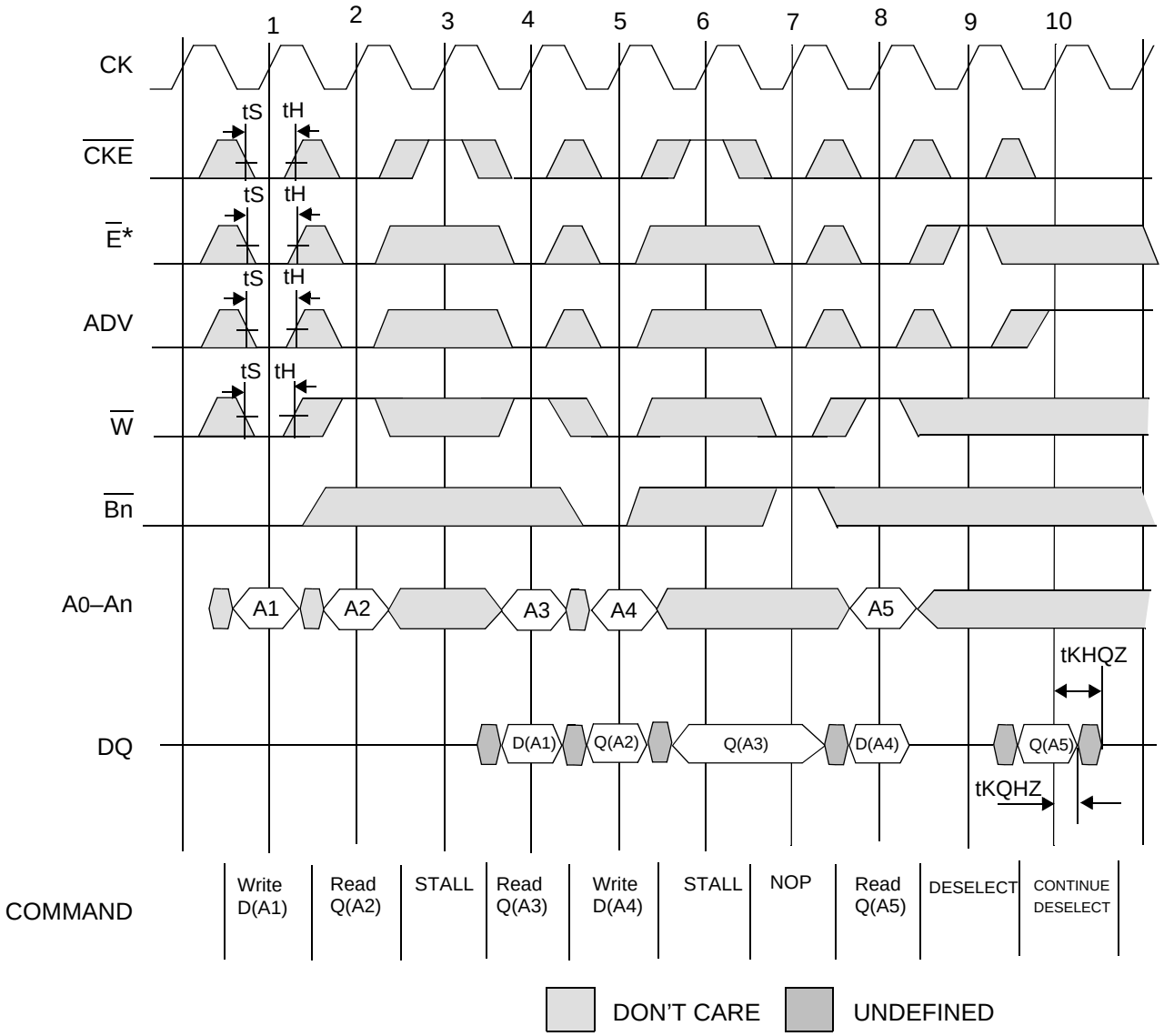
Pipeline Mode Read/Write Cycle Timing



*Note: $\overline{E}$ = High (False) if $\overline{E}_1$ = 1 or E_2 = 0 or $\overline{E}_3$ = 1

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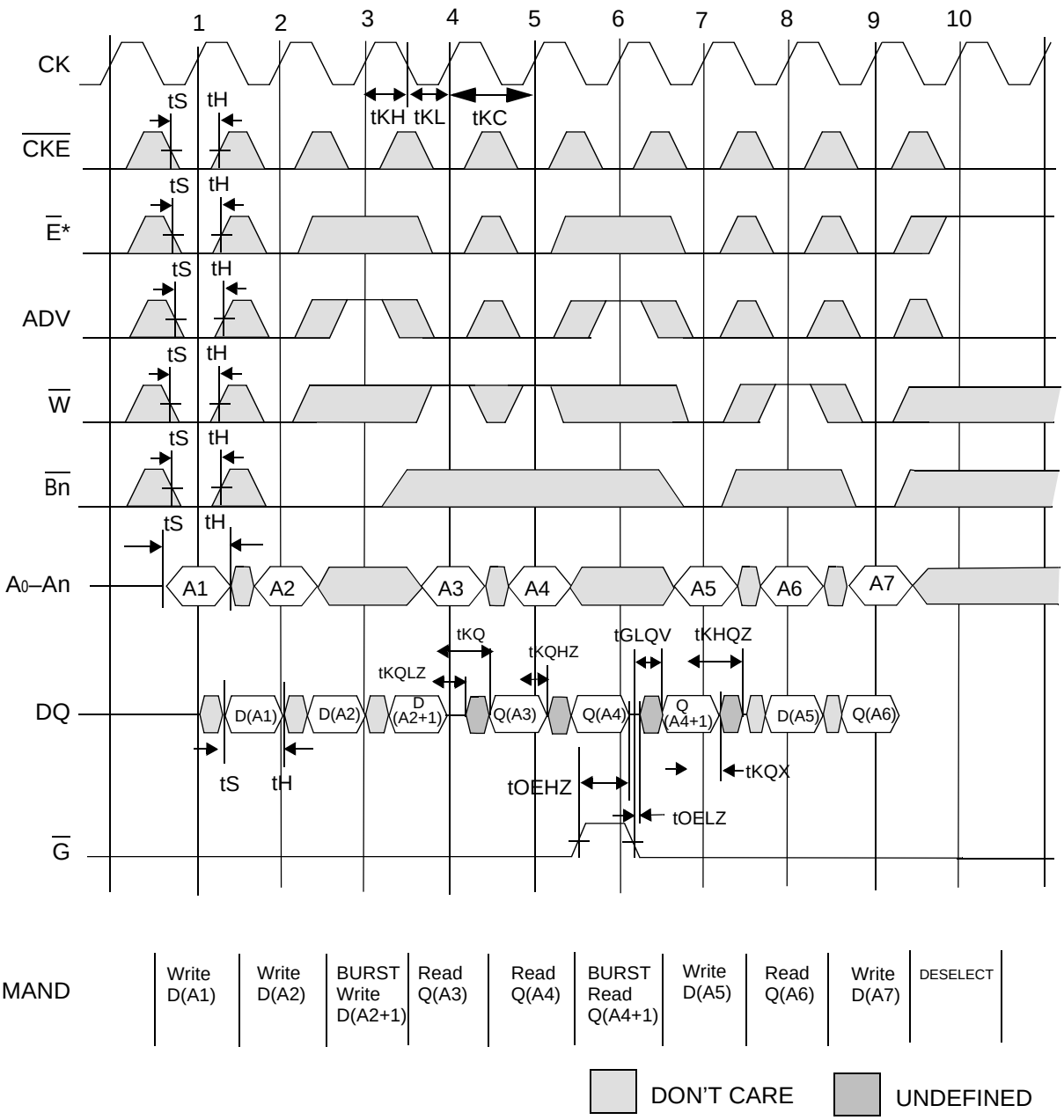
Pipeline Mode No-Op, Stall and Deselect Timing



*Note: $\overline{E}$ = High (False) if $\overline{E}_1$ = 1 or E_2 = 0 or $\overline{E}_3$ = 1

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Flow Through Mode Read/Write Cycle Timing



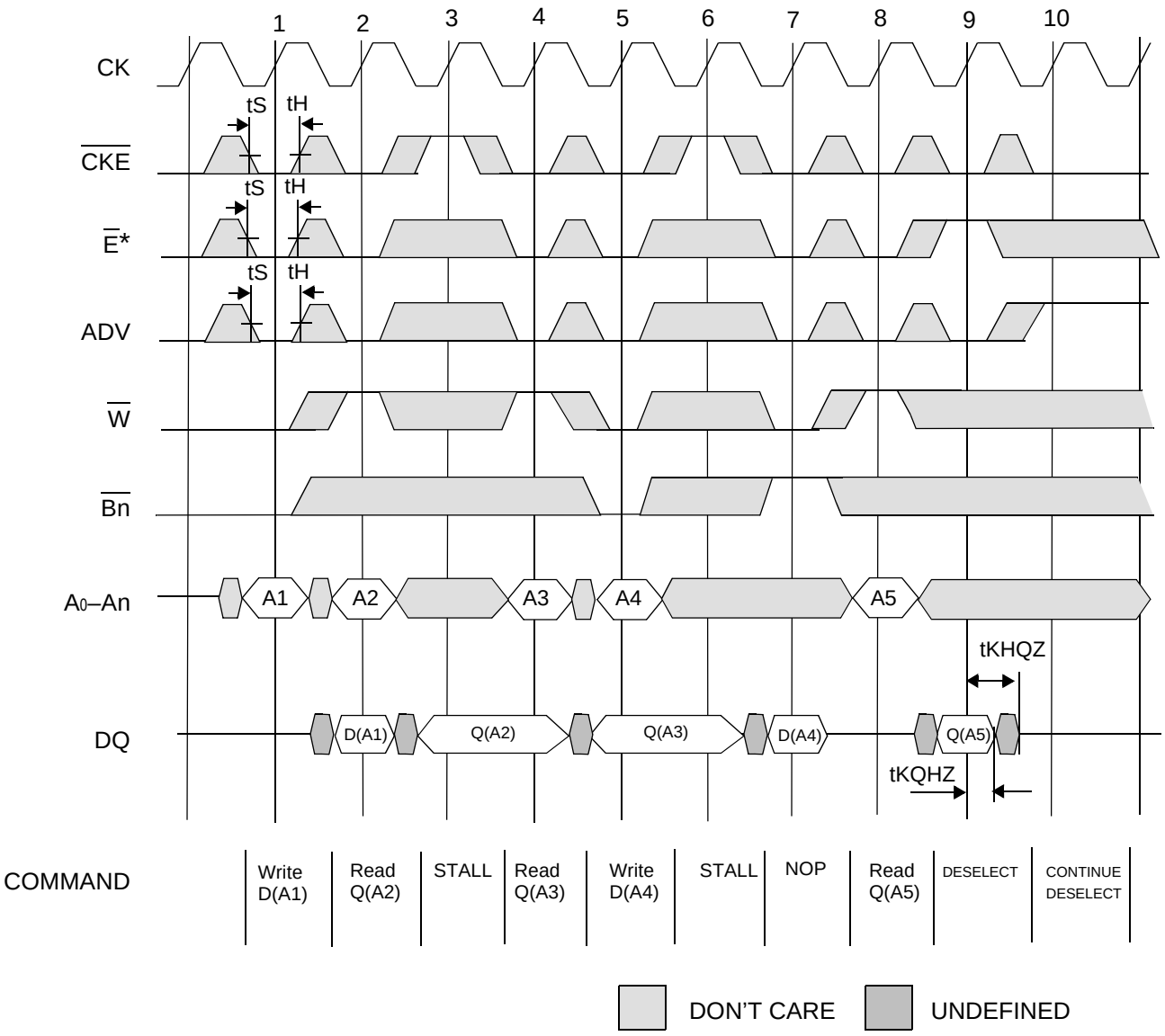
COMMAND	Write D(A1)	Write D(A2)	BURST Write D(A2+1)	Read Q(A3)	Read Q(A4)	BURST Read Q(A4+1)	Write D(A5)	Read Q(A6)	Write D(A7)	DESELECT

DON'T CARE UNDEFINED

*Note: $\overline{E}$ = High (False) if $\overline{E}_1$ = 1 or E_2 = 0 or $\overline{E}_3$ = 1

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Flow Through Mode No-Op, Stall and Deselect Timing



*Note: $\overline{E}$ = High (False) if $\overline{E}_1$ = 1 or E_2 = 0 or $\overline{E}_3$ = 1

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JTAG Port Operation

Due to the fact that this device is built from two die, the two JTAG parts are chained together internally. The following describes the behavior of each die.

Overview

The JTAG Port on this RAM operates in a manner that is compliant with IEEE Standard 1149.1-1990, a serial boundary scan interface standard (commonly referred to as JTAG). The JTAG Port input interface levels scale with V_{DD}. The JTAG output drivers are powered by V_{DDQ}.

Disabling the JTAG Port

It is possible to use this device without utilizing the JTAG port. The port is reset at power-up and will remain inactive unless clocked. TCK, TDI, and TMS are designed with internal pull-up circuits.To assure normal operation of the RAM with the JTAG Port unused, TCK, TDI, and TMS may be left floating or tied to either V_{DD} or V_{SS}. TDO should be left unconnected.

JTAG Pin Descriptions

Pin	Pin Name	I/O	Description
TCK	Test Clock	In	Clocks all TAP events. All inputs are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.
TMS	Test Mode Select	In	The TMS input is sampled on the rising edge of TCK. This is the command input for the TAP controller state machine. An undriven TMS input will produce the same result as a logic one input level.
TDI	Test Data In	In	The TDI input is sampled on the rising edge of TCK. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP Controller state machine and the instruction that is currently loaded in the TAP Instruction Register (refer to the TAP Controller State Diagram). An undriven TDI pin will produce the same result as a logic one input level.
TDO	Test Data Out	Out	Output that is active depending on the state of the TAP state machine. Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO.

Note:
This device does not have a TRST (TAP Reset) pin. TRST is optional in IEEE 1149.1. The Test-Logic-Reset state is entered while TMS is held high for five rising edges of TCK. The TAP Controller is also reset automaticly at power-up.

JTAG Port Registers

Overview

The various JTAG registers, refered to as Test Access Port orTAP Registers, are selected (one at a time) via the sequences of 1s and 0s applied to TMS as TCK is strobed. Each of the TAP Registers is a serial shift register that captures serial input data on the rising edge of TCK and pushes serial data out on the next falling edge of TCK. When a register is selected, it is placed between the TDI and TDO pins.

Instruction Register

The Instruction Register holds the instructions that are executed by the TAP controller when it is moved into the Run, Test/Idle, or the various data register states. Instructions are 3 bits long. The Instruction Register can be loaded when it is placed between the TDI and TDO pins. The Instruction Register is automatically preloaded with the IDCODE instruction at power-up or whenever the controller is placed in Test-Logic-Reset state.

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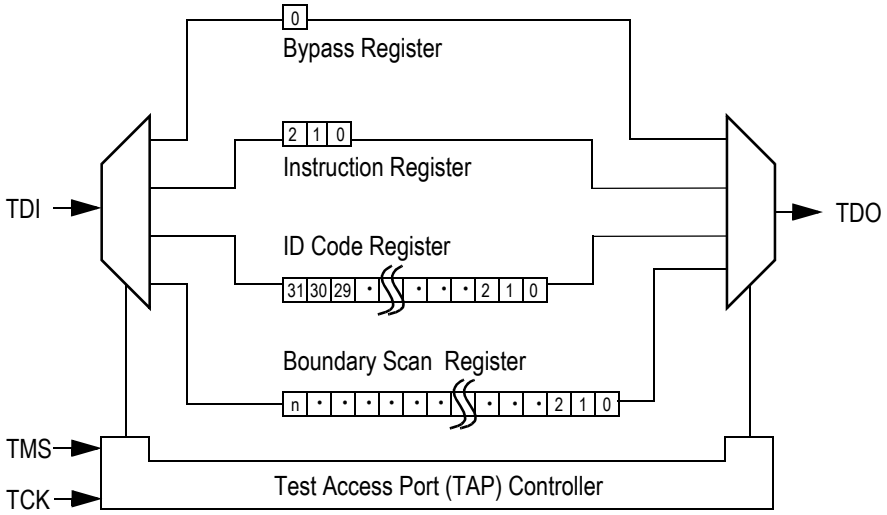
Bypass Register

The Bypass Register is a single bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the RAM's JTAG Port to another device in the scan chain with as little delay as possible.

Boundary Scan Register

The Boundary Scan Register is a collection of flip flops that can be preset by the logic level found on the RAM's input or I/O pins. The flip flops are then daisy chained together so the levels found can be shifted serially out of the JTAG Port's TDO pin. The Boundary Scan Register also includes a number of place holder flip flops (always set to a logic 1). The relationship between the device pins and the bits in the Boundary Scan Register is described in the Scan Order Table following. The Boundary Scan Register, under the control of the TAP Controller, is loaded with the contents of the RAMs I/O ring when the controller is in Capture-DR state and then is placed between the TDI and TDO pins when the controller is moved to Shift-DR state. SAMPLE-Z, SAMPLE/PRELOAD and EXTEST instructions can be used to activate the Boundary Scan Register.

JTAG TAP Block Diagram



Identification (ID) Register

The ID Register is a 32-bit register that is loaded with a device and vendor specific 32-bit code when the controller is put in Capture-DR state with the IDCODE command loaded in the Instruction Register. The code is loaded from a 32-bit on-chip ROM. It describes various attributes of the RAM as indicated below. The register is then placed between the TDI and TDO pins when the controller is moved into Shift-DR state. Bit 0 in the register is the LSB and the first to reach TDO when shifting begins.

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ID Register Contents

	Die Revision Code				Not Used												I/O Configuration				GSI Technology JEDEC Vendor ID Code											Presence Register
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x72	X	X	X	X	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	1	1	0	1	1	0	0	1	1
x36	X	X	X	X	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1	0	1	1	0	0	1	1
x32	X	X	X	X	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	1	1	0	1	1	0	0	1	1
x18	X	X	X	X	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	1	1	0	1	1	0	0	1	1
x16	X	X	X	X	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	1	1	0	1	1	0	0	1	1

Tap Controller Instruction Set

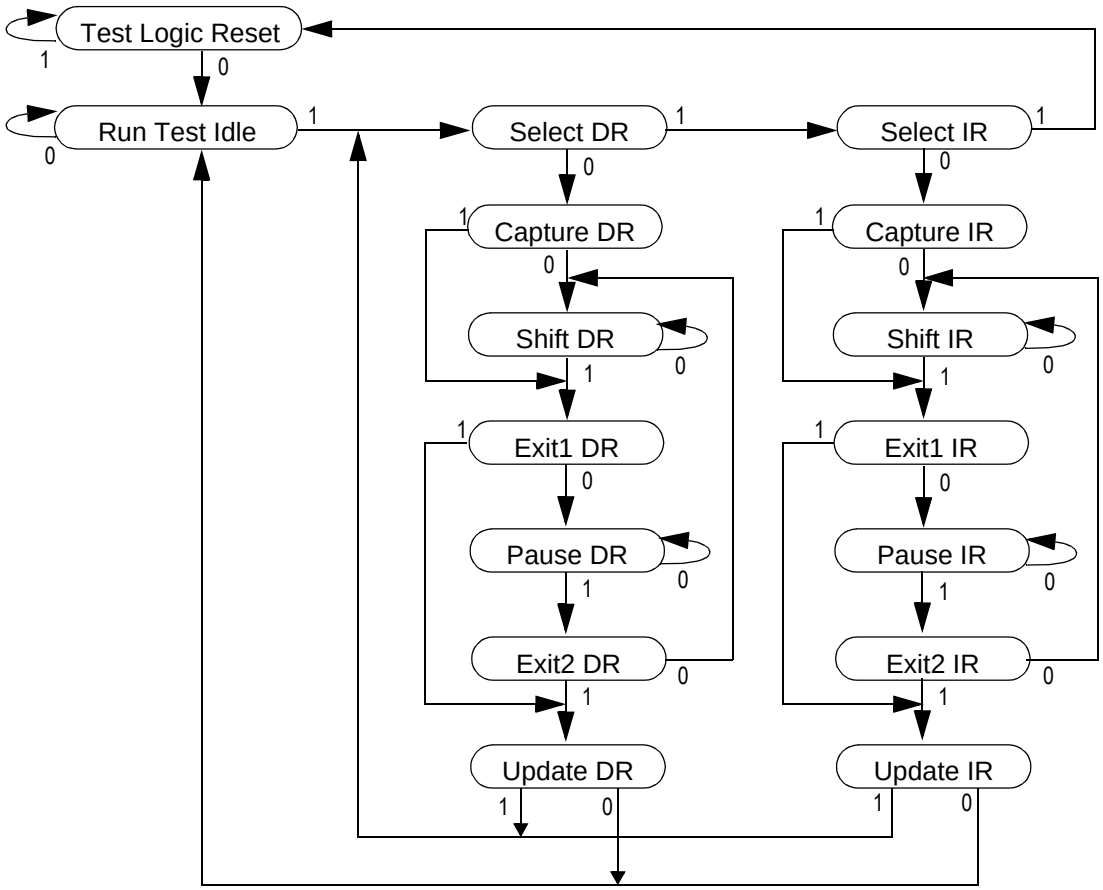
Overview

There are two classes of instructions defined in the Standard 1149.1-1990; the standard (Public) instructions, and device specific (Private) instructions. Some Public instructions are mandatory for 1149.1 compliance. Optional Public instructions must be implemented in prescribed ways. The TAP on this device may be used to monitor all input and I/O pads, and can be used to load address, data or control signals into the RAM or to preload the I/O buffers.

When the TAP controller is placed in Capture-IR state the two least significant bits of the instruction register are loaded with 01. When the controller is moved to the Shift-IR state the Instruction Register is placed between TDI and TDO. In this state the desired instruction is serially loaded through the TDI input (while the previous contents are shifted out at TDO). For all instructions, the TAP executes newly loaded instructions only when the controller is moved to Update-IR state. The TAP instruction set for this device is listed in the following table.

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JTAG Tap Controller State Diagram



Instruction Descriptions

BYPASS

When the BYPASS instruction is loaded in the Instruction Register the Bypass Register is placed between TDI and TDO. This occurs when the TAP controller is moved to the Shift-DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a Standard 1149.1 mandatory public instruction. When the SAMPLE / PRELOAD instruction is loaded in the Instruction Register, moving the TAP controller into the Capture-DR state loads the data in the RAMs input and I/O buffers into the Boundary Scan Register. Boundary Scan Register locations are not associated with an input or I/O pin, and are loaded with the default state identified in the Boundary Scan Chain table at the end of this section of the datasheet. Because the RAM clock is independent from the TAP Clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e. in a metastable state). Although allowing the TAP to sample metastable inputs will not harm the device, repeatable results cannot be expected. RAM input signals must be stabilized for long enough to meet the TAPs input data capture set-up plus hold time (tTS plus tTH). The RAMs clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the Boundary Scan Register. Moving the controller to Shift-DR state then places the boundary scan register between the TDI and TDO pins.

EXTEST

EXTEST is an IEEE 1149.1 mandatory public instruction. It is to be executed whenever the instruction register is loaded with all logic 0s.

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The EXTEST command does not block or override the RAM's input pins; therefore, the RAM's internal state is still determined by its input pins.

Typically, the Boundary Scan Register is loaded with the desired pattern of data with the SAMPLE/PRELOAD command. Then the EXTEST command is used to output the Boundary Scan Register's contents, in parallel, on the RAM's data output drivers on the falling edge of TCK when the controller is in the Update-IR state.

Alternately, the Boundary Scan Register may be loaded in parallel using the EXTEST command. When the EXTEST instruction is selected, the sate of all the RAM's input and I/O pins, as well as the default values at Scan Register locations not associated with a pin, are transferred in parallel into the Boundary Scan Register on the rising edge of TCK in the Capture-DR state, the RAM's output pins drive out the value of the Boundary Scan Register location with which each output pin is associated.

IDCODE

The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in Capture-DR mode and places the ID register between the TDI and TDO pins in Shift-DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the Test-Logic-Reset state.

SAMPLE-Z

If the SAMPLE-Z instruction is loaded in the instruction register, all RAM outputs are forced to an inactive drive state (high-Z) and the Boundary Scan Register is connected between TDI and TDO when the TAP controller is moved to the Shift-DR state.

RFU

These instructions are Reserved for Future Use. In this device they replicate the BYPASS instruction.

JTAG TAP Instruction Set Summary

Instruction	Code	Description	Notes
EXTEST	000	Places the Boundary Scan Register between TDI and TDO.	1
IDCODE	001	Preloads ID Register and places it between TDI and TDO.	1, 2
SAMPLE-Z	010	Captures I/O ring contents. Places the Boundary Scan Register between TDI and TDO. Forces all RAM output drivers to High-Z.	1
RFU	011	Do not use this instruction; Reserved for Future Use. Replicates BYPASS instruction. Places Bypass Register between TDI and TDO.	1
SAMPLE/ PRELOAD	100	Captures I/O ring contents. Places the Boundary Scan Register between TDI and TDO.	1
GSI	101	GSI private instruction.	1
RFU	110	Do not use this instruction; Reserved for Future Use. Replicates BYPASS instruction. Places Bypass Register between TDI and TDO.	1
BYPASS	111	Places Bypass Register between TDI and TDO.	1

Notes:
1. Instruction codes expressed in binary, MSB on left, LSB on right.
2. Default instruction automatically loaded at power-up and in test-logic-reset state.

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JTAG Port Recommended Operating Conditions and DC Characteristics

Parameter	Symbol	Min.	Max.	Unit	Notes
3.3 V Test Port Input High Voltage	V_{IHJ3}	2.0	V_{DD3} +0.3	V	1
3.3 V Test Port Input Low Voltage	V_{ILJ3}	–0.3	0.8	V	1
2.5 V Test Port Input High Voltage	V_{IHJ2}	0.6 * V_{DD2}	V_{DD2} +0.3	V	1
2.5 V Test Port Input Low Voltage	V_{ILJ2}	–0.3	0.3 * V_{DD2}	V	1
TMS, TCK and TDI Input Leakage Current	I_{INHJ}	–300	1	uA	2
TMS, TCK and TDI Input Leakage Current	I_{INLJ}	–1	100	uA	3
TDO Output Leakage Current	I_{OLJ}	–1	1	uA	4
Test Port Output High Voltage	V_{OHJ}	1.7	—	V	5, 6
Test Port Output Low Voltage	V_{OLJ}	—	0.4	V	5, 7
Test Port Output CMOS High	V_{OHJC}	V_{DDQ} – 100 mV	—	V	5, 8
Test Port Output CMOS Low	V_{OLJC}	—	100 mV	V	5, 9

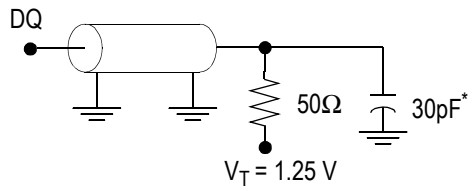
Notes:
1. Input Under/overshoot voltage must be –2 V > Vi < V_{DDn} +2 V not to exceed 4.6 V maximum, with a pulse width not to exceed 20% tTKC.
2. $V_{ILJ} \leq V_{IN} \leq V_{DDn}$
3. $0\ V \leq V_{IN} \leq V_{ILJn}$
4. Output Disable, V_{OUT} = 0 to V_{DDn}
5. The TDO output driver is served by the V_{DDQ} supply.
6. I_{OHJ} = –4 mA
7. I_{OLJ} = + 4 mA
8. I_{OHJC} = –100 uA
9. I_{OHJC} = +100 uA

JTAG Port AC Test Conditions

Parameter	Conditions
Input high level	2.3 V
Input low level	0.2 V
Input slew rate	1 V/ns
Input reference level	1.25 V
Output reference level	1.25 V

Notes:
1. Include scope and jig capacitance.
2. Test conditions as as shown unless otherwise noted.

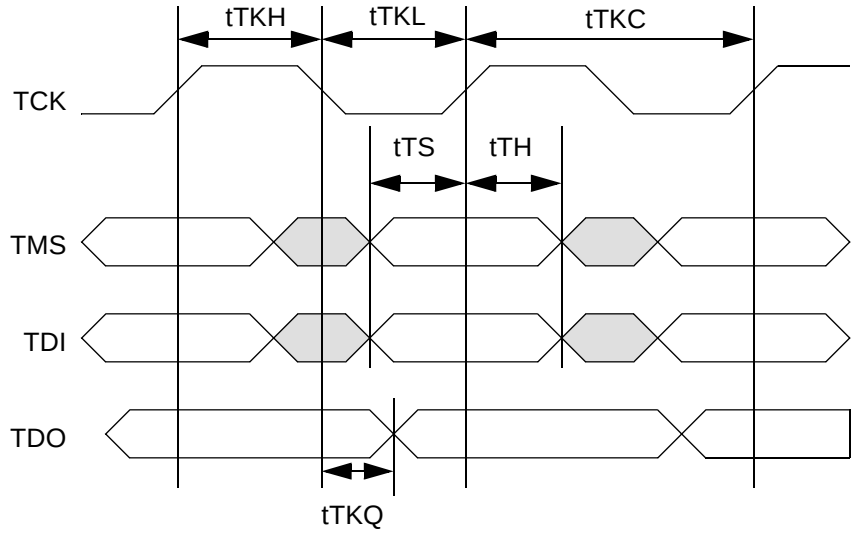
JTAG Port AC Test Load



* Distributed Test Jig Capacitance

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JTAG Port Timing Diagram



JTAG Port AC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
TCK Cycle Time	tTKC	50	—	ns
TCK Low to TDO Valid	tTKQ	—	20	ns
TCK High Pulse Width	tTKH	20	—	ns
TCK Low Pulse Width	tTKL	20	—	ns
TDI & TMS Set Up Time	tTS	10	—	ns
TDI & TMS Hold Time	tTH	10	—	ns

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GS8324Z18/36/72 Boundary Scan Chain Order

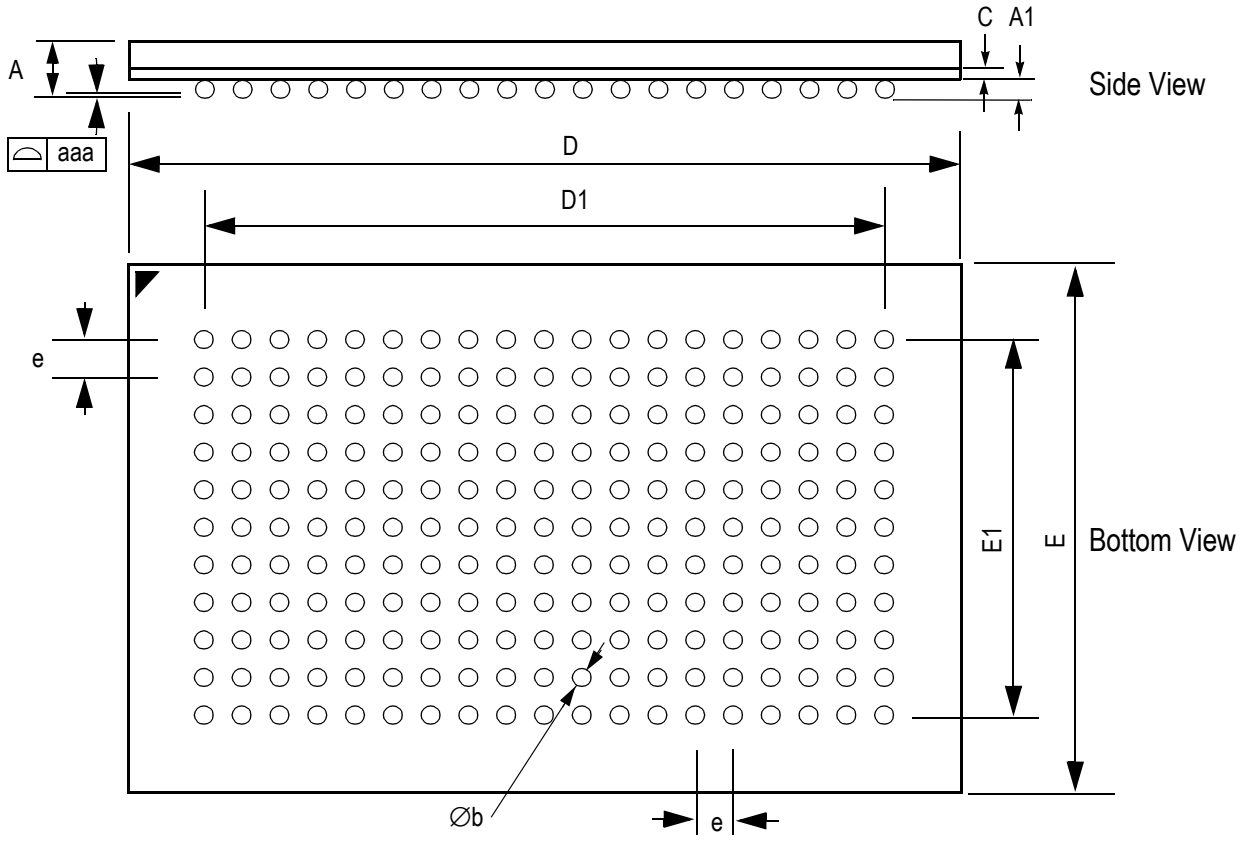
Order	x72	x36	x18	Bump		
				x72	x36	x18
1(TBD)						

Notes:
1. Depending on the package, some input pads of the scan chain may not be connected to any external pin. In such case: $\overline{LBO}$ = 1, ZQ = 1, PE = 0, $\overline{SD}$ = 0, ZZ = 0, $\overline{FT}$ = 1, DP = 1, and SCD = 1.
2. Every DQ pad consists of two scan registers—D is for input capture, and Q is for output capture.
3. A single register (#194) for controlling tristate of all the DQ pins is at the end of the scan chain (i.e., the last bit shifted in this tristate control is effective after JTAG EXTEST instruction is executed.
4. 1 = no connect, internally set to logic value 1
5. 0 = no connect, internally set to logic value 0
6. X = no connect, value is undefined

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209 BGA Package Drawing

14 mm x 22 mm Body, 1.0 mm Bump Pitch, 11 x 19 Bump Array



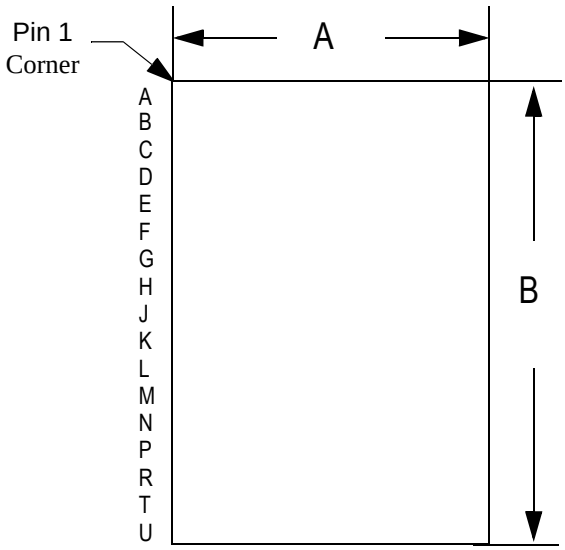
Symbol	Min	Typ	Max	Units
A			1.70	mm
A1	0.40	0.50	0.60	mm
Øb	0.50	0.60	0.70	mm
c	0.31	0.36	0.38	mm
D	21.9	22.0	22.1	mm
D1		18.0 (BSC)		mm
E	13.9	14.0	14.1	mm
E1		10.0 (BSC)		mm
e		1.00 (BSC)		mm
aaa		0.15		mm

Rev 1.0

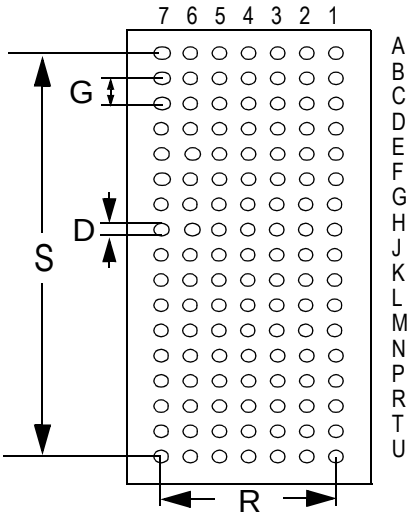
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Package Dimensions—119-Pin PBGA

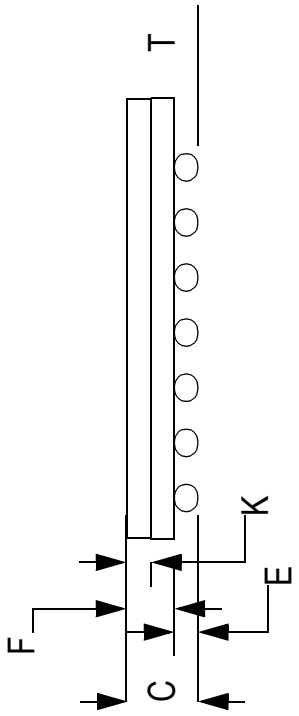
119-Bump BGA Package



Top View



Bottom View



Side View

Package Dimensions—119-Pin PBGA

Symbol	Description	Min.	Nom.	Max
A	Width	13.9	14.0	14.1
B	Length	21.9	22.0	22.1
C	Package Height (including ball)	1.73	1.86	1.99
D	Ball Size	0.60	0.75	0.90
E	Ball Height	0.50	0.60	0.70
F	Package Height (excluding balls)	1.16	1.26	1.36
G	Width between Balls		1.27	
K	Package Height above board	0.65	0.70	0.75
R	Width of package between balls		7.62	
S	Length of package between balls		20.32	
T	Variance of Ball Height		0.15	

Unit: mm

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Ordering Information for GSI Synchronous NBT SRAMs

Org	Part Number[1]	Type	Package	Speed[2] (MHz/ns)	T_A[3]
2M x 18	GS8324Z18B-250	Pipeline/Flow Through	119 BGA	250/6	C
2M x 18	GS8324Z18B-225	Pipeline/Flow Through	119 BGA	225/6.5	C
2M x 18	GS8324Z18B-200	Pipeline/Flow Through	119 BGA	200/7.5	C
2M x 18	GS8324Z18B-166	Pipeline/Flow Through	119 BGA	166/8.5	C
2M x 18	GS8324Z18B-150	Pipeline/Flow Through	119 BGA	150/10	C
2M x 18	GS8324Z18B-133	Pipeline/Flow Through	119 BGA	133/11	C
2M x 18	GS8324Z18C-250	Pipeline/Flow Through	209 BGA	250/6	C
2M x 18	GS8324Z18C-225	Pipeline/Flow Through	209 BGA	225/6.5	C
2M x 18	GS8324Z18C-200	Pipeline/Flow Through	209 BGA	200/7.5	C
2M x 18	GS8324Z18C-166	Pipeline/Flow Through	209 BGA	166/8.5	C
2M x 18	GS8324Z18C-150	Pipeline/Flow Through	209 BGA	150/10	C
2M x 18	GS8324Z18C-133	Pipeline/Flow Through	209 BGA	133/11	C
1M x 36	GS8324Z36B-250	Pipeline/Flow Through	119 BGA	250/6	C
1M x 36	GS8324Z36B-225	Pipeline/Flow Through	119 BGA	225/6.5	C
1M x 36	GS8324Z36B-200	Pipeline/Flow Through	119 BGA	200/7.5	C
1M x 36	GS8324Z36B-166	Pipeline/Flow Through	119 BGA	166/8.5	C
1M x 36	GS8324Z36B-150	Pipeline/Flow Through	119 BGA	150/10	C
1M x 36	GS8324Z36B-133	Pipeline/Flow Through	119 BGA	133/11	C
1M x 36	GS8324Z36C-250	Pipeline/Flow Through	209 BGA	250/6	C
1M x 36	GS8324Z36C-225	Pipeline/Flow Through	209 BGA	225/6.5	C
1M x 36	GS8324Z36C-200	Pipeline/Flow Through	209 BGA	200/7.5	C
1M x 36	GS8324Z36C-166	Pipeline/Flow Through	209 BGA	166/8.5	C
1M x 36	GS8324Z36C-150	Pipeline/Flow Through	209 BGA	150/10	C
1M x 36	GS8324Z36C-133	Pipeline/Flow Through	209 BGA	133/11	C
512K x 72	GS8324Z72C-250	Pipeline/Flow Through	209 BGA	250/6	C
512K x 72	GS8324Z72C-225	Pipeline/Flow Through	209 BGA	225/6.5	C
512K x 72	GS8324Z72C-200	Pipeline/Flow Through	209 BGA	200/7.5	C
512K x 72	GS8324Z72C-166	Pipeline/Flow Through	209 BGA	166/8.5	C
512K x 72	GS8324Z72C-150	Pipeline/Flow Through	209 BGA	150/10	C

Notes:

1. Customers requiring delivery in Tape and Reel should add the character "T" to the end of the part number. Example: GS8324Z18B-150IB.
2. The speed column indicates the cycle frequency (MHz) of the device in Pipeline mode and the latency (ns) in Flow Through mode. Each device is Pipeline/Flow Through mode-selectable by the user.
3. T_A = C = Commercial Temperature Range. T_A = I = Industrial Temperature Range.
4. GSI offers other versions this type of device in many different configurations and with a variety of different features, only some of which are covered in this data sheet. See the GSI Technology web site (www.gsitechnology.com) for a complete listing of current offerings.

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Ordering Information for GSI Synchronous NBT SRAMs (Continued)

Org	Part Number[1]	Type	Package	Speed[2] (MHz/ns)	T_A[3]
512K x 72	GS8324Z72C-133	Pipeline/Flow Through	209 BGA	133/11	C
2M x 18	GS8324Z18B-250I	Pipeline/Flow Through	119 BGA	250/6	I
2M x 18	GS8324Z18B-225I	Pipeline/Flow Through	119 BGA	225/6.5	I
2M x 18	GS8324Z18B-200I	Pipeline/Flow Through	119 BGA	200/7.5	I
2M x 18	GS8324Z18B-166I	Pipeline/Flow Through	119 BGA	166/8.5	I
2M x 18	GS8324Z18B-150I	Pipeline/Flow Through	119 BGA	150/10	I
2M x 18	GS8324Z18B-133I	Pipeline/Flow Through	119 BGA	133/11	I
2M x 18	GS8324Z18C-250I	Pipeline/Flow Through	209 BGA	250/6	I
2M x 18	GS8324Z18C-225I	Pipeline/Flow Through	209 BGA	225/6.5	I
2M x 18	GS8324Z18C-200I	Pipeline/Flow Through	209 BGA	200/7.5	I
2M x 18	GS8324Z18C-166I	Pipeline/Flow Through	209 BGA	166/8.5	I
2M x 18	GS8324Z18C-150I	Pipeline/Flow Through	209 BGA	150/10	I
2M x 18	GS8324Z18C-133I	Pipeline/Flow Through	209 BGA	133/11	I
1M x 36	GS8324Z36B-250I	Pipeline/Flow Through	119 BGA	250/6	I
1M x 36	GS8324Z36B-225I	Pipeline/Flow Through	119 BGA	225/6.5	I
1M x 36	GS8324Z36B-200I	Pipeline/Flow Through	119 BGA	200/7.5	I
1M x 36	GS8324Z36B-166I	Pipeline/Flow Through	119 BGA	166/8.5	I
1M x 36	GS8324Z36B-150I	Pipeline/Flow Through	119 BGA	150/10	I
1M x 36	GS8324Z36B-133I	Pipeline/Flow Through	119 BGA	133/11	I
1M x 36	GS8324Z36C-250I	Pipeline/Flow Through	209 BGA	250/6	I
1M x 36	GS8324Z36C-225I	Pipeline/Flow Through	209 BGA	225/6.5	I
1M x 36	GS8324Z36C-200I	Pipeline/Flow Through	209 BGA	200/7.5	I
1M x 36	GS8324Z36C-166I	Pipeline/Flow Through	209 BGA	166/8.5	I
1M x 36	GS8324Z36C-150I	Pipeline/Flow Through	209 BGA	150/10	I
1M x 36	GS8324Z36C-133I	Pipeline/Flow Through	209 BGA	133/11	I
512K x 72	GS8324Z72C-250I	Pipeline/Flow Through	209 BGA	250/6	I

Notes:
1. Customers requiring delivery in Tape and Reel should add the character "T" to the end of the part number. Example: GS8324Z18B-150IB.
2. The speed column indicates the cycle frequency (MHz) of the device in Pipeline mode and the latency (ns) in Flow Through mode. Each device is Pipeline/Flow Through mode-selectable by the user.
3. T_A = C = Commercial Temperature Range. T_A = I = Industrial Temperature Range.
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Ordering Information for GSI Synchronous NBT SRAMs (Continued)

Org	Part Number[1]	Type	Package	Speed[2] (MHz/ns)	T_A[3]
512K x 72	GS8324Z72C-225I	Pipeline/Flow Through	209 BGA	225/6.5	I
512K x 72	GS8324Z72C-200I	Pipeline/Flow Through	209 BGA	200/7.5	I
512K x 72	GS8324Z72C-166I	Pipeline/Flow Through	209 BGA	166/8.5	I
512K x 72	GS8324Z72C-150I	Pipeline/Flow Through	209 BGA	150/10	I
512K x 72	GS8324Z72C-133I	Pipeline/Flow Through	209 BGA	133/11	I

Notes:
1. Customers requiring delivery in Tape and Reel should add the character "T" to the end of the part number. Example: GS8324Z18B-150IB.
2. The speed column indicates the cycle frequency (MHz) of the device in Pipeline mode and the latency (ns) in Flow Through mode. Each device is Pipeline/Flow Through mode-selectable by the user.
3. T_A = C = Commercial Temperature Range. T_A = I = Industrial Temperature Range.
4. GSI offers other versions this type of device in many different configurations and with a variety of different features, only some of which are covered in this data sheet. See the GSI Technology web site (www.gsitechnology.com) for a complete listing of current offerings.

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36Mb Sync SRAM Datasheet Revision History

DS/DateRev. Code: Old; New	Types of Changes Format or Content	Page;Revisions;Reason
8324Z18_r1		• Creation of new datasheet

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- *Специальные условия для постоянных клиентов.*
- *Подбор аналогов.*
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- *Приемлемые сроки поставки, возможна ускоренная поставка.*
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- *Тестирование поставляемой продукции.*
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