Application Notes for AP3770 System Solution

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1. Introduction

The AP3770 uses Pulse Frequency Modulation (PFM) method to realize Discontinuous Conduction Mode (DCM) operation for FLYBACK power supplies. The principle of PFM is different with that of Pulse Width Modulation (PWM), so the design of transformer is also different.

The AP3770 can provide accurate constant voltage, constant current (CV/CC) regulation by using Primary Side Regulation (PSR). AP3770 has the special technique to suppress the audio noise, internal line compensation to reduce the number of system components, fixed cable compensation to compensate the voltage drop on different output cable for achieving good CV regulation.

The AP3770 can achieve low standby power less than 30mW.

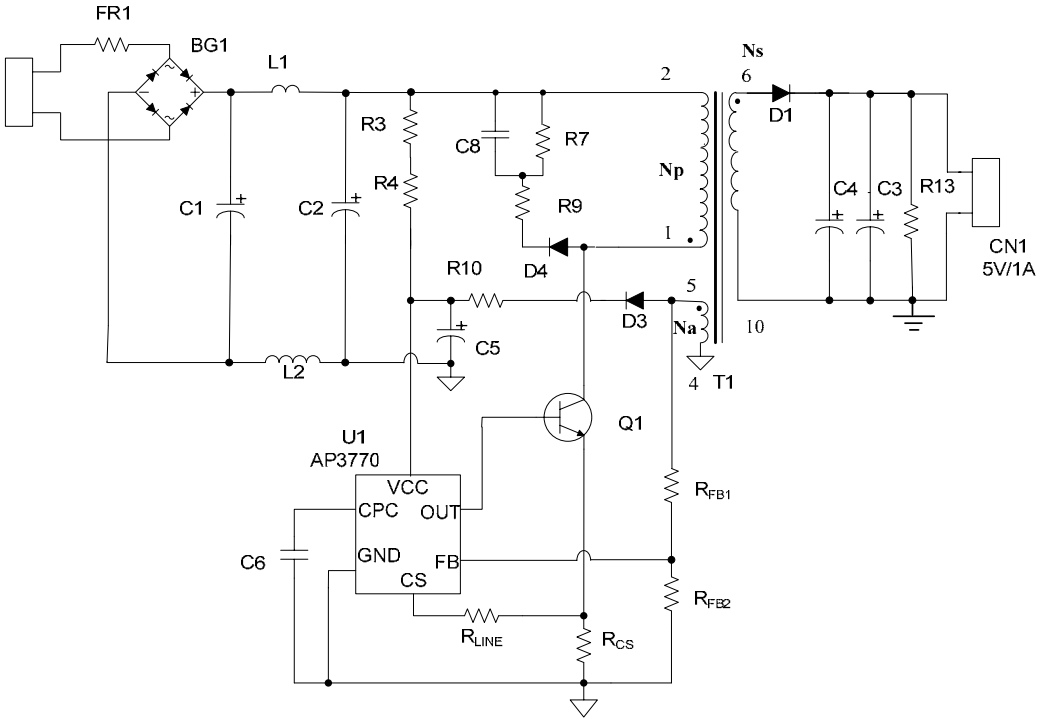

Figure 1. 5V/1A Output for Battery Charger of Mobile Phone

Figure 1 is AP3770 typical application circuit, which is a FLYBACK converter controlled by AP3770 with a 3-winding transformer---Primary winding (**Np**), Secondary winding (**Ns**) and Auxiliary winding (**Na**). The AP3770 senses the auxiliary winding feedback voltage at FB pin and obtains power supply at VCC pin.

Figure 2 is the typical operation waveforms of PFM controller. In this figure, a series of relative idea operation waveforms are given to illustrate some parameters used in following design steps. And the nomenclature of the parameters in Figure 2 is illustrated.

$\mathbf{V_{dri}}$---A simplified driving signal of primary transistor
$\mathbf{I_p}$---The primary side current
$\mathbf{I_s}$ ---The secondary side current
$\mathbf{V_{SEC}}$---The voltage of secondary
$\mathbf{t_{SW}}$---The period of switching frequency
$\mathbf{t_{ONP}}$ ---The time of primary side "ON"
$\mathbf{t_{ONS}}$ ---The time of secondary side "ON"
$\mathbf{t_{OFF}}$ ---The discontinuous time
$\mathbf{t_{OFFS}}$ --- The time of secondary side "Off"
$\mathbf{I_{PK}}$---Peak current of primary side
$\mathbf{I_{PKS}}$---Peak current of secondary side
$\mathbf{V_S}$---the sum of Vo and forward voltage of rectification diode

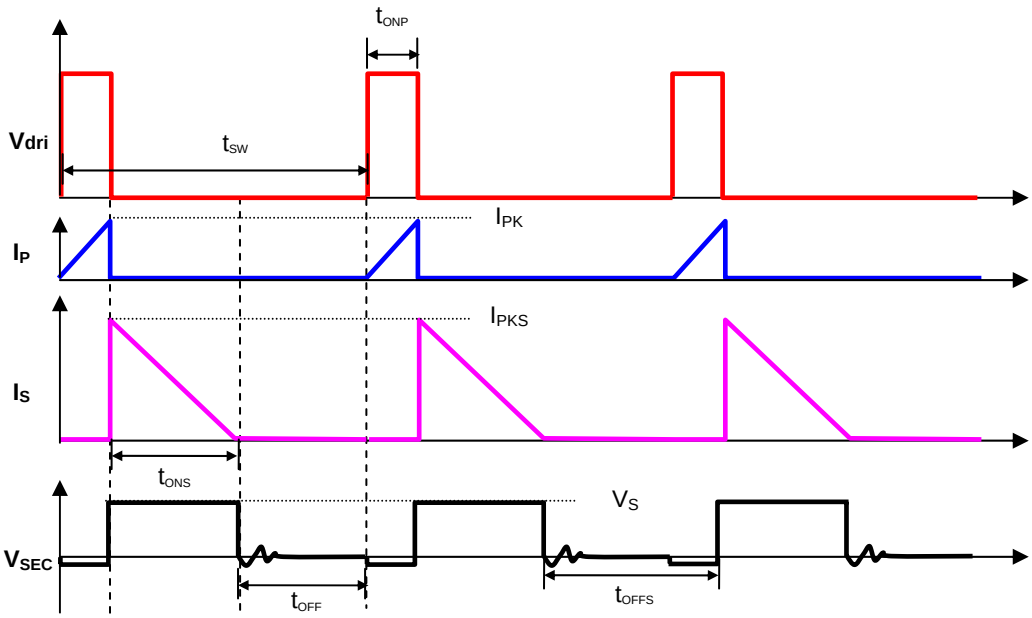

Figure 2. Operation Waveforms

2. Five Aspects for System Design

1. Low Standby Power Design
2. Switching Frequency Design
3. Transformer and Power Devices Design
4. Feedback Resistors Design
5. Line Compensation Design

2.1 Low Standby Power Design

In order to achieve low standby power, AP3770 decreases the minimum operating voltage. And due to proprietary Zero-Startup-Current technique, the startup up resistors R3+R4 should be higher to 10M to 14MΩ to further lower the power loss. The recommended value of dummy load resistor R13 is 4.7KΩ to 10KΩ for an model with 5V output voltage. The selection of dummy load resistor is a tradeoff between standby power and I-V Curve.

2.2 Switching Frequency Design

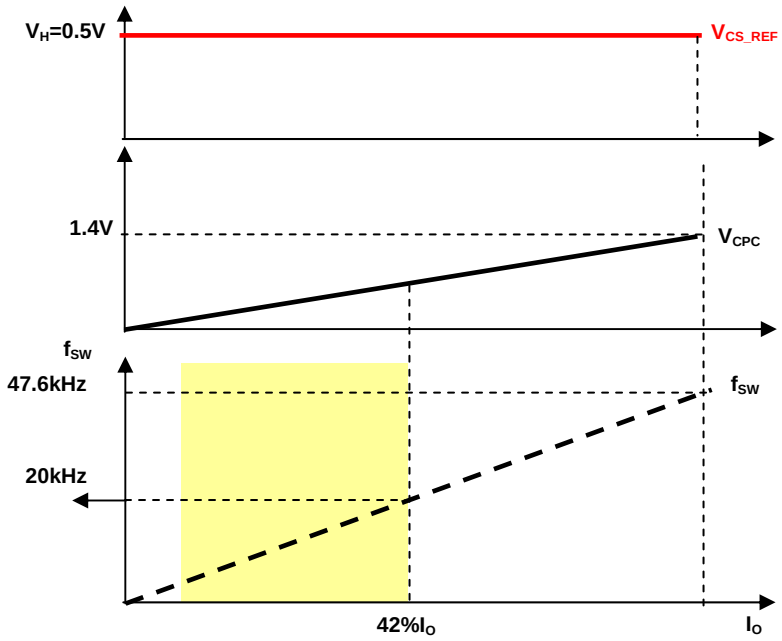

Figure 3. Relationship Between V_{CPC}, f_{SW} and I_O with Constant Peak Current

When the constant peak current is adopted, the voltage of CPC pin is increased linearly with load increasing. The maximum value of V_{CPC} is equal to

$$\frac{t_{ONS}}{t_{SW}} \cdot VDD = \frac{4}{10} \cdot 3.5V = 1.4V \quad (1)$$

The primary current ip(t) is sensed by a current sense resistor R_{CS} as shown in Figure 2. The power transferring from input to output is given by:

$$P_O = \frac{1}{2} \cdot L_P \cdot I_{pk}^{\ 2} \cdot f_{SW} \quad (2)$$

Where, the f_{SW} is the switching frequency. When the peak current I_{PK} is constant, the output power depends on the switching frequency f_{SW}. f_{SW} is linearly increased with load increasing.

In AP3770, two-segmented peak current is used to realize audio noise suppression. The peak current is about 0.5V when I_O>42%$I_O$max, and the peak current is about 0.5V/1.5 when I_O<42%$I_O$max.

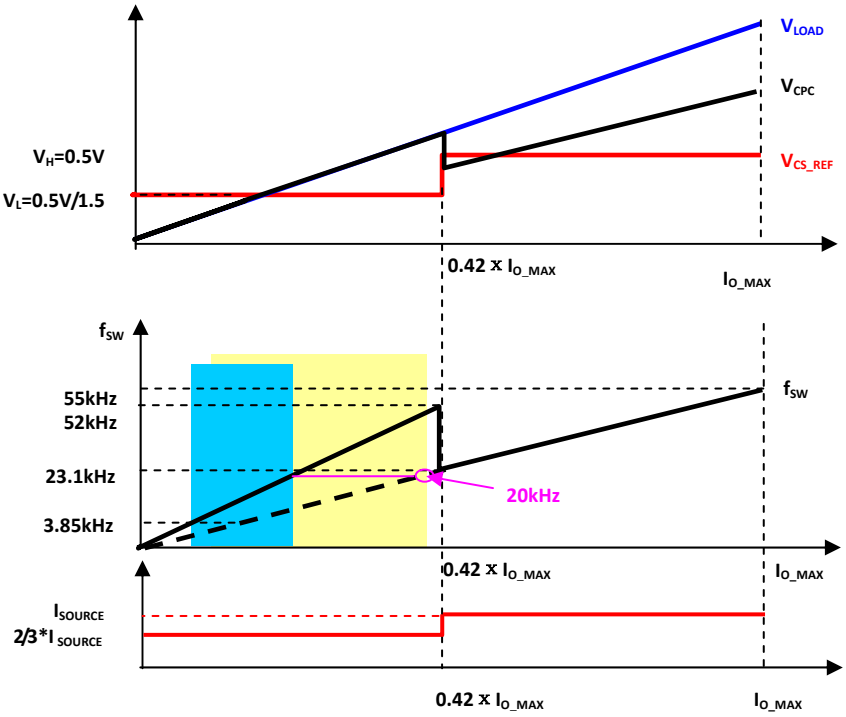

Figure 4. Relationship Between V_{CPC}, f_{SW} and I_O with Variable Peak Current

So, the voltage of CPC pin and switching frequency has a mutation at about 42% of load. At the mutation point, if the peak current is changed from 0.5V(high I_{PK}) to 0.33V(low I_{PK}), the voltage of CPC pin at low I_{PK} will be increased to 1.5 times of V_{CPC} at high I_{PK} and the switching frequency f_{SW} at low I_{PK} will be increased to 2.25 times of f_{SW} at high I_{PK}. So the range of load working in the audio frequency is suppressed.

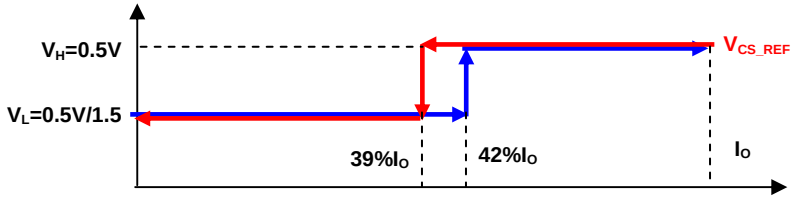

Figure 5. Hysteresis at Conversion Between Low I_{PK} and High I_{PK}

In order to avoid oscillation, a hysteresis is added at the conversion between low I_{PK} and high I_{PK}. Considering the relationship between audio noise and flux density of transformer, deltaB≤2500 gauss is better for audio noise suppression.

The low limitation of maximum switching frequency is given by audio noise suppression. And the upper limit of the AP3770 can be up to 120kHz. But this is only the limit of the IC; the finally designed maximum switching frequency is determined by the tradeoff between the efficiency, mechanical dimensions and thermal performance.

2.3 Transformer and Power Devices Design

In Constant Current operation of AP3770, the CC loop control function of AP3770 will keep a fixed proportion between D1 (in Figure 1) on-time t_{ONS} and D1 off-time t_{OFFS} (in Figure 2) by discharging or charging a capacitor embedded in the IC. The fixed proportion is

$$\frac{t_{ONS}}{t_{OFFS}} = \frac{4}{6} \tag{3}$$

The relationship between the output constant-current and secondary peak current I_{PKS} is given by:

$$I_O = \frac{1}{2} \cdot I_{pks} \cdot \frac{t_{ONS}}{t_{ONS} + t_{OFFS}} \tag{4}$$

At the instant of D1 turn-on, the primary current transfers to the secondary at an amplitude of:

$$I_{pks} = \frac{N_P}{N_S} \cdot I_{pk} \tag{5}$$

Thus the output constant-current is given by:

$$I_O = \frac{1}{2} \cdot \frac{N_P}{N_S} \cdot I_{pk} \cdot \frac{t_{ONS}}{t_{ONS} + t_{OFFS}} = \frac{1}{5} \cdot \frac{N_P}{N_S} \cdot I_{pk} \tag{6}$$

Design Steps:

Step 1, a reasonable I_{PK} of FLYBACK with AP3770 should be designed

1-1. Calculate the Max. turn ratio of XFMR

The maximum turn ration of XFRM should be designed first, which is to ensure that the system should work in DCM in all working conditions, especially at the min. input voltage and full load.

As we know, if the system can meet equation (7) at minimum input voltage and full load, it can work in DCM in all working conditions.

$$t_{SW} \geq t_{ONS} + t_{OFFS} \tag{7}$$

For the primary side current,

$$t_{ONP} = I_{pk} \cdot \frac{L_p}{V_{indc}} \tag{8}$$

Where L_P is the inductance of primary winding.
V_{indc} is the rectified DC voltage of input.
When V_{indc} is the minimum value, the maximum t_{ONP} can be obtained. So,

$$t_{ONP\_MAX} = I_{pk} \cdot \frac{L_p}{V_{indc\_min}} \tag{9}$$

For the secondary side current,

$$t_{ONS} = I_{pks} \cdot \frac{L_S}{V_S} \tag{10}$$

In (10), L_S is the inductance of secondary winding.

$V_S = V_O + V_d$, V_d is the forward voltage of secondary diode.

For (10), in CV regulation, the V_S is a constant voltage, so t_{ONS} is a constant value with different input voltage.

In FLYBACK converter, when the primary transistor turns ON, the energy stored in the magnetizing inductance Lp. So the power transferring from the input to the output is given by,

$$P_{in}' = P_{in} \cdot \eta_{in} = V_{in} \cdot I_{in} \cdot \eta_{in} \tag{11}$$

$$P_{in}' = \frac{1}{2} \cdot L_p \cdot I_{pk}^2 \cdot f_{SW} \tag{12}$$

Here, P_{in}' is input power of transformer, not including the all of the power loss at primary side (Rectifier, RCD snubber, BJT and so on).

η_{in} is definition to the input efficiency of system, which is about 0.9.

Then,

$$t_{SW} = \frac{L_p \cdot I_{pk}^2}{2 \cdot P_{in} \cdot \eta_{in}} \tag{13}$$

t_{SW}, t_{ONP} and t_{ONS} in (7) are replaced with (13), (9) and (10),

$$\frac{L_p \cdot I_{pk}^2}{2 \cdot P_{in} \cdot \eta_{in}} \geq I_{pks} \cdot \frac{L_s}{V_s} + I_{pk} \cdot \frac{L_p}{V_{indc\_min}} \tag{14}$$

Because the peak current and inductance of primary side and secondary side have the following relationship,

$$I_{pks} = N \cdot I_{pk} \cdot \eta_i \tag{15}$$

$$L_s = \frac{L_p}{N^2} \tag{16}$$

Here, N is the turn ratio of primary and secondary sides.

With (14), (15) and (16), then,

$$\frac{I_{pk}}{2 \cdot P_{in} \cdot \eta_{in}} \geq \frac{\eta_i}{V_S \cdot N} + \frac{1}{V_{in}} \tag{17}$$

Because,

$$P_{in} = \frac{V_O \cdot I_O}{\eta} \tag{18}$$

η is the system efficiency.

At full load, the system will work in the boundary of CC regulation. I_O can be given by,

$$I_O = \frac{1}{2} \cdot \frac{t_{ONS}}{t_{SW}} \cdot I_{pks} \tag{19}$$

Then, I_{PKS} can be defined,

$$I_{pks} = k \cdot I_O \tag{20}$$

In the design of AP3770,

$$k = \frac{2 \cdot t_{SW}}{t_{ONS}} = 5 \tag{21}$$

The following can be obtained,

$$N \leq V_{indc\_min} \cdot \left(\frac{k \cdot \eta}{2 \cdot V_O \cdot \eta_{in} \cdot \eta_i} - \frac{\eta_i}{V_O + V_d} \right) \tag{22}$$

1-2. Calculate the peak current of primary side and current sensed resistor

I_{PK} can be calculated by the output current.

$$I_{pk} \cdot \eta_i = \frac{I_{pks}}{N} = \frac{k \cdot I_O}{N} \tag{23}$$

Here, k=5, $\eta_i = 0.9$, which is the efficiency of I_{PK} and I_{PKS}.

N is the calculated value of Nmax.

In AP3770, 0.5V is an internal reference voltage. If the sensed voltage V_{CS} reaches 0.5V, the power transistor will be shut down and t_{ONP} will be ended.

$$R_{CS} = \frac{0.5V}{I_{pk}} \tag{24}$$

So R_{CS} can be obtained from (24) and selected with a real value from the standard resistor series. After R_{CS} selected, I_{PK} should be modified based on the selected R_{CS}.

From now on, I_{PK} and R_{CS} have been designed.

Step 2, Design Transformer

2-1. Calculate the inductance of primary side---L_P

The primary side inductance L_P is relative with the stored energy. L_P should be big enough to store enough energy, so that P_{O_Max} can be obtained from this system.

From formula (18), the output power can be given by,

$$P_O = \frac{1}{2} \cdot L_p \cdot I_{pk}^2 \cdot f_{SW} \cdot \frac{\eta}{\eta_{in}} \tag{25}$$

Where f_{SW} was set by the user based on definite requirement.

Then, L_P can be gotten by,

$$L_P = \frac{2 \cdot P_O}{I_{PK}^2 \cdot f_{SW}} \cdot \frac{\eta_{in}}{\eta} \tag{26}$$

2-2. Re-calculate the turn ratio of primary and secondary side---N

From formula (24), the turn ratio of primary and secondary side N can be re-calculated.

$$N = \frac{k \cdot I_O}{I_{pk} \cdot \eta_i} (k = 5) \tag{27}$$

2-3. Calculate the turns of primary, secondary and auxiliary sides

First, the reasonable core-type and ΔB should be selected. Then, the turns of 3-winding transformer can be obtained respectively.

The turns of primary winding,

$$N_p = \frac{L_P \cdot I_{PK}}{Ae \cdot \Delta B} \tag{28}$$

The turns of secondary winding,

$$N_S = \frac{N_P}{N} \tag{29}$$

The turns of auxiliary winding,

$$N_A = \frac{N_S \cdot V_A}{V_S} \tag{30}$$

Where V_A=V_{CC}+ V_{da}, V_{CC} is the set IC supply voltage and V_{da} is the voltage drop of the auxiliary diode.

For AP3770, the typical value of UVLO is decreased to 5.5V, so the supply voltage of IC，V_{CC} can be set to a typical value---12V.

V_S is equal to V_O+V_d.

Ae can be gotten automatically after core-type is selected.

2-4. Check the maximum duty cycle of primary side

After turn ratio of primary side and secondary side is designed, the maximum duty cycle of primary side at low line voltage can be calculated again.

Considering the Volt-second balance between magnetizing and de-magnetizing, the formula of duty cycle is

$$D = \frac{(V_O + V_d) \cdot N \cdot 0.4}{V_{indc}} \quad (31)$$

Step 3, Select diode and primary transistor

3-1. Select diodes of secondary and auxiliary sides

Maximum reverse voltage of secondary side，

$$V_{dr} = V_O + \frac{V_{indc\_max} \cdot N_S}{N_P} \quad (32)$$

Maximum reverse voltage of auxiliary side,

$$V_{dar} = V_A + \frac{V_{indc\_max} \cdot N_A}{N_P} \quad (33)$$

In (32) and (33), the maximum DC input voltage should be used.

3-2. Select the primary side transistor

$$V_{dc\_max} = V_{dc\_spike} + V_{indc\_max} + \frac{V_S \cdot N_P}{N_S} \quad (34)$$

Be careful that the value of V_{dc_spike} will be different with different snubber circuit.

Design Example:

Specification:
Input voltage: $85V_{AC}$ to $265V_{AC}$
Output voltage: V_O=5.3V (Considering the cable compensation)
Output current: I_O=1.1A
Efficiency: 80%

It is higher than the total efficiency because the loss in the input rectifier and the BJT are not included.

Other setting by users:
Switching frequency: f_{SW}=54kHz (Should be equal to or higher than 54kHz)
Forward voltage of secondary diode: Vd=0.4V
Forward voltage of auxiliary diode: Vda=1.1V
V_{CC} voltage: V_{CC}=12V
Core_type: EE16 (Ae=19.2mm^2)
Set ΔB: ΔB<3000GS
V_{dc_spike}=100V (with snubber circuit)

Design Steps:

Step 1, a reasonable I_{PK} of FLYBACK with AP3770 should be designed.

1-1. Calculate the maximum turn ratio of XFMR

$$N_{MAX} = V_{indc\_min} \cdot \left(\frac{k \cdot \eta}{2 \cdot V_O \cdot \eta_{in} \cdot \eta_i} - \frac{\eta_i}{V_O + V_d} \right) (k = 5) \quad (35)$$

$V_{indc\_min} = V_{inac\_min} \cdot \sqrt{2} - 40$, $\eta = 0.75$, $\eta_{in} = 0.9$, $\eta_i = 0.9$

$N_{MAX} \approx 22$ (36)

The turn ratio is finally selected as: $N = 18.5$

1-2. Calculate the peak current of primary side and current sensed resistor

$I_{pk} \cdot \eta_i = \frac{I_{pks}}{N} = \frac{k \cdot I_O}{N}$ ($\eta_i = 0.9$, which is the transfer efficiency of Ipk and Ipks)

$$I_{pk\_max} = 330mA \quad (37)$$

Sensed current resistor,

$$R_{CS} = \frac{V_{CS}}{I_{pk\_max}} = \frac{0.5V}{359m} \quad (38)$$

$$R_{CS} \approx 1.5\Omega \quad (39)$$

Re-calculate peak current of primary side,

$$I_{pk\_max} = 333mA \quad (40)$$

Step 2, Design Transformer
2-1. Calculate the inductance of primary side---L_P

$$L_P = \frac{2 \cdot P_O}{I_{PK}^2 \cdot f_{SW}} \cdot \frac{\eta_{in}}{\eta} \quad (41)$$

$$L_p = 2.035mH \quad (42)$$

2-2. Re-calculate the turn ratio of primary and secondary side---N

$$N = \frac{k \cdot I_O}{I_{pk} \cdot \eta_i} (k = 5) \quad (43)$$

$$N = 18.3 \quad (44)$$

2-3. Calculate the turns of primary, secondary and auxiliary sides

The turns of primary winding,

$$N_p = \frac{L_P \cdot I_{PK}}{Ae \cdot \Delta B} \quad (45)$$

$$N_P > 118T \quad (46)$$

The turns of secondary winding,

$$N_S = \frac{N_P}{N} \quad (47)$$

$$N_S \approx 7T \quad (48)$$

Recalculate the primary winding,

$$N_P = N_S \cdot N \quad (49)$$

$$N_P \approx 128T \quad (50)$$

The turns of auxiliary winding,

$$N_A = \frac{N_S \cdot V_A}{V_o + V_d} \quad (51)$$

$$N_A \approx 15T \quad (52)$$

2-4. Check the maximum duty cycle of primary side

The maximum duty cycle of primary side is calculated as following,

$$D = \frac{(V_O + V_d) \cdot N \cdot 0.4}{V_{indc}} \quad (53)$$

$$D|_{V_{indc\_min}} = \frac{(V_O + V_d) \cdot N \cdot 0.4}{V_{indc\_min}} = \frac{(5.3 + 0.4) \cdot 18.3 \cdot 0.4}{80} = 0.528 \quad (54)$$

Step 3, Select diode and primary transistor

3-1. Select diodes of secondary and auxiliary sides

Maximum reverse voltage of secondary side，

$$V_{dr} = V_O + \frac{V_{indc\_max} \cdot N_S}{N_P} \quad (55)$$

$$V_{indc\_max} = 265V \cdot \sqrt{2} \quad (56)$$

$$V_{dr} = 5.4 + \frac{375}{17} \approx 28V \quad (57)$$

Maximum reverse voltage of auxiliary side,

$$V_{dar} = V_A + \frac{V_{indc\_max} \cdot N_A}{N_P} \quad (58)$$

$$V_{dar} = 12 + \frac{375 \cdot 15}{128} \approx 56V \quad (59)$$

3-2. Select primary side transistor

$$V_{dc\_max} = V_{dc\_spike} + V_{indc\_max} + \frac{V_S \cdot N_P}{N_S} \quad (60)$$

$$V_{dc\_max} = 100 + 375 + 5.4 * 17 \approx 567V \quad (61)$$

Design Results Summary:

1.Calculate the maximum peak current of primary side and R_{CS}			
I_{PK}=	333	mA	Peak current of primary side
R_{CS}=	1.5	Ω	Current sensed resistor
2.Design transformer			
L_P=	2	mH(+/-8%)	Inductance of primary side
N=	17	Turn ratio of primary and secondary	
N_P=	128	T	Turns of primary side
N_S=	7	T	Turns of secondary side
N_A=	15	T	Turns of auxiliary side
D_{MAX}	0.52		Maximum duty cycle of primary side at V_{INDC}=80V
3. Select diode and primary transistor			
V_{dr}=	28	V	Maximum reverse voltage of secondary diode
V_{dar}=	56	V	Maximum reverse voltage of auxiliary diode
V_{dcMax}=	567	V	Voltage stress of primary transistor

2.4 Feedback Resistors Design

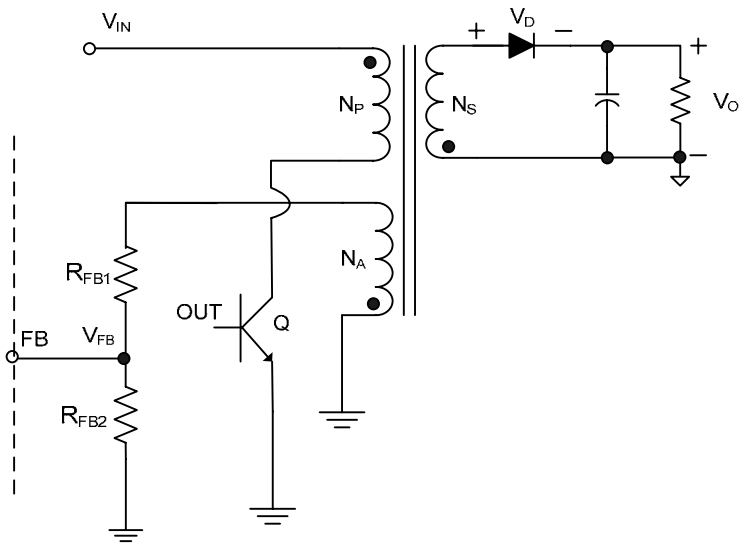

Figure 6. Feedback Resistors Circuit

From above Figure 6,

$$V_o = V_{FB} \cdot \frac{(R_{FB1} + R_{FB2})}{R_{FB2}} \cdot \frac{N_S}{N_A} - V_D \qquad (62)$$

Through adjusting R_{FB1} and R_{FB2}, a suitable output voltage can be achieved. The recommended values of R_{FB1} and R_{FB2} are within 5kΩ to 50kΩ.

2.5 Line Compensation Design

The internal line compensation function in AP3770 is shown in Figure 7. S1 is closed when the primary switch is "ON". The line voltage can be detected from the FB pin. The detected voltage internally compensates the peak current. So the line compensation is determined by R_{LINE}. In different application, the value of R_{LINE} is different.

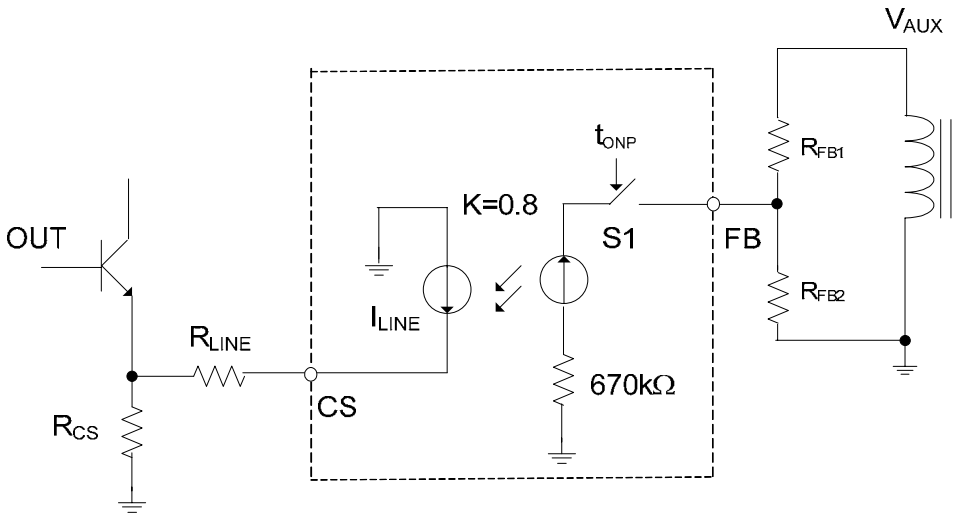

Figure 7. Line Compensation Circuit

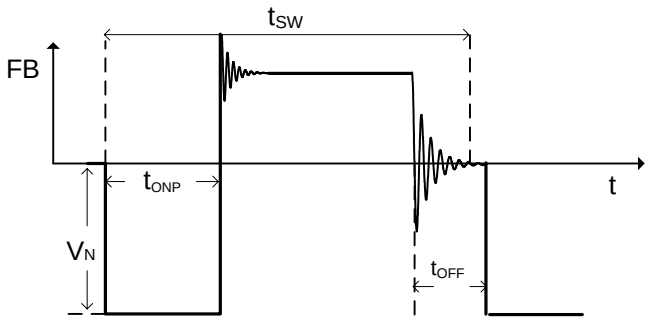

Figure 8. Waveform of FB Pin

The negative voltage V_N of FB pin (in Figure 8) is linear to line voltage. The AP3770 samples V_N to realize the line compensation.

$$V_N = \frac{R_{FB2}}{R_{FB1} + R_{FB2}} \cdot \frac{N_a}{N_p} \cdot V_{indc} \quad (63)$$

The compensated voltage of line compensation (V_{CS_LINE}) can be calculated by the following formula,

$$V_{cs\_line} = R_{line} \cdot K \cdot \frac{1}{670k} \cdot V_N = R_{line} \cdot 0.8 \cdot \frac{1}{670k} \cdot \frac{R_{FB2}}{R_{FB1} + R_{FB2}} \cdot \frac{N_a}{N_p} \cdot V_{indc} \quad (64)$$

So, R_{LINE} can be adjusted to achieve excellent line regulation of output current.

3. Summary

In order to get good performance of AP3770, it's important to design transformer, line compensation and feedback resistance correctly. This application only gives a preliminary design guideline about these aspects and considers ideal conditions, so some parameters need to be adjusted slightly on the basis of the calculated results.

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