D2-IPS Audio SOC

Digital Audio Amplifier Power Stage

The D2-IPS family (D2-24044) device is a high performance, integrated Class-D amplifier power stage. The four power stage outputs are configurable as four separate Half-Bridge outputs, as two Full-Bridge outputs, or combinations of Half-Bridge and Full-Bridge. Individual power stage overload monitoring, on-chip temperature monitoring, and common alert logic outputs provide protection to integrate with the final system's controller.

Related Literature

For a full list of related documents, visit our website:

- D2-24044 device page

Features

- All digital class-D power stage
- Four configurable power stage outputs supporting:
  - 2 Channels, Bridged
  - 4 Channels, Half-Bridge
  - 2 Channels, Half-Bridge, plus 1 Channel, Bridged
- Output Power (bridged)
  - 25W (8Ω, <1% THD)
  - 30W (8Ω, <10% THD)
- Single HV supply - wide 9V-26V range, plus internally-generated gate drive supply
- Individual channel protection monitoring
- Temperature and undervoltage monitoring
- Efficient 38 Ld HTSSOP package

Applications

- PC/multimedia speakers
- Digital TV audio systems
- Portable device docking stations
- Powered speaker systems

Digital Amplifier Power Stage
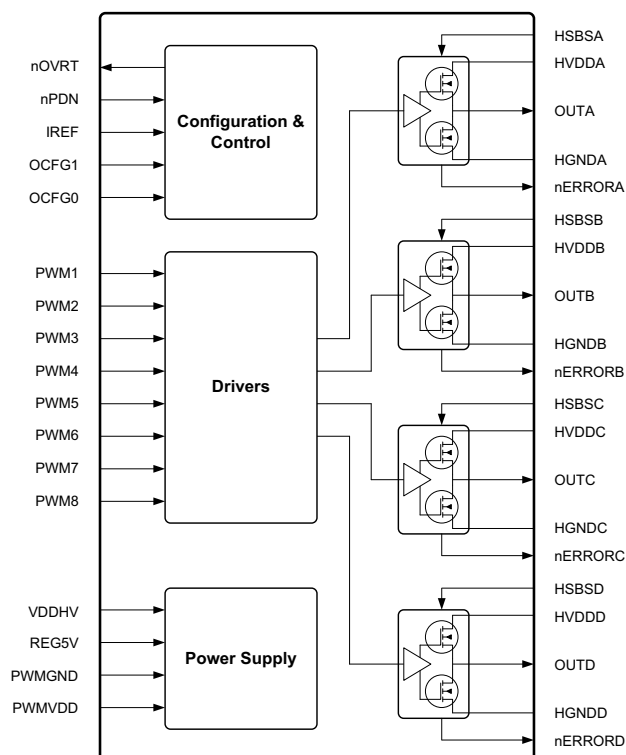
Ordering Information

PART NUMBER (Note 3)	PART MARKING	APPLICATION SUPPORT	TEMP. RANGE (°C)	TAPE AND REEL (UNITS) (Note 1)	PACKAGE (Pb-Free)	PKG. DWG. #
D2-24044-MR	D2-24044-MR	Commercial	-10 to +85	-	38 Ld HTSSOP	M38.173C
D2-24044-MR-T	D2-24044-MR	Commercial	-10 to +85	2.5k	38 Ld HTSSOP	M38.173C

NOTES:

1. See TB347 for details about reel specifications.

2. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). The Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

3. For Moisture Sensitivity Level (MSL), see the D2-24044 device page. For more information about MSL, see TB363.

Table of Contents

Absolute Maximum Ratings

Supply Voltage
  HVDD[A:D], VDDHV. . . . . 0V to +28.0V
  PWMVDD . . . . 0V to 4.0V
Input Voltage
  Any Input . . . . -0.3V to PWMVDD + 0.3V

Thermal Information

Thermal Resistance (Typical) θ_{JA} (°C/W) θ_{JC} (°C/W)
  38 Ld HTSSOP Package (Notes 4, 5)   29   1.3
Maximum Storage Temperature . . . . -55°C to +150°C
Pb-Free Reflow Profile . . . . see TB493

Recommended Operating Conditions

Temperature Range. . . . .-10ºC to +85ºC
High Voltage Supply Voltage,
  HVDD[A:D], VDDHV . . . . 9.0V to 26.5V
Digital I/O Supply Voltage, PWMVDD. 3.3V
Minimum Load Impedance (HVDD[A:D] ≤24.0V), Z_L 4Ω

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with "direct attach" features. See TB379.

5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

6. Absolute Maximum parameters are not tested in production.

Electrical Specifications

TA = +25°C, PWMVDD = 3.3V ±10%. All grounds at 0.0V. All voltages referenced to ground.

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Digital Input High Logic Level		V_{IH}	2	-	-	V
Digital Input Low Logic Level		V_{IL}	-	-	0.4	V
High Level Output Drive Voltage (I_{OUT} at -Pin Drive Strength Current)		V_{OH}	PWMVDD-0.4	-	-	V
Low Level Output Drive Voltage (I_{OUT} at +Pin Drive Strength Current)		V_{OL}	-	-	0.4	V
Input Leakage Current	Pins 1, 2, 3	I_{IN}	-	-	±10	µA
	PWM Input Pins (includes 100kΩ internal pull-down resistor current)		-	-	±50	µA
Input Capacitance		C_{IN}	-	9	-	pF
Output Capacitance	All Outputs Except OUT[A:D]	C_{OUT}	-	9	-	pF
	OUT[A:D]		-	190	-	
Internal Pull-Up Resistance to PWMVDD (for nERRORA-D, nOVRT)			-	100	-	kΩ
Digital I/O Supply Pin Voltage, Current		PWMVDD	3	3.3	3.6	V
	Active Current		-	0.47	-	mA
	Power-Down Current		-	0.15	-	mA
3.3V (PWMVDD) BROWN-OUT DETECTION						
Logic Supply Undervoltage Threshold			-	2.6	-	V
Logic Supply Undervoltage Threshold Hysteresis			-	200	-	mV
Logic Supply Undervoltage Glitch Rejection			-	50	-	ns

Electrical Specifications

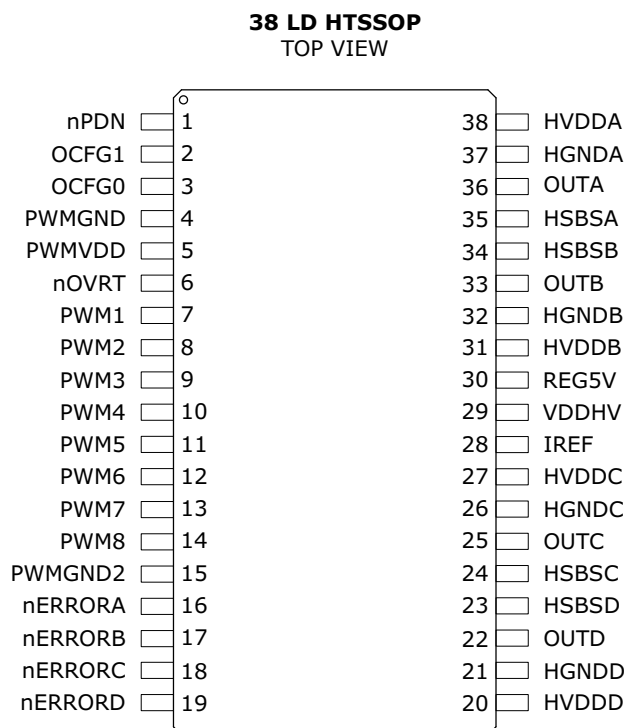TA = +25°C, PWMVDD = 3.3V ±10%. All grounds at 0.0V. All voltages referenced to ground.

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
GATE DRIVE INTERNAL +5V BROWN-OUT DETECTION						
Gate Drive Supply Undervoltage Threshold			-	4.5	-	V
Gate Drive Supply Undervoltage Threshold Hysteresis			-	200	-	mV
Gate Drive Supply Undervoltage Threshold Glitch Rejection			-	50	-	ns
PROTECTION DETECT						
High Voltage Undervoltage Protection			-	7	9	V
Overcurrent Trip Threshold			-	4	-	A
Overcurrent De-glitch			-	2.5	-	ns
Short-Circuit Current Limit (Peak)			-	8	-	A
Overcurrent Response Time			-	20	-	ns
Thermal Shut-Down OTmax			-	140	-	°C
Thermal Warning Temperature OTmin			-	125	-	°C
Thermal Shut-Down Hysteresis			-	30	-	°C
Thermal Warning Hysteresis			-	20	-	°C

Performance Specifications

T_A = +25°C, PWMVDD = 3.3V ±10%. All grounds at 0.0V. All voltages referenced to ground.   -

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
$r_{DS(ON)}$ (MOSFETs @ +25°C)	$r_{DS(ON)}$	-	200	-	mΩ
$r_{DS(ON)}$ Mismatch		-	1	-	%
PWM Switching Rate		-	384	-	kHz
Minimum PWM Pulse Width		-	3.5	-	ns
PWM Off Sensor Time		-	10	-	µs
PWM Input to Output Delay		-		50	ns
PWM Input to Output Delay Matching		-	3	-	ns
nPDN Input Off Delay	T_{PDNOFF}	-	1.4	-	ms
nPDN Input On Delay	T_{PDNON}	-	1.4	-	ms
POWER OUTPUT					
<1% THD, Bridged, Load = 8Ω, HVDD[A:D] = 24V	P_{OUT}	-	25	-	W
<10% THD, Bridged, Load = 8Ω, HVDD[A:D] = 24V	P_{OUT}	-	30	-	W
<1% THD, Half-Bridge, Load = 8Ω, HVDD[A:D] = 24V	P_{OUT}	-	7	-	W
<10% THD, Half-Bridge, Load = 8Ω, HVDD[A:D] = 24V	P_{OUT}	-	9	-	W
THD+N					
Load = 8Ω, Power = 25W, Bridged, 1kHz	THD+N	-	0.3	-	%
Load = 8Ω, Power = 1W, Bridged, 1kHz		-	0.05	-	%
SNR	SNR	-	110	-	dB
Efficiency (Load = 8Ω)		-	90	-	%

RENESAS

Pin Configuration

38 LD HTSSOP
TOP VIEW

Left pin	#		#	Right pin
nPDN	1		38	HVDDA
OCFG1	2		37	HGNDA
OCFG0	3		36	OUTA
PWMGND	4		35	HSBSA
PWMVDD	5		34	HSBSB
nOVRT	6		33	OUTB
PWM1	7		32	HGNDB
PWM2	8		31	HVDDB
PWM3	9		30	REG5V
PWM4	10		29	VDDHV
PWM5	11		28	IREF
PWM6	12		27	HVDDC
PWM7	13		26	HGNDC
PWM8	14		25	OUTC
PWMGND2	15		24	HSBSC
nERRORA	16		23	HSBSD
nERRORB	17		22	OUTD
nERRORC	18		21	HGNDD
nERRORD	19		20	HVDDD

Pin Description

PIN	PIN NAME (Note 7)	TYPE	VOLTAGE LEVEL (V)	DESCRIPTION
1	nPDN	I	3.3	Power-down and mute input. Active low. When this input is low, all four outputs become inactive, their output stages float, and their output is muted. Internal logic and other references remain active during this power-down state.
2	OCFG1	I	3.3	Output configuration control select. OCFG0 and OCFG1 are logic inputs to select the output configuration mode of the output stages. Connects to either PWMGND ground or PWMVDD (+3.3V) through a nominal 10kΩ resistor to select the output configuration.
3	OCFG0	I	3.3	
4	PWMGND	GND	0	Low-voltage ground. Connects to ground of circuitry providing PWM inputs. Both PWMGND and PWMGND2 must be tied together to the same ground.
5	PWMVDD	P	3.3	Low-voltage power. This 3.3V supply connects to the same system low-voltage power used for providing PWM inputs.
6	nOVRT	O	3.3	Over-temperature warning output. Open drain, 16mA drive strength output with pull-up. Pulls low when active from over-temperature detection.
7	PWM1	I	3.3	PWM Input. Routes to output channel, dependent on output configuration settings.
8	PWM2	I	3.3	
9	PWM3	I	3.3	
10	PWM4	I	3.3	
11	PWM5	I	3.3	
12	PWM6	I	3.3	
13	PWM7	I	3.3	
14	PWM8	I	3.3	

Pin Description (Continued)

PIN	PIN NAME ([Note 7](#))	TYPE	VOLTAGE LEVEL (V)	DESCRIPTION
15	PWMGND2	GND	0	Low-voltage ground. Connects to ground of circuitry providing PWM inputs. Both PWMGND and PWMGND2 must be tied together to the same ground.
16	nERRORA	O	3.3	Overcurrent protection output, channel A output stage. Open drain, 16mA drive strength output with pull-up. Pulls low when active from overcurrent detection of output stage.
17	nERRORB	O	3.3	Overcurrent protection output, channel B output stage. Open drain, 16mA drive strength output with pull-up. Pulls low when active from overcurrent detection of output stage.
18	nERRORC	O	3.3	Overcurrent protection output, channel C output stage. Open drain, 16mA drive strength output with pull-up. Pulls low when active from overcurrent detection of output stage.
19	nERRORD	O	3.3	Overcurrent protection output, channel D output stage. Open drain, 16mA drive strength output with pull-up. Pulls low when active from overcurrent detection of output stage.
20	HVDDD	P	HV	Output stage D high voltage supply power. A separate power pin connection is provided for each of the output stages. All of the HVDD[A:D] pins and the VDDHV pin connect to the system "HV" power source.
21	HGNDD	GND	HV	Output stage D high voltage supply ground. A separate ground pin connection is provided for each of the output stages. All of the HGND[A:D] pins connect to the system "HV" power ground (also see Note 8).
22	OUTD	O	HV	PWM power amplifier output, channel D.
23	HSBSD	I	HV	High side boot strap input, output channel D. Capacitor couples to the OUTD amplifier output.
24	HSBSC	I	HV	High side boot strap input, output channel C. Capacitor couples to the OUTC amplifier output.
25	OUTC	O	HV	PWM power amplifier output, channel C.
26	HGNDC	GND	HV	Output stage C high voltage supply ground. A separate ground pin connection is provided for each of the output stages. All of the HGND[A:D] pins connect to system "HV" power ground (also see [Note 8](#)).
27	HVDDC	P	HV	Output stage C high voltage supply power. A separate power pin connection is provided for each of the output stages. All of the HVDD[A:D] pins and the VDDHV pin connect to the system "HV" power source.
28	IREF	I	-	Overcurrent reference analog input used to set the overcurrent error to detect externally-set threshold. The pin needs to be connected to a 100kΩ resistor to ground to set the overcurrent threshold according to the specified limits.
29	VDDHV	P	+HV	High Voltage internal driver supply power. All of the HVDD[A:D] pins and the VDDHV pin connect to the system "HV" power source. The internal +5V supply regulators also operate from this VDDHV input.
30	REG5V	P	5	5V internal regulator filter connect. A +5V supply is internally generated from the voltage source provided at the VDDHV pin. REG5V is used for external connection of a decoupling capacitor.
31	HVDDB	P	HV	Output stage B high voltage supply power. A separate power pin connection is provided for each of the output stages. All of the HVDD[A:D] pins and the VDDHV pin connect to the system "HV" power source.
32	HGNDB	GND	HV	Output stage B high voltage supply ground. A separate ground pin connection is provided for each of the output stages. All of the HGND[A:D] pins connect to the system "HV" power ground (also see [Note 8](#)).
33	OUTB	O	HV	PWM power amplifier output, channel B.
34	HSBSB	I	HV	High side boot strap input, output channel B. Capacitor couples to the OUTB amplifier output.
35	HSBSA	I	HV	High side boot strap input, output channel A. Capacitor couples to the OUTA amplifier output.

Pin Description (Continued)

PIN	PIN NAME (Note 7)	TYPE	VOLTAGE LEVEL (V)	DESCRIPTION
36	OUTA	O	HV	PWM power amplifier output, channel A.
37	HGNDA	GND	HV	Output stage A high voltage supply ground. A separate ground pin connection is provided for each of the output stages. All of the HGND[A:D] pins connect to the system "HV" power ground (also see Note 8).
38	HVDDA	P	HV	Output stage A high voltage supply power. A separate power pin connection is provided for each of the output stages. All of the HVDD[A:D] pins and the VDDHV pin connect to the system "HV" power source.

NOTES:

7. Unless otherwise specified all pin names are active high. Those that are active low have an "n" prefix, such as nERRORA.

8. Thermal pad is internally connected to all 4 HGND ground pins (HGNDA, HGNDB, HGNDC, HGNDD). Any connection to the thermal pad must be made to the common ground for these 4 ground pins.

Typical Performance Characteristics

Full-Bridge Typical Performance Curves
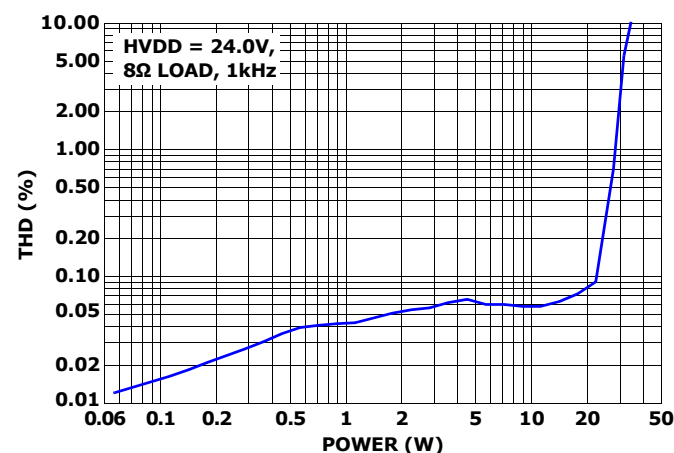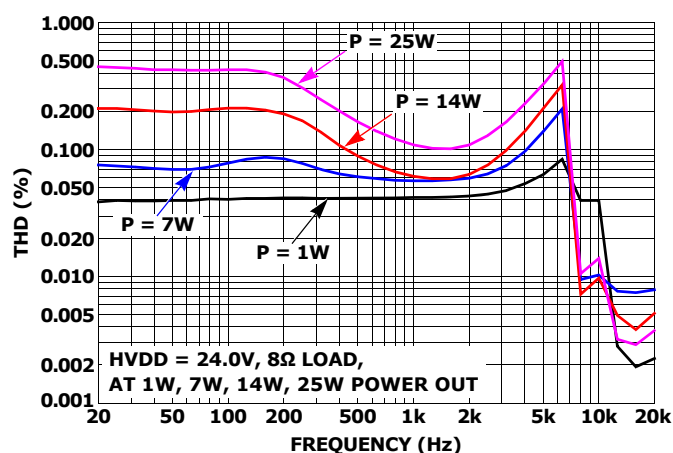

FIGURE 1. THD vs POWER, FULL-BRIDGE

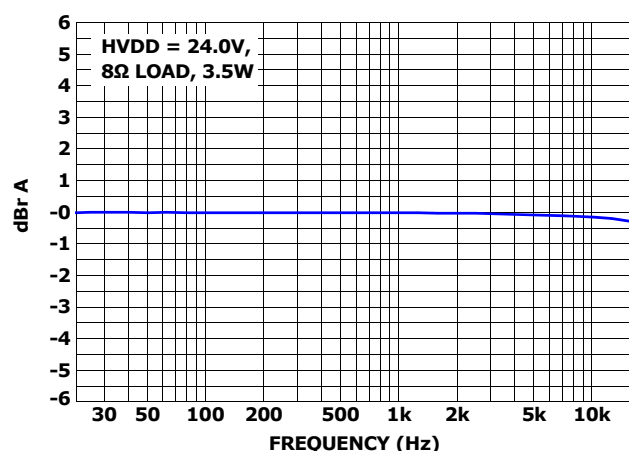FIGURE 2. THD vs FREQUENCY, FULL-BRIDGE
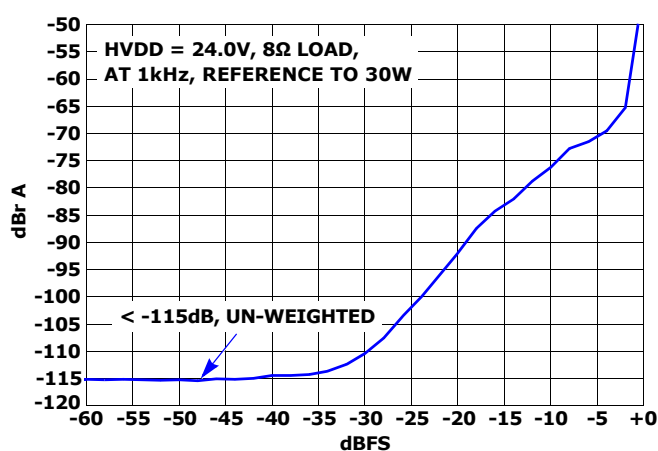

FIGURE 3. FREQUENCY RESPONSE, FULL-BRIDGE

FIGURE 4. NOISE FLOOR, FULL-BRIDGE

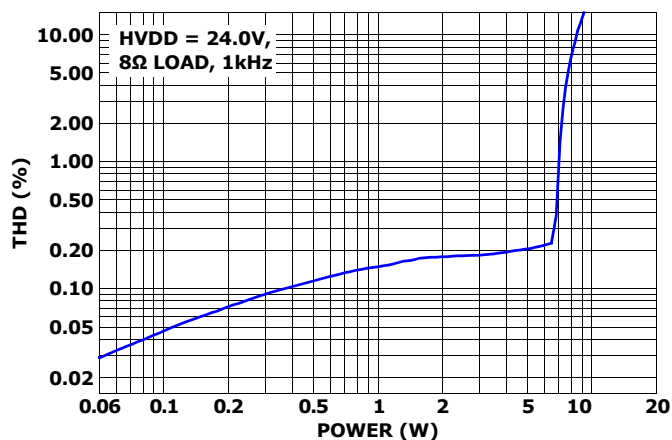## Half-Bridge Typical Performance Curves
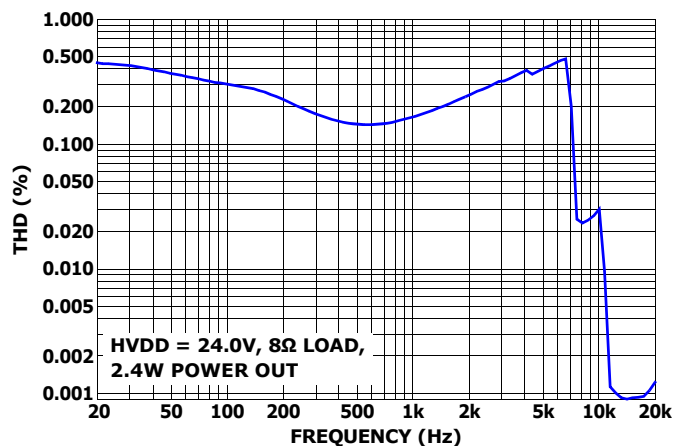

FIGURE 5. THD vs POWER, HALF-BRIDGE

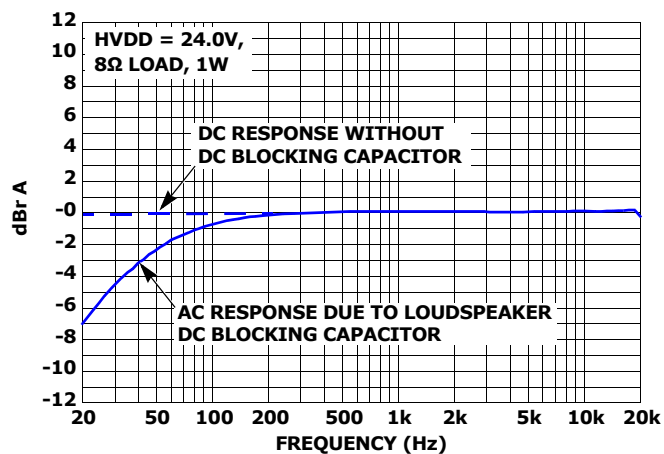FIGURE 6. THD vs FREQUENCY, HALF-BRIDGE

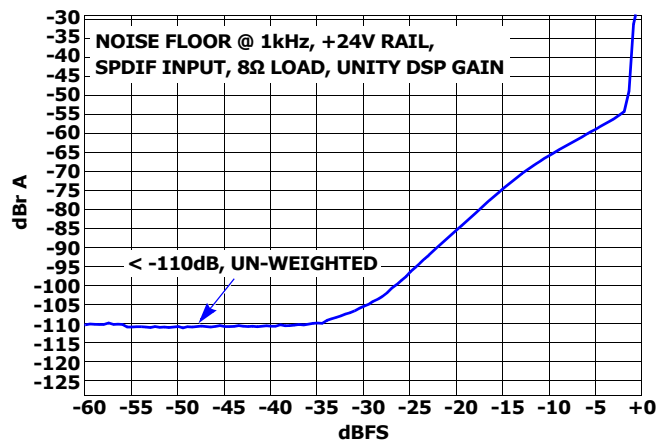FIGURE 7. FREQUENCY RESPONSE, HALF-BRIDGE

FIGURE 8. NOISE FLOOR, HALF-BRIDGE

Functional Overview

The devices include four independent output stages ([Figure 9](#)) that are each implemented using a high side (to the positive VDDHV supply) and a low side (to the HV supply ground) FET pair. Drivers and overcurrent monitoring are included in each of these four output stages. Depending on the selected configuration mode, these four stages can be used independently as single half-bridge outputs, or as pairs for full-bridge outputs.

Digital PWM inputs are connected to the PWM input pins, where their signals are routed through the configuration select logic to the individual output FETs and drivers.

On-chip temperature and undervoltage monitoring, and individual per-output current monitoring provides protection and status reporting outputs to the system controller.

Upon application of power, the on-chip voltage sensors monitor presence of the required power voltages. Until all voltages are at their design specifications, the outputs remain off and floating.

After supply voltages are within limits and stable, the output configuration is set by the logic levels at the OCFG0 and OCFG1 input pins, and the PWM inputs are routed to their appropriate output stage FETs.
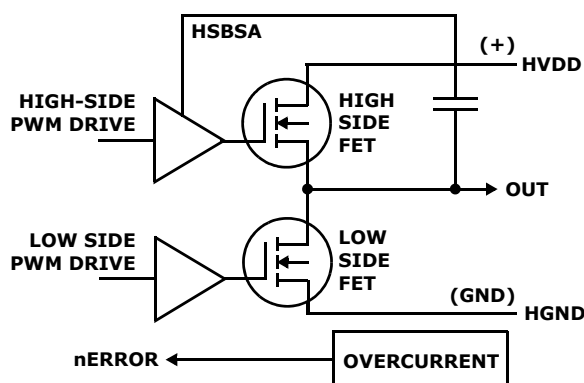

FIGURE 9. OUTPUT STAGE

Output Options

The D2-IPS family devices provide four configuration options for the outputs. These options are selected by strapping the OCFG0 and OCFG1 pins high or low. These defined configurations include:

- 2 Channels of Full Bridge, 4-Quadrant Outputs

- 2 Channels of Full Bridge, 2-Quadrant Outputs

- 4 Channels of Half-Bridge Outputs

- 2 Channels Half-Bridge, Plus 1 Channel Full Bridge

When a configuration is set that includes a full-bridge output, each input channel's PWM input signal is routed to the high and low side FETs, appropriate for that full bridge operation. Note however, that the device can be configured as four independent half-bridge outputs

(using mode "11" as described in the configuration assignment table on [page 14](#)) and two of those outputs can be used in a full bridge configuration, by connecting the appropriate PWM input pins to the input source. This configuration allows flexibility in applications that require combinations other than the four defined by the output configuration modes.

Power Supply Requirements

The device operates from two supply voltages:

- PWMVDD is a nominal 3.3V supply voltage and operates the logic and control.

- HVDD (HVDD[A:D], and VDDHV) is the "high voltage" used for operating the output power stages.

Individual HVDD and its ground (HGND) pins are included for each of the four power stage outputs, providing channel isolation and low impedance source connections to each of the outputs. A separate VDDHV pin is used for the output drivers, and is the source for the on-chip regulated 5V source needed for the drivers. All the HVDD/VDDHV pins connect to the same voltage source.

PWMVDD is the reference for the PWM inputs and device control logic, and is the same voltage as used by the PWM/system controller.

High Side Gate Drive Voltage

An on-chip bootstrap circuit provides the high-side gate drive voltage used by each output stage. A pin is included for each output channel (HSBS[A:D]) for connection of a capacitor (nominal, 0.22µF/50V) from this pin to that channel's PWM output. The charge pumping actions uses this capacitor to filter and hold this gate drive voltage, and enables amplifier operation without need of connection to an additional power supply voltage.

Supply Bypass Connection

Connect power supply bypass capacitors across each of the power supply connection pins, as follows:

- Four HVDD power pins and their respective HGND ground pins. These should be a parallel combination of a nominal 100µF and 0.1µF capacitors, located as close as possible to the HVDD/HGND pin pair.

- Connect a 0.1µF capacitor at the VDDHV pin.

- The PWMVDD power pin should include a 1µF and 0.1µF capacitor.

REG5V

The on-chip gate drive power supply operates from the VDDHV power input to produce the 5V supply voltage. The REG5V pin is used for external capacitor connection to filter this regulated voltage. A 1.0µF and 0.1µF capacitor should be connected to this pin, and the connection should be made as close as practical to the pin. Do not make any other connections to be made to this pin.

Input and Control Functions

PWM Inputs

Eight PWM input pins provide the PWM inputs to the amplifier's output stages. The PWM input pins are electrically single-ended and are referenced to the PWMVDD and PWMGND supplies.

PWM drive to the output stages is provided differentially on-chip, with the PWM input channels mapped to each of the high-side output FETs and the low-side output FETs that implement the individual power stages. Routing and assignment of the PWM input pins to the output FETS is defined by the configuration mode. Figures 11, 12, 13, and 14 show the mapping of these input pins to the outputs for each of the four configuration modes.

All eight input pins however are not always used in each of the configuration modes. For example, in mode "00", providing 3-level drive of two channels of full bridge outputs, or in mode "11" providing four independent half-bridge outputs, one PWM input is dedicated to each of the FETs. But in mode "01" that implements two 2-quadrant full-bridge outputs, only four PWM inputs are used, and the logical high/low states are routed to the FETs as needed.

nPDN Input Pin

The nPDN pin is a control input that is used to set the inactive (powered down) state, and also mute the outputs. It operates by turning off drive and internal sources to the PWM outputs, as well as turning off the PWM drive to those outputs.

When an overcurrent condition is detected on an output, causing its overcurrent protection to latch and turn off that output, asserting the nPDN input resets the device and clears this overcurrent state.

The nPDN pin is active low, and inactive when at logic high level.

nERRORA-D Output Pins

Each of the four outputs includes an overload and overcurrent monitor. An overcurrent or overload condition asserts the nERROR output for that channel. These outputs are active low and open drain. Depending on the output mode configuration and need to monitor more than one output, these nERROR pins can be wire-or connected together.

nOVRT Output Pin

The nOVRT pin is an output that provides warning of a high temperature condition. It is an open drain, active low output. This pin only provides an indication for the high-temperature condition.

IREF Pin

The IREF pin is used to control the overcurrent monitoring threshold. A 100kΩ resistor connects from this pin to ground.

OCFG0, OCFG1 Input Pins

These two pins are used to define the configuration of the four output stages. They are connected to logic high (PWMVDD) or logic ground (PWMGND) to set their level. See "Output Mode Configurations" on page 14 for additional reference and definition.

Protection

The D2-IPS family device includes monitors for protection of the system as well as the device itself. Certain levels of protection are managed on-chip, as shown in Figure 10. Other protection is integrated at the system level through the system controller, and involves system design decisions based on:

- A short-circuit, over-temperature, or undervoltage event shuts down the outputs.
- Other operation depends on the PWM/system controller to properly manage full system protection operation.
- Power supply sensors shut down the device if supply voltages drop below their design thresholds.
- Overload and overcurrent monitors provide dual threshold status of high current conditions, providing both indication, and device shutdown if needed.
- Chip temperature monitoring provides dual threshold status of high temperature conditions, providing both indication, and device shutdown if needed.

Short-Circuit and Overcurrent Sensing

Each PWM output FET includes a dual-threshold overcurrent sensor. Multiple functions occur depending on detection of overcurrent conditions:

- The lower threshold is used to monitor fault conditions after the output stage filter inductor, such as shorts or overloads on the loudspeaker outputs.
- The higher threshold monitors fault conditions of the PWM output pin.
- The nERROR output asserts for the channel detecting the fault.
- For the lower level threshold, nERROR remains asserted only through the duration of the overcurrent event.
- For the higher level threshold, the output is shut down and its nERROR output is asserted. These outputs remain latched until the controller acknowledges the fault event by turning off the channel's PWM drive. (When the output is shutdown, its PWM output pin floats.)

Thermal Protection and Monitoring

An on-chip temperature sensor provides two temperature monitoring thresholds.

If the device reaches the lower threshold, the nOVRT output is asserted and provides a warning indication to an external controller. The low threshold setting provides indication only and does not have any effect on device operation.

• The lower high-temperature threshold (warning) is set at approximately +125°C.

If the device reaches the higher threshold, it drives all four nERRORA-D outputs low (active) and shuts down the device, in addition to asserting the nOVRT output. This shutdown in non-latching, and operation resumes automatically when temperature returns to normal.

• The higher high-temperature threshold (over-temperature) is set at approximately +140°C.

Power Supply Voltage Monitoring

Undervoltage monitors are included for the output drive (HVDD) supply voltage, the on-chip generated gate drive (REG5V) supply voltage, and the low-level PWMVDD supply voltage. Detection occurs at approximately 2.5V for PWMVDD, approximately 4V for the gate drive supply, and approximately 7V for the HVDD supply. (Limits are listed in the electrical specification tables starting on page 4.)

If any of the monitored voltages drop below their thresholds, the device shuts down its outputs and asserts all four of the nERROR outputs. Operation resumes normally after the undervoltage condition is cleared.
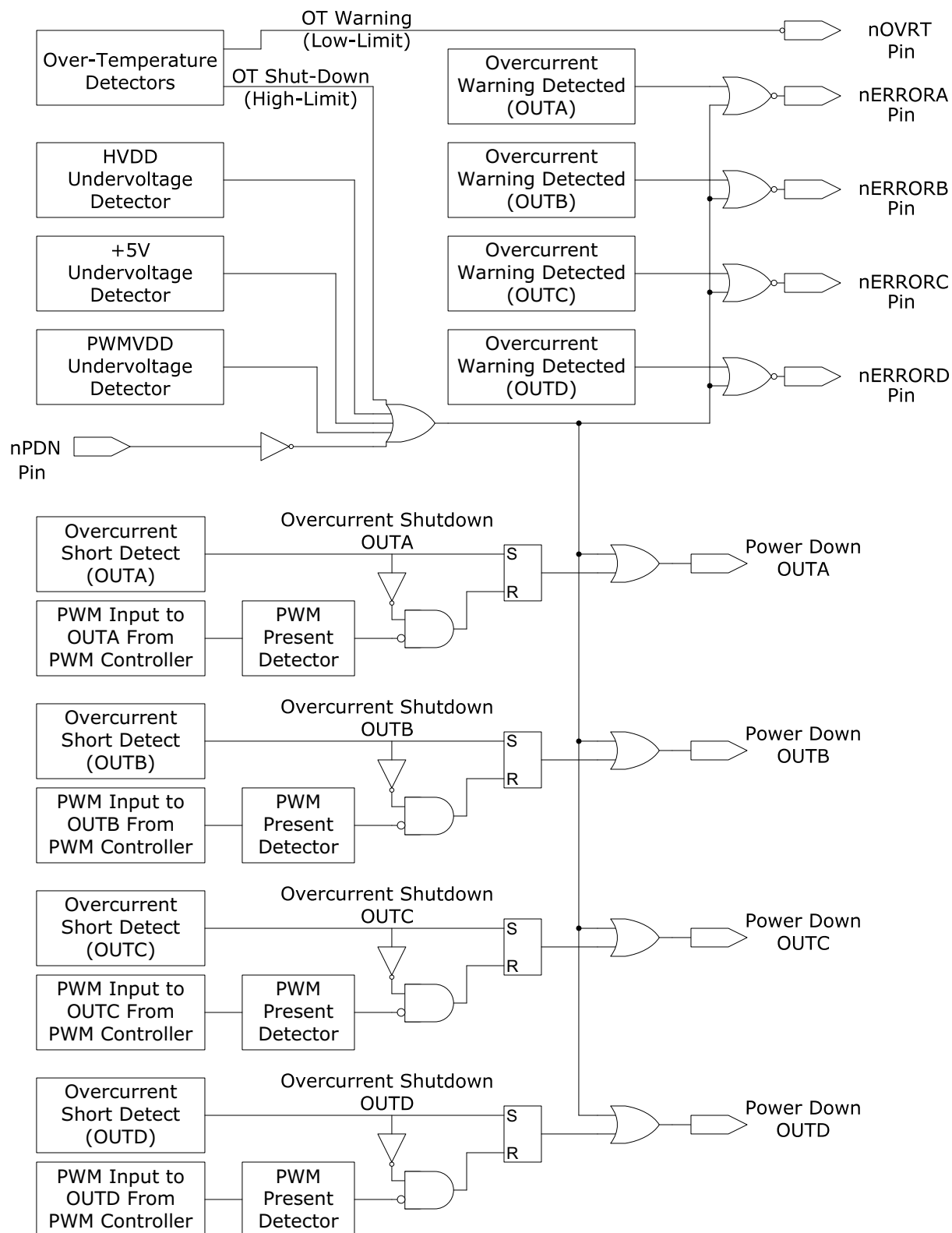
Overcurrent (OC) Shutdown: OC detect condition is latched, shutting down output. Latched shutdown is then cleared after overcurrent condition has cleared, AND PWM data clocking has stopped from PWM controller.

Output Mode Configurations

The D2-IPS family device supports four amplifier output configuration modes, utilizing the device's four power stage outputs.

Configuration selection is controlled by the OCFG0 and OCFG1 pins by connecting them to either a high (+3.3V, PWMVDD = 1) or low (ground = 0) level. Settings are chosen based on the output configuration and topology of the design. Their connections must be hard-connected on the design, and they must be dynamic or subject to change during system operation.

For each of the four configurations, the PWM input pin signals route to the individual FETs of each of the power stages to implement the channel drive and topology needed for those configurations. Figures 11, 12, 13, and 14 show this routing of the PWM inputs to each of the power stages, and how the particular topology is implemented for that configuration. Table 1 shows the configuration functions that are defined with the combinations of the OCFG pins, and these diagrams show the implementation that is listed in this table.

TABLE 1. D2-IPS FAMILY CONFIGURATION PWM AND OUTPUT CHANNEL ASSIGNMENTS

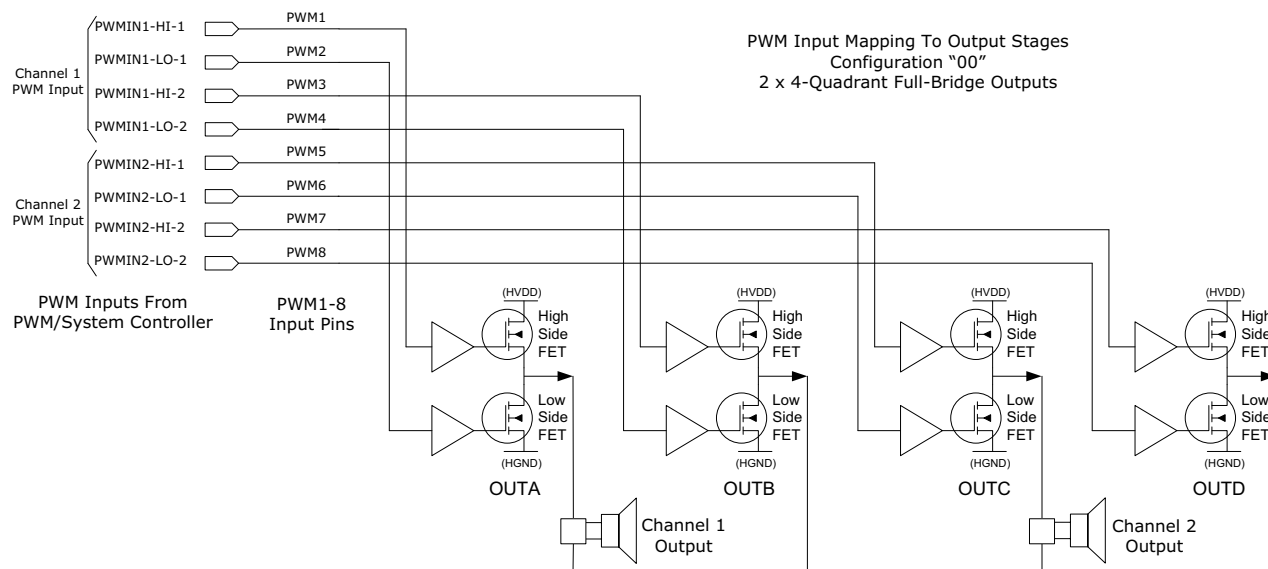| CONFIG PINS | | | CONFIGURATION DESCRIPTION | POWER STAGE OUTPUT | | | | nERROR CHANNEL USE | | | |
OCFG1	OCFG0	CONFIG		OUTA	OUTB	OUTC	OUTD	nERRORA	nERRORB	nERRORC	nERRORD
0	0	"00"	2-Channel Full Bridge 3-Level PWM Drive (Figure 11)	Output Channel 1		Output Channel 2		Connect (wire-or) nERRORA & nERRORB together. Use for Output Channel 1 Protect		Connect (wire-or) nERRORC & nERRORD together. Use for Output Channel 2 Protect	
				High-Side FET PWM Input Assignments							
				PWM1	PWM3	PWM5	PWM7				
				Low-Side FET PWM Input Assignments							
				PWM2	PWM4	PWM6	PWM8				
0	1	"01"	2-Channel Full Bridge, 2-Quadrant PWM Drive (Figure 12)	Output Channel 1		Output Channel 2		Connect (wire-or) nERRORA & nERRORB together. Use for Output Channel 1 Protect		Connect (wire-or) nERRORC & nERRORD together. Use for Output Channel 2 Protect	
				High-Side FET PWM Input Assignments							
				PWM1	PWM2	PWM3	PWM4				
				Low-Side FET PWM Input Assignments							
				PWM2	PWM1	PWM4	PWM3				
1	0	"10"	2-Channel Half-Bridge plus 1-Channel Full Bridge (Figure 13)	Output Ch. 1	Output Ch 2	Output Channel 3		nERRORA Use for Channel 1 Protect	nERRORB Use for Channel 2 Protect	Connect (wire-or) nERRORC & nERRORD together. Use for Output Channel 3 Protect	
				High-Side FET PWM Input Assignments							
				PWM1	PWM3	PWM5	PWM6				
				Low-Side FET PWM Input Assignments							
				PWM2	PWM4	PWM6	PWM5				
1	1	"11"	4-Channel Half-Bridge (Figure 14)	Output Ch. 1	Output Ch 2	Output Ch. 3	Output Ch 4	nERRORA Use for Channel 1 Protect	nERRORB Use for Channel 2 Protect	nERRORC Use for Channel 3 Protect	nERRORD Use for Channel 4 Protect
				High-Side FET PWM Input Assignments							
				PWM1	PWM3	PWM5	PWM7				
				Low-Side FET PWM Input Assignments							
				PWM2	PWM4	PWM6	PWM8				

FIGURE 11. CONFIGURATION "00" PWM INPUT-TO-OUTPUT POWER STAGE MAPPING
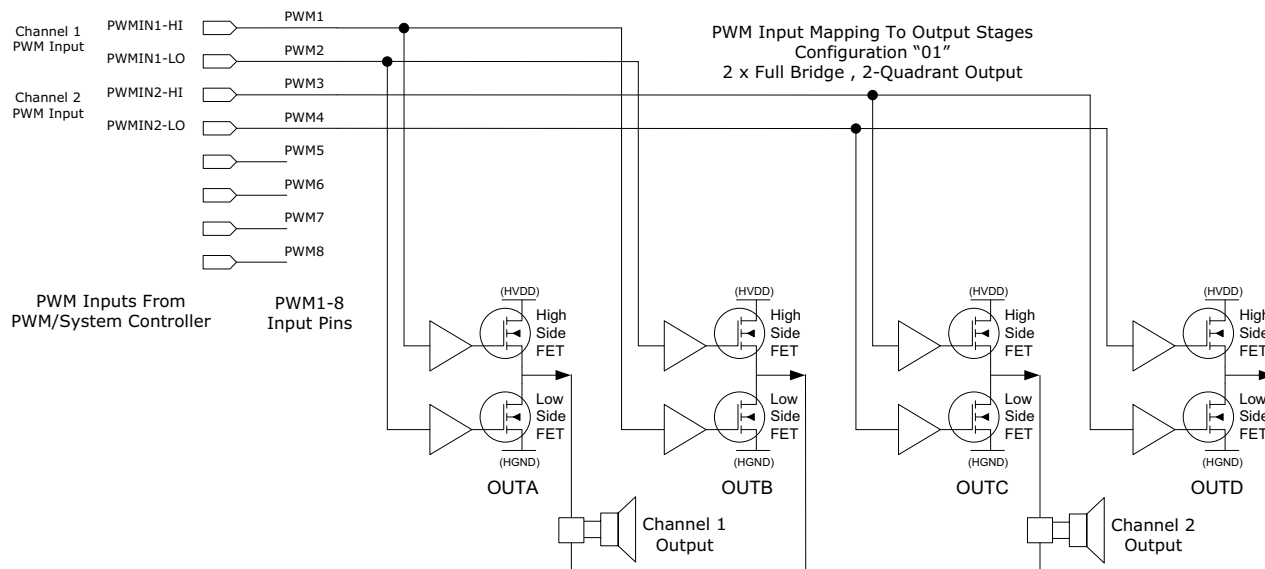
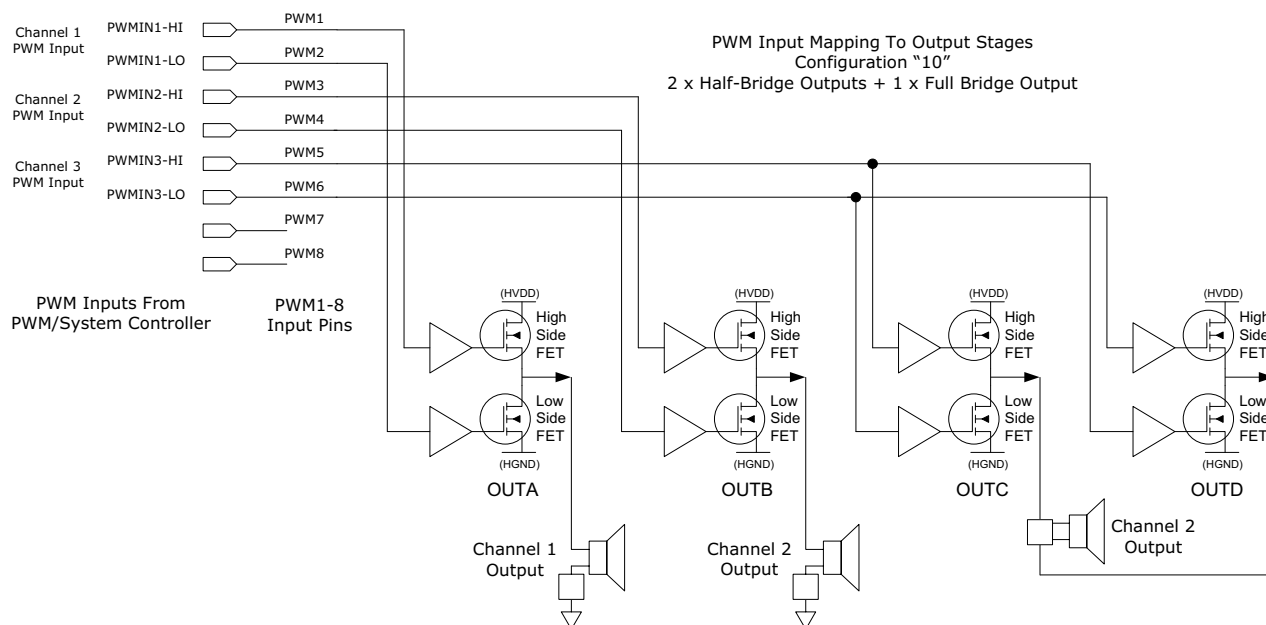FIGURE 12. CONFIGURATION "01" PWM INPUT-TO-OUTPUT POWER STAGE MAPPING

FIGURE 13. CONFIGURATION "10" PWM INPUT-TO-OUTPUT POWER STAGE MAPPING
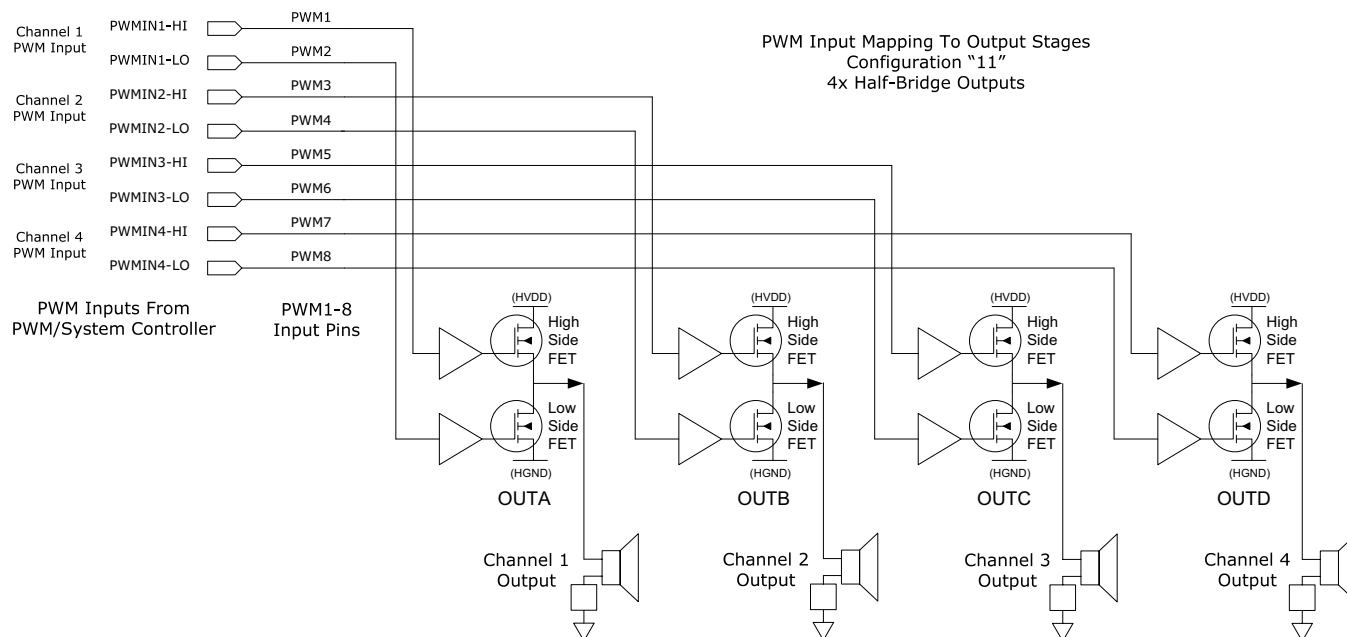
FIGURE 14. CONFIGURATION "11" PWM INPUT-TO-OUTPUT POWER STAGE MAPPING

Typical Application Examples

These examples show functional circuit examples of typical applications using the D2-IPS family device. (Note: These examples are provided to show typical applications only and are not intended to represent complete production-qualified reference designs.)

2-Channel Full Bridge Example

This example (Figure 15) uses configuration mode "01" to provide two full-bridge loudspeaker output channels. The PWM controller provides input into four PWM input pins.

FIGURE 15. 2-CHANNEL FULL BRIDGE EXAMPLE

2.1-Channel Example

This example (Figure 16) uses configuration mode "10" to provide two independent half-bridge loudspeaker output channels, plus one full-bridge loudspeaker output. The PWM controller provides input into all eight PWM input pins.

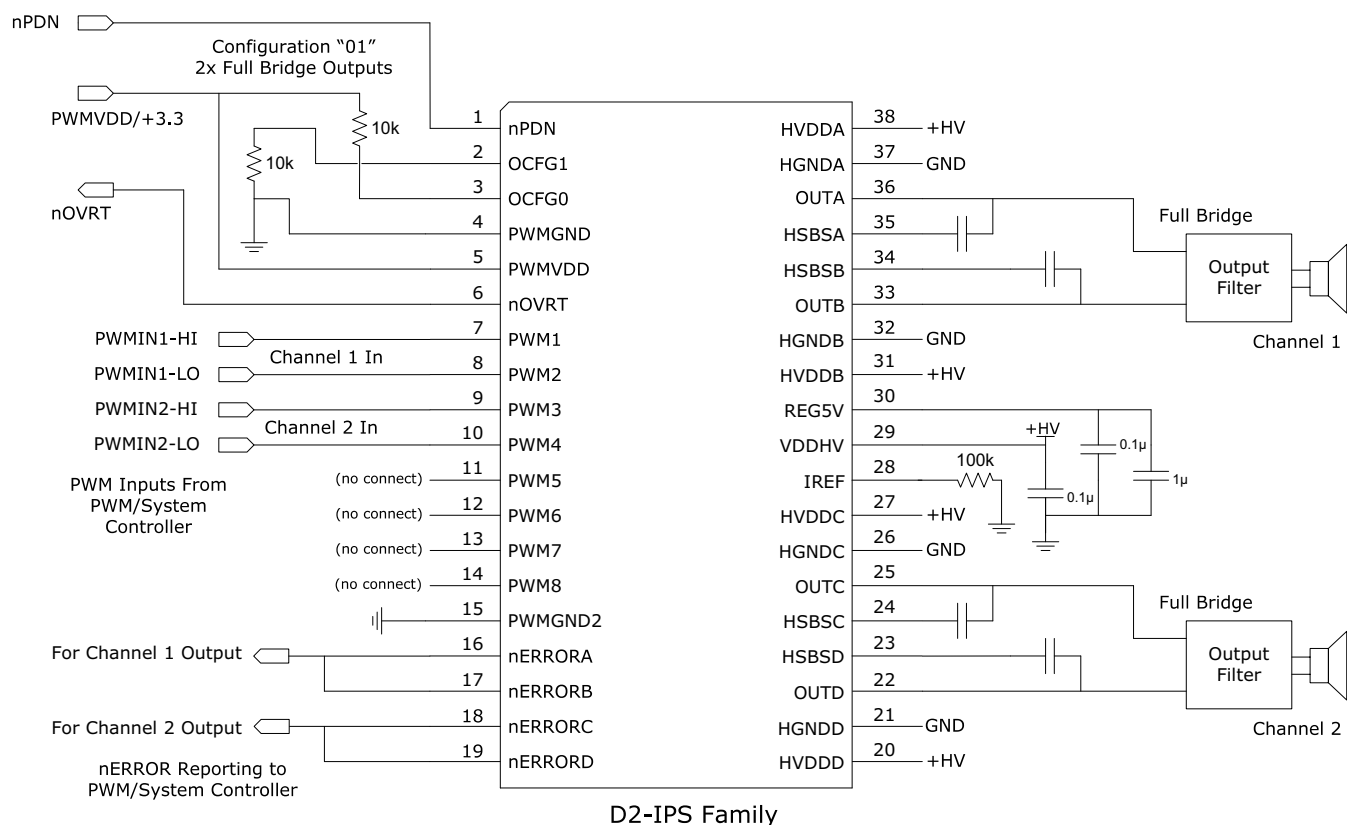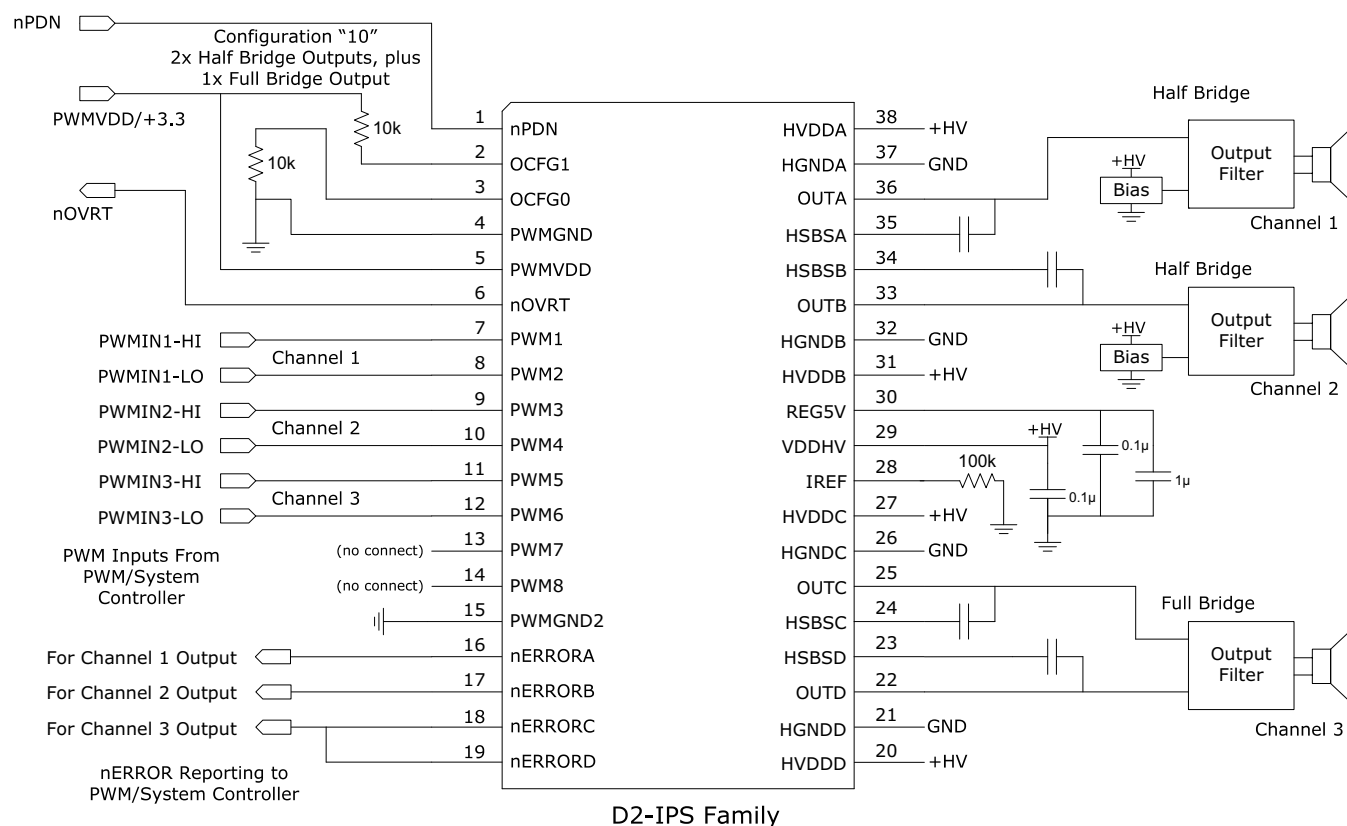FIGURE 16. 2-CHANNEL HALF BRIDGE PLUS 1-CHANNEL FULL BRIDGE EXAMPLE

4-Channel Half-Bridge Example

This example (Figure 17) uses configuration mode "11" to provide four independent half-bridge loudspeaker output channels. The PWM controller provides input into all eight PWM input pins.
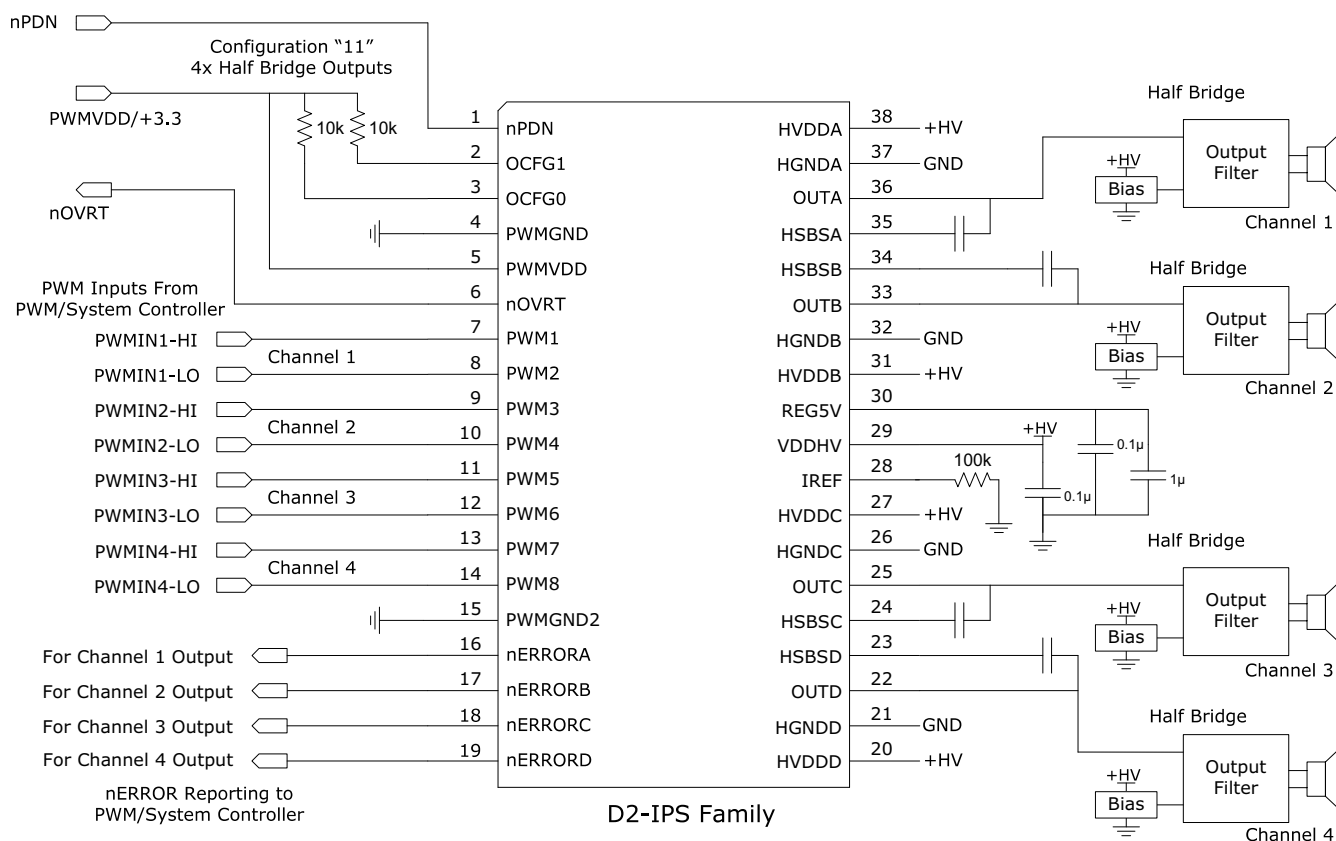
FIGURE 17. 4-CHANNEL HALF BRIDGE EXAMPLE

Revision History
The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Visit our website to make sure you have the latest datasheet revision.

DATE	REVISION	CHANGE
Mar 18, 2019	FN7678.1	Updated title to "D2-IPS Audio SOC". Updated "D2-24044" to "D2 IPS Family". Removed About Intersil section. Updated disclaimer.
Sep 3, 2010	FN7678.0	Initial Release

Package Outline Drawing

M38.173C
38 LEAD HEAT-SINK THIN SHRINK SMALL OUTLINE PLASTIC PACKAGE (HTSSOP)
Rev 0, 4/10

TOP VIEW

PIN 1 ID

B

3 2 1

D

6.4

4.4±0.10

4

38

0.20 C A-B D
2X N/2 TIPS

A

0.17-0.27 ⊕ 0.08 Ⓜ C A-B D 5

END VIEW

0.09-0.20

SEE
DETAIL "A"

EXPOSED PAD VIEW

4.6±0.10

1 2 3

3.20±0.10

SIDE VIEW

0.05 C

1.10 MAX

0.90±0.05

C

0.50

0.10 C

4

9.70±0.10

0.05/0.15

SEATING
PLANE

DETAIL "A"
SCALE: 30/1
(VIEW ROTATED 90°C.W.)

(14°) TYP

(1.00)

0.25

(0-8°)

0.6±0.10

PARTING
LINE

H 3

TYPICAL RECOMMENDED LAND PATTERN

(4.60)

(1.30)

(5.80)

(3.20)

(36X 0.50)

(38X 0.28)

NOTES:

1. Die thickness allowable is 0.279±0.0127 (0.0110±0.0005 inches).
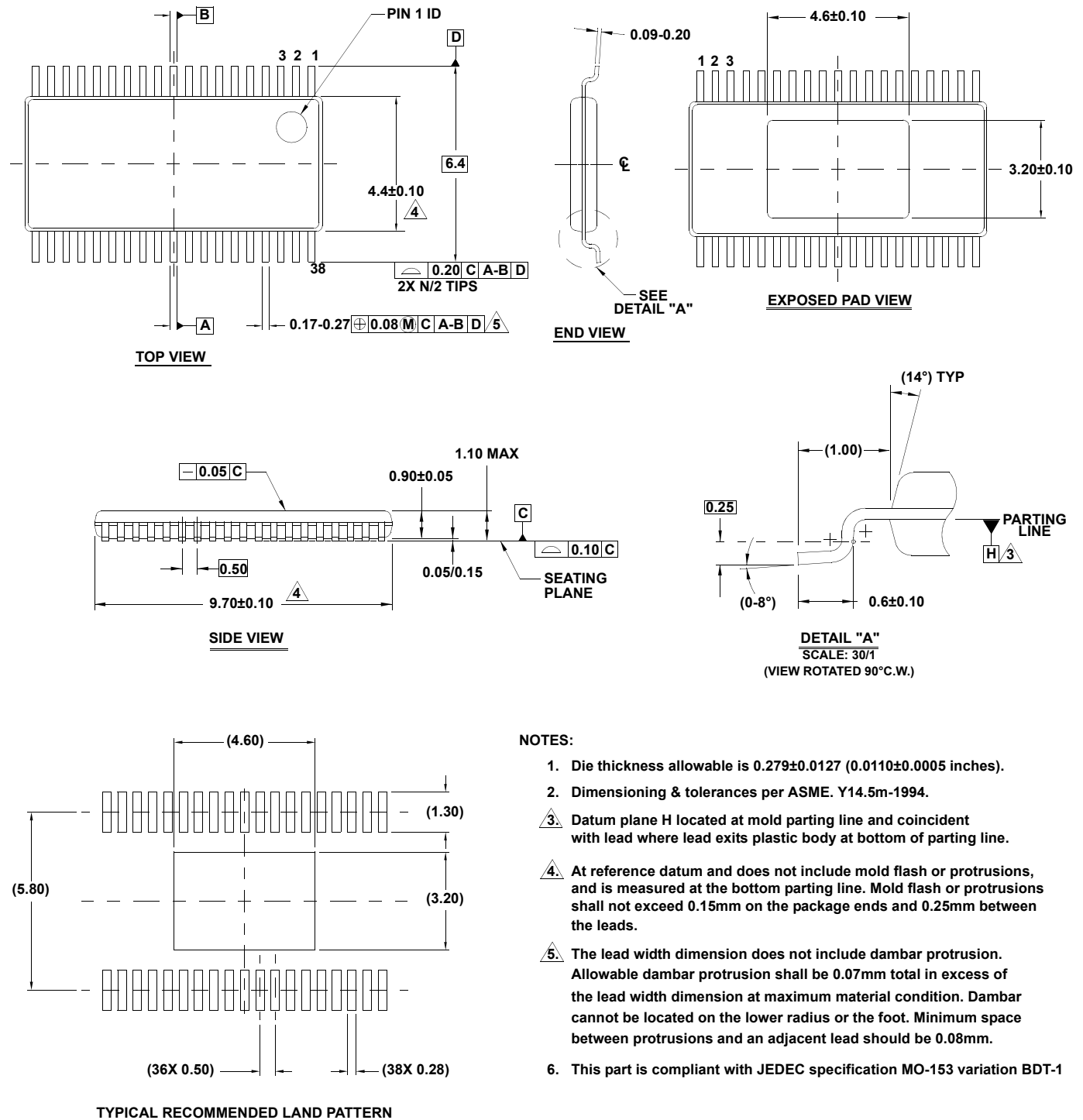
2. Dimensioning & tolerances per ASME. Y14.5m-1994.

3. Datum plane H located at mold parting line and coincident with lead where lead exits plastic body at bottom of parting line.

4. At reference datum and does not include mold flash or protrusions, and is measured at the bottom parting line. Mold flash or protrusions shall not exceed 0.15mm on the package ends and 0.25mm between the leads.

5. The lead width dimension does not include dambar protrusion. Allowable dambar protrusion shall be 0.07mm total in excess of the lead width dimension at maximum material condition. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusions and an adjacent lead should be 0.08mm.

6. This part is compliant with JEDEC specification MO-153 variation BDT-1

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