

# VSC8486

## 10 Gbps XAUI or XGMII to XFI LAN/WAN Transceiver

The VSC8486 is a LAN/WAN XAUI or XGMII transceiver that converts 3 Gbps XAUI data to a 10 Gbps serial stream. At just 750 mW, the VSC8486 is ideal for applications requiring low power. The device is also equipped with an additional full-rate data port that can be utilized for bypass monitoring or channel monitoring applications. The device meets all specifications for 10 gigabit Ethernet (GbE) Layer 1 processing, as defined in IEEE 802.3ae. The VSC8486 offers exceptional 10 Gbps mixed-signal performance with a data output that features programmable pre-emphasis to enable longer traces of copper. The VSC8486 high-speed serial I/O supports 9.9 Gbps, 10.3 Gbps, and 10.5 Gbps, as defined by IEEE 802.3ae and T11 10 GFC, and is fully compliant with the SONET jitter specification defined by Bellcore GR253.

There are four main data processing blocks in the device: XGXS, PCS, WIS, and PMA. The 10 GbE extender sublayer (XGXS) accepts 8b/10b data running at 3.125 Gbps and decodes it for transmission to the physical coding sublayer (PCS). The XGXS is capable of deskewing more than 60 bit times between lanes. The PCS receives data from the XGXS at 10 Gbps and encodes data according to the 64b/66b algorithm described in IEEE 802.3ae clause 49.

The PCS features an optional extended mode (E-PCS) that also runs at the 64b/66b rate. This extended mode uses an alternative framing algorithm that adds forward error correction (FEC) to provide ~2.5 dB of net electrical coding gain. The E-PCS is available for LAN mode but not WAN mode.

The PCS outputs data to the WAN interface sublayer (WIS). (This mode is bypassed in LAN mode.) The WIS optionally takes data from the PCS at 9.953 Gbps and frames data in a SONET STS-192c frame, as described in IEEE 802.3ae clause 50. Additionally, the WIS block contains extended SONET and SDH processing capabilities that allow system operators to leverage valuable performance monitoring data. Finally, data is delivered to the physical media attachment (PMA) block. The PMA multiplexes the internal parallel data bus into a 10 Gbps data stream. The 10 Gbps to XAUI data channel performs the operations described above in reverse. Notable features in this path are a SONET-compliant LOS detector and a 10 Gbps receiver that is fully compliant with XFI specifications, including stressed eye criteria.

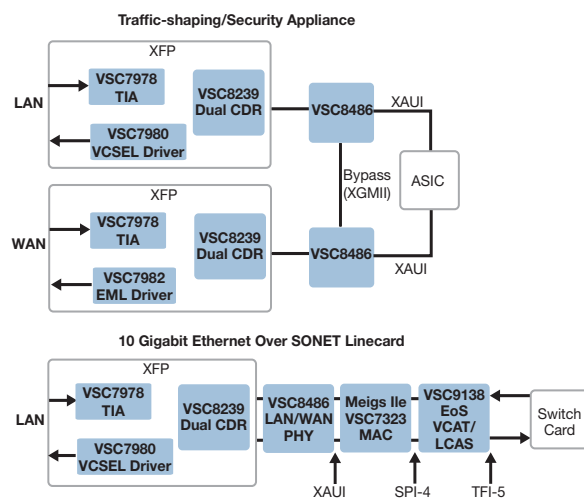
The device operates using a 1.2 V supply dissipating only 700 mW in LAN mode and 750 mW in WAN mode. The VSC8486 is available in standard and lead(Pb)-free (second-level interconnect only) packages, measuring 17 mm × 17 mm with 256 pins and 1.0 mm pin pitch.

### Applications

- 10 Gbps Ethernet LAN/WAN switches, routers, and router to WAN interconnects
- 10 Gbps Ethernet network interface cards
- 10 Gbps fibre channel host bus adapters and switches

### Specifications

- Total power: 750 mW
- Supply voltage: 1.2 V



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### Low Power

- Exceptionally low power (700 mW LAN mode or 750 mW WAN mode) allows for higher port densities

### Wide Range of Support

- Fully compatible with IEEE 802.3ae and T11 10 GFC
- Extended-WIS (E-WIS) provides full Clause 50 support and enables transport over existing SONET networks
- 10 Gbps serial interface exceeds all SONET and 10 GbE requirements
- 4 x 3.125 Gbps and 3.182 Gbps XAUI I/O enable interconnection with a wide range of Layer 2 devices
- Seamless connectivity to XFP and SFP+ modules
- 10 Gbps receiver exceeds all 10 GbE stressed eye requirements

### Tools For Rapid Design

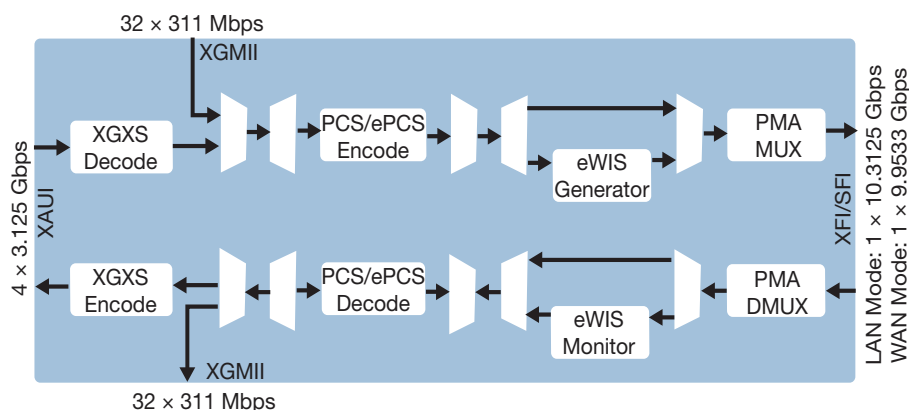
- Multiple loopback modes and built-in self test (BIST) capabilities reduce system development costs, enable manufacturing tests, and improve time to market
- JTAG access port facilitates boundary scan for in-circuit test to improve board yield
- Single 1.2 voltage for the whole chip with optional power supply range (1.2 V, 1.8 V, and 3.3 V) for the TTL interface

### Flexibility

- XAUI I/O programmability for lane swap, invert, amplitude, pre-emphasis, and equalization
- KX4-compatible 3 Gbps I/O for long-reach copper interconnect provides additional margin to traverse connectors and the backplane up to 40 inches
- Extended-PCS (E-PCS) mode with forward error correction (FEC) auto-negotiation allows extended reach over single-mode and multimode fiber with 10–15 error floor
- Enhanced de-emphasis and equalization compensates for connector and channel losses and makes the device SFP+ compatible
- Accessibility of the recovered clock from high-speed input and separate clock paths for CMU and CRU enable Layer 1 support for synchronous Ethernet
- XGMII interface enables the device to be used in a roll-over redundant link application to provide fault tolerance

### Related Products

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