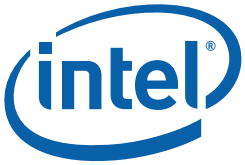

Intel® 965 Express Chipset Family

Datasheet

- For the Intel® 82Q965, 82Q963, 82G965 Graphics and Memory Controller Hub (GMCH) and Intel® 82P965 Memory Controller Hub (MCH)

July 2006

Document Number: 313053-002

Contents

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Revision History

Revision	Description	Date
-001	• Initial Release	June 2006
-002	• Added 82Q965, 82G965, and 82Q963 GMCH components.	July 2006

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Intel® 82Q965, 82Q963, 82G965, 82P965 (G)MCH Features

- Processor/Host Interface (FSB)
  - —Supports a single Intel® Core™2 Duo desktop processor, Intel® Pentium® 4 processor, or Intel® Pentium® D processor.
  - —Supports Pentium 4 processor / Pentium D processor subset of the Extended Mode Scaleable Bus Protocol.
  - —Supports Pentium 4 processor / Pentium D processor FSB interrupt delivery
  - —533/800/1066 MT/s (133/200/266 MHz) FSB
  - —Hyper-Threading Technology (HT Technology)
  - —FSB Dynamic Bus Inversion (DBI)
  - —36-bit host bus addressing
  - —12-deep In-Order Queue
  - —1-deep Defer Queue
  - —GTL+ bus driver with integrated GTL termination resistors
  - —Supports cache Line Size of 64 bytes
- System Memory Interface
  - —One or two channels (each channel consisting of 64 data lines)
  - —Channels are asymmetric, interleaved
  - —DDR2-800/667/533 frequencies
  - —Unbuffered DIMMs only
  - —Supports 256-Mb, 512-Mb, and 1-Gb technologies for x8 and x16 devices
  - —Supports four banks for all DDR2 devices up to 512-Mbit density. Supports eight banks for 1-Gbit DDR2 devices
  - —8 GB maximum memory
- Direct Media Interface (DMI)
  - —Chip-to-chip connection interface to Intel ICH8
  - —2 GB/s point-to-point DMI to ICH8 (1 GB/s each direction)
  - —100 MHz reference clock (shared with PCI Express graphics attach)
  - —32-bit downstream addressing
  - —Messaging and Error Handling
- PCI Express* Interface (82Q965, 82G965, 82P965 (G)MCH only)
  - —One x16 PCI Express port
  - —Compatible with the *PCI Express Base Specification, Revision 1.1a*
  - —Raw bit rate on data pins of 2.5 Gb/s resulting in a real bandwidth per pair of 250 MB/s
- Intel® Active Management Technology (82G965 GMCH only)
  - —Asset Management
  - —OOB diagnostics
  - —Network protection with NOC filters and agent presence
  - —Integrated hardware/software platform solution
- Integrated Graphics Device (82Q965, 82Q963, 82G965 GMCH only)
  - —Core frequency of 400 MHz
  - —1.6 GP/s pixel rate
  - —High-Quality 3D Setup and Render Engine
  - —High-Quality Texture Engine
  - —3D Graphics Rendering Enhancements
  - —2D Graphics
  - —Video Overlay
  - —Multiple Overlay Functionality
- Analog Display (82Q965, 82Q963, 82G965 GMCH only)
  - —400 MHz Integrated 24-bit RAMDAC
  - —Up to 2048x1536 @ 75 Hz refresh
  - —Hardware Color Cursor Support
  - —DDC2B Compliant Interface
- Digital Display (82Q965, 82Q963, 82G965 GMCH only)
  - —SDVO ports in either single/single-combined or dual operation modes supported
  - —270 MHz dot clock on each 12-bit interface
  - —Flat panels up to 2048x1536 @ 60 Hz or digital CRT/HDTV at 1920x1080 @ 85Hz
  - —Dual independent display options with digital display
  - —Multiplexed digital display channels (supported with ADD2 Card).
  - —Supports TMDS transmitters or TV-Out encoders
  - —ADD2/ADD2+ card uses PCI Express graphics x16 connector
  - —Two channels multiplexed with PCI Express* Graphics port
  - —Supports Hot-Plug and Display
  - —Supports TMDS transmitters or TV-out encoders
- Thermal Sensor
  - —Catastrophic Trip Point support
  - —Hot Trip Point support for SMI generation
- Power Management
  - —PC99 suspend to DRAM support (“STR”, mapped to ACPI state S3)
  - —ACPI Revision 1.0 compatible power management
  - —Supports processor states: C0 and C1
  - —Supports System states: S0, S1D, S3, S4, and S5
  - —Supports processor Thermal Management 2 (TM2)
- Package
  - —34 mm × 34 mm. The 1226 balls are located in a non-grid pattern

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1 Introduction

The Intel® Q965/Q963/G965G/P965 Express chipsets are designed for use with the Intel® Core™2 Duo desktop processor, Intel® Pentium® D processor, and Intel® Pentium® 4 processor based platforms. Each chipset contains two components: GMCH (or MCH) for the host bridge and I/O Controller Hub 8 (ICH8) for the I/O subsystem. The 82Q965 GMCH is part of the Q965 Express chipset, 82Q963 GMCH is part of the Q963 Express chipset, 82G965 GMCH is part of the G965 Express chipset, and 82P965 MCH is part of the P965 Express chipset. The ICH8 is the eighth generation I/O Controller Hub and provides a multitude of I/O related functions. The following figures show example system block diagrams for the Q965, Q963, G965, and P965 Express chipsets.

This document is the datasheet for the Intel® 82Q965 Graphics and Memory Controller Hub (GMCH), Intel® 82Q963 Graphics and Memory Controller Hub (GMCH), Intel® 82G965 Graphics and Memory Controller Hub (MCH), and Intel® 82P965 Memory Controller Hub (MCH). Topics covered include; signal description, system memory map, PCI register description, a description of the (G)MCH interfaces and major functional units, electrical characteristics, ballout definitions, and package characteristics.

Note: Unless otherwise specified, the information in this document applies to the Intel® 82Q965 Graphics and Memory Controller Hub (GMCH), Intel® 82Q963 Graphics and Memory Controller Hub (GMCH), Intel® 82G965 Graphics and Memory Controller Hub (GMCH), and Intel® 82P965 Memory Controller Hub (MCH).

Note: The term (G)MCH refers to the 82Q965/82Q963/82G965 GMCH and 82P965 MCH.

Note: Unless otherwise specified, ICH8 refers to the Intel® 82801HB ICH8 and 82801HR ICH8R I/O Controller Hub 8 components.

The primary differences between the 82Q965 GMCH, 82Q963 GMCH, 82G965 GMCH, and 82P965 MCH are:

Capability	Intel® 82Q965	Intel® 82Q963	Intel® 82G965	Intel® 82P965
Memory Speed	DDR2-800/667/533	DDR2-667/533	DDR2-800/667/533	DDR2-800/667/533
Integrated Graphics Device	Yes	Yes	Yes	No
Discrete Graphics	PCI Express x16	None	PCI Express x16	PCI Express x16
PCI Express Interface	Yes (1) x16, (6) x1	No (6) x1	Yes (1) x16, (6) x1	Yes (1) x16, (6) x1
Advanced Media Capabilities	No	No	Yes	No
SDVO Expansion	MEC / ADD2	Add2 only	MEC / ADD2	—
Dual Independent Display	Yes	No	Yes	—
Intel® Active Management Technology (AMT)[2]	Yes[1]	No	No	No
Alerting Standard Format (ASF)	Yes[1]	Yes	No	No

NOTE:

1. For the 82Q965, only one manageability solution can be supported, AMT or ASF.
2. Intel® Active Management Technology requires the platform to have an Intel® AMT-enabled chipset, network hardware and software, connection with a power source and an active LAN port.

Figure 1-1. Intel® Q965/G965 Express Chipset System Block Diagram Example

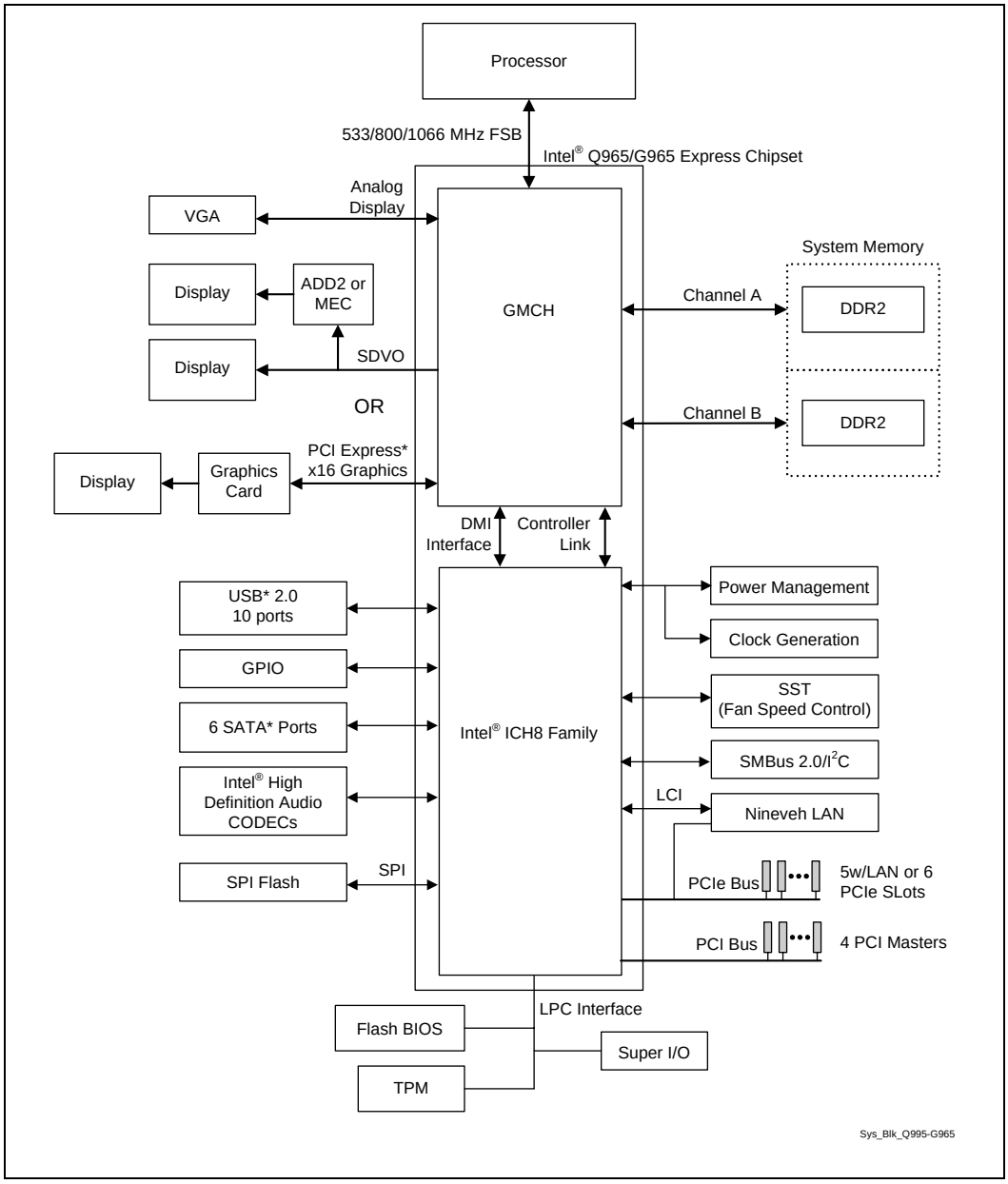


Figure 1-2. Intel® Q963 Express Chipset System Block Diagram Example

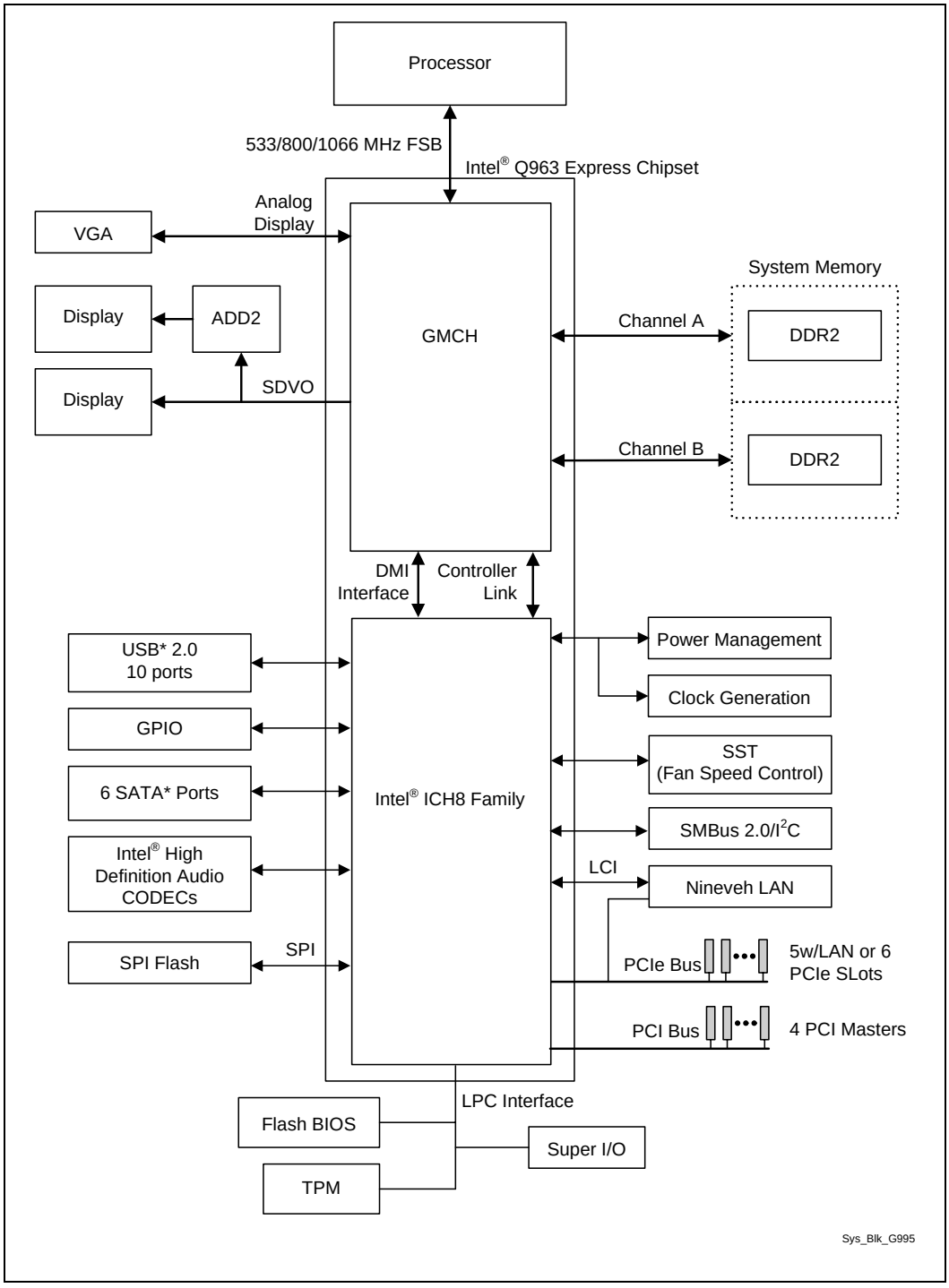
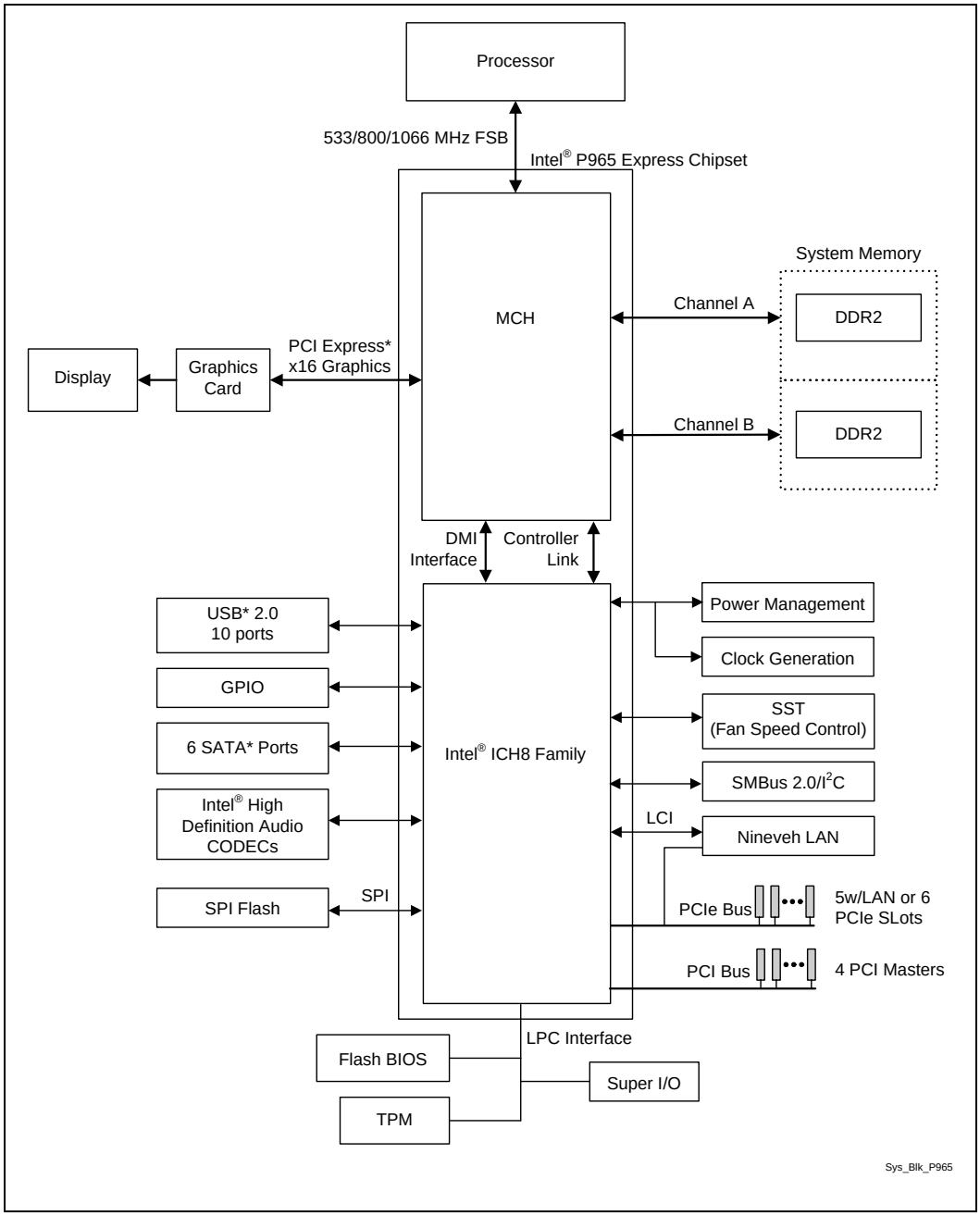


Figure 1-3. Intel® P965 Express Chipset System Block Diagram Example



1.1 Terminology

Term	Description
ADD Card	Advanced Digital Display Card. Provides digital display options for an Intel Graphics Controller that supports ADD cards (have DVOs multiplexed with AGP interface). Keyed like an AGP 4x card and plugs into an AGP connector. Will **not** work with an Intel Graphics Controller that implements Intel® SDVO.
ADD2 Card	Advanced Digital Display Card – **2**nd Generation. Provides digital display options for an Intel graphics controller that supports ADD2 cards. Plugs into an x16 PCI Express* connector but utilizes the multiplexed SDVO interface. Will **not** work with an Intel Graphics Controller that supports Intel® DVO and ADD cards.
Media Expansion Card (MEC)	Media Expansion Card –. Provides digital display options for an Intel Graphics Controller that supports MEC cards. Plugs into an x16 PCI Express connector but utilizes the multiplexed SDVO interface. Adds Video In capabilities to platform. Will **not** work with an Intel Graphics Controller that supports DVO and ADD cards. Will function as an ADD2 card in an ADD2 supported system, but Video In capabilities will not work.
Core	The internal base logic in the (G)MCH
Processor	Refers to the Intel® Core™2 Duo desktop processor, Intel® Pentium® D processor, and Intel® Pentium® 4 processor.
CRT	Cathode Ray Tube
DBI	Dynamic Bus Inversion
DDR2	A second generation Double Data Rate SDRAM memory technology
DMI	(G)MCH-Intel® ICH8 Direct Media Interface
DVI	Digital Video Interface. Specification that defines the connector and interface for digital displays.
FSB	Front Side Bus, synonymous with Host or processor bus
Full Reset	Full reset is when PWROK is de-asserted. Warm reset is when both RSTIN# and PWROK are asserted.
GMCH	Graphics Memory Controller Hub component that contains the processor interface, DRAM controller, internal graphics controller (IGD), and graphics interfaces. It communicates with the I/O controller hub (Intel® ICH8*) over the DMI interconnect and Control interfaces.
(G)MCH	Term used when referring to both GMCH and MCH components.
HDMI	High Definition Multimedia Interface – HDMI supports standard, enhanced, or high-definition video, plus multi-channel digital audio on a single cable. It transmits all ATSC HDTV standards and supports 8-channel digital audio, with bandwidth to spare for future requirements and enhancements (additional details available through http://www.hdmi.org/)
Host	This term is used synonymously with processor
INTx	An interrupt request signal where X stands for interrupts A, B, C and D
IOQ	In Order Queue
Intel® AMT	Intel® Active Management Technology. Second generation system management technology.

Term	Description
Intel® ICH8	Eighth generation I/O Controller Hub component that contains additional functionality compared to previous Intel® ICHs, The Intel® I/O Controller Hub component contains the primary PCI interface, LPC interface, USB2, SATA, and other I/O functions. It communicates with the (G)MCH over a proprietary interconnect called DMI.
IGD	Internal Graphics Device
LCD	Liquid Crystal Display
LVDS	Low Voltage Differential Signaling. A high speed, low power data transmission standard used for display connections to LCD panels.
OOQ	Out of Order Queuing:
MCH	Memory Controller Hub that contains a host interface, DRAM controller, and DMI/Controller interface connections to the ICH8. In this document MCH refers to the 82P965 MCH.
ME	Manageability engine for BTS '06 Intel® AMT
MSI	Message Signaled Interrupt. A transaction initiated outside the host, conveying interrupt information to the receiving agent through the same path that normally carries read and write commands.
PCI Express*	Third Generation Input Output (PCI Express) Graphics Attach called PCI Express Graphics. A high-speed serial interface whose configuration is software compatible with the existing PCI specifications. The specific PCI Express implementation intended for connecting the (G)MCH to an external Graphics Controller is an x16 link and replaces AGP.
Primary PCI	The physical PCI bus that is driven directly by the Intel® ICH8 component. Communication between Primary PCI and the (G)MCH occurs over DMI. Note that the Primary PCI bus is **not** PCI Bus 0 from a configuration standpoint.
SCI	System Control Interrupt. Used in ACPI protocol.
SDVO	Serial Digital Video Out (SDVO). Digital display channel that serially transmits digital display data to an external SDVO device. The SDVO device accepts this serialized format and then translates the data into the appropriate display format (i.e. TMDS, LVDS, and TV-Out). This interface is not electrically compatible with the previous digital display channel - DVO. For the 82Q965, 82G965, the SDVO ports are multiplexed on a portion of the x16 graphics PCI Express interface.
SDVO Device	Third party codec that utilizes SDVO as an input. May have a variety of output formats, including DVI, LVDS, HDMI, TV-out, etc.
SERR	An indication that an unrecoverable error has occurred on an I/O bus.
SMI	System Management Interrupt. Used to indicate any of several system conditions such as thermal sensor events, throttling activated, access to System Management RAM, chassis open, or other system state related activity.
Rank	A unit of DRAM corresponding to eight x8 SDRAM devices in parallel or four x16 SDRAM devices in parallel, ignoring ECC. These devices are usually, but not always, mounted on a single side of a DIMM.
TMDS	Transition Minimized Differential Signaling**.** Signaling interface from Silicon Image that is used in DVI and HDMI.
VCO	Voltage Controlled Oscillator
UMA	Unified Memory Architecture. Describes an IGD using system memory for its frame buffers.

1.2 Reference Documents

Document Name	Location
Intel® 965 Express Chipset Family Specification Update	www.intel.com/design/chipsets/specupdt/313054.htm
Intel® 965 Express Chipset Family Thermal Mechanical Design Guide.	www.intel.com/design/chipsets/designex/313055.htm
Intel® Pentium® D Processor 900 Sequence, Intel® Pentium® Processor Extreme Edition, and Intel® Pentium® 4 Processor Thermal and Mechanical Design Guidelines	http://intel.com/design/pentiumXE/designex/306830.htm
Intel® Core™2 Duo Desktop Processor E6000 Sequence Thermal and Mechanical Design Guidelines	313685
Intel® I/O Controller Hub 8 (ICH8) Family Thermal Mechanical Design Guide.	www.intel.com/design/chipsets/designex/313058.htm
Advanced Configuration and Power Interface Specification, Version 2.0	http://www.acpi.info/
Advanced Configuration and Power Interface Specification, Version 1.0b	http://www.acpi.info/
The PCI Local Bus Specification, Version 2.3	http://www.pcisig.com/specifications
PCI Express Specification, Version 1.1*	http://www.pcisig.com/specifications

1.3 (G)MCH Overview

The (G)MCH is designed for use with the Intel Core™2 Duo desktop processor, Pentium D processor and Pentium 4 processor desktop platforms. The role of a (G)MCH in a system is to manage the flow of information between its four interfaces: the processor interface (FSB), the System Memory interface (DRAM controller), the External Graphics interface (82Q965, 82G965, 82P965 (G)MCH only), and the I/O Controller through the DMI interface. This includes arbitrating between the four interfaces when each initiates transactions. The processor interface supports the Pentium 4 processor subset of the Extended Mode of the Scalable Bus Protocol. The (G)MCH is optimized for the Intel® Pentium® 4 and Pentium D processor family in an LGA775 socket. The (G)MCH supports one or two channels of DDR2 SDRAM. It also supports the PCI Express based external graphics attach (82Q965, 82Q963), 82G965 GMCH only). The Q965/Q963/G965/P965 express chipset platforms support the eighth generation I/O Controller Hub (Intel ICH8) to provide a multitude of I/O related features.

1.3.1 Host Interface

The (G)MCH can use a single LGA775 socket processor. The (G)MCH supports a FSB frequency of 533/800/1066 MHz using a scalable FSB Vcc_CPU. It supports 36-bit host addressing, decoding up to 8 GB of the processor's memory address space. Host-initiated I/O cycles are decoded to PCI Express (82Q965, 82G965, 82P965 (G)MCH only), DMI, or the (G)MCH configuration space. Host-initiated memory cycles are decoded to PCI Express, DMI or system memory. PCI Express device accesses (82Q965, 82G965, 82P965 (G)MCH only) to non-cacheable system memory are not snooped on the host bus. Memory accesses initiated from PCI Express using PCI semantics and from DMI to system SDRAM will be snooped on the host bus.

Capabilities of the Processor/Host Interface (FSB) interface include:

- Supports a single the Intel Core™2 Duo desktop processor, Pentium D processor and Pentium 4 processor. Processors supported include: Intel® Pentium® D processor 900 sequence, Intel® Pentium® processor Extreme Edition 965, 955, Intel® Pentium® 4 processor 6x1 sequence in an LGA775 package.
- Supports the Pentium 4 and Pentium D processor subset of the Extended Mode Scaleable Bus Protocol. The primary enhancements over the Compatible Mode P6 bus protocol are:
  - Source synchronous double-pumped (2x) Address
  - Source synchronous quad-pumped (4x) Data
- Supports Pentium 4 processor and Pentium D processor FSB interrupt delivery
- Supports Pentium 4 processor and Pentium D processor Front Side Bus (FSB) at the following frequency ranges:
  - 533 MT/s (133 MHz)
  - 800 MT/s (200 MHz)
  - 1066 MT/s (266 MHz)
- Supports Hyper-Threading Technology (HT Technology)
- Supports FSB Dynamic Bus Inversion (DBI)
- Supports 36-bit host bus addressing, allowing the processor to access the entire 64 GB of the (G)MCH's memory address space
- Has a 12-deep In-Order Queue to support up to twelve outstanding pipelined address requests on the host bus
- Has a 1-deep Defer Queue
- Uses GTL+ bus driver with integrated GTL termination resistors
- Supports a Cache Line Size of 64 bytes

1.3.2 System Memory Interface

The (G)MCH integrates a system memory DDR2 controller with two, 64-bit wide interfaces.
Only Double Data Rate (DDR2) memory is supported; consequently, the buffers support only SSTL_1.8 V signal interfaces. The memory controller interface is fully configurable through a set of control registers.

Capabilities of the system memory interface include:

- Enhanced scheduling and out of order accesses using Intel® Fast Memory Access
- The (G)MCH System Memory Controller directly supports one or two channels of memory (each channel consisting of 64 data lines)
  - The memory channels are asymmetric: "Flex Memory" channels are assigned addresses serially. Channel B addresses are assigned after all Channel A addresses
  - The memory channels are interleaved: Addresses are bounced between the channels after each cache line (64-B boundary)
- Supports DDR2 memory DIMM frequencies of 533, 667 and 800 MHz. The speed used in all channels is the speed of the slowest DIMM in the system
- I/O Voltage of 1.8 V for DDR2
- Supports only unbuffered DIMMs
- Supports maximum memory bandwidth of 6.4 GB/s in single-channel or dual-channel asymmetric mode, or 12.8 GB/s in dual-channel interleaved mode assuming DDR2 800MHz
- Supports 256-Mb, 512-Mb, and 1-Gb technologies for x8 and x16 devices (DDR2 800MHz 1Gb technology not supported)
- Supports four banks for all DDR2 devices up to 512-Mbit density. Supports eight banks for 1-Gbit DDR2 devices
- Using 256 Mb technologies, the smallest memory capacity possible is 128 MB, assuming Single-Channel Mode. (8 K rows * 512 columns * 1 cell/(row * column) * 16 b/cell * 4 banks/devices * 4 devices/DIMM-side * 1 DIMM-side/channel * 1 channel * 1 B/8 b * 1 M/1024 K = 128 MB)
- By using 1 Gb technology (DDR2 800MHz 1 Gb technology is not supported) in Dual Channel Interleaved Mode, the largest memory capacity possible is 8 GB. (16 K rows * 1 K columns * 1 cell/(row * column) * 8 b/cell * 8 banks/device * 8 devices/DIMM-side * 4 DIMM-sides/channel * 2 channels * 1 B/8 b * 1 G/1024 M * 1 M/(K*K) = 8 GB)
- Maximum DRAM address decode space is 8 GB (assuming 36-bit addressing)
- Supports up to 32 simultaneous open pages per channel (assuming 4 ranks of 8 bank devices)
- Supports opportunistic refresh scheme
- Supports Partial Writes to memory using Data Mask (DM) signals
- Supports page sizes of 4 KB, 8 KB and 16 KB
- Supports a burst length of 8 for single-channel and dual-channel interleaved and asymmetric operating modes
- Improved flexible memory architecture

1.3.3 Direct Media Interface (DMI)

Direct Media Interface (DMI) is the chip-to-chip connection between the (G)MCH and ICH8. This high-speed interface integrates advanced priority-based servicing allowing for concurrent traffic and true isochronous transfer capabilities. Base functionality is completely software transparent permitting current and legacy software to operate normally.

To provide for true isochronous transfers and configurable Quality of Service (QoS) transactions, the ICH8 supports two virtual channels on DMI: VC0 and VC1. These two channels provide a fixed arbitration scheme where VC1 is always the highest priority. VC0 is the default conduit of traffic for DMI and is always enabled. VC1 must be specifically enabled and configured at both ends of the DMI link (i.e., the ICH8 and (G)MCH).

- A chip-to-chip connection interface to Intel ICH8
- 2 GB/s point-to-point DMI to ICH8 (1 GB/s each direction)
- 100 MHz reference clock (shared with PCI Express Graphics Attach)
- 32-bit downstream addressing
- APIC and MSI interrupt messaging support. Will send Intel-defined "End Of Interrupt" broadcast message when initiated by the processor.
- Message Signaled Interrupt (MSI) messages
- SMI, SCI and SERR error indication
- Legacy support for ISA regime protocol (PHOLD/PHOLDA) required for parallel port DMA, floppy drive, and LPC bus masters

1.3.4 PCI Express* Interface (Intel® 82Q965, 82G965, 82P965 (G)MCH Only)

The (G)MCH contains one 16-lane (x16) PCI Express port intended for an external PCI Express graphics card. The PCI Express port is compliant to the *PCI Express* Base Specification* revision 1.1. The x16 port operates at a frequency of 2.5 Gb/s on each lane while employing 8b/10b encoding; the port supports a maximum theoretical bandwidth of 40 Gb/s in each direction. The 82Q965 and 82G965 GMCHs multiplex the PCI Express interface with the Intel® SDVO ports.

- One, 16-lane PCI Express port intended for graphics attach, compatible to the PCI Express* Base Specification revision 1.1a.
- PCI Express frequency of 1.25 GHz resulting in 2.5 Gb/s each direction
- Raw bit-rate on the data pins of 2.5 Gb/s, resulting in a real bandwidth per pair of 250 MB/s given the 8b/10b encoding used to transmit data across this interface
- Maximum theoretical realized bandwidth on the interface of 4 GB/s in each direction simultaneously, for an aggregate of 8 GB/s when x16.
- PCI Express* Graphics Extended Configuration Space. The first 256 bytes of configuration space alias directly to the PCI Compatibility configuration space. The remaining portion of the fixed 4-KB block of memory-mapped space above that (starting at 100h) is known as extended configuration space.

- PCI Express Enhanced Addressing Mechanism. Accessing the device configuration space in a flat memory mapped fashion.
- Automatic discovery, negotiation, and training of link out of reset
- Supports traditional PCI style traffic (asynchronous snooped, PCI ordering)
- Supports traditional AGP style traffic (asynchronous non-snooped, PCI Express-relaxed ordering)
- Hierarchical PCI-compliant configuration mechanism for downstream devices (i.e., normal PCI 2.3 Configuration space as a PCI-to-PCI bridge)
- Supports "static" lane numbering reversal. This method of lane reversal is controlled by a Hardware Reset strap, and reverses both the receivers and transmitters for all lanes (e.g., TX[15]->TX[0], RX[15]->RX[0]). This method is transparent to all external devices and is different than lane reversal as defined in the PCI Express Specification. In particular, link initialization is not affected by static lane reversal.

1.3.5 Intel® Active Management Technology (Intel® AMT) (Intel® 82Q965 GMCH Only)

Intel® AMT combines highly-available OOB remote management and network protection into an OS-independent and tamper-resistant solution to help address company IT department top issues of network protection, asset management, and system reliability.

- Hardware and software asset management
- Provide OOB diagnostics
- Network protection with NOC filters and agent presence
- Integrated hardware and software platform solution

Intel® AMT integrates advanced manageability features into hardware and firmware. Intel AMT extends the capabilities of existing management solutions by enabling system and S/W asset information, remote diagnostics, recovery and network protection through the OOB (Out-Of-Band) channel (i.e., it is available even when the system is in a low-power "off" state or the operating system is hung).

Intel® Active Management Technology is only supported by the Q965 Express chipset.

1.3.6 Alerting Standard Format (ASF) (Intel® 82Q965 and 82Q963 GMCH Only)

ASF is a specification that Intel and IBM developed jointly back in 1997 and updated in 1999. Alerting Standard Format (ASF) provides alerting capabilities (no event log - history must be stored on server) to notify IT of system problems over the network. ASF provides basic power-up/power-down capabilities.

An ASF design contains several required components (a list of components is provided later in this section), and Intel provides some (but not all) of them. Each OEM must (1) decide what features to support and what devices are required, (2) ensure that these devices meet the ASF specification, and (3) acquire/develop any software/hardware not provided by Intel.

ASF can be supported by the Q965 Q963 Express chipsets. For Q965 Express chipset platforms, only one manageability solution can be supported.

1.3.7 Graphics Features (Intel® 82Q965, 82Q963, 82G965 GMCH)

The GMCH provides an integrated graphics device (IGD) delivering cost competitive 3D, 2D and video capabilities. The GMCH contains an extensive set of instructions for 3D operations, 2D operations, motion compensation, overlay, and display control. The GMCH's video engines support video conferencing and other video applications. The GMCH uses a UMA configuration with up to 256 MB of DVMT for graphics memory. The GMCH also has the capability to support external graphics accelerators via the PCI Express* Graphics (PEG) port but cannot work concurrently with the integrated graphics device. High bandwidth access to data is provided through the system memory port.

1.3.8 SDVO and Analog Display Features (Intel® 82Q965, 82Q963, 82G965 GMCH Only)

The GMCH provides interfaces to a progressive scan analog monitor and two SDVO ports (multiplexed with PCI Express x16 graphics port signals on the 82Q965 and 82G965 GMCH) capable of driving an Advanced Digital Display (ADD2) card or Media Expansion card (82Q965 and 82G965 GMCH only). The digital display channels are capable of driving a variety of SDVO devices (e.g., TMDS, TV-Out). Note that SDVO only works with the Integrated Graphics Device (IGD). The Media Expansion card adds Video-in capabilities. The GMCH provides two multiplexed SDVO ports that are capable of driving up to a 270 MHz pixel clock each. When combined with a DVI compliant external device and connector, the GMCH has a high-speed interface to a digital display (e.g., flat panel or digital CRT).

The GMCH SDVO ports can each support a single-channel SDVO device. If both ports are active in single-channel mode, they can have different display timing and data. The GMCH is compliant with DVI Specification 1.0. Capabilities of the SDVO and Analog Display interfaces include:

- SDVO Support
  - SDVO ports in either single/single-combined or dual operation modes supported
  - 3x3 Built In full panel scalar
  - 180 degree Hardware screen rotation
  - Multiplexed Digital Display Channels (Supported with ADD2 Card)
  - Two channels multiplexed with PCI Express* Graphics port
  - 270 MHz dot clock on each 12-bit interface
  - Supports flat panels up to 2048x1536 @ 60 Hz or digital CRT/HDTV at 1920x1080 @ 85 Hz
  - Supports Hot-Plug and Display
  - Supports TMDS transmitters or TV-out encoders
  - ADD2/Media Expansion card use PCI Express Graphics x16 connector
- Analog Display Support
  - 400 MHz Integrated 24-bit RAMDAC
  - Up to 2048x1536 @ 75 Hz refresh
  - Hardware Color Cursor Support
  - DDC2B Compliant Interface
- Dual Independent Display options with digital display

1.3.9 (G)MCH Clocking

- Differential Host clock of 133/200/266 MHz (HCLKP/HCLKN). These clock frequencies support transfer rates of 533/800/1066 MT/s. The Host PLL generates 2x, 4x, and 8x versions of the host clock for internal optimizations.
- Chipset core clock synchronized to host clock
- Internal and external memory clocks of 266 MHz, 333 MHz, and 400 MHz generated from one of two (G)MCH PLLs that use the host clock as a reference. This includes 2x and 4x for internal optimizations.
- The PCI Express* PLL of 100 MHz. This serial reference clock (GCLKP/GCLKN) generates the PCI Express core clock of 250 MHz (82Q965, 82G965, 82P965 (G)MCH only).
- Display timings are generated from display PLLs that use a 96 MHz differential non-spread spectrum clock as a reference. Display PLLs can also use the SDVO_TVCLKIN[+/-] from an SDVO device as a reference. (82Q965, 82Q963, 82G965 GMCH Only)
- All of the above clocks are capable of tolerating Spread Spectrum clocking as defined in the Clock Generator specification.
- Host, Memory, and PCI Express Graphics PLLs, and all associated internal clocks are disabled until PWROK is asserted.

1.3.10 Thermal Sensor

The (G)MCH Thermal Sensor support includes:

- Catastrophic Trip Point support for emergency clock gating for the (G)MCH at 118 °C
- Hot Trip Point support for SMI generation between 85 °C and 105 °C

1.3.11 Power Management

(G)MCH Power Management support includes:

- PC99 suspend to DRAM support (“STR”, mapped to ACPI state S3)
- SMRAM space remapping to A0000h (128 KB)
- Supports extended SMRAM space above 256 MB, additional 1-MB TSEG from the Base of graphics stolen memory (BSM) when enabled, and cacheable (cacheability controlled by processor)
- ACPI Rev 1.0 compatible power management
- Supports processor states: C0 and C1
- Supports System states: S0, S1D, S3, S4, and S5
- Supports processor Thermal Management 2 (TM2)

§

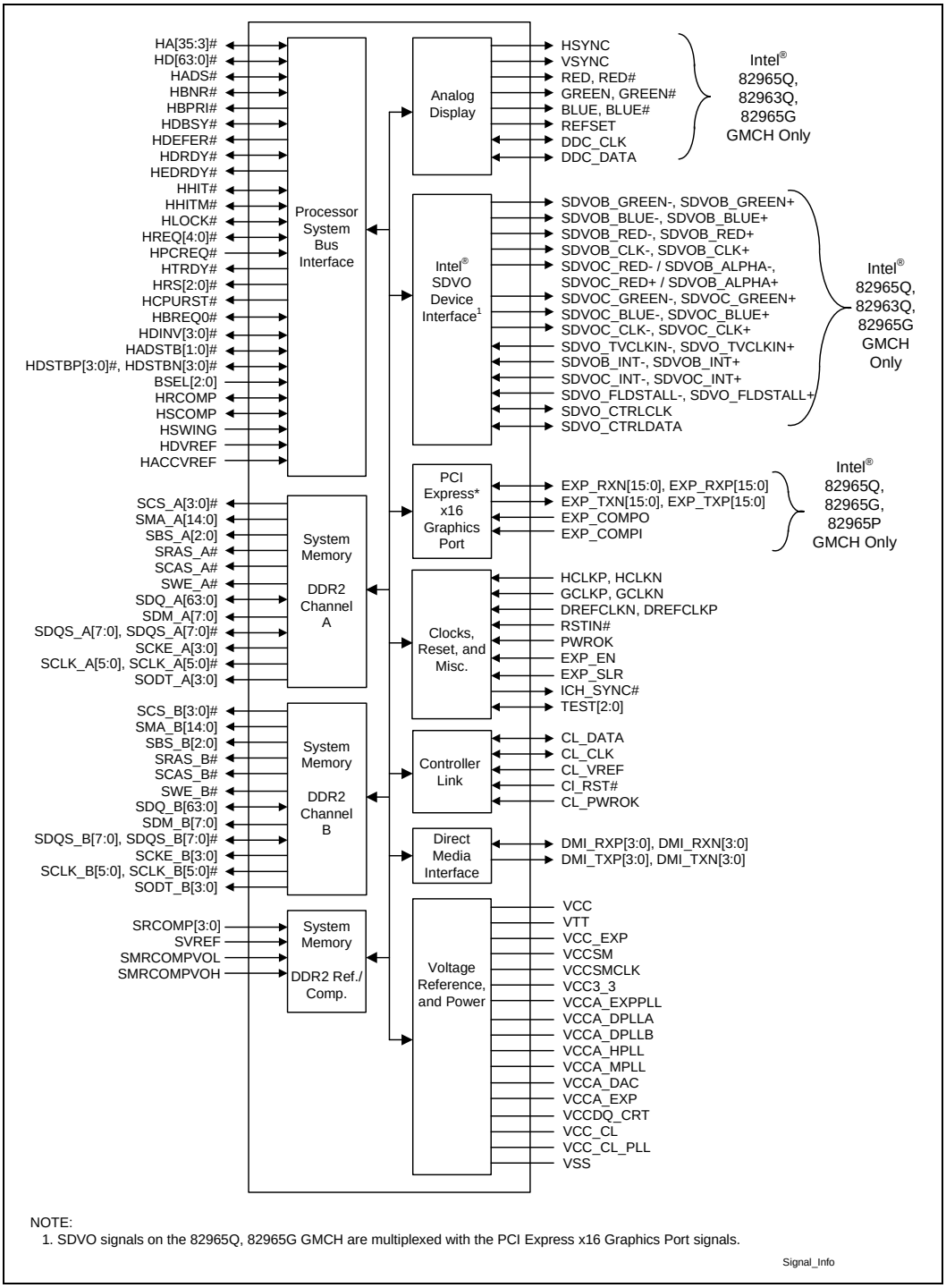
2 Signal Description

This section provides a detailed description of (G)MCH signals. The signals are arranged in functional groups according to their associated interface (see Figure 2-1). Table 2-1 lists the notations used to describe the signal type.

Table 2-1. Signal Terminology

Term	Description
PCI Express*	**PCI-Express interface signals.** These signals are compatible with PCI Express 1.1 Signaling Environment AC Specifications and are AC coupled. The buffers are not 3.3 V tolerant. Differential voltage spec = (|D+ - D-|) * 2 = 1.2Vmax. Single-ended maximum = 1.25 V. Single-ended minimum = 0 V.
DMI	**Direct Media Interface signals.** These signals are compatible with PCI Express 1.0 Signaling Environment AC Specifications, but are DC coupled. The buffers are not 3.3 V tolerant. Differential voltage spec = (|D+ - D-|) * 2 = 1.2Vmax. Single-ended maximum = 1.25 V. Single-ended minimum = 0 V.
CMOS	**CMOS buffers.** 1.5 V tolerant.
COD	**CMOS Open Drain buffers.** 3.3 V tolerant.
HCSL	**Host Clock Signal Level buffers.** Current mode differential pair. Differential typical swing = (|D+ - D-|) * 2 = 1.4V. Single ended input tolerant from -0.35 V to 1.2 V. Typical crossing voltage 0.35 V.
HVCMOS	**High Voltage CMOS buffers.** 3.3 V tolerant.
HVIN	**High Voltage CMOS input-only buffers.** 3.3 V tolerant.
SSTL-1.8	**Stub Series Termination Logic.** These are 1.8 V output capable buffers. 1.8 V tolerant.
A	**Analog reference or output.** May be used as a threshold voltage or for buffer compensation.
GTL+	**Gunning Transceiver Logic signaling technology.** Implements a voltage level as defined by VTT of 1.2 V.

Figure 2-1. Signal Information Diagram



NOTE:
1. SDVO signals on the 82965Q, 82965G GMCH are multiplexed with the PCI Express x16 Graphics Port signals.

Signal_Info

2.1 Host Interface Signals

Note: Unless otherwise noted, the voltage level for all signals in this interface is tied to the termination voltage of the Host Bus (V_{TT}).

Signal Name	Type	Description
HADS#	I/O GTL+	**Address Strobe:** The processor bus owner asserts HADS# to indicate the first of two cycles of a request phase. The (G)MCH can assert this signal for snoop cycles and interrupt messages.
HBNR#	I/O GTL+	**Block Next Request:** This signal is used to block the current request bus owner from issuing new requests. This signal is used to dynamically control the processor bus pipeline depth.
HBPRI#	O GTL+	**Priority Agent Bus Request:** The (G)MCH is the only Priority Agent on the processor bus. It asserts this signal to obtain the ownership of the address bus. This signal has priority over symmetric bus requests and will cause the current symmetric owner to stop issuing new transactions unless the HLOCK# signal was asserted.
HBREQ0#	I/O GTL+	**Bus Request 0:** The (G)MCH pulls the processor's bus HBREQ0# signal low during HCPURST#. The processor samples this signal on the active-to-inactive transition of HCPURST#. The minimum setup time for this signal is 4 HCLKs. The minimum hold time is 2 HCLKs and the maximum hold time is 20 HCLKs. HBREQ0# should be tri-stated after the hold time requirement has been satisfied.
HCPURST#	O GTL+	**CPU Reset:** The HCPURST# pin is an output from the (G)MCH. The (G)MCH asserts HCPURST# while RSTIN# is asserted and for approximately 1 ms after RSTIN# is de-asserted. The HCPURST# allows the processors to begin execution in a known state. Note that the Intel® ICH8 must provide processor frequency select strap setup and hold times around HCPURST#. This requires strict synchronization between (G)MCH HCPURST# de-assertion and the ICH8 driving the straps.
HDBSY#	I/O GTL+	**Data Bus Busy:** This signal is used by the data bus owner to hold the data bus for transfers requiring more than one cycle.
HDEFER#	O GTL+	**Defer:** This signal indicates that the (G)MCH will terminate the transaction currently being snooped with either a deferred response or with a retry response.

Signal Name	Type	Description
HDINV[3:0]#	I/O GTL+	**Dynamic Bus Inversion:** These signals are driven along with the HD[63:0]# signals. They indicate if the associated signals are inverted. HDINV[3:0]# are asserted such that the number of data bits driven electrically low (low voltage) within the corresponding 16 bit group never exceeds 8. **HDINVx# — Data Bits** HDINV3# — HD[63:48]# HDINV2# — HD[47:32]# HDINV1# — HD[31:16]# HDINV0# — HD[15:0]#
HA[35:3]#	I/O GTL+	**Host Address Bus:** HA[35:3]# connect to the processor address bus. During processor cycles, the HA[35:3]# are inputs. The (G)MCH drives HA[35:3]# during snoop cycles on behalf of DMI and PCI Express* Graphics initiators. HA[35:3]# are transferred at 2x rate.
HADSTB[1:0]#	I/O GTL+	**Host Address Strobe:** HADSTB[1:0]# are source synchronous strobes used to transfer HA[35:3]# and HREQ[4:0] at the 2x transfer rate.
HD[63:0]#	I/O GTL+	**Host Data:** These signals are connected to the processor data bus. Data on HD[63:0] are transferred at 4x rate. Note that the data signals may be inverted on the processor bus, depending on the HDINV[3:0]# signals.
HDSTBP[3:0]# HDSTBN[3:0]#	I/O GTL+	**Differential Host Data Strobes:** These signals are differential source synchronous strobes used to transfer HD[63:0]# and HDINV[3:0]# at 4x transfer rate. These signals are not level sensitive. Data is captured on the falling edge of both strobes. Hence, they are pseudo-differential, and not true differential. **Strobes — Bits — Data** HDSTBP3#, HDSTBN3# — HDINV3# — HD[63:48]# HDSTBP2#, HDSTBN2# — HDINV2# — HD[47:32]# HDSTBP1#, HDSTBN1# — HDINV1# — HD[31:16]# HDSTBP0#, HDSTBN0# — HDINV0# — HD[15:0]#
HHIT#	I/O GTL+	**Hit:** This signal indicates that a caching agent holds an unmodified version of the requested line. This signal is also driven in conjunction with HHITM# by the target to extend the snoop window.
HHITM#	I/O GTL+	**Hit Modified:** This signal indicates that a caching agent holds a modified version of the requested line and that this agent assumes responsibility for providing the line. This signal is also driven in conjunction with HHIT# to extend the snoop window.
HLOCK#	I/O GTL+	**Host Lock:** All processor bus cycles sampled with the assertion of HLOCK# and HADS#, until the negation of HLOCK#, must be atomic (i.e., no DMI or PCI Express* Graphics accesses to system memory are allowed when HLOCK# is asserted by the processor).

Signal Name	Type	Description
HREQ[4:0]#	I/O GTL+	**Host Request Command:** These signals define the attributes of the request. HREQ[4:0]# are transferred at 2x rate. They are Asserted by the requesting agent during both halves of Request Phase. In the first half, the signals define the transaction type to a level of detail that is sufficient to begin a snoop request. In the second half, the signals carry additional information to define the complete transaction type.
HTRDY#	O GTL+	**Host Target Ready:** This signal indicates that the target of the processor transaction is able to enter the data transfer phase.
HRS[2:0]#	O GTL+	**Response Signals:** These signals indicate the type of response according to the following: 000 Idle state 001 Retry response 010 Deferred response 011 Reserved (not driven by (G)MCH) 100 Hard Failure (not driven by (G)MCH) 101 No data response 110 Implicit Writeback 111 Normal data response
BSEL[2:0]	I CMOS	**Bus Speed Select:** At the de-assertion of RSTIN#, the value sampled on these signals determine the expected frequency of the bus.
HRCOMP	I/O CMOS	**Host RCOMP:** This signal is used to calibrate the Host GTL+ I/O buffers. This signal is powered by the Host Interface termination rail (V_{TT}).
HSCOMP	I/O CMOS	**Slew Rate Compensation:** This signal is used for compensation for the Host Interface.
HSCOMP#	I/O A	**Slew Rate Compensation:** This signal is used for compensation for the Host Interface for falling edges.
HSWING	I A	**Host Voltage Swing:** This signal provides the reference voltage used by FSB RCOMP circuits. HSWING is used for the signals handled by HRCOMP.
HDVREF	I A	**Host Reference Voltage:** This signal is the voltage input for the data signals of the Host GTL interface.
HACCVREF	I A	**Host Reference Voltage:** This signal is used the voltage input for the Address signals of the Host GTL interface.

2.2 DDR2 DRAM Channel A Interface

Signal Name	Type	Description
SCLK_A[5:0]	O SSTL-1.8	**SDRAM Differential Clock:** (3 per DIMM). SCLK_Ax and its complement, SCLK_Ax# make a differential clock pair output. The crossing of the positive edge of SCLK_Ax and the negative edge of its complement SCLK_Ax# are used to sample the command and control signals on the SDRAM.
SCLK_A[5:0]#	O SSTL-1.8	**SDRAM Complementary Differential Clock:** (3 per DIMM). These are the complementary differential DDR2 clock signals.
SCS_A[3:0]#	O SSTL-1.8	**Chip Select:** (1 per Rank) These signals select particular SDRAM components during the active state. There is one chip select for each SDRAM rank.
SMA_A[14:0]	O SSTL-1.8	**Memory Address:** These signals are used to provide the multiplexed row and column address to the SDRAM.
SBS_A[2:0]	O SSTL-1.8	**Bank Select:** These signals define which banks are selected within each SDRAM rank. DDR2: 1-Gb technology uses 8 banks.
SRAS_A#	O SSTL-1.8	**Row Address Strobe:** This signal is used with SCAS_A# and SWE_A# (along with SCS_Ax#) to define the SDRAM commands.
SCAS_A#	O SSTL-1.8	**Column Address Strobe:** This signal is used with SRAS_A# and SWE_A# (along with SCS_Ax#) to define the SDRAM commands.
SWE_A#	O SSTL-1.8	**Write Enable:** This signal is used with SCAS_A# and SRAS_A# (along with SCS_Ax#) to define the SDRAM commands.
SDQ_A[63:0]	I/O SSTL-1.8	**Data Lines:** SDQ_Ax signals interface to the SDRAM data bus.
SDM_A[7:0]	O SSTL-1.8	**Data Mask:** When activated during writes, the corresponding data groups in the SDRAM are masked. There is one SDM_Ax bit for every data byte lane.
SDQS_A[7:0]	I/O SSTL-1.8	**Data Strobes:** For DDR2, SDQS_Ax, and its complement SDQS_Ax# make up a differential strobe pair. The data is captured at the crossing point of SDQS_Ax and its complement SDQS_Ax# during read and write transactions.
SDQS_A[7:0]#	I/O SSTL-1.8	**Data Strobe Complements:** These are the complementary DDR2 strobe signals.
SCKE_A[3:0]	O SSTL-1.8	**Clock Enable:** (1 per Rank). SCKE_Ax is used to initialize the SDRAMs during power-up, to power-down SDRAM ranks, and to place all SDRAM ranks into and out of self-refresh during Suspend-to-RAM.
SODT_A[3:0]	O SSTL-1.8	**On Die Termination:** SODT_A[3:0] are active On-die termination control signals for DDR2 devices.

2.3 DDR2 DRAM Channel B Interface

Signal Name	Type	Description
SCLK_B[5:0]	O SSTL-1.8	**SDRAM Differential Clock:** (3 per DIMM). SCLK_Bx and its complement, SCLK_Bx#, make a differential clock pair output. The crossing of the positive edge of SCLK_Bx and the negative edge of its complement SCLK_Bx# are used to sample the command and control signals on the SDRAM.
SCLK_B[5:0]#	O SSTL-1.8	**SDRAM Complementary Differential Clock:** (3 per DIMM). These are the complementary differential DDR2 clock signals.
SCS_B[3:0]#	O SSTL-1.8	**Chip Select:** (1 per Rank) These signals select particular SDRAM components during the active state. There is one chip select for each SDRAM rank
SMA_B[14:0]	O SSTL-1.8	**Memory Address:** These signals are used to provide the multiplexed row and column address to the SDRAM.
SBS_B[2:0]	O SSTL-1.8	**Bank Select:** These signals define which banks are selected within each SDRAM rank DDR2: 1-Gb technology uses 8 banks.
SRAS_B#	O SSTL-1.8	**Row Address Strobe:** This signal is used with SCAS_B# and SWE_B# (along with SCS_Bx#) to define the SDRAM commands
SCAS_B#	O SSTL-1.8	**Column Address Strobe:** This signal is used with SRAS_B# and SWE_B# (along with SCS_Bx#) to define the SDRAM commands.
SWE_B#	O SSTL-1.8	**Write Enable:** This signal is used with SCAS_B# and SRAS_B# (along with SCS_Bx#) to define the SDRAM commands.
SDQ_B[63:0]	I/O SSTL-1.8	**Data Lines:** SDQ_Bx signals interface to the SDRAM data bus.
SDM_B[7:0]	O SSTL-1.8	**Data Mask:** When activated during writes, the corresponding data groups in the SDRAM are masked. There is one SBDM_Bx for every data byte lane.
SDQS_B[7:0]	I/O SSTL-1.8	**Data Strobes:** For DDR2, SDQS_Bx, and its complement ,SDQS_Bx#, make up a differential strobe pair. The data is captured at the crossing point of SDQS_Bx and its complement SDQS_Bx# during read and write transactions.
SDQS_B[7:0]#	I/O SSTL-1.8	**Data Strobe Complements:** These are the complementary DDR2 strobe signals.
SCKE_B[3:0]	O SSTL-1.8	**Clock Enable:** (1 per Rank). SCKE_Bx is used to initialize the SDRAMs during power-up, to power-down SDRAM ranks, and to place all SDRAM ranks into and out of self-refresh during Suspend-to-RAM.
SODT_B[3:0]	O SSTL-1.8	**On Die Termination:** SODT_B[3:0] are active On-die termination control signals for DDR2 devices.

2.4 DDR2 DRAM Reference and Compensation

Signal Name	Type	Description
SRCOMP[3:0]	I A	**System Memory RCOMP:**
SVREF	I A	**SDRAM Reference Voltage:** Reference voltage input for DQ, DQS, and DQS# input signals.
SMRCOMPVOL	I A	**System Memory RCOMP Reference:**
SMRCOMPVOH	I A	**System Memory RCOMP Reference:**

2.5 PCI Express* Interface Signals (Intel® 82Q965, 82G965, 82P965 (G)MCH Only)

Signal Name	Type	Description
EXP_RXN[15:0] EXP_RXP[15:0]	I PCI Express	**PCI Express Receive Differential Pair (RX):**
EXP_TXN[15:0] EXP_TXP[15:0]	O PCI Express	**PCI Express Graphics Transmit Differential Pair (TX):**
EXP_COMPO	I A	**PCI Express Graphics Output Current Compensation:**
EXP_COMPI	I A	**PCI Express Graphics Input Current Compensation:**

2.6 Analog Display Signals (Intel® 82Q965, 82Q963, 82G965 GMCH Only)

Note: This interface and associated signals are not used on the 82P965 MCH. Contact your field representative for details on termination of the associated package balls.

Signal Name	Type	Description
RED	O A	**RED Analog Video Output:** This signal is a CRT analog video output from the internal color palette DAC. The DAC is designed for a 37.5 ohm routing impedance, but the terminating resistor to ground will be 75 ohms (e.g., 75 ohm resistor on the board, in parallel with a 75 ohm CRT load).
RED#	O A	**RED# Analog Output:** This signal is an analog video output from the internal color palette DAC. It should be shorted to the ground plane.
GREEN	O A	**GREEN Analog Video Output:** This signal is a CRT analog video output from the internal color palette DAC. The DAC is designed for a 37.5 ohm routing impedance, but the terminating resistor to ground will be 75 ohms (e.g., 75 ohm resistor on the board, in parallel with a 75 ohm CRT load).
GREEN#	O A	**GREEN# Analog Output:** This signal is an analog video output from the internal color palette DAC. It should be shorted to the ground plane.
BLUE	O A	**BLUE Analog Video Output:** This signal is a CRT analog video output from the internal color palette DAC. The DAC is designed for a 37.5 ohm routing impedance, but the terminating resistor to ground will be 75 ohms (e.g., 75 ohm resistor on the board, in parallel with a 75 ohm CRT load).
BLUE#	O A	**BLUE# Analog Output:** This signal is an analog video output from the internal color palette DAC. It should be shorted to the ground plane.
REFSET	O A	**Resistor Set:** Set point resistor for the internal color palette DAC. A 255 ohm 1% resistor is required between REFSET and motherboard ground.
HSYNC	O 3.3V CMOS	**CRT Horizontal Synchronization:** This signal is used as the horizontal sync (polarity is programmable) or "sync interval", 3.3 V output.
VSYNC	O 3.3V CMOS	**CRT Vertical Synchronization:** This signal is used as the vertical sync (polarity is programmable) 3.3 V output.
DDC_CLK	I/O 3.3V CMOS	**Monitor Control Clock:** This signal may be used as the DDC_CLK for a secondary multiplexed digital display connector.
DDC_DATA	I/O 3.3V CMOS	**Monitor Control Data:** This signal may be used as the DDC_Data for a secondary multiplexed digital display connector.

2.7 Clocks, Reset, and Miscellaneous

Signal Name	Type	Description
HCLKP HCLKN	I HCSL	**Differential Host Clock In:** These signals receive a differential host clock from the external clock synthesizer. This clock is used by all of the (G)MCH logic that is in the Host clock domain. Memory domain clocks are also derived from this source.
GCLKP GCLKN	I HCSL	**Differential PCI Express* Graphics Clock In:** These signals receive a differential 100 MHz serial reference clock from the external clock synthesizer. This clock is used to generate the clocks necessary for the support of PCI Express.
DREFCLKN DREFCLKP	I HCSL	**Display PLL Differential Clock In:**
RSTIN#	I HVIN	**Reset In:** When asserted, this signal will asynchronously reset the (G)MCH logic. This signal is connected to the PCIRST# output of the Intel® ICH8. All PCI Express Graphics Attach output signals will also tri-state compliant to *PCI Express* Specification Rev 1.1*. This input should have a Schmitt trigger to avoid spurious resets. This signal is required to be 3.3 V tolerant.
PWROK	I HVIN	**Power OK:** When asserted, PWROK is an indication to the (G)MCH that core power has been stable for at least 10 us.
EXP_EN	I CMOS	**PCI Express* SDVO Concurrent Select** 0 = Only SDVO or PCI Express Operational 1 = SDVO and PCI Express operating simultaneously via PCI Express* Graphics port **NOTE:** For the 82Q963 GMCH and 82P965 MCH, this signal should be pulled low.
EXP_SLR	I CMOS	**PCI Express* Static Lane Reversal/Form Factor Selection:** For the 82Q965, 82G965, 82P965 (G)MCH components, this signal selects if the PCI Express lane numbers are reversed to differentiate BTX or ATX form factors. 0 = (G)MCH's PCI Express lane numbers are reversed (BTX Platforms) 1 = Normal operation (ATX Platforms) **NOTE:** This signal does not apply to the 82Q963 GMCH.
ICH_SYNC#	O HVCMOS	**ICH Sync:** This signal is connected to the MCH_SYNCH# signal on the ICH8.

Signal Name	Type	Description
TEST[2:0]	I/O	**In Circuit Test:** These signals should be connected to test points on the motherboard. They are internally shorted to the package ground and can be used to determine if the corner balls on the (G)MCH are correctly soldered down to the motherboard. These signals should NOT connect to ground on the motherboard. If TEST[2:0] are not going to be used, they should be left as no connects
XORTEST	I/O GTL+	**XOR Test:** As an input this signal is used for Bed of Nails testing by OEMs to execute XOR Chain test. It is used as an output for XOR chain testing.
ALLZTEST	I/O GTL	**ALL Z Test:** As an input this signal is used for Bed of Nails testing by OEMS to Execute XOR Chain test. It is used as an output for XOR chain testing.
SDVO_CTRL CLK	I/O COD	**Serial Digital Video Device Control Clock.** This signal is not used on the 82P965 MCH.
SDVO_CTRL DATA	I/O COD	**Serial Digital Video Device Control Data.** This signal is not used on the 82P965 MCH.

2.8 Direct Media Interface (DMI)

Signal Name	Type	Description
DMI_RXP[3:0] DMI_RXN[3:0]	I DMI	**Direct Media Interface:** Receive differential pair (Rx)
DMI_TXP[3:0] DMI_TXN[3:0]	O DMI	**Direct Media Interface:** Transmit differential pair (Tx)

2.9 Controller Link (CL)

Signal Name	Type	Description
CL_DATA	I/O CMOS	**Controller Link DATA: Data signal for the Controller Link interface**
CL_CLK	I/O CMOS	**Controller Link Clock: Clock signal for the Controller Link interface**
CL_VREF	I CMOS	**Controller Link VREF: Voltage refference for Controller Link**
CL_RST#	I CMOS	**Controller Link RESET:**
CL_PWROK	I CMOS	**Controller Link Power OK:**

2.10 Intel® Serial DVO (SDVO) Interface (Intel® 82Q965, 82Q963, 82G965 GMCH Only)

Only the 82Q965, 82G965, 82Q963 GMCHs have SDVO signals. For the 82Q965 and 82G965 GMCH, the SDVO signals are multiplexed with PCI Express signals; SDVO_CTTCLK and SDVO_CTRLDATA are the only unmultiplexed signals on the SDVO interface. For the 82Q963 GMCH, the SDVO signals are not multiplexed.

Signal Name	Type	Description
SDVOB_CLKN	O PCI Express*	**Serial Digital Video Channel B Clock Complement**
SDVOB_CLKP	O PCI Express	**Serial Digital Video Channel B Clock**
SDVOB_RED#	O PCI Express	**Serial Digital Video Channel C Red Complement**
SDVOB_RED	O PCI Express	**Serial Digital Video Channel C Red**
SDVOB_GREEN#	O PCI Express	**Serial Digital Video Channel B Green Complement**
SDVOB_GREEN	O PCI Express	**Serial Digital Video Channel B Green**
SDVOB_BLUE#	O PCI Express	**Serial Digital Video Channel B Blue Complement**
SDVOB_BLUE	O PCI Express	**Serial Digital Video Channel B Blue**
SDVOC_RED#	O PCI Express	**Serial Digital Video Channel C Red Complement**
SDVOC_RED	O PCI Express	**Serial Digital Video Channel C Red Channel B Alpha**
SDVOC_GREEN#	O PCI Express	**Serial Digital Video Channel C Green Complement**
SDVOC_GREEN	O PCI Express	**Serial Digital Video Channel C Green**
SDVOC_BLUE#	O PCI Express	**Serial Digital Video Channel C Blue Complement**
SDVOC_BLUE	O PCI Express	**Serial Digital Video Channel C Blue**
SDVOC_CLKN	O PCI Express *	**Serial Digital Video Channel C Clock Complement**
SDVOC_CLKP	O PCI Express	**Serial Digital Video Channel C Clock**
SDVO_TVCLKIN#	I PCI Express	**Serial Digital Video TVOUT Synchronization Clock Complement**
SDVO_TVCLKIN	I PCI Express	**Serial Digital Video TVOUT Synchronization Clock**
SDVOB_INT#	I PCI Express	**Serial Digital Video Input Interrupt Complement**

Signal Name	Type	Description
SDVOB_INT	I PCI Express	**Serial Digital Video Input Interrupt**
SDVOC_INT#	I PCI Express	**Serial Digital Video Input Interrupt Complement**
SDVOC_INT	I PCI Express	**Serial Digital Video Input Interrupt**
SDVO_FLDSTALL#	I PCI Express	**Serial Digital Video Field Stall Complement**.
SDVO_FLDSTALL	I PCI Express	**Serial Digital Video Field Stall**
SDVO_CTRLCLK	I/O COD	**Serial Digital Video Device Control Clock.** This signal is not used on the 82P965 MCH.
SDVO_CTRLDATA	I/O COD	**Serial Digital Video Device Control Data.** This signal is not used on the 82P965 MCH.

Table 2-2 shows the mapping of SDVO signals to the PCI Express* lanes in the various possible configurations as determined by the strapping configuration. Note that slot-reversed configurations do not apply to the Integrated-graphics only variants.

Table 2-2. SDVO/PCI Express* Signal Mapping (Intel® 82Q965 and 82G965 Only)

SDVO Signal	Configuration-wise Mapping			
	SDVO Only – Normal	SDVO Only – Reversed	Concurrent SDVO and PCI Express* – Normal	Concurrent SDVO and PCI Express* – Reversed
SDVOB_RED#	EXP_TXN0	EXP_TXN15	EXP_TXN15	EXP_TXN0
SDVOB_RED	EXP_TXP0	EXP_TXP15	EXP_TXP15	EXP_TXP0
SDVOB_GREEN#	EXP_TXN1	EXP_TXN14	EXP_TXN14	EXP_TXN1
SDVOB_GREEN	EXP_TXP1	EXP_TXP14	EXP_TXP14	EXP_TXP1
SDVOB_BLUE#	EXP_TXN2	EXP_TXN13	EXP_TXN13	EXP_TXN2
SDVOB_BLUE	EXP_TXP2	EXP_TXP13	EXP_TXP13	EXP_TXP2
SDVOB_CLKN	EXP_TXN3	EXP_TXN12	EXP_TXN12	EXP_TXN3
SDVOB_CLKP	EXP_TXP3	EXP_TXP12	E XP_TXP12	EXP_TXP3
SDVOC_RED#	EXP_TXN4	EXP_TXN11	EXP_TXN11	EXP_TXN4
SDVOC_RED	EXP_TXP4	EXP_TXP11	EXP_TXP11	EXP_TXP4
SDVOC_GREEN#	EXP_TXN5	EXP_TXN10	EXP_TXN10	EXP_TXN5
SDVOC_GREEN	EXP_TXP5	EXP_TXP10	EXP_TXP10	EXP_TXP5
SDVOC_BLUE#	EXP_TXN6	EXP_TXN9	EXP_TXN9	EXP_TXN6
SDVOC_BLUE	EXP_TXP6	EXP_TXP9	EXP_TXP9	EXP_TXP6
SDVOC_CLKN	EXP_TXN7	EXP_TXN8	EXP_TXN8	EXP_TXN7
SDVOC_CLKP	EXP_TXP7	EXP_TXP8	EXP_TXP8	EXP_TXP7
SDVO_TVCLKIN#	EXP_RXN0	EXP_RXN15	EXP_RXN15	EXP_RXN0
SDVO_TVCLKIN	EXP_RXP0	EXP_RXP15	EXP_RXP15	EXP_RXP0

SDVO Signal	Configuration-wise Mapping			
	SDVO Only – Normal	SDVO Only – Reversed	Concurrent SDVO and PCI Express* – Normal	Concurrent SDVO and PCI Express* – Reversed
SDVOB_INT#	EXP_RXN1	EXP_RXN14	EXP_RXN14	EXP_RXN1
SDVOB_INT	EXP_RXP1	EXP_RXP14	EXP_RXP14	EXP_RXP1
SDVOC_INT#	EXP_RXN5	EXP_RXN10	EXP_RXN10	EXP_RXN5
SDVOC_INT	EXP_RXP5	EXP_RXP10	EXP_RXP10	EXP_RXP5
SDVO_FLDSTALL#	EXP_RXN2	EXP_RXN13	EXP_RXN13	EXP_RXN2
SDVO_FLDSTALL	EXP_RXP2	EXP_RXP13	EXP_RXP13	EXP_RXP2

2.11 Power and Ground

Signal Name	Voltage	Description
VCC	1.25 V	**Core Power**
VTT	1.05 V / 1.2 V	**Processor System Bus Power**
VCC_EXP	1.25 V	**PCI Express* and DMI Power**
VCCSM	1.8 V	**System Memory Power**
VCC_SMCLK	1.8 V	**System Clock Memory Power**
VCC3_3	3.3 V	**3.3 V CMOS Power**
VCCA_EXPPLL	1.25 V	**PCI Express PLL Analog Power**
VCCA_DPLLA	1.25 V	**Display PLL A Analog Power:** For the 82P965 MCH, contact your Intel field representative for proper termination.
VCCA_DPLLB	1.25 V	**Display PLL B Analog Power:** For the 82P965 MCH, contact your Intel field representative for proper termination.
VCCA_HPLL	1.25 V	**Host PLL Analog Power**
VCCA_MPLL	1.25 V	**System Memory PLL Analog Power**
VCCA_DAC	3.3 V	**Display DAC Analog Power**
VCCA_EXP	3.3 V	**PCI Express Analog Power**
VCCDQ_CRT	1.5 V / 1.8 V	**Display Digital Quiet Supply Power**
VCCD_CRT	1.5 V / 1.8 V	**Display Digital Supply Power**
VCC_CL	1.25 V	**Controller Link Aux Power**
VCC_CL_PLL	1.25V	**Controller Link PLL Analog Power**
VSS	0 V	**Ground**

§

3 System Address Map

The (G)MCH supports 64 GB (64 bit addressing) or 4 GB of addressable memory space and 64 KB+3 of addressable I/O space. There is a programmable memory address space under the 1 MB region that is divided into regions that can be individually controlled with programmable attributes (e.g., Disable, Read/Write, Write Only, or Read Only). Attribute programming is described in the Chapter 5. This chapter focuses on how the memory space is partitioned and what the separate memory regions are used for. I/O address space has simpler mapping and is explained near the end of this section.

Note: Address mapping information for the Integrated Graphics Device applies to the 82Q965, 82Q963, and 82G965 GMCH only. The 82P965 MCH does not have an IGD.

Note: References to PCI Express applies to the 82Q965/82G965/82P965 (G)MCH only. The 82Q963 GMCH does not support PCI Express.

The HREQ[4:3] FSB signals are decoded to determine whether the access is 32 bit or 36 bit.

The (G)MCH supports a maximum of 8 GB of DRAM; no DRAM memory will be accessible above 8 GB. DRAM capacity is limited by the number of address pins available. There is no hardware lock to stop someone from inserting more memory than is addressable.

In the following sections, it is assumed that all of the compatibility memory ranges reside on the DMI Interface. The exception to this rule is VGA ranges, which may be mapped to PCI-Express*, DMI, or to the internal graphics device (IGD). In the absence of more specific references, cycle descriptions referencing PCI should be interpreted as the DMI Interface/PCI, while cycle descriptions referencing PCI Express or IGD are related to the PCI Express bus or the internal graphics device respectively. The reclaim base/reclaim limit registers remap logical accesses bound for addresses above 4 GB onto physical addresses that fall within DRAM.

The address map includes a number of programmable ranges:

- Device 0
  - PXPEPBAR (82Q965, 82G965, 82P965 (G)MCH only) – Egress port registers. Necessary for setting up VC1 as an isochronous channel using time based weighted round robin arbitration. (4 KB window)
  - MCHBAR – Memory mapped range for internal(G)MCH registers. For example, memory buffer register controls. (16 KB window)
  - PCIEXBAR (82Q965/82G965/82P965 (G)MCH only) – Flat memory-mapped address spaced to access device configuration registers. This mechanism can be used to access PCI configuration space (0h–FFh) and Extended configuration space (100h–FFFh) for PCI Express devices.
  - DMIBAR –This window is used to access registers associated with the (G)MCH/ICH8 Serial Interconnect (DMI) register memory range. (4 KB window)
  - GGC – GMCH graphics control register (82Q965, 82Q963, and 82G965 GMCH only). Used to select the amount of main memory that is pre-allocated to support the internal graphics device in VGA (non-linear) and Native (linear) modes. (0–64 MB options).

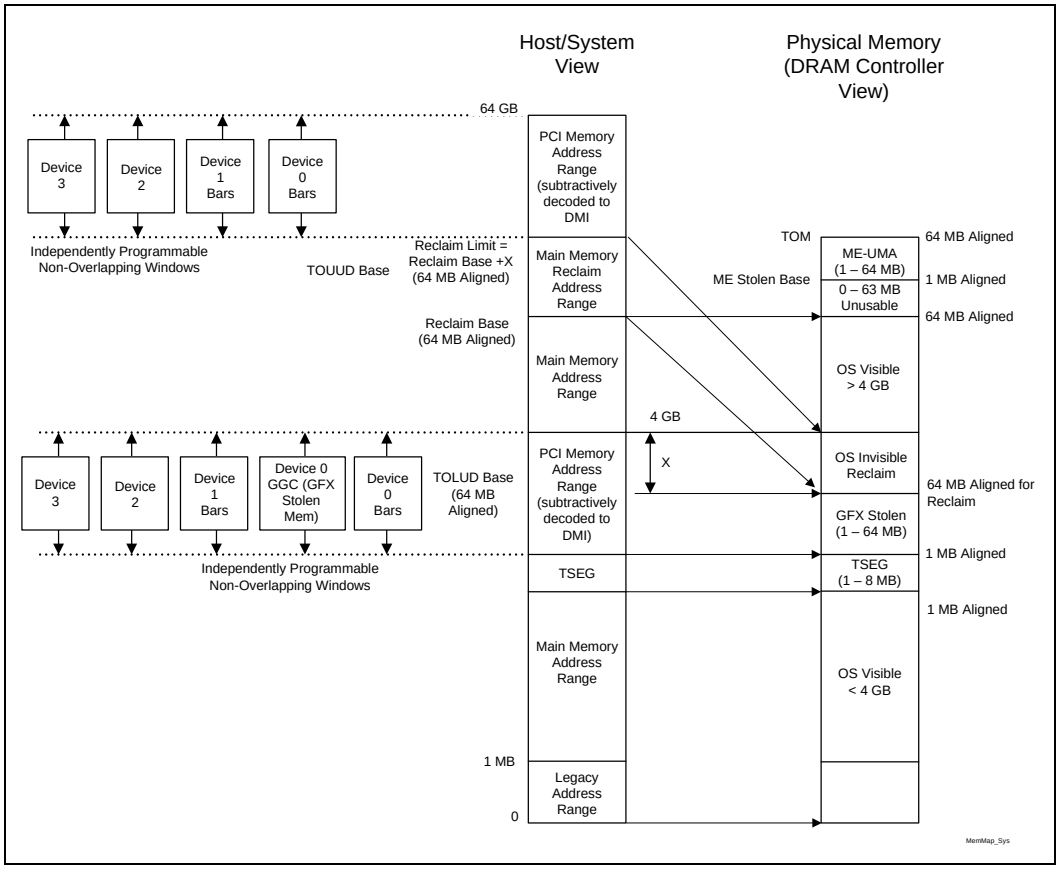
- Device 1 (82Q965, 82Q963, and 82G965 GMCH only)
  - MBASE1/MLIMIT1 – PCI Express port non-prefetchable memory access window.
  - PMUBASE1/PMULIMIT1 – PCI Express port prefetchable memory access window.
  - IOBASE1/IOLIMIT1 – PCI Express port IO access window.
- Device 2, Function 0 (82Q965, 82Q963, and 82G965 GMCH only)
  - MMADR – IGD registers and internal graphics instruction port. (512 KB window)
  - IOBAR – IO access window for internal graphics. Though this window address/data register pair, using I/O semantics, the IGD and internal graphics instruction port registers can be accessed. Note, this allows accessing the same registers as MMADR. In addition, the IOBAR can be used to issue writes to the GTT address table.
  - GMADR – Internal graphics translation window (128 MB, 256 MB or 512 MB window).
  - GTTADR – Internal graphics translation table location. (128 KB, 256 KB or 512 KB window).
- Device 2, Function 1 (82Q965, 82Q963, and 82G965 GMCH only)
  - MMADR – Function 1 IGD registers and internal graphics instruction port. (512 KB window)
- Device 3, Function 0
  - MEHECIBAR – Function 0 HECI memory mapped registers (16 B window)
- Device 3, Function 1
  - MEHECIBAR – Function 1 HECI2 memory mapped registers (16 B window)
- Device 3, Function 2
  - MEIDEPCTRLIO – Function 2 I/O space used in Native Mode for the Primary Controller's Control Block (4 B window)
  - MEIDESCMDIO – Function 2 /O space used in Native Mode for the Secondary Controller's Command Block (8 B window)
- Device 3, Function 3:
  - MEIDESCMDIO – Function 2 /O space used in Native Mode for the Secondary Controller's Command Block (8 B window)

The rules for the above programmable ranges are:

1. ALL of these ranges MUST be unique and NON-OVERLAPPING. It is the BIOS or system designers responsibility to limit memory population so that adequate PCI, PCI Express , High BIOS, PCI Express memory mapped space, and APIC memory space can be allocated.
2. In the case of overlapping ranges with memory, the memory decode will be given priority.
3. There are NO Hardware Interlocks to prevent problems in the case of overlapping ranges.
4. Accesses to overlapped ranges may produce indeterminate results.
5. The only peer-to-peer cycles allowed below the top of Low Usable memory (register TOLUD) are DMI Interface to PCI Express VGA range writes. Note that peer to peer cycles to the Internal Graphics VGA range are not supported.

Figure 3-1 represents system memory address map in a simplified form.

Figure 3-1. System Address Ranges



NOTES:

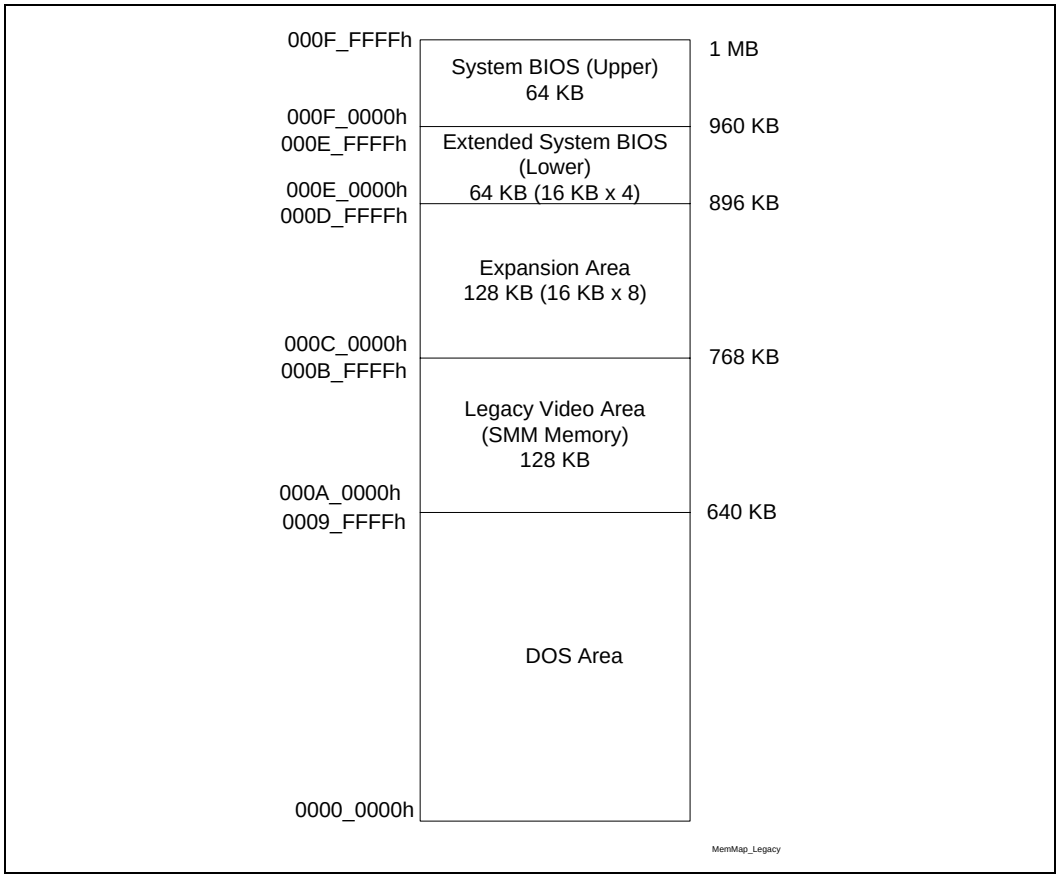
1. References to Internal Graphics Device/address ranges are for the 82Q965, 82Q963, and 82G965 GMCH only.
2. References to PCI Express devices/address ranges are for the 82Q965, 82G965, 82P965 (G)MCH only.

3.1 Legacy Address Range

This area is divided into the following address regions:

- 0 – 640 KB: DOS Area
- 640 – 768 KB: Legacy Video Buffer Area
- 768 – 896 KB in 16 KB sections (total of 8 sections): Expansion Area
- 896 – 960 KB in 16 KB sections (total of 4 sections): Extended System BIOS Area
- 960 KB – 1 MB Memory: System BIOS Area

Figure 3-2. DOS Legacy Address Range



3.1.1 DOS Range (0h – 9_FFFFh)

The DOS area is 640 KB (0000_0000h – 0009_FFFFh) in size and is always mapped to the main memory controlled by the (G)MCH.

3.1.2 Legacy Video Area (A_0000h–B_FFFFh)

The legacy 128KB VGA memory range, frame buffer, (000A_0000h – 000B_FFFFh) can be mapped to Device 2 IGD (82Q965, 82Q963, 82G965 GMCH only), to Device 1 PCI Express(82Q965, 82G965, 82P965 (G)MCH only), and/or to the DMI Interface. The appropriate mapping depends on which devices are enabled and the programming of the VGA steering bits. Based on the VGA steering bits, priority for VGA mapping is constant. The (G)MCH always decodes internally mapped devices first. Internal to the 82Q965, 82Q963, 82G965 GMCH, decode precedence is always given to IGD. The (G)MCH always positively decodes internally mapped devices, namely the IGD and PCI-Express. Subsequent decoding of regions mapped to PCI Express or the DMI Interface depends on the Legacy VGA configuration bits (VGA Enable & MDAP). This region is also the default for SMM space.

Compatible SMRAM Address Range (A_0000h–B_FFFFh)

When compatible SMM space is enabled, SMM-mode processor accesses to this range are routed to physical system DRAM at 000A_0000h – 000B_FFFFh. Non-SMM-mode processor accesses to this range are considered to be to the Video Buffer Area as described above. PCI Express and DMI originated cycles to enabled SMM space are not allowed and are considered to be to the Video Buffer Area if IGD is not enabled as the VGA device. PCI Express and DMI initiated cycles are attempted as Peer cycles, and will master abort on PCI if no external VGA device claims them.

Monochrome Adapter (MDA) Range (B_0000h–B_7FFFh)

Legacy support requires the ability to have a second graphics controller (monochrome) in the system. Accesses in the standard VGA range are forwarded to IGD, PCI-Express, or the DMI Interface (depending on configuration bits). Since the monochrome adapter may be mapped to anyone of these devices, the (G)MCH must decode cycles in the MDA range (000B_0000h – 000B_7FFFh) and forward either to IGD (82Q965, 82Q963, 82G965 GMCH only), PCI-Express (82Q965, 82G965, 82P965 (G)MCH only), or the DMI Interface. This capability is controlled by a VGA steering bits and the legacy configuration bit (MDAP bit). In addition to the memory range B0000h to B7FFFh, the (G)MCH decodes IO cycles at 3B4h, 3B5h, 3B8h, 3B9h, 3BAh and 3BFh and forwards them to the either IGD, PCI-Express, and/or the DMI Interface.

3.1.3 Expansion Area (C_0000h–D_FFFFh)

This 128 KB ISA Expansion region (000C_0000h – 000D_FFFFh) is divided into eight 16 KB segments. Each segment can be assigned one of four read/write states: read-only, write-only, read/write, or disabled. Typically, these blocks are mapped through (G)MCH and are subtractive decoded to ISA space. Memory that is disabled is not remapped.

Non-snooped accesses from PCI Express or DMI to this region are always sent to system memory.

Table 3-1. Expansion Area Memory Segments

Memory Segments	Attributes	Comments
0C0000h – 0C3FFFh	WE, RE	Add-on BIOS
0C4000h – 0C7FFFh	WE, RE	Add-on BIOS
0C8000h – 0CBFFFh	WE, RE	Add-on BIOS
0CC000h – 0CFFFFh	WE, RE	Add-on BIOS
0D0000h – 0D3FFFh	WE, RE	Add-on BIOS
0D4000h – 0D7FFFh	WE, RE	Add-on BIOS
0D8000h – 0DBFFFh	WE, RE	Add-on BIOS
0DC000h – 0DFFFFh	WE, RE	Add-on BIOS

3.1.4 Extended System BIOS Area (E_0000h–E_FFFFh)

This 64 KB area (000E_0000h – 000E_FFFFh) is divided into four 16 KB segments. Each segment can be assigned independent read and write attributes so it can be mapped either to main DRAM or to DMI Interface. Typically, this area is used for RAM or ROM. Memory segments that are disabled are not remapped elsewhere.

Non-snooped accesses from PCI Express or DMI to this region are always sent to DRAM.

Table 3-2. Extended System BIOS Area Memory Segments

Memory Segments	Attributes	Comments
0E0000h – 0E3FFFh	WE, RE	BIOS Extension
0E4000h – 0E7FFFh	WE, RE	BIOS Extension
0E8000h – 0EBFFFh	WE, RE	BIOS Extension
0EC000h – 0EFFFFh	WE, RE	BIOS Extension

3.1.5 System BIOS Area (F_0000h–F_FFFFh)

This area is a single 64 KB segment (000F_0000h – 000F_FFFFh). This segment can be assigned read and write attributes. It is by default (after reset) read/write disabled and cycles are forwarded to DMI Interface. By manipulating the read/write attributes, the (G)MCH can "shadow" BIOS into the main DRAM. When disabled, this segment is not remapped.

Non-snooped accesses from PCI Express or DMI to this region are always sent to DRAM.

Table 3-3. System BIOS Area Memory Segments

Memory Segments	Attributes	Comments
0F0000h – 0FFFFFh	WE, RE	BIOS Area

3.1.6 PAM Memory Area Details

The 13 sections from 768 KB to 1 MB comprise what is also known as the PAM Memory Area.

The (G)MCH does not handle IWB (Implicit Write-Back) cycles targeting DMI. Since all memory residing on DMI should be set as non-cacheable, there will normally not be IWB cycles targeting DMI.

However, DMI becomes the default target for processor and DMI originated accesses to disabled segments of the PAM region. If the MTRRs covering the PAM regions are set to writeback (WB) or RD it is possible to get IWB cycles targeting DMI. This may occur for processor-originated cycles (in a dual-processor system) and for DMI-originated cycles to disabled PAM regions.

For example, say that a particular PAM region is set for "Read Disabled" and the MTRR associated with this region is set to WB. A DMI master generates a memory read targeting the PAM region. A snoop is generated on the FSB and the result is an IWB. Since the PAM region is "Read Disabled" the default target for the Memory Read becomes DMI. The IWB associated with this cycle will cause the (G)MCH to hang.

3.1.7 Legacy Interrupt Routing

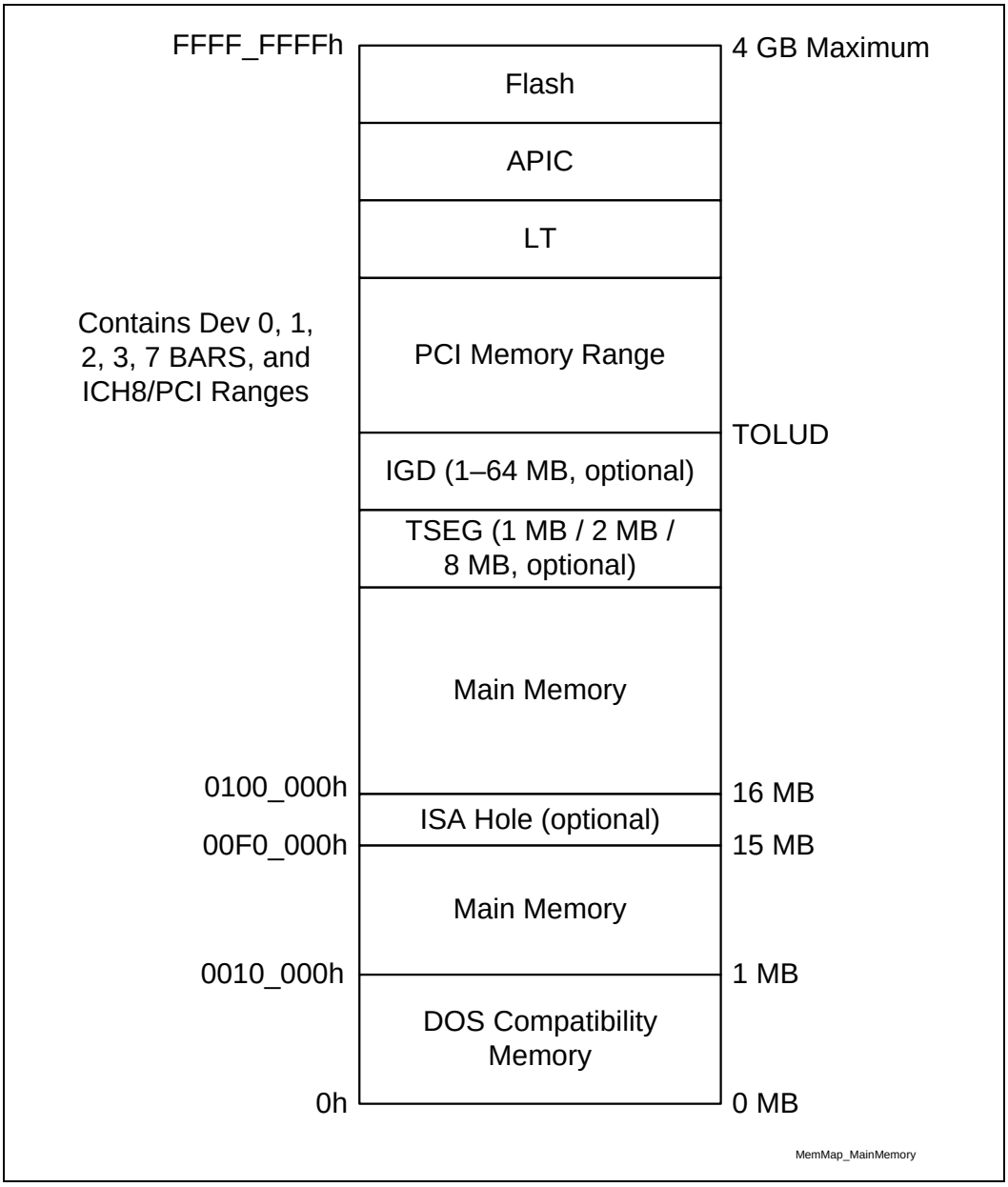
Table 3-4. Specifics of Legacy Interrupt Routing

Interrupt Source	Default Interrupt A/B/C/D
Internal Graphics D2:F0 (82Q965, 82Q963, and 82G965 GMCH only)	A
PEG (External Graphics Device)	Function of what is defined in Interrupt Pin register of the PEG device
PEG (Internally generated Interrupt) D1:F0	A
ME (HECI) D3, F0 (82Q965 and 82Q963 GMCH only)	C
ME (IDER) D3, F2 (82Q965 and 82Q963 GMCH only)	B
ME (KT) D3, F3 (82Q965 and 82Q963 GMCH only)	A

3.2 Main Memory Address Range (1 MB – TOLUD)

This address range extends from 1 MB to the top of Low Usable physical memory that is permitted to be accessible by the (G)MCH (as programmed in the TOLUD register). All accesses to addresses within this range will be forwarded by the (G)MCH to main memory unless it falls into the optional TSEG, optional ISA Hole, or optional IGD stolen VGA memory.

Figure 3-3. Main Memory Address Range



NOTES:
1. References to Internal Graphics Device/address ranges are for the 82Q965, 82Q963, and 82G965 GMCH only.
2. References to PCI Express devices/address ranges are for the 82Q965, 82G965, 82P965 (G)MCH only.

3.2.1 ISA Hole (15 MB – 16 MB)

A hole can be created at 15 MB–16 MB as controlled by the fixed hole enable in Device 0 space. Accesses within this hole are forwarded to the DMI Interface. The range of physical DRAM memory disabled by opening the hole is not remapped to the top of the memory – that physical DRAM space is not accessible. This 15 MB–16 MB hole is an optionally enabled ISA hole.

3.2.2 TSEG

TSEG size is optionally 1 MB, 2 MB, or 8 MB. For the 82Q965, 82Q963, and 82G965 GMCH. TSEG is below IGD stolen memory, which is at the top of Low Usable physical memory (TOLUD). SMM-mode processor accesses to enabled TSEG access the physical DRAM at the same address. Non-processor originated accesses are not allowed to SMM space. PCI-Express, DMI, and IGD originated cycle to enabled SMM space are handled as invalid cycle type with reads and writes to location 0 and byte enables turned off for writes. When the extended SMRAM space is enabled, processor accesses to the TSEG range without SMM attribute or without WB attribute are also forwarded to memory as invalid accesses (see Table 3-5). Non-SMM-mode writeback cycles that target TSEG space are completed to main memory for cache coherency. When SMM is enabled, the maximum amount of memory available to the system is equal to the amount of physical DRAM minus the value in the TSEG register which is fixed at 1 MB, 2 MB, or 8 MB.

3.2.3 Pre-allocated Memory

Voids of physical addresses that are not accessible as general system memory and reside within system memory address range (< TOLUD) are created for SMM-mode and legacy VGA graphics compatibility. **It is the responsibility of BIOS to properly initialize these regions**. Table 3-5 details the location and attributes of the regions. Enabling/Disabling these ranges are described in the (G)MCH Control register (GCC register, device 0, offset 52h).

Table 3-5. Pre-allocated Memory Example for 64 MB DRAM, 1 MB VGA, and 1 MB TSEG

Memory Segments	Attributes	Comments
0000_0000h – 03DF_FFFFh	R/W	Available System Memory 62 MB
03E0_0000h – 03EF_FFFFh	SMM Mode Only - Processor Reads	TSEG Address Range & Pre-allocated Memory
03F0_0000h – 03FF_FFFFh	R/W	Pre-allocated Graphics VGA memory. 1 MB (or 4/8/16/32/64 MB) when IGD is enabled on the 82Q965, 82Q963, 82G965 GMCH.

3.3 PCI Memory Address Range (TOLUD – 4 GB)

This address range, from the top of low usable DRAM (TOLUD) to 4 GB is normally mapped to the DMI Interface. With PCI Express* port (82Q965, 82G965, 82P965 (G)MCH), there is one exceptions to this rule.

- Addresses decoded to the PCI Express Memory Window defined by the MBASE1, MLIMIT1, registers are mapped to PCI Express.

Note: AGP Aperture no longer exists with PCI-Express.

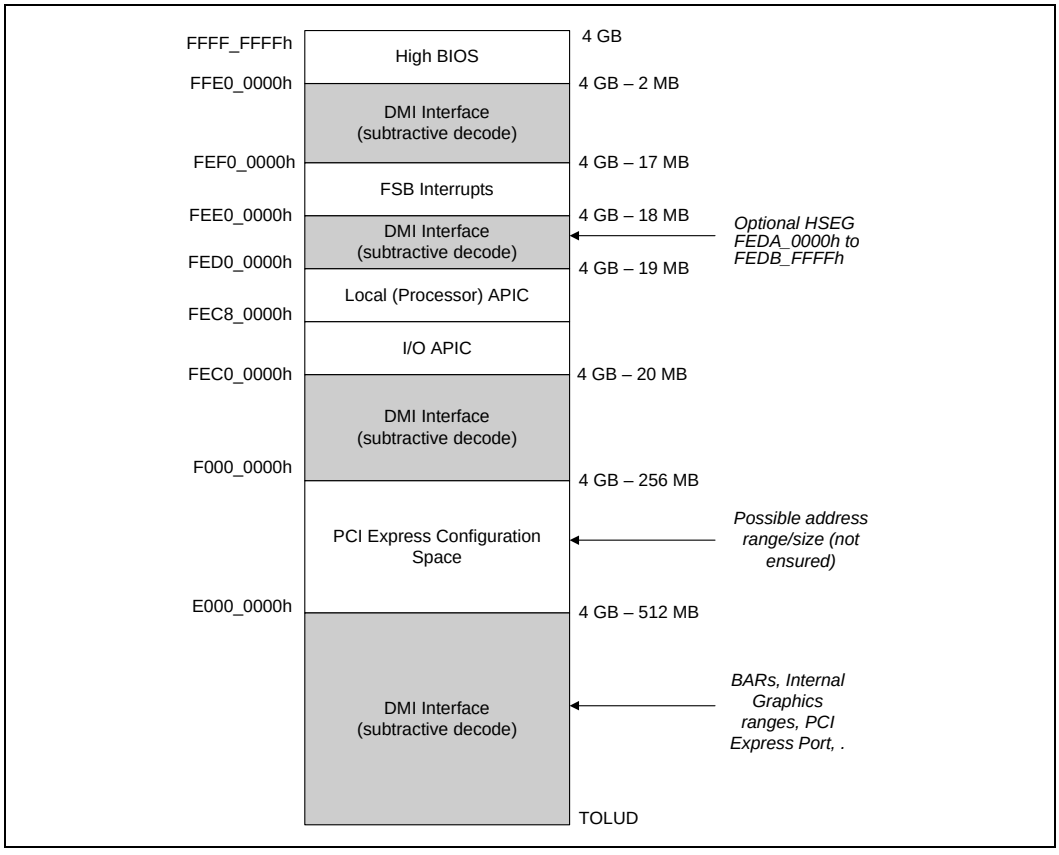
In a Manageability Engine configuration, there is the following exception to this rule.

- Addresses decoded to the ME Keyboard and Text MMIO range (EPKTBAR)

There are other MMIO Bars that may be mapped to this range or to the range above TOUUD.

There are sub-ranges within the PCI Memory address range defined as APIC Configuration Space, FSB Interrupt Space, and High BIOS Address Range. The exceptions listed above for internal graphics and the PCI Express ports ***MUST NOT*** *overlap with these ranges.*

Figure 3-4. PCI Memory Address Range



3.3.1 APIC Configuration Space (FEC0_0000h–FECF_FFFFh)

This range is reserved for APIC configuration space. The I/O APIC(s) usually reside in the ICH8 portion of the chipset, but may also exist as stand-alone components like PXH.

The IOAPIC spaces are used to communicate with IOAPIC interrupt controllers that may be populated in the system. Since it is difficult to relocate an interrupt controller using plug-and-play software, fixed address decode regions have been allocated for them. Processor accesses to the default IOAPIC region (FEC0_0000h to FEC7_FFFFh) are always forwarded to DMI.

The (G)MCH optionally supports additional I/O APICs behind the PCI Express "Graphics" port (82Q965, 82G965, 82P965 (G)MCH only). When enabled via the PCI Express Configuration register (Device 1, offset 200h), the PCI Express port will positively decode a subset of the APIC configuration space – specifically FEC8_0000h thru FECF_FFFFh. Memory request to this range will then be forwarded to the PCI Express port. This mode is intended for the entry Workstation/Server components of the (G)MCH, and would be disabled in typical Desktop systems. When disabled, any access within entire APIC Configuration space (FEC0_0000h to FECF_FFFFh) is forwarded to DMI.

3.3.2 HSEG (FEDA_0000h–FEDB_FFFFh)

This optional segment from FEDA_0000h to FEDB_FFFFh provides a remapping window to SMM Memory. It is sometimes called the High SMM memory space. SMM-mode processor accesses to the optionally enabled HSEG are remapped to 000A-_0000h – 000B_FFFFh. Non-SMM-mode processor accesses to enabled HSEG are considered invalid and are terminated immediately on the FSB. The exceptions to this rule are Non-SMM-mode writeback cycles that are remapped to SMM space to maintain cache coherency. PCI Express and DMI originated cycles to enabled SMM space are not allowed. Physical DRAM behind the HSEG transaction address is not remapped and is not accessible. All cacheline writes with WB attribute or Implicit writebacks to the HSEG range are completed to DRAM like an SMM cycle.

3.3.3 FSB Interrupt Memory Space (FEE0_0000–FEEF_FFFF)

The FSB Interrupt space is the address used to deliver interrupts to the FSB. Any device on PCI Express or DMI may issue a Memory Write to 0FEEx_xxxxh. The (G)MCH will forward this Memory Write along with the data to the FSB as an Interrupt Message Transaction. The (G)MCH terminates the FSB transaction by providing the response and asserting HTRDYB. This memory write cycle does not go to main memory.

3.3.4 High BIOS Area

The top 2 MB (FFE0_0000h – FFFF_FFFFh) of the PCI memory address range is reserved for system BIOS (High BIOS), extended BIOS for PCI devices, and the A20 alias of the system BIOS. The processor begins execution from the High BIOS after reset. This region is mapped to DMI interface so that the upper subset of this region aliases to 16 MB–256 KB range. The actual address space required for the BIOS is less than 2 MB; however, the minimum processor MTRR range for this region is 2 MB so that full 2 MB must be considered.

3.4 Main Memory Address Space (4 GB to TOUUD)

The (G)MCH supports 36-bit addressing. The maximum main memory size supported is 8 GB total DRAM memory. A hole between TOLUD and 4 GB occurs when main memory size approaches 4 GB or larger. As a result, TOM, and TOUUD registers and RECLAIMBASE/RECLAIMLIMIT registers become relevant.

The new reclaim configuration registers exist to reclaim lost main memory space. The "greater than 32 bit reclaim handling" will be handled similar to previous (G)MCHs.

Upstream read and write accesses above 36-bit addressing will be treated as invalid cycles by PCI Express and DMI.

Top of Memory

The "Top of Memory" (TOM) register reflects the total amount of populated physical memory. This is NOT necessarily the highest main memory address (holes may exist in main memory address map due to addresses allocated for memory mapped IO above TOM). TOM is used to allocate Manageability Engine (ME) stolen memory. The Manageability Engine's stolen size register reflects the total amount of physical memory stolen by the ME. The ME stolen memory is located at the top of physical memory. The ME stolen memory base is calculated by subtracting the amount of memory stolen by ME from TOM.

The Top of Upper Usable DRAM (TOUUD) register reflects the total amount of addressable DRAM. If reclaim is disabled, TOUUD will reflect TOM minus ME's stolen size. If reclaim is enabled, then it will reflect the reclaim limit. Also, the reclaim base will be the same as TOM minus ME stolen memory size to the nearest 64 MB alignment.

The TOLUD register is restricted to 4 GB memory (A[31:20]), but the (G)MCH can support up to 16 GB, limited by DRAM pins. For physical memory greater than 4 GB, the TOUUD register helps identify the address range in between the 4 GB boundary and the top of physical memory. This identifies memory that can be directly accessed (including reclaim address calculation) that is useful for memory access indication, early path indication, and trusted read indication. When reclaim is enabled, TOLUD must be 64 MB aligned, but when reclaim is disabled, TOLUD can be 1 MB aligned.

C1DRB3 cannot be used directly to determine the effective size of memory as the values programmed in the DRBs depend on the memory mode (Flex memory mode, interleaved). The Reclaim Base/Limit registers also can not be used because reclaim can be disabled. The C0DRB3 register is used for memory channel identification (channel 0 vs. channel 1) in the case of Flex memory mode operation.

3.4.1 Memory Re-claim Background

The following are examples of memory-mapped I/O devices that are typically located below 4 GB:

- High BIOS
- HSEG
- TSEG
- Graphics stolen
- XAPIC
- Local APIC
- FSB Interrupts
- Mbase/Mlimit
- Memory-mapped I/O space that supports only 32B addressing

The (G)MCH provides the capability to re-claim the physical memory overlapped by the memory-mapped I/O logical address space. The (G)MCH re-maps physical memory from the Top of Low Memory (TOLUD) boundary up to the 4 GB boundary to an equivalent sized logical address range located just below the Manageability Engine's stolen memory.

3.4.2 Memory Reclaiming

An incoming address (referred to as a logical address) is checked to see if it falls in the memory re-map window. The bottom of the re-map window is defined by the value in the RECLAIMBASE register. The top of the re-map window is defined by the value in the RECLAIMLIMIT register. An address that falls within this window is reclaimed to the physical memory starting at the address defined by the TOLUD register. The TOLUD register must be 64 MB aligned when RECLAIM is enabled, but can be 1 MB aligned when reclaim is disabled.

3.5 PCI Express* Configuration Address Space (Intel® 82Q965, 82G965, 82P965 (G)MCH Only)

The PCIEXBAR registers (Device 0, Function 0 defines the base address for the configuration space associated with all devices and functions that are potentially a part of the PCI Express root complex hierarchy. The size of this range is programmable. BIOS must assign this address range such that it will not conflict with any other address ranges. See Chapter 6 for more details.

3.6 PCI Express* Graphics Attach (PEG) (Intel® 82Q965, 82G965, 82P965 (G)MCH Only)

The (G)MCH can be programmed to direct memory accesses to the PCI Express interface when addresses are within either of two ranges specified via registers in (G)MCH's Device 1 configuration space.

- The first range is controlled via the Memory Base Register (MBASE) and Memory Limit Register (MLIMIT) registers.
- The second range is controlled via the Pre-fetchable Memory Base (PMBASE) and Pre-fetchable Memory Limit (PMLIMIT) registers.

Conceptually, address decoding for each range follows the same basic concept. The top 12 bits of the respective Memory Base and Memory Limit registers correspond to address bits 31:20 of a memory address. For the purpose of address decoding, the (G)MCH assumes that address bits 19:0 of the memory base are zero and that address bits 19:0 of the memory limit address are FFFFFh. This forces each memory address range to be aligned to 1 MB boundary and to have a size granularity of 1 MB.

The (G)MCH positively decodes memory accesses to PCI Express memory address space as defined by the following equations:

$$Memory\_Base\_Address \leq Address \leq Memory\_Limit\_Address$$

$$Prefetchable\_Memory\_Base\_Address \leq Address \leq Prefetchable\_Memory\_Limit\_Address$$

The window size is programmed by the plug-and-play configuration software. The window size depends on the size of memory claimed by the PCI Express device. Normally these ranges will reside above the Top-of-Low Usable-DRAM and below High BIOS and APIC address ranges. They MUST reside above the top of low memory (TOLUD) if they reside below 4 GB and MUST reside above top of upper memory (TOUUD) if they reside above 4 GB, or they will steal physical DRAM memory space.

It is essential to support a separate Pre-fetchable range in order to apply USWC attribute (from the processor point of view) to that range. The USWC attribute is used by the processor for write combining.

Note that the (G)MCH Device 1 memory range registers described above are used to allocate memory address space for any PCI Express devices sitting on PCI Express that require such a window.

The PCICMD1 register can override the routing of memory accesses to PCI Express. Thus, the memory access enable bit must be set in the device 1 PCICMD1 register to enable the memory base/limit and pre-fetchable base/limit windows.

The upper PMUBASE1/PMULIMIT1 registers have been implemented for PCI Express Specification compliance. The (G)MCH's 36 bit addressing locates MMIO space above 4 GB using these registers.

3.7 Graphics Memory Address Ranges (Intel® 82Q965, 82Q963, 82G965 GMCH Only)

The (G)MCH can be programmed to direct memory accesses to the IGD when addresses are within any of five ranges specified via registers in (G)MCH's Device 2 configuration space.

1. The Memory Map Base Register (MMADR) is used to access graphics control registers.
6. The Graphics Memory Aperture Base Register (GMADR) is used to access graphics memory allocated via the graphics translation table.
7. The Graphics Translation Table Base Register (GTTADR) is used to access the translation table.
8. The LT Graphics Memory Aperture Base Register (TGABAR) is used to access protected graphics memory allocated via the graphics translation table.
9. The LT Graphics Translation Table Base Register (TGGTT) is used to access the protected translation table.

These ranges can reside above the Top-of-Low-DRAM and below High BIOS and APIC address ranges or above Top of upper DRAM (TOUUD). They MUST reside above the top of memory (TOLUD) and below 4 GB or above TOUUD so they do not steal any physical DRAM memory space.

GMADR is a Prefetchable range in order to apply the USWC attribute (from the processor point of view) to that range. The USWC attribute is used by the processor for write combining.

3.8 System Management Mode (SMM)

System Management Mode uses main memory for System Management RAM (SMM RAM). The (G)MCH supports: Compatible SMRAM (C_SMRAM), High Segment (HSEG), and Top of Memory Segment (TSEG). System Management RAM space provides a memory area that is available for the SMI handlers and code and data storage. This memory resource is normally hidden from the system OS so that the processor has immediate access to this memory space upon entry to SMM. (G)MCH provides three SMRAM options:

- Below 1 MB option that supports compatible SMI handlers.
- Above 1 MB option that allows new SMI handlers to execute with writeback cacheable SMRAM.
- Optional TSEG area of 1 MB, 2 MB, or 8 MB in size. For the 82Q965, 82Q963, and 82G965 GMCH, the TSEG area lies below IGD stolen memory.

The above 1 MB solutions require changes to compatible SMRAM handlers code to properly execute above 1 MB.

Note: DMI Interface and PCI Express masters are not allowed to access the SMM space.

3.8.1 SMM Space Definition

SMM space is defined by its **addressed** SMM space and its DRAM SMM space. The addressed SMM space is defined as the range of bus addresses used by the processor to access SMM space. DRAM SMM space is defined as the range of physical DRAM memory locations containing the SMM code. SMM space can be accessed at one of three transaction address ranges: Compatible, High and TSEG. The Compatible and TSEG SMM space is not remapped and therefore the addressed and DRAM SMM space is the same address range. Since the High SMM space is remapped the addressed and DRAM SMM space is a different address range. Note that the High DRAM space is the same as the Compatible Transaction Address space. Table 3-6 describes three unique address ranges.

Table 3-6. Pre-Allocated Memory Example for 64-MB DRAM, 1-MB VGA and 1-MB TSEG

SMM Space Enabled	Transaction Address Space	DRAM Space (DRAM)
Compatible	000A_0000h to 000B_FFFFh	000A_0000h to 000B_FFFFh
High	FEDA_0000h to FEDB_FFFFh	000A_0000h to 000B_FFFFh
TSEG	(TOLUD – STOLEN[1] – TSEG) to (TOLUD – STOLEN[1])	(TOLUD – STOLEN[1] – TSEG) to (TOLUD – STOLEN[1])

NOTES:
1. STOLEN memory is only for the 82Q965, 82Q963, and 82G965 GMCH.

3.8.2 SMM Space Restrictions

If any of the following conditions are violated, the results of SMM accesses are unpredictable and may cause the system to hang:

1. The Compatible SMM space **must not** be set up as cacheable.
2. High or TSEG SMM transaction address space **must not** overlap address space assigned to system DRAM, or to any "PCI" devices (including DMI Interface, PCI-Express, and graphics devices). This is a BIOS responsibility.
3. Both D_OPEN and D_CLOSE **must not** be set to 1 at the same time.
4. When TSEG SMM space is enabled, the TSEG space **must not** be reported to the OS as available DRAM. This is a BIOS responsibility.
5. Any address translated through the GMADR TLB must not target DRAM from A_0000h–F_FFFFh.

3.8.3 SMM Space Combinations

When High SMM is enabled (G_SMRAME=1 and H_SMRAM_EN=1), the Compatible SMM space is effectively disabled. Processor-originated accesses to the Compatible SMM space are forwarded to PCI Express if VGAEN=1 (also depends on MDAP); otherwise, they are forwarded to the DMI Interface. PCI Express and DMI Interface originated accesses are **never** allowed to access SMM space.

Table 3-7. SMM Space Table

Global Enable G_SMRAME	High Enable H_SMRAM_EN	TSEG Enable TSEG_EN	Compatible (C) Range	High (H) Range	TSEG (T) Range
0	X	X	Disable	Disable	Disable
1	0	0	Enable	Disable	Disable
1	0	1	Enable	Disable	Enable
1	1	0	Disabled	Enable	Disable
1	1	1	Disabled	Enable	Enable

3.8.4 SMM Control Combinations

The G_SMRAME bit provides a global enable for all SMM memory. The D_OPEN bit allows software to write to the SMM ranges without being in SMM mode. BIOS software can use this bit to initialize SMM code at powerup. The D_LCK bit limits the SMM range access to only SMM mode accesses. The D_CLS bit causes SMM data accesses to be forwarded to the DMI Interface or PCI Express . The SMM software can use this bit to write to video memory while running SMM code out of DRAM.

Table 3-8. SMM Control Table

G_SMRAME	D_LCK	D_CLS	D_OPEN	Processor in SMM Mode	SMM Code Access	SMM Data Access
0	x	X	x	x	Disable	Disable
1	0	X	0	0	Disable	Disable
1	0	0	0	1	Enable	Enable
1	0	0	1	x	Enable	Enable
1	0	1	0	1	Enable	Disable
1	0	1	1	x	Invalid	Invalid
1	1	X	x	0	Disable	Disable
1	1	0	x	1	Enable	Enable
1	1	1	x	1	Enable	Disable

3.8.5 SMM Space Decode and Transaction Handling

Only the processor is allowed to access SMM space. PCI Express and DMI Interface originated transactions are not allowed to SMM space. The following tables indicate the action taken by the (G)MCH when the accesses to the various enabled SMM space occurs.

3.8.6 Processor WB Transaction to an Enabled SMM Address Space

Processor writeback transactions (REQa[1]# = 0) to enabled SMM address space must be written to the associated SMM DRAM even though D_OPEN=0 and the transaction is not performed in SMM mode. This ensures SMM space cache coherency when cacheable extended SMM space is used.

3.8.7 SMM Access Through GTT TLB (Intel® 82Q965, 82Q963, 82G965 GMCH Only)

Accesses through GTT TLB address translation to enabled SMM DRAM space are not allowed. Writes will be routed to memory address 000C_0000h with byte enables de-asserted and reads will be routed to memory address 000C_0000h. If a GTT TLB translated address hits enabled SMM DRAM space, an error is recorded.

PCI Express and DMI Interface originated accesses are **never** allowed to access SMM space directly or through the GTT TLB address translation. If a GTT TLB translated address hits enabled SMM DRAM space, an error is recorded.

PCI Express and DMI Interface write accesses through GMADR range will be snooped. Assesses to GMADR linear range are supported. PCI Express and DMI interface tileY and tileX writes to GMADR are not supported. If, when translated, the resulting physical address is to enabled SMM DRAM space, the request will be remapped to address 000C_0000h with de-asserted byte enables.

PCI Express and DMI Interface read accesses to the GMADR range are not supported; therefore, will have no address translation concerns. PCI Express and DMI interface reads to GMADR will be remapped to address 000C_0000h. The read will complete with UR (unsupported request) completion status.

GTT fetches are always decoded (at fetch time) to ensure not in SMM (actually, anything above base of TSEG or 640 KB–1 MB). Thus, they will be invalid and go to address 000C_0000h. This is not specific to PCI Express or DMI; it applies to processor or internal graphics engines. Also, since the GMADR snoop would not be directly to the SMM space, there would not be a writeback to SMM. In fact, the writeback would also be invalid (because it uses the same translation) and go to address 000C_0000h.

3.9 Memory Shadowing

Any block of memory that can be designated as read-only or write-only can be "shadowed" into (G)MCH DRAM memory. Typically this is done to allow ROM code to execute more rapidly out of main DRAM. ROM is used as a read-only during the copy process while DRAM at the same time is designated write-only. After copying, the DRAM is designated read-only so that ROM is shadowed. Processor bus transactions are routed accordingly.

3.10 I/O Address Space

The (G)MCH does not support the existence of any other I/O devices beside itself on the processor bus. The (G)MCH generates either DMI interface or PCI Express (82Q965, 82G965, 82P965 (G)MCH only) bus cycles for all processor I/O accesses that it does not claim. Within the host bridge, the (G)MCH contains two internal registers in the processor I/O space, Configuration Address Register (CONFIG_ADDRESS) and the Configuration Data Register (CONFIG_DATA). These locations are used to implement configuration space access mechanism.

The processor allows 64K+3 bytes to be addressed within the I/O space. The (G)MCH propagates the processor I/O address without any translation on to the destination bus and therefore provides addressability for 64K+3 byte locations. Note that the upper 3 locations can be accessed only during I/O address wraparound when processor bus HA16# address signal is asserted. HA16# is asserted on the processor bus whenever an I/O access is made to 4 bytes from address 0FFFDh, 0FFFEh, or 0FFFFh. HA16# is also asserted when an I/O access is made to 2 bytes from address 0FFFFh.

A set of I/O accesses (other than ones used for configuration space access) are consumed by the internal graphics device, if it is enabled (82Q965, 82Q963, 82G965 GMCH only). The mechanisms for internal graphics I/O decode and the associated control is explained later.

The I/O accesses (other than ones used for configuration space access) are forwarded normally to the DMI interface bus, unless they fall within the PCI Express I/O address range as defined by the mechanisms explained below. I/O writes are NOT posted. Memory writes to ICH8 or PCI Express are posted. For the 82Q965, 82G965, 82P965 (G)MCH, the PCICMD1 register can disable the routing of I/O cycles to the PCI Express.

The (G)MCH responds to I/O cycles initiated on PCI Express or DMI with an UR status. Upstream I/O cycles and configuration cycles should never occur. If one does occur, the request will route as a read to memory address 000C_0000h so a completion is naturally generated (whether the original request was a read or write). The transaction will complete with an UR completion status.

For Pentium 4 processors, I/O reads that lie within 8-byte boundaries but cross 4-byte boundaries are issued from the processor as 1 transaction. The (G)MCH will break this into 2 separate transactions. I/O writes that lie within 8-byte boundaries but cross 4-byte boundaries are assumed to be split into 2 transactions by the processor.

3.10.1 PCI Express* I/O Address Mapping (Intel® 82Q965, 82G965, 82P965 (G)MCH Only)

The (G)MCH can be programmed to direct non-memory (I/O) accesses to the PCI Express bus interface when processor-initiated I/O cycle addresses are within the PCI Express I/O address range. This range is controlled via the I/O Base Address (IOBASE) and I/O Limit Address (IOLIMIT) registers in (G)MCH Device 1 configuration space.

Address decoding for this range is based on the following concept. The top 4 bits of the respective I/O Base and I/O Limit registers correspond to address bits 15:12 of an I/O address. For the purpose of address decoding, the (G)MCH assumes that lower 12 address bits 11:0 of the I/O base are zero and that address bits 11:0 of the I/O limit address are FFFh. This forces the I/O address range alignment to 4 KB boundary and produces a size granularity of 4 KB.

The (G)MCH positively decodes I/O accesses to PCI Express I/O address space as defined by the following equation:

$$I/O\_Base\_Address \leq Processor\ I/O\ Cycle\ Address \leq I/O\_Limit\_Address$$

The effective size of the range is programmed by the plug-and-play configuration software and it depends on the size of I/O space claimed by the PCI Express device.

The (G)MCH also forwards accesses to the Legacy VGA I/O ranges according to the settings in the Device 1 configuration registers BCTRL (VGA Enable bit) and PCICMD1 (IOAE1 bit), unless a second adapter (monochrome) is present on the DMI interface/PCI (or ISA). The presence of a second graphics adapter is determined by the MDAP configuration bit. When MDAP is set, the (G)MCH will decode legacy monochrome I/O ranges and forward them to the DMI Interface. The I/O ranges decoded for the monochrome adapter are 3B4h, 3B5h, 3B8h, 3B9h, 3BAh, and 3BFh.

Note that the (G)MCH Device 1 I/O address range registers defined above are used for all I/O space allocation for any devices requiring such a window on PCI-Express.

The PCICMD1 register can disable the routing of I/O cycles to PCI-Express.

3.11 (G)MCH Decode Rules and Cross-Bridge Address Mapping

VGAA = 000A_0000h – 000A_FFFFh
MDA = 000B_0000h – 000B_7FFFh
VGAB = 000B_8000h – 000B_FFFFh

MAINMEM = 0100_0000h to TOLUD

HIGHMEM = 4 GB to TOM

RECLAIMMEM = RECLAIMBASE to RECLAIMLIMIT

3.11.1 Legacy VGA and I/O Range Decode Rules

The legacy 128 KB VGA memory range 000A_0000h–000B_FFFFh can be mapped to IGD (Device 2), to PCI Express (Device 1), and/or to the DMI Interface depending on the programming of the VGA steering bits. Priority for VGA mapping is constant in that the (G)MCH always decodes internally mapped devices first. Internal to the 82Q965, 82Q963, and 82G965 GMCH, decode precedence is always given to IGD. The (G)MCH always positively decodes internally mapped devices, namely the IGD and PCI-Express. Subsequent decoding of regions mapped to PCI Express or the DMI Interface depends on the Legacy VGA configurations bits (VGA Enable and MDAP).

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4 (G)MCH Register Description

The (G)MCH contains two sets of software accessible registers, accessed via the Host processor I/O address space: Control registers and internal configuration registers.

- Control registers are I/O mapped into the processor I/O space, which control access to PCI and PCI Express configuration space (see section entitled I/O Mapped Registers).
- Internal configuration registers residing within the (G)MCH are partitioned into logical device register sets (“logical” since they reside within a single physical device). One register set is dedicated to Host Bridge functionality (i.e., DRAM configuration, other chipset operating parameters and optional features). For the 82Q965/82G965/82P965 (G)MCH, there is a register block dedicated to Host-PCI Express Bridge functions (controls PCI Express interface configurations and operating parameters). For the 82Q965/82Q963/82G965 GMCH, there is a register block for the internal graphics functions.

The (G)MCH internal registers (I/O Mapped, Configuration and PCI Express Extended Configuration registers) are accessible by the Host processor. The registers that reside within the lower 256 bytes of each device can be accessed as Byte, Word (16-bit), or DWord (32-bit) quantities, with the exception of CONFIG_ADDRESS, which can only be accessed as a DWord. All multi-byte numeric fields use "little-endian" ordering (i.e., lower addresses contain the least significant parts of the field). Registers which reside in bytes 256 through 4095 of each device may only be accessed using memory mapped transactions in DWord (32-bit) quantities.

Some of the (G)MCH registers described in this section contain reserved bits. These bits are labeled "Reserved”. Software must deal correctly with fields that are reserved. On reads, software must use appropriate masks to extract the defined bits and not rely on reserved bits being any particular value. On writes, software must ensure that the values of reserved bit positions are preserved. That is, the values of reserved bit positions must first be read, merged with the new values for other bit positions and then written back. Note the software does not need to perform read, merge, and write operation for the configuration address register.

In addition to reserved bits within a register, the (G)MCH contains address locations in the configuration space of the Host Bridge entity that are marked either "Reserved" or “Intel Reserved”. The (G)MCH responds to accesses to “Reserved” address locations by completing the host cycle. When a “Reserved” register location is read, a zero value is returned. (“Reserved” registers can be 8-, 16-, or 32-bits in size). Writes to “Reserved” registers have no effect on the (G)MCH. Registers that are marked as “Intel Reserved” must not be modified by system software. Writes to “Intel Reserved” registers may cause system failure. Reads from “Intel Reserved” registers may return a non-zero value.

Upon a full reset, the (G)MCH sets its entire set of internal configuration registers to predetermined default states. Some register values at reset are determined by external strapping options. The default state represents the minimum functionality feature set required to successfully bringing up the system. Hence, it does not represent the optimal system configuration. It is the responsibility of the system initialization software (usually BIOS) to properly determine the DRAM configurations, operating parameters and optional system features that are applicable, and to program the (G)MCH registers accordingly.

4.1 Register Terminology

The following table shows the register-related terminology that is used.

Item	Description
RO	Read Only bit(s). Writes to these bits have no effect.
RS/WC	Read Set / Write Clear bit(s). These bits are set to '1' when read and then will continue to remain set until written. A write of '1' clears (sets to '0') the corresponding bit(s) and a write of '0' has no effect.
R/W	Read / Write bit(s). These bits can be read and written.
R/WC	Read / Write Clear bit(s). These bits can be read. Internal events may set this bit. A write of '1' clears (sets to '0') the corresponding bit(s) and a write of '0' has no effect.
R/WC/S	Read / Write Clear / Sticky bit(s). These bits can be read. Internal events may set this bit. A write of '1' clears (sets to '0') the corresponding bit(s) and a write of '0' has no effect. Bits are not cleared by "warm" reset, but will be reset with a cold/complete reset (for PCI Express* related bits a cold reset is "Power Good Reset" as defined in the *PCI Express* Specification*).
R/W/K	Read / Write / Key bit(s). These bits can be read and written by software. Additionally this bit when set, prohibits some other bit field(s) from being writeable (bit fields become Read Only).
R/W/L	Read / Write / Lockable bit(s). These bits can be read and written. Additionally there is a bit (which may or may not be a bit marked R/W/L) that, when set, prohibits this bit field from being writeable (bit field becomes Read Only).
R/W/S	Read / Write / Sticky bit(s). These bits can be read and written. Bits are not cleared by "warm" reset, but will be reset with a cold/complete reset (for PCI Express related bits a cold reset is "Power Good Reset" as defined in the *PCI Express* Specification*).
R/WSC	Read / Write Self Clear bit(s). These bits can be read and written. When the bit is '1', hardware may clear the bit to '0' based upon internal events, possibly sooner than any subsequent read could retrieve a '1'.
R/WSC/L	Read / Write Self Clear / Lockable bit(s). These bits can be read and written. When the bit is '1', hardware may clear the bit to '0' based upon internal events, possibly sooner than any subsequent read could retrieve a '1'. Additionally there is a bit (which may or may not be a bit marked R/W/L) that, when set, prohibits this bit field from being writeable (bit field becomes Read Only).
R/WO	Write Once bit(s). Once written, bits with this attribute become Read Only. These bits can only be cleared by a Reset.
W	Write Only. Whose bits may be written, but will always-return zeros when read. They are used for write side effects. Any data written to these registers cannot be retrieved.
B/D/F/Type	Bus/Device/Function/Type.

4.2 Configuration Process and Registers

4.2.1 Platform Configuration Structure

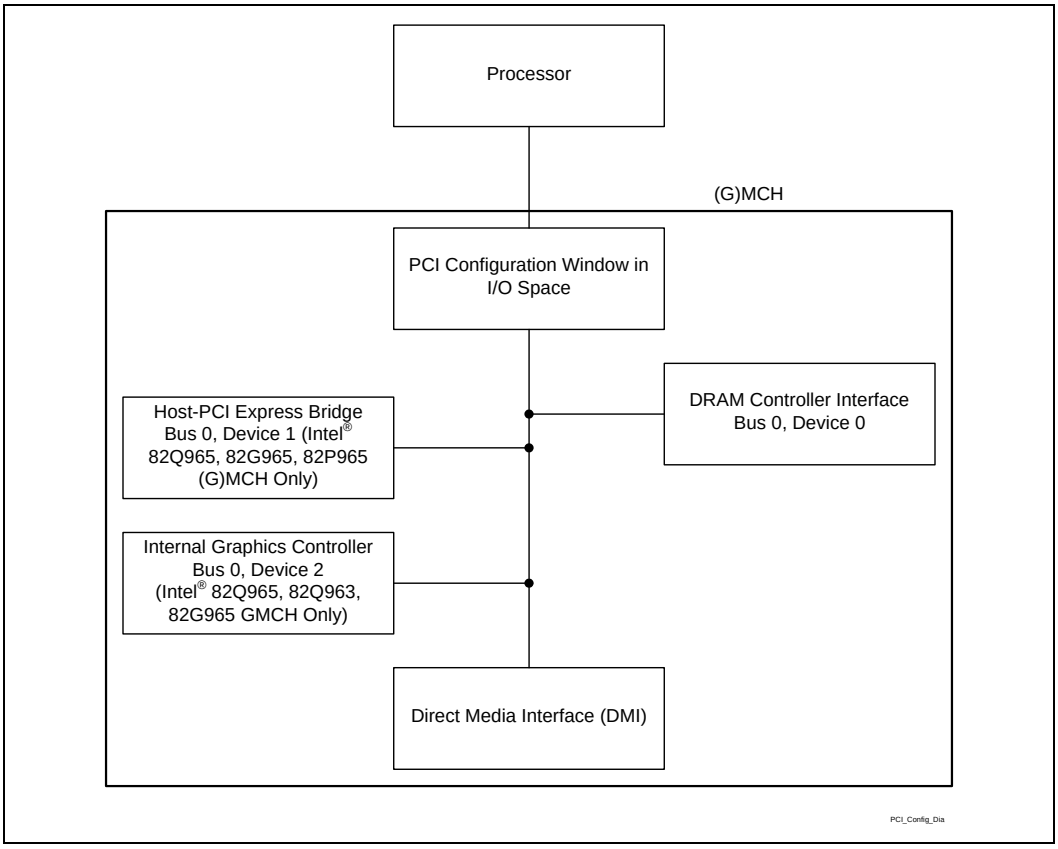
The DMI physically connects the (G)MCH and ICH8; thus, from a configuration standpoint, the DMI is logically PCI bus 0. As a result, all devices internal to the (G)MCH and the ICH8 appear to be on PCI bus 0.

Note: The ICH8 internal LAN controller does not appear on bus 0; it appears on the external PCI bus (whose number is configurable).

The system's primary PCI expansion bus is physically attached to the ICH8 and, from a configuration perspective, appears to be a hierarchical PCI bus behind a PCI-to-PCI bridge and therefore has a programmable PCI Bus number. The PCI Express Graphics Attach appears to system software to be a real PCI bus behind a PCI-to-PCI bridge that is a device resident on PCI bus 0.

Note: A physical PCI bus 0 does not exist and that DMI and the internal devices in the (G)MCH and ICH8 logically constitute PCI Bus 0 to configuration software. This is shown in Figure 4-1.

Figure 4-1. Conceptual Platform PCI Configuration Diagram



The (G)MCH contains four PCI devices within a single physical component. The configuration registers for the three devices are mapped as devices residing on PCI bus 0.

- **Device 0: Host Bridge/DRAM Controller.** Logically, this appears as a PCI device residing on PCI bus 0. Device 0 contains the standard PCI header registers, PCI Express base address register, DRAM control (including thermal/throttling control), and configuration for the DMI and other (G)MCH specific registers.
- **Device 1: Host-PCI Express Bridge (82Q965, 82G965, 82P965 (G)MCH only).** Logically this appears as a "virtual" PCI-to-PCI bridge residing on PCI bus 0 and is compliant with *PCI Express* Specification* Rev 1.1. Device 1 contains the standard PCI-to-PCI bridge registers and the standard PCI Express/PCI configuration registers (including the PCI Express memory address mapping). It also contains Isochronous and Virtual Channel controls in the PCI Express extended configuration space.
- **Device 2: Internal Graphics Control (82Q965, 82Q963, 82G965 GMCH only).** Logically, this appears as a PCI device residing on PCI bus 0. Physically, device 2 contains the configuration registers for 3D, 2D, and display functions.
- **Device 3: Manageability Engine Device**. Logically, this appears as a PCI device residing on PCI bus 0; physically, device 3.

4.3 Configuration Mechanisms

The processor is the originator of configuration cycles; thus, the FSB is the only interface in the platform where these mechanisms are used. Internal to the (G)MCH transactions received through both configuration mechanisms are translated to the same format.

4.3.1 Standard PCI Configuration Mechanism

The following is the mechanism for translating processor I/O bus cycles to configuration cycles.

The PCI specification defines a slot based "configuration space" that allows each device to contain up to 8 functions with each function containing up to 256 8-bit configuration registers. The PCI specification defines two bus cycles to access the PCI configuration space: Configuration Read and Configuration Write. Memory and I/O spaces are supported directly by the processor. Configuration space is supported by a mapping mechanism implemented within the (G)MCH.

The configuration access mechanism makes use of the CONFIG_ADDRESS Register (at I/O address 0CF8h though 0CFBh) and CONFIG_DATA Register (at I/O address 0CFCh though 0CFFh). To reference a configuration register a DW I/O write cycle is used to place a value into CONFIG_ADDRESS that specifies the PCI bus, the device on that bus, the function within the device and a specific configuration register of the device function being accessed. CONFIG_ADDRESS[31] must be 1 to enable a configuration cycle. CONFIG_DATA then becomes a window into the four bytes of configuration space specified by the contents of CONFIG_ADDRESS. Any read or write to CONFIG_DATA will result in the (G)MCH translating the CONFIG_ADDRESS into the appropriate configuration cycle.

The (G)MCH is responsible for translating and routing the processor's I/O accesses to the CONFIG_ADDRESS and CONFIG_DATA registers to internal (G)MCH configuration registers, DMI or PCI Express.

4.3.2 PCI Express* Enhanced Configuration Mechanism (Intel® 82Q965, 82G965, 82P965 (G)MCH Only)

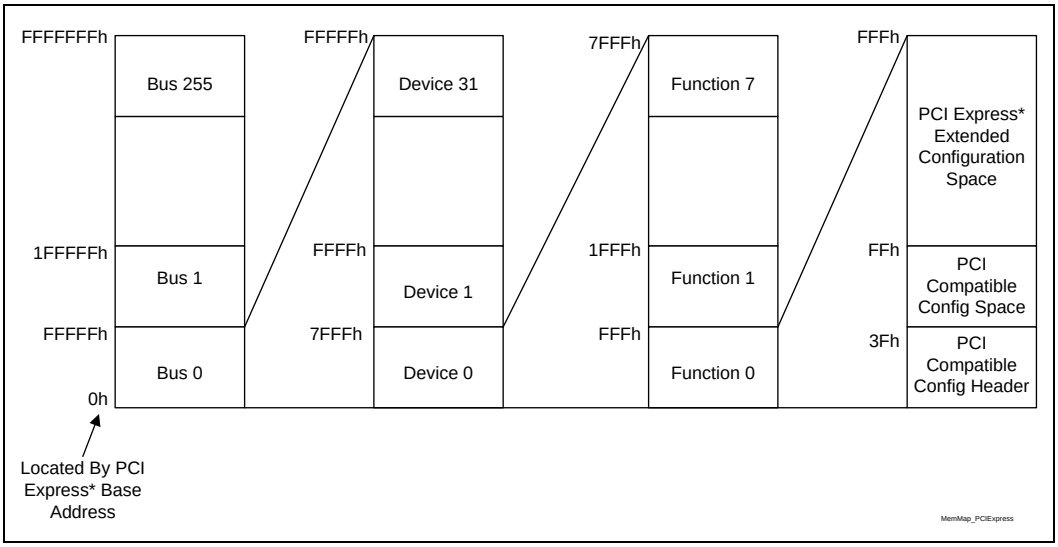
PCI Express extends the configuration space to 4096 bytes per device/function as compared to 256 bytes allowed by the PCI Specification, Revision 2.3. PCI Express configuration space is divided into a PCI 2.3 compatible region consisting of the first 256B of a logical device's configuration space and a PCI Express extended region that consists of the remaining configuration space.

The PCI compatible region can be accessed using either the Standard PCI configuration mechanism or using the PCI Express enhanced configuration mechanism described in this section. The extended configuration registers may only be accessed using the PCI Express enhanced configuration mechanism. To maintain compatibility with PCI configuration addressing mechanisms, system software must access the extended configuration space using 32-bit operations (32-bit aligned) only. These 32-bit operations include byte enables allowing only appropriate bytes within the DWord to be accessed. Locked transactions to the PCI Express memory-mapped configuration address space are not supported. All changes made using either access mechanism are equivalent.

The PCI Express enhanced configuration mechanism uses a flat memory-mapped address space to access device configuration registers. This address space is reported by the system firmware to the operating system. The PCI EXPRESS*XBAR register defines the base address for the block of addresses below 4 GB for the configuration space associated with busses, devices, and functions that are potentially a part of the PCI Express root complex hierarchy. Control bits In the PCI EXPRESS*XBAR register limit the size of this reserved memory mapped space; 256 MB is the amount of address space required to reserve space for every bus, device, and function that could possibly exist. Options for 128 MB and 64 MB exist in order to free up those addresses for other uses. In these cases the number of busses and all of their associated devices and functions are limited to 128 or 64 busses respectively.

The PCI Express Configuration Transaction Header includes an additional 4 bits (ExtendedRegisterAddress[3:0]) between the Function Number and Register Address fields to provide indexing into the 4 KB of configuration space allocated to each potential device. For PCI Compatible Configuration Requests, the Extended Register Address field must be all zeros.

Figure 4-2. Memory Map to PCI Express* Device Configuration Space



As with PCI devices, each device is selected based on decoded address information that is provided as a part of the address portion of Configuration Request packets. A PCI Express device will decode all address information fields (bus, device, function and extended address numbers) to provide access to the correct register.

To access this space (steps 1, 2, 3 are performed only once by BIOS):

1. Use the PCI compatible configuration mechanism to enable the PCI Express enhanced configuration mechanism by writing 1 to bit 0 of the PCI EXPRESS*XBAR register.

2. Use the PCI compatible configuration mechanism to write an appropriate PCI Express base address into the PCI EXPRESS*XBAR register

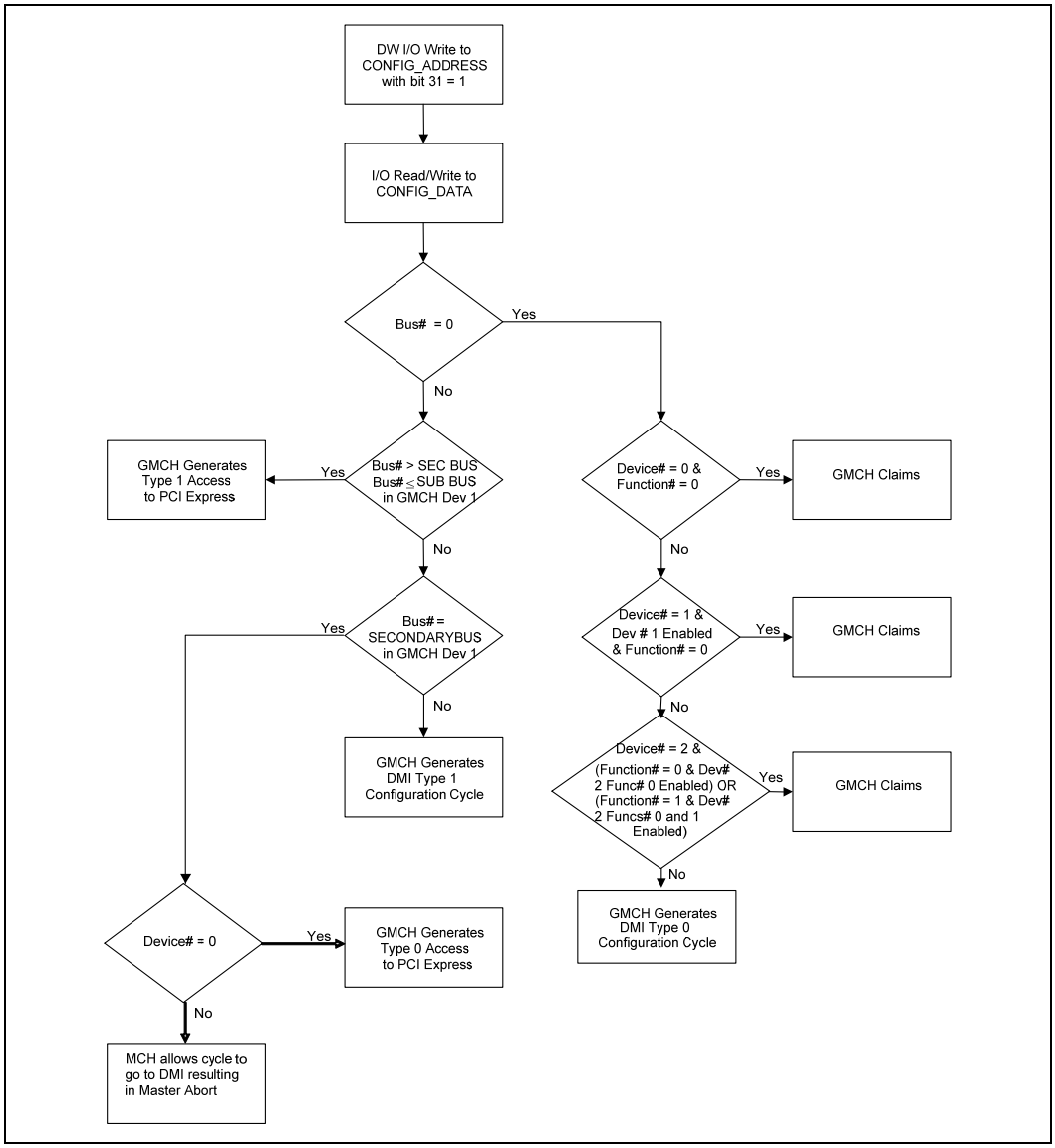
3. Calculate the host address of the register you wish to set using (PCI Express base + (bus number * 1 MB) + (device number * 32 KB) + (function number * 4 KB) + (1 B * offset within the function) = host address)

4. Use a memory write or memory read cycle to the calculated host address to write or read that register.

4.4 Routing Configuration Accesses

The (G)MCH supports two PCI related interfaces: DMI and PCI Express (82Q965, 82G965, 82P965 (G)MCH only). The (G)MCH is responsible for routing PCI and PCI Express configuration cycles to the appropriate device that is an integrated part of the (G)MCH or to one of these two interfaces. Configuration cycles to the ICH8 internal devices and Primary PCI (including downstream devices) are routed to the ICH8 via DMI. Configuration cycles to both the PCI Express Graphics PCI compatibility configuration space and the PCI Express Graphics extended configuration space are routed to the PCI Express Graphics port device or associated link.

Figure 4-3. GMCH Configuration Cycle Flow Chart



4.4.1 Internal Device Configuration Accesses

The (G)MCH decodes the Bus Number (bits 23:16) and the Device Number fields of the CONFIG_ADDRESS register. If the Bus Number field of CONFIG_ADDRESS is 0 the configuration cycle is targeting a PCI Bus 0 device.

If the targeted PCI Bus 0 device exists in the (G)MCH and is not disabled, the configuration cycle is claimed by the appropriate device.

4.4.2 Bridge Related Configuration Accesses

Configuration accesses on PCI Express or DMI are PCI Express configuration TLPs (Transaction Layer Packets).

- Bus Number [7:0] is Header Byte 8 [7:0]
- Device Number [4:0] is Header Byte 9 [7:3]
- Function Number [2:0] is Header Byte 9 [2:0]

And special fields for this type of TLP:

- Extended Register Number [3:0] is Header Byte 10 [3:0]
- Register Number [5:0] is Header Byte 11 [7:2]

See the PCI Express specification for more information on both the PCI 2.3 compatible and PCI Express Enhanced configuration mechanism and transaction rules.

4.4.2.1.1 PCI Express* Configuration Accesses (Intel® 82Q965, 82G965, 82P965 (G)MCH Only)

When the Bus Number of a type 1 Standard PCI configuration cycle or PCI Express enhanced configuration access matches the Device 1 Secondary Bus Number a PCI Express type 0 configuration TLP is generated on the PCI Express link targeting the device directly on the opposite side of the link. This should be Device 0 on the bus number assigned to the PCI Express link (likely Bus 1).

The device on other side of link must be Device 0. The (G)MCH will Master Abort any type 0 configuration access to a non-zero device number. If there is to be more than one device on that side of the link, there must be a bridge implemented in the downstream device.

When the Bus Number of a type 1 Standard PCI configuration cycle or PCI Express enhanced configuration access is within the claimed range (between the upper bound of the bridge device's Subordinate Bus Number register and the lower bound of the bridge device's Secondary Bus Number register) but does not match the Device 1 Secondary Bus Number, a PCI Express type 1 configuration TLP is generated on the secondary side of the PCI Express link.

PCI Express Configuration Writes:

- Internally the host interface unit will translate writes to PCI Express extended configuration space to configuration writes on the backbone.
- Writes to extended space are posted on the FSB, but non-posted on the PCI Express or DMI (i.e., translated to configuration writes)

4.4.2.1.2 DMI Configuration Accesses

Accesses to disabled (G)MCH internal devices, bus numbers not claimed by the Host-PCI Express bridge, or PCI Bus 0 devices not part of the (G)MCH will subtractively decode to the ICH8 and consequently be forwarded over the DMI via a PCI Express configuration TLP.

If the Bus Number is zero, the (G)MCH will generate a Type 0 configuration cycle TLP on DMI. If the Bus Number is non-zero, and falls outside the range claimed by the Host-PCI Express bridge, the (G)MCH will generate a Type 1 configuration cycle TLP on DMI.

The ICH8 routes configurations accesses in a manner similar to the (G)MCH. The ICH8 decodes the configuration TLP and generates a corresponding configuration access. Accesses targeting a device on PCI Bus 0 may be claimed by an internal device. The ICH8 compares the non-zero Bus Number with the Secondary Bus Number and Subordinate Bus Number registers of its PCI-to-PCI bridges to determine if the configuration access is meant for primary PCI, or some other downstream PCI bus or PCI Express link.

Configuration accesses that are forwarded to the ICH8, but remain unclaimed by any device or bridge will result in a master abort.

4.5 I/O Mapped Registers

The (G)MCH contains two registers that reside in the processor I/O address space – the Configuration Address (CONFIG_ADDRESS) register and the Configuration Data (CONFIG_DATA) register. The Configuration Address register enables/disables the configuration space and determines what portion of configuration space is visible through the configuration data window.

4.5.1 CONFIG_ADDRESS—Configuration Address Register

I/O Address: 0CF8h Accessed as a DW
Default Value: 00000000h
Access: R/W
Size: 32 bits

CONFIG_ADDRESS is a 32-bit register that can be accessed only as a DWord. A Byte or Word reference will "pass through" the Configuration Address register and DMI onto the primary PCI bus as an I/O cycle. The CONFIG_ADDRESS register contains the Bus Number, Device Number, Function Number, and Register Number for which a subsequent configuration access is intended.

Bit	Access & Default	Description
31	R/W 0b	**Configuration Enable (CFGE)** 0 = Disable. Accesses to PCI configuration space are disabled. 1 = Enable. Accesses to PCI configuration space are enabled.
30:24		Reserved

Bit	Access & Default	Description
23:16	R/W 00h	**Bus Number.** If the Bus Number is programmed to 00h the target of the Configuration Cycle is a PCI Bus 0 agent. If this is the case and the (G)MCH is not the target (i.e., the device number is ≥ 2), then a DMI Type 0 configuration cycle is generated. If the Bus Number is non-zero, and does not fall within the ranges enumerated by device 1's Secondary Bus Number or Subordinate Bus Number Register, then a DMI Type 1 configuration cycle is generated. If the Bus Number is non-zero and matches the value programmed into the Secondary Bus Number Register of device 1, a Type 0 PCI configuration cycle will be generated on PCI Express-G. If the Bus Number is non-zero, greater than the value in the Secondary Bus Number Register of device 1 and less than or equal to the value programmed into the Subordinate Bus Number Register of device 1, a Type 1 PCI configuration cycle will be generated on PCI Express-G. This field is mapped to byte 8 [7:0] of the request header format during PCI Express Configuration cycles and A[23:16] during the DMI Type 1 configuration cycles.
15:11	R/W 00h	**Device Number.** This field selects one agent on the PCI bus selected by the Bus Number. When the Bus Number field is 00h, the (G)MCH decodes the Device Number field. The (G)MCH is always Device Number 0 for the Host bridge entity, Device Number 1 for the Host-PCI Express entity. Therefore, when the Bus Number =0 and the Device Number equals 0, 1, or 2, the internal (G)MCH devices are selected. This field is mapped to byte 6 [7:3] of the request header format during PCI Express Configuration cycles and A [15:11] during the DMI configuration cycles.
10:8	R/W 000b	**Function Number.** This field allows the configuration registers of a particular function in a multi-function device to be accessed. The (G)MCH ignores configuration cycles to its internal devices if the function number is not equal to 0 or 1. This field is mapped to byte 6 [2:0] of the request header format during PCI Express Configuration cycles and A[10:8] during the DMI configuration cycles.
7:2	R/W 00h	**Register Number.** This field selects one register within a particular Bus, Device, and Function as specified by the other fields in the Configuration Address Register. This field is mapped to byte 7 [7:2] of the request header format during PCI Express Configuration cycles and A[7:2] during the DMI Configuration cycles.
1:0		Reserved

4.5.2 CONFIG_DATA—Configuration Data Register

I/O Address: 0CFCh
Default Value: 00000000h
Access: R/W
Size: 32 bits

CONFIG_DATA is a 32-bit read/write window into configuration space. The portion of configuration space that is referenced by CONFIG_DATA is determined by the contents of CONFIG_ADDRESS.

Bit	Access & Default	Description
31:0	R/W 0000 0000h	**Configuration Data Window (CDW).** If bit 31 of CONFIG_ADDRESS is 1, any I/O access to the CONFIG_DATA register will produce a configuration transaction using the contents of CONFIG_ADDRESS to determine the bus, device, function, and offset of the register to be accessed.

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5 Host Bridge/DRAM Controller Registers (Device 0, Function 0)

This chapter provides register descriptions for the Host Bridge/DRAM Controller registers, MCHBAR registers, and MEBAR registers.

5.1 Host Bridge/DRAM Controller Configuration Register Details (Device 0, Function 0)

The DRAM Controller registers are in Device 0 (D0), Function 0 (F0). Table 5-1 provides an address map of the D0:F0 registers listed by address offset in ascending order.

Warning: Address locations that are not listed are considered Intel Reserved registers locations. Reads to Reserved registers may return non-zero values. Writes to reserved locations may cause system failures.

All registers that are defined in the PCI 2.3 specification, but are not necessary or implemented in this component are simply not included in this document. The reserved/unimplemented space in the PCI configuration header space is not documented as such in this summary.

Table 5-1. DRAM Controller Register Address Map (Device 0, Function 0)

Address Offset	Symbol	Register Name	Default Value	Access
00–01h	VID	Vendor Identification	8086h	RO
02–03h	DID	Device Identification	2980h	RO
04–05h	PCICMD	PCI Command	0006h	RO, R/W
06–07h	PCISTS	PCI Status	0090h	RO, R/WC
08h	RID	Revision Identification	See register description	RO
09–0Bh	CC	Class Code	060000h	RO
0Dh	MLT	Master Latency Timer	00h	RO
0Eh	HDR	Header Type	00h	RO
2C–2Dh	SVID	Subsystem Vendor Identification	0000h	R/WO
2E–2Fh	SID	Subsystem Identification	0000h	R/WO

Address Offset	Symbol	Register Name	Default Value	Access
34–34h	CAPPTR	Capabilities Pointer	E0h	RO
40–47h	PXPEPBAR	PCI Express* Egress Port Base Address (82Q965, 82G965, 82P965 (G)MCH Only)	000000000 0000000h	R/W, RO
48–4Fh	MCHBAR	(G)MCH Memory Mapped Register Range Base	000000000 0000000h	R/W, RO
52–53h	GGC	GMCH Graphics Control Register (82Q965, 82Q963, 82G965 GMCH Only)	0030h	RO, R/W/L, R/W
54–57h	DEVEN	Device Enable	000003DBh	RO, R/W/L
60–67h	PCI EXPRESS*XBAR	PCI Express Register Range Base Address (82Q965, 82G965, 82P965 (G)MCH Only)	00000000E 0000000h	RW/L R/W/K, R/W, RO
68–6Fh	DMIBAR	Root Complex Register Range Base Address	000000000 0000000h	R/W, RO
90–90h	PAM0	Programmable Attribute Map 0	00h	RO, R/W
91h	PAM1	Programmable Attribute Map 1	00h	RO, R/W
92h	PAM2	Programmable Attribute Map 2	00h	RO, R/W
93h	PAM3	Programmable Attribute Map 3	00h	RO, R/W
94h	PAM4	Programmable Attribute Map 4	00h	RO, R/W
95h	PAM5	Programmable Attribute Map 5	00h	RO, R/W
96h	PAM6	Programmable Attribute Map 6	00h	RO, R/W
97h	LAC	Legacy Access Control	00h	R/W, RO
98–99h	REMAPBASE	Remap Base Address Register	03FFh	RO, R/W
9A–9Bh	REMAPLIMIT	Remap Limit Address Register	0000h	RO, R/W
9D–9Dh	SMRAM	System Management RAM Control	02h	RO, R/W/L, R/W/L/K
9E–9Eh	ESMRAMC	Extended System Management RAM Control	38h	R/W/L, R/WC, RO
A0–A1h	TOM	Top of Memory	0001h	RO, R/W/L
A2–A3h	TOUUD	Top of Upper Usable DRAM	0000h	R/W/L
A4–ABh	GBSM	Graphics Base of Stolen Memory (82Q965/82Q963/82G965 GMCH Only)	000000000 0000000h	RO, R/W/L
AC–AFh	TSEGMB	TSEG Memory Base	00000000h	R/W/L, RO

Address Offset	Symbol	Register Name	Default Value	Access
B0–B1h	TOLUD	Top of Low Usable DRAM	0010h	R/W/L, RO
C8–C9h	ERRSTS	Error Status	0000h	RO, R/WC/S
CA–CBh	ERRCMD	Error Command	0000h	RO, R/W
CC–CDh	SMICMD	SMI Command	0000h	RO, RW
DC–DFh	SKPD	Scratchpad Data	00000000h	R/W
E0–E9h	CAPID0	Capability Identifier	000000000 000010900 09h	RO

5.1.1 VID—Vendor Identification

B/D/F/Type: 0/0/0/PCI
Address Offset: 00–01h
Default Value: 8086h
Access: RO
Size: 16 bits

This register combined with the Device Identification register uniquely identifies any PCI device.

Bit	Access & Default	Description
15:0	RO 8086h	**Vendor Identification Number (VID):** This field is the PCI standard identification for Intel.

5.1.2 DID—Device Identification

B/D/F/Type: 0/0/0/PCI
Address Offset: 02–03h
Default Value: 2980h
Access: RO
Size: 16 bits

This register combined with the Vendor Identification register uniquely identifies any PCI device.

Bit	Access & Default	Description
15:0	RO 2980h	**Device Identification Number (DID):** This field is the identifier assigned to the (G)MCH core/primary PCI device. I

5.1.3 PCICMD—PCI Command

B/D/F/Type: 0/0/0/PCI
Address Offset: 04–05h
Default Value: 0006h
Access: RO, R/W
Size: 16 bits

Since (G)MCH Device 0 does not physically reside on PCI_A many of the bits are not implemented.

Bit	Access & Default	Description
15:10	RO 00h	Reserved
9	RO 0b	**Fast Back-to-Back Enable (FB2B):** This bit controls whether or not the master can do fast back-to-back writes. Since device 0 is strictly a target, this bit is not implemented and is hardwired to 0.
8	R/W 0b	**SERR Enable (SERRE):** This bit is a global enable bit for Device 0 SERR messaging. The (G)MCH does not have a SERR signal. The (G)MCH communicates the SERR condition by sending an SERR message over DMI to the ICH. 0 = Disable. The SERR message is **Not** generated by the (G)MCH for Device 0. 1 = Enable. The (G)MCH generates SERR messages over DMI for specific Device 0 error conditions that are individually enabled in the ERRCMD and DMIUEMSK registers. The error status is reported in the ERRSTS, PCISTS, and DMIUEST registers. Note that this bit only controls SERR messaging for the Device 0. Device 1 has its own SERRE bits to control error reporting for error conditions occurring in that device. The control bits are used in a logical OR manner to enable the SERR DMI message mechanism.
7	RO 0b	**Address / Data Stepping Enable (ADSTEP):** Not implemented, hardwired to a 0.
6	R/W 0b	**Parity Error Enable (PERRE)**: This bit controls whether or not the Master Data Parity Error bit in the PCI Status register can bet set. 0 = Disable. 1 = Enable.
5	RO 0b	**VGA Palette Snoop Enable (VGASNOOP):** Not implemented, hardwired to a 0.
4	RO 0b	**Memory Write and Invalidate Enable (MWIE):** The (G)MCH will never issue memory write and invalidate commands. This bit is therefore hardwired to 0.
3	RO 0b	Reserved
2	RO 1b	**Bus Master Enable (BME):** The (G)MCH is always enabled as a master on the backbone. This bit is hardwired to 1.
1	RO 1b	**Memory Access Enable (MAE):** The (G)MCH always allows access to main memory. This bit is not implemented and is hardwired to 1.
0	RO 0b	**I/O Access Enable (IOAE):** Not implemented, hardwired to a 0.

5.1.4 PCISTS—PCI Status

B/D/F/Type: 0/0/0/PCI
Address Offset: 06–07h
Default Value: 0090h
Access: RO, R/WC
Size: 16 bits

This status register reports the occurrence of error events on Device 0's PCI interface. Since the (G)MCH Device 0 does not physically reside on PCI_A many of the bits are not implemented.

Bit	Access & Default	Description
15	RO 0b	**Detected Parity Error (DPE):** This bit is set when this Device receives a Poisoned TLP.
14	R/WC 0b	**Signaled System Error (SSE):** Software clears this bit by writing a 1 to it. 1 = (G)MCH Device 0 generated a SERR message over DMI for any enabled Device 0 error condition. Device 0 error conditions are enabled in the PCICMD, ERRCMD, and DMIUEMSK registers. Device 0 error flags are read/reset from the PCISTS, ERRSTS, or DMIUEST registers.
13	R/WC 0b	**Received Master Abort Status (RMAS):** Software clears this bit by writing a 1 to it. 1 = (G)MCH generated a DMI request that receives an Unsupported Request completion packet.
12	R/WC 0b	**Received Target Abort Status (RTAS):** Software clears this bit by writing a 1 to it. 1 = (G)MCH generated a DMI request that receives a Completer Abort completion packet.
11	RO 0b	**Signaled Target Abort Status (STAS):** Not implemented, hardwired to a 0. The (G)MCH will not generate a Target Abort DMI completion packet or Special Cycle.
10:9	RO 00b	**DEVSEL Timing (DEVT):** These bits are hardwired to 00. Device 0 does not physically connect to PCI_A. These bits are set to 00 (fast decode) so that optimum DEVSEL timing for PCI_A is not limited by the (G)MCH.
8	R/WC 0b	**Master Data Parity Error Detected (DPD):** Software clears this bit by writing a 1 to it. 1 = DMI received a Poisoned completion from ICH8. **NOTE:** This bit can only be set when the Parity Error Enable bit in the PCI Command register is set.
7	RO 1b	**Fast Back-to-Back (FB2B):** Hardwired to 1. Device 0 does not physically connect to PCI_A. This bit is set to 1 (indicating fast back-to-back capability) so that the optimum setting for PCI_A is not limited by the (G)MCH.
6	RO 0b	Reserved
5	RO 0b	**66 MHz Capable:** Hardwired to 0. Does not apply to PCI Express.

Bit	Access & Default	Description
4	RO 1b	**Capability List (CLIST):** This bit is hardwired to 1 to indicate to the configuration software that this device/function implements a list of new capabilities. A list of new capabilities is accessed via register CAPPTR at configuration address offset 34h. Register CAPPTR contains an offset pointing to the start address within configuration space of this device where the Capability Identification register resides.
3:0	RO 0000b	Reserved

5.1.5 RID—Revision Identification

B/D/F/Type: 0/0/0/PCI
Address Offset: 8h
Default Value: See table description
Access: RO
Size: 8 bits

This register contains the revision number of the (G)MCH Device 0.

Bit	Access & Default	Description
7:0	RO	**Revision Identification Number (RID):** This is an 8-bit value that indicates the revision identification number for the (G)MCH Device 0. Refer to the *Intel® 965 Express Chipset Family Specification Update* for the value of the Revision ID register.

5.1.6 CC—Class Code

B/D/F/Type: 0/0/0/PCI
Address Offset: 09–0Bh
Default Value: 060000h
Access: RO
Size: 24 bits

This register identifies the basic function of the device, a more specific sub-class, and a register-specific programming interface.

Bit	Access & Default	Description
23:16	RO 06h	**Base Class Code (BCC):** This is an 8-bit value that indicates the base class code for the (G)MCH. 06h = Bridge device.
15:8	RO 00h	**Sub-Class Code (SUBCC):** This is an 8-bit value that indicates the category of Bridge into which the (G)MCH falls. 00h = Host Bridge.
7:0	RO 00h	**Programming Interface (PI):** This is an 8-bit value that indicates the programming interface of this device. This value does not specify a particular register set layout and provides no practical use for this device.

5.1.7 MLT—Master Latency Timer

B/D/F/Type: 0/0/0/PCI
Address Offset: Dh
Default Value: 00h
Access: RO
Size: 8 bits

Device 0 in the (G)MCH is not a PCI master. Therefore, this register is not implemented.

Bit	Access & Default	Description
7:0	RO 00h	Reserved

5.1.8 HDR—Header Type

B/D/F/Type: 0/0/0/PCI
Address Offset: Eh
Default Value: 00h
Access: RO
Size: 8 bits

This register identifies the header layout of the configuration space. No physical register exists at this location.

Bit	Access & Default	Description
7:0	RO 00h	**PCI Header (HDR):** This field always returns 0s to indicate that the (G)MCH is a single function device with standard header layout.

5.1.9 SVID—Subsystem Vendor Identification

B/D/F/Type: 0/0/0/PCI
Address Offset: 2C–2Dh
Default Value: 0000h
Access: R/WO
Size: 16 bits

This register is used to identify the vendor of the subsystem.

Bit	Access & Default	Description
15:0	R/WO 0000h	**Subsystem Vendor ID (SUBVID):** This field should be programmed during boot-up to indicate the vendor of the system board. After it has been written once, it becomes read only.

5.1.10 SID—Subsystem Identification

B/D/F/Type: 0/0/0/PCI
Address Offset: 2E–2Fh
Default Value: 0000h
Access: R/WO
Size: 16 bits

This value is used to identify a particular subsystem.

Bit	Access & Default	Description
15:0	R/WO 0000h	**Subsystem ID (SUBID):** This field should be programmed during BIOS initialization. After it has been written once, it becomes read only.

5.1.11 CAPPTR—Capabilities Pointer

B/D/F/Type: 0/0/0/PCI
Address Offset: 34h
Default Value: E0h
Access: RO
Size: 8 bits

The CAPPTR register provides an offset that is the pointer to the location of the first device capability in the capability list.

Bit	Access & Default	Description
7:0	RO E0h	**Capabilities Pointer (CAPPTR):** This field is a pointer to the offset of the first capability ID register block. In this case the first capability is the product-specific Capability Identifier (CAPID0).

5.1.12 PXPEPBAR—PCI Express* Egress Port Base Address (Intel® 82Q965/82G965/82P965 (G)MCH Only)

B/D/F/Type:	0/0/0/PCI
Address Offset:	40–47h
Default Value:	0000000000000000h
Access:	R/W, RO
Size:	64 bits

This is the base address for the PCI Express Egress Port MMIO Configuration space. There is no physical memory within this 4 KB window that can be addressed. The 4 KB reserved by this register does not alias to any PCI 2.3 compliant memory-mapped space. On reset, the EGRESS port MMIO configuration space is disabled and must be enabled by writing a 1 to PXPEPBAREN [Dev 0, offset 40h, bit 0].

Bit	Access & Default	Description
63:36	RO 0000000h	Reserved
35:12	R/W 000000h	**PCI Express Egress Port MMIO Base Address (PXPEPBAR):** This field corresponds to bits 35 to 12 of the base address PCI Express Egress Port MMIO configuration space. BIOS will program this register resulting in a base address for a 4 KB block of contiguous memory address space. This register ensures that a naturally aligned 4 KB space is allocated within the first 4 GB of addressable memory space. System Software uses this base address to program the (G)MCH MMIO register set. All the bits in this register are locked in LT mode.
11:1	RO 000h	Reserved
0	R/W 0b	**PXPEPBAR Enable (PXPEPBAREN):** 0 = Disable. PXPEPBAR does not claim any memory. 1 = Enable. PXPEPBAR memory mapped accesses are claimed and decoded appropriately.

5.1.13 MCHBAR—(G)MCH Memory-Mapped Register Range Base

B/D/F/Type: 0/0/0/PCI
Address Offset: 48–4Fh
Default Value: 0000000000000000h
Access: R/W, RO
Size: 64 bits

This is the base address for the (G)MCH memory-mapped configuration space. There is no physical memory within this 16 KB window that can be addressed. The 16 KB reserved by this register does not alias to any PCI 2.3 compliant memory mapped space. On reset, the (G)MCH MMIO memory-mapped configuration space is disabled and must be enabled by writing a 1 to MCHBAREN [Dev 0, offset 48h, bit 0].

Bit	Access & Default	Description
63:36	RO 0000000h	Reserved
35:14	R/W 000000h	**(G)MCH Memory Mapped Base Address (MCHBAR):** This field corresponds to bits 35 to 14 of the base address (G)MCH memory-mapped configuration space. BIOS will program this register resulting in a base address for a 16 KB block of contiguous memory address space. This register ensures that a naturally aligned 16 KB space is allocated within the first 4 GB of addressable memory space. System Software uses this base address to program the (G)MCH memory-mapped register set.
13:1	RO 0000h	Reserved
0	R/W 0b	**MCHBAR Enable (MCHBAREN):** 0 = Disable. MCHBAR does not claim any memory 1 = Enable. MCHBAR memory-mapped accesses are claimed and decoded appropriately.

5.1.14 GGC—GMCH Graphics Control Register (Intel® 82Q965, 82Q963, 82G965 GMCH Only)

B/D/F/Type: 0/0/0/PCI
Address Offset: 52–53h
Default Value: 0030h
Access: RO, R/W/L, R/W
Size: 16 bits

Bit	Access & Default	Description
15:7	RO 000h	Reserved
6:4	R/W/L 011b	**Graphics Mode Select (GMS):** This field is used to select the amount of main memory that is pre-allocated to support the internal graphics device in VGA (non-linear) and Native (linear) modes. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled. 000 = No memory pre-allocated. Device 2 (IGD) does not claim VGA cycles (Memory and I/O), and the Sub-Class Code field within Device 2:Function 0 Class Code register is 80. 001 = DVMT (UMA) mode, 1 MB of memory pre-allocated for frame buffer. 010 = Reserved 011 = DVMT (UMA) mode, 8 MB of memory pre-allocated for frame buffer. 100 = Reserved 101 = Reserved 110 = Reserved 111 = Reserved **NOTE:** This register is locked and becomes Read Only when the D_LCK bit in the SMRAM register is set.
3:2	RO 00b	Reserved
1	R/W 0b	**IGD VGA Disable (IVD):** 0 = Enable. Device 2 (IGD) claims VGA memory and I/O cycles, the Sub-Class Code within Device 2 Class Code register is 00. 1 = Disable. Device 2 (IGD) does not claim VGA cycles (Memory and I/O), and the Sub- Class Code field within Device 2 function 0 Class Code register is 80h.
0	RO 0b	Reserved

5.1.15 DEVEN—Device Enable

B/D/F/Type: 0/0/0/PCI
Address Offset: 54–57h
Default Value: 000003DBh
Access: RO, R/W/L
Size: 32 bits

This register enables/disables of PCI devices and functions that are within the (G)MCH.

Bit	Access & Default	Description
31:10	RO 0s	Reserved
9	R/W/L 1b	**ME Function 3 (D3F3EN):** If Device 3, Function 0 is disabled and hidden, then Device 3, Function 3 is also disabled and hidden independent of the state of this bit. 0 = Disable. Bus 0, Device 3, Function 3 is disabled and hidden 1 = Enable. Bus 0, Device 3, Function 3 is enabled and visible.
8	R/W/L 1b	**ME Function 2 (D3F2EN):** If Device 3, Function 0 is disabled and hidden, then Device 3, Function 2 is also disabled and hidden independent of the state of this bit. 0 = Disable. Bus 0, Device 3, Function 2 is disabled and hidden 1 = Enable. Bus 0, Device 3, Function 2 is enabled and visible.
7	RO 1b	Reserved
6	R/W/L 1b	**ME Function 0 (D3F0EN):** If the (G)MCH does not have ME capability, then Device 3, Function 0 is disabled and hidden independent of the state of this bit. 0 = Disable. Bus 0, Device 3, Function 0 is disabled and hidden 1 = Enable. Bus 0, Device 3, Function 0 is enabled and visible.
5	RO 0b	Reserved
4	R/W/L 1b	**82Q965 / 82Q963 / 82G965 GMCH** **Internal Graphics Engine Function 1 (D2F1EN):** If Device 2, Function 0 is disabled and hidden, then Device 2, Function 1 is also disabled and hidden independent of the state of this bit. 0 = Disable. Bus 0, Device 2, Function 1 is disabled and hidden 1 = Enable. Bus 0, Device 2, Function 1 is enabled and visible **82P965 MCH** Reserved.

Bit	Access & Default	Description
3	R/W/L 1b	**82Q965/82Q963/82G965 GMCH** **Internal Graphics Engine Function 0 (D2F0EN):** 0 = Disable. Bus 0, Device 2, Function 0 is disabled and hidden 1 = Enable. Bus 0, Device 2, Function 0 is enabled and visible **82P965 MCH** Reserved.
2	RO 0b	Reserved
1	R/W/L 1b	**82Q965/82G965/82P965 (G)MCH** **PCI Express Port (D1EN):** 0 = Disable. Bus 0, Device 1, Function 0 is disabled and hidden. 1 = Enable. Bus 0, Device 1, Function 0 is enabled and visible. **82Q963 GMCH** Reserved.
0	RO 1b	**Host Bridge (D0EN):** Hardwired to 1. Bus 0 Device 0, Function 0 can not be disabled.

5.1.16 PCI EXPRESS*XBAR—PCI Express* Register Range Base Address (Intel® 82Q965, 82G965, 82P965 (G)MCH Only)

B/D/F/Type: 0/0/0/PCI
Address Offset: 60–67h
Default Value: 00000000E0000000h
Access: R/W/L, R/W/K, R/W, RO
Size: 64 bits

This is the base address for the PCI Express configuration space. This window of addresses contains the 4 KB of configuration space for each PCI Express device that can potentially be part of the PCI Express Hierarchy associated with the (G)MCH. There is not actual physical memory within this window of up to 256 MB that can be addressed. The actual length is determined by a field in this register. Each PCI Express Hierarchy requires a PCI Express BASE register. The (G)MCH supports one PCI Express hierarchy. The region reserved by this register does not alias to any PCI 2.3 compliant memory mapped space. For example, MCHBAR reserves a 16 KB space and CHAPADR reserves a 4 KB space, both outside of PCI EXPRESS*XBAR space. They cannot be overlayed on the space reserved by PCI EXPRESS*XBAR for devices 0.

On reset, this register is disabled and must be enabled by writing a 1 to the enable field in this register. This base address shall be assigned on a boundary consistent with the number of buses (defined by the Length field in this register), above TOLUD and still within 64 bit addressable memory space. All other bits not decoded are read only and return a 0. The PCI Express Base Address cannot be less than the maximum address written to the top of physical memory register (TOLUD). Software must ensure that these ranges do not overlap with known ranges located above TOLUD. Software must ensure that the sum of length of enhanced configuration region + TOLUD + (other known ranges reserved above TOLUD) is not greater than the 64-bit

addressable limit of 64 GB. In general system implementation and number of PCI/PCI express buses supported in the hierarchy will dictate the length of the region.

Bit	Access & Default	Description
63:36	RO 0s	Reserved
35:28	R/W 0Eh	**PCI Express* Base Address (PCI EXPRESS*XBAR):** This field corresponds to bits 31:28 of the base address for PCI Express enhanced configuration space. BIOS will program this register resulting in a base address for a contiguous memory address space; size is defined by bits 2:1 of this register. This base address shall be assigned on a boundary consistent with the number of buses (defined by the Length field in this register) above TOLUD and still within 64-bit addressable memory space. The address bits decoded depend on the length of the region defined by this register. The address used to access the PCI Express configuration space for a specific device can be determined as follows: PCI Express Base Address + Bus Number * 1MB + Device Number * 32KB + Function Number * 4KB The address used to access PCI Express configuration space for Device 1 in this component would be PCI Express Base Address + 0 * 1MB + 1 * 32KB + 0 * 4KB = PCI Express Base Address + 32KB. Remember that this address is the beginning of the 4 KB space that contains both the PCI compatible configuration space and the PCI Express extended configuration space.
27	R/W/L 0b	**128 MB Base Address Mask (128ADMSK):** This bit is either part of the PCI Express Base Address (R/W) or part of the Address Mask (RO, read 0b), depending on the value of bits 2:1 in this register.
26	R/W/L 0b	**64 MB Base Address Mask (64ADMSK):** This bit is either part of the PCI Express Base Address (R/W) or part of the Address Mask (RO, read 0b), depending on the value of bits 2:1 in this register.
25:3	RO 000000h	Reserved
2:1	R/W/K 00b	**Length (LENGTH):** This Field describes the length of this region (enhanced configuration space region/buses decoded). 00 = 256 MB (buses 0–255h). Bits 31:28 are decoded in the PCI Express Base Address field 01 = 128 MB (Buses 0–127h). Bits 31:27 are decoded in the PCI Express Base Address field. 10 = 64 MB (Buses 0–63h). Bits 31:26 are decoded in the PCI Express Base Address field. 11 = Reserved

Bit	Access & Default	Description
0	R/W 0b	**PCI EXPRESS*XBAR Enable (PCI EXPRESS*XBAREN):** 0 = Disable the PCI EXPRESS*XBAR register. Memory read and write transactions proceed as if there were no PCI EXPRESS*XBAR register. PCI EXPRESS*XBAR bits 31:26 are R/W with no functionality behind them. 1 = Enable the PCI EXPRESS*XBAR register. Memory read and write transactions whose address bits 31:26 match PCI EXPRESS*XBAR will be translated to configuration reads and writes within the (G)MCH.

5.1.17 DMIBAR—Root Complex Register Range Base Address

B/D/F/Type: 0/0/0/PCI
Address Offset: 68–6Fh
Default Value: 0000000000000000h
Access: R/W, RO
Size: 64 bits

This is the base address for the Root Complex configuration space. This window of addresses contains the Root Complex Register set for the PCI Express Hierarchy associated with the (G)MCH. There is no physical memory within this 4 KB window that can be addressed. The 4 KB reserved by this register does not alias to any PCI 2.3 compliant memory mapped space. On reset, the Root Complex configuration space is disabled and must be enabled by writing a 1 to DMIBAREN.

Bit	Access & Default	Description
63:36	RO 0s	Reserved
35:12	R/W 0s	**DMI Base Address (DMIBAR):** This field corresponds to bits 35:12 of the base address DMI configuration space. BIOS will program this register resulting in a base address for a 4 KB block of contiguous memory address space. This register ensures that a naturally aligned 4 KB space is allocated within the first 64 GB of addressable memory space. System Software uses this base address to program the DMI register set.
11:1	RO 0s	Reserved
0	R/W 0b	**DMIBAR Enable (DMIBAREN):** 0 = DMIBAR is disabled and does not claim any memory 1 = DMIBAR memory mapped accesses are claimed and decoded appropriately

5.1.18 PAM0—Programmable Attribute Map 0

B/D/F/Type: 0/0/0/PCI
Address Offset: 90h
Default Value: 00h
Access: RO, R/W
Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS area from 0F0000h– 0FFFFFh. The (G)MCH allows programmable memory attributes on 13 Legacy memory segments of various sizes in the 768 KB to 1 MB address range. Seven Programmable Attribute Map (PAM) Registers are used to support these features. Cacheability of these areas is controlled via the MTRR registers in the P6 processor. Two bits are used to specify memory attributes for each memory segment. These bits apply to both host accesses and PCI initiator accesses to the PAM areas. These attributes are:

- RE - Read Enable. When RE = 1, the processor read accesses to the corresponding memory segment are claimed by the (G)MCH and directed to main memory. Conversely, when RE = 0, the host read accesses are directed to PCI_A.
- WE - Write Enable. When WE = 1, the host write accesses to the corresponding memory segment are claimed by the (G)MCH and directed to main memory. Conversely, when WE = 0, the host write accesses are directed to PCI_A.

The RE and WE attributes permit a memory segment to be read only, write only, read/write, or disabled. For example, if a memory segment has RE = 1 and WE = 0, the segment is read only. Each PAM Register controls two regions, typically 16 KB in size.

Note: The (G)MCH may hang if a PCI Express Graphics Attach (82Q965/82Q963/82G965 GMCH Only) or DMI originated access to Read Disabled or Write Disabled PAM segments occur (due to a possible IWB to non-DRAM).

For these reasons, the following critical restriction is placed on the programming of the PAM regions: At the time that a DMI or PCI Express Graphics Attach (82Q965/82Q963/82G965 GMCH Only) accesses to the PAM region may occur, the targeted PAM segment must be programmed to be both readable and writeable.

Bit	Access & Default	Description
7:6	RO 00b	Reserved
5:4	R/W 00b	**0F0000–0FFFFF Attribute (HIENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0F0000h to 0FFFFFh. 00 = DRAM Disabled: All accesses are directed to DMI. 01 = Read Only: All reads are sent to DRAM. All writes are forwarded to DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:0	RO 0h	Reserved

5.1.19 PAM1—Programmable Attribute Map 1

B/D/F/Type: 0/0/0/PCI
Address Offset: 91h
Default Value: 00h
Access: RO, R/W
Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0C0000h– 0C7FFFh.

Bit	Access & Default	Description
7:6	RO 00b	Reserved
5:4	R/W 00b	**0C4000–0C7FFF Attribute (HIENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0C4000h to 0C7FFFh. 00 = DRAM Disabled: All accesses are directed to DMI. 01 = Read Only: All reads are sent to DRAM. All writes are forwarded to DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:2	RO 00b	Reserved
1:0	R/W 00b	**0C0000–0C3FFF Attribute (LOENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0C0000h to 0C3FFFh. 00 = DRAM Disabled: All accesses are directed to DMI. 01 = Read Only: All reads are sent to DRAM. All writes are forwarded to DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM..

5.1.20 PAM2—Programmable Attribute Map 2

B/D/F/Type: 0/0/0/PCI
Address Offset: 92h
Default Value: 00h
Access: RO, R/W
Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0C8000h– 0CFFFFh.

Bit	Access & Default	Description
7:6	RO 00b	Reserved
5:4	R/W 00b	**0CC000–0CFFFF Attribute (HIENABLE):** 00 = DRAM Disabled: All accesses are directed to DMI. 01 = Read Only: All reads are sent to DRAM. All writes are forwarded to DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:2	RO 00b	Reserved
1:0	R/W 00b	**0C8000–0CBFFF Attribute (LOENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0C8000h to 0CBFFFh. 00 = DRAM Disabled: All accesses are directed to DMI. 01 = Read Only: All reads are sent to DRAM. All writes are forwarded to DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.

5.1.21 PAM3—Programmable Attribute Map 3

B/D/F/Type: 0/0/0/PCI
Address Offset: 93h
Default Value: 00h
Access: RO, R/W
Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0D0000h– 0D7FFFh.

Bit	Access & Default	Description
7:6	RO 00b	Reserved
5:4	R/W 00b	**0D4000–0D7FFF Attribute (HIENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0D4000h to 0D7FFFh. 00 = DRAM Disabled: All accesses are directed to DMI. 01 = Read Only: All reads are sent to DRAM. All writes are forwarded to DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:2	RO 00b	Reserved
1:0	R/W 00b	**0D0000–0D3FFF Attribute (LOENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0D0000h to 0D3FFFh. 00 = DRAM Disabled: All accesses are directed to DMI. 01 = Read Only: All reads are sent to DRAM. All writes are forwarded to DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.

5.1.22 PAM4—Programmable Attribute Map 4

B/D/F/Type: 0/0/0/PCI
Address Offset: 94h
Default Value: 00h
Access: RO, R/W
Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0D8000h– 0DFFFFh.

Bit	Access & Default	Description
7:6	RO 00b	Reserved
5:4	R/W 00b	**0DC000–0DFFFF Attribute (HIENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0DC000h to 0DFFFFh. 00 = DRAM Disabled: All accesses are directed to DMI. 01 = Read Only: All reads are sent to DRAM. All writes are forwarded to DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:2	RO 00b	Reserved
1:0	R/W 00b	**0D8000–0DBFFF Attribute (LOENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0D8000h to 0DBFFFh. 00 = DRAM Disabled: All accesses are directed to DMI. 01 = Read Only: All reads are sent to DRAM. All writes are forwarded to DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.

5.1.23 PAM5—Programmable Attribute Map 5

B/D/F/Type: 0/0/0/PCI
Address Offset: 95h
Default Value: 00h
Access: RO, R/W
Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0E0000h–0E7FFFh.

Bit	Access & Default	Description
7:6	RO 00b	Reserved
5:4	R/W 00b	**0E4000–0E7FFF Attribute (HIENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0E4000h to 0E7FFFh. 00 = DRAM Disabled: All accesses are directed to DMI. 01 = Read Only: All reads are sent to DRAM. All writes are forwarded to DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:2	RO 00b	Reserved
1:0	R/W 00b	**0E0000–0E3FFF Attribute (LOENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0E0000h to 0E3FFFh. 00 = DRAM Disabled: All accesses are directed to DMI. 01 = Read Only: All reads are sent to DRAM. All writes are forwarded to DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.

5.1.24 PAM6—Programmable Attribute Map 6

B/D/F/Type: 0/0/0/PCI
Address Offset: 96h
Default Value: 00h
Access: RO, R/W
Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0E8000h– 0EFFFFh.

Bit	Access & Default	Description
7:6	RO 00b	Reserved
5:4	R/W 00b	**0EC000–0EFFFF Attribute (HIENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0E4000h to 0E7FFFh. 00 = DRAM Disabled: All accesses are directed to DMI. 01 = Read Only: All reads are sent to DRAM. All writes are forwarded to DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:2	RO 00b	Reserved
1:0	R/W 00b	**0E8000–0EBFFF Attribute (LOENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0E0000h to 0E3FFFh. 00 = DRAM Disabled: All accesses are directed to DMI. 01 = Read Only: All reads are sent to DRAM. All writes are forwarded to DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.

5.1.25 LAC—Legacy Access Control

B/D/F/Type: 0/0/0/PCI
Address Offset: 97h
Default Value: 00h
Access: R/W, RO
Size: 8 bits

This 8-bit register controls a fixed DRAM hole from 15–16 MB.

Bit	Access & Default	Description
7	R/W 0b	**Hole Enable (HEN):** This field enables a memory hole in DRAM space. The DRAM that lies "behind" this space is not remapped. 0 =No memory hole. 1 = Memory hole from 15 MB to 16 MB.
6:1	RO 00h	Reserved

Bit	Access & Default	Description
0	R/W 0b	**MDA Present (MDAP):** This bit works with the VGA Enable bits in the BCTRL register of Device 1 to control the routing of processor-initiated transactions targeting MDA compatible I/O and memory address ranges. This bit should not be set if device 1's VGA Enable bit is not set. If device 1's VGA enable bit is not set, then accesses to I/O address range x3BCh–x3BFh are forwarded to DMI. If the VGA enable bit is set and MDA is not present, then accesses to I/O address range x3BCh–x3BFh are forwarded to PCI Express (82Q965, 82G965, 82P965 (G)MCH Only) if the address is within the corresponding IOBASE and IOLIMIT, otherwise they are forwarded to DMI. MDA resources are defined as the following: Memory: 0B0000h – 0B7FFFh I/O: 3B4h, 3B5h, 3B8h, 3B9h, 3BAh, 3BFh, (including ISA address aliases, A[15:10] are not used in decode) Any I/O reference that includes the I/O locations listed above, or their aliases, will be forwarded to the DMI even if the reference includes I/O locations not listed above. The following table shows the behavior for all combinations of MDA and VGA: **VGAEN / MDAP / Description** 0 / 0 / All References to MDA and VGA space are routed to DMI 0 / 1 / Invalid combination 1 / 0 / All VGA and MDA references are routed to PCI Express Graphics Attach (82Q965/82Q963/82G965 GMCH Only). 1 / 1 / All VGA references are routed to PCI Express Graphics Attach (82Q965/82Q963/82G965 GMCH Only). MDA references are routed to DMI. VGA and MDA memory cycles can only be routed across the PEG when MAE (PCICMD1[1]) is set. VGA and MDA I/O cycles can only be routed across the PEG if IOAE (PCICMD1[0]) is set.

5.1.26 REMAPBASE—Remap Base Address Register

B/D/F/Type: 0/0/0/PCI
Address Offset: 98–99h
Default Value: 03FFh
Access: RO, R/W
Size: 16 bits

Bit	Access & Default	Description
15:10	RO 000000b	Reserved
9:0	R/W 3FFh	**Remap Base Address [35:26] (REMAPBASE):** The value in this register defines the lower boundary of the Remap window. The Remap window is inclusive of this address. In the decoder A[25:0] of the Remap Base Address are assumed to be 0s. Thus, the bottom of the defined memory range will be aligned to a 64 MB boundary. When the value in this register is greater than the value programmed into the Remap Limit register, the Remap window is disabled. **Note:** Bit 0 (Address Bit 26) must be a 0.

5.1.27 REMAPLIMIT—Remap Limit Address Register

B/D/F/Type: 0/0/0/PCI
Address Offset: 9A–9Bh
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

Bit	Access & Default	Description
15:10	RO 000000b	Reserved
9:0	R/W 000h	**Remap Limit Address [35:26] (REMAPLMT):** The value in this register defines the upper boundary of the Remap window. The Remap window is inclusive of this address. In the decoder A[25:0] of the remap limit address are assumed to be Fhs. Thus, the top of the defined range will be one less than a 64 MB boundary. When the value in this register is less than the value programmed into the Remap Base register, the Remap window is disabled. **Note:** bit 0 (address bit 26) must be a 0.

5.1.28 SMRAM—System Management RAM Control

B/D/F/Type: 0/0/0/PCI
Address Offset: 9Dh
Default Value: 02h
Access: RO, R/W/L, R/W/L/K
Size: 8 bits

The SMRAMC register controls how accesses to Compatible and Extended SMRAM spaces are treated. The Open, Close, and Lock bits function only when G_SMRAME bit is set to a 1. Also, the OPEN bit must be reset before the LOCK bit is set.

Bit	Access & Default	Description
7	RO 0b	Reserved
6	R/W/L 0b	**SMM Space Open (D_OPEN):** When D_OPEN=1 and D_LCK=0, the SMM space DRAM is made visible even when SMM decode is not active. This is intended to help BIOS initialize SMM space. Software should ensure that D_OPEN=1 and D_CLS=1 are not set at the same time.
5	R/W/L 0b	**SMM Space Closed (D_CLS):** When D_CLS = 1 SMM space DRAM is not accessible to data references, even if SMM decode is active. Code references may still access SMM space DRAM. This will allow SMM software to reference through SMM space to update the display even when SMM is mapped over the VGA range. Software should ensure that D_OPEN=1 and D_CLS=1 are not set at the same time.
4	R/W/L/K 0b	**SMM Space Locked (D_LCK):** When D_LCK is set to 1, then D_OPEN is reset to 0 and D_LCK, D_OPEN, C_BASE_SEG, H_SMRAM_EN, TSEG_SZ and TSEG_EN become read only. D_LCK can be set to 1 via a normal configuration space write but can only be cleared by a Full Reset. The combination of D_LCK and D_OPEN provide convenience with security. The BIOS can use the D_OPEN function to initialize SMM space and then use D_LCK to "lock down" SMM space in the future so that no application software (or BIOS itself) can violate the integrity of SMM space, even if the program has knowledge of the D_OPEN function.
3	R/W/L 0b	**Global SMRAM Enable (G_SMRAME):** If set to a 1, then Compatible SMRAM functions are enabled, providing 128 KB of DRAM accessible at the A0000h address while in SMM (ADSB with SMM decode). To enable Extended SMRAM function this bit has be set to 1. Refer to the section on SMM for more details. Once D_LCK is set, this bit becomes read only.
2:0	RO 010b	**Compatible SMM Space Base Segment (C_BASE_SEG):** This field indicates the location of SMM space. SMM DRAM is not remapped. It is simply made visible if the conditions are right to access SMM space, otherwise the access is forwarded to DMI. Since the (G)MCH supports only the SMM space between A0000h and BFFFFh, this field is hardwired to 010.

5.1.29 ESMRAMC—Extended System Management RAM Control

B/D/F/Type: 0/0/0/PCI
Address Offset: 9Eh
Default Value: 38h
Access: R/W/L, R/WC, RO
Size: 8 bits

The Extended SMRAM register controls the configuration of Extended SMRAM space. The Extended SMRAM (E_SMRAM) memory provides a write-back cacheable SMRAM memory space that is above 1 MB.

Bit	Access & Default	Description
7	R/W/L 0b	**Enable High SMRAM (H_SMRAME):** This bit controls the SMM memory space location (i.e., above 1 MB or below 1 MB) When G_SMRAME is 1 and H_SMRAME is set to 1, the high SMRAM memory space is enabled. SMRAM accesses within the range 0FEDA0000h to 0FEDBFFFFh are remapped to DRAM addresses within the range 000A0000h to 000BFFFFh. Once D_LCK has been set, this bit becomes read only.
6	R/WC 0b	**Invalid SMRAM Access (E_SMERR):** This bit is set when the processor has accessed the defined memory ranges in Extended SMRAM (High Memory and T-segment) while not in SMM space and with the D-OPEN bit = 0. It is software's responsibility to clear this bit. The software must write a 1 to this bit to clear it.
5	RO 1b	**SMRAM Cacheable (SM_CACHE):** This bit is forced to 1 by the (G)MCH.
4	RO 1b	**L1 Cache Enable for SMRAM (SM_L1):** This bit is forced to 1 by the (G)MCH.
3	RO 1b	**L2 Cache Enable for SMRAM (SM_L2):** This bit is forced to 1 by the (G)MCH.

Bit	Access & Default	Description
2:1	R/W/L 00b	**TSEG Size (TSEG_SZ):** This field selects the size of the TSEG memory block if enabled. Memory from the top of DRAM space is partitioned away so that it may only be accessed by the processor interface and only then when the SMM bit is set in the request packet. Non-SMM accesses to this memory region are sent to DMI when the TSEG memory block is enabled. If Graphics stolen memory is placed above 4 GB, TSEG base is determined as if graphics stolen memory size is 0. 00 = 1 MB TSEG. (TOLUD – Graphics Stolen Memory Size – 1 MB) to (TOLUD – Graphics Stolen Memory Size). 01 = 2 MB TSEG. (TOLUD – Graphics Stolen Memory Size – 2 MB) to (TOLUD – Graphics Stolen Memory Size). 10 = 8 MB TSEG. (TOLUD – Graphics Stolen Memory Size – 8 MB) to (TOLUD – Graphics Stolen Memory Size). 11 = Reserved. Once D_LCK has been set, these bits becomes read only. **NOTE:** Graphics Stolen Memory is on the 82Q995, 82Q963, and 82G965 GMCH only.
0	R/W/L 0b	**TSEG Enable (T_EN):** This bit enables SMRAM memory for Extended SMRAM space only. When G_SMRAME = 1 and TSEG_EN = 1, TSEG is enabled to appear in the appropriate physical address space. Note that once D_LCK is set, this bit becomes read only.

5.1.30 TOM—Top of Memory

B/D/F/Type: 0/0/0/PCI
Address Offset: A0–A1h
Default Value: 0001h
Access: RO, R/W/L
Size: 16 bits

This register contains the size of physical memory. BIOS determines the memory size reported to the OS using this register.

Bit	Access & Default	Description
15:10	RO 00h	Reserved
9:0	R/W/L 001h	**Top of Memory (TOM):** This register reflects the total amount of populated physical memory. This is NOT necessarily the highest main memory address (holes may exist in main memory address map due to addresses allocated for memory mapped I/O). These bits correspond to address bits 35:26 (64 MB granularity). Bits 25:0 are assumed to be 0.

5.1.31 TOUUD—Top of Upper Usable DRAM

B/D/F/Type: 0/0/0/PCI
Address Offset: A2–A3h
Default Value: 0000h
Access: R/W/L
Size: 16 bits

This 16 bit register defines the Top of Upper Usable DRAM.

Bit	Access & Default	Description
15:0	R/W/L 0000h	**TOUUD (TOUUD):** This register contains bits 35:20 of an address one byte above the maximum DRAM memory above 4 GB that is usable by the operating system. Configuration software must set this value to TOM minus all ME stolen memory if reclaim is disabled. If reclaim is enabled, this value must be set to reclaim limit 64 MB aligned since reclaim limit is 64 MB aligned. Address bits 19:0 are assumed to be 000_0000h for the purposes of address comparison. The Host interface positively decodes an address towards system memory if the incoming address is less than the value programmed in this register and greater than 4 GB.

5.1.32 GBSM—Graphics Base of Stolen Memory (Intel® 82G965, 82Q965, 82063Q GMCH Only)

B/D/F/Type: 0/0/0/PCI
Address Offset: A4–ABh
Default Value: 0000000000000000h
Access: RO, R/W/L
Size: 64 bits

This register contains the base address of stolen DRAM memory.

Note: This register is locked and becomes read only when the D_LCK bit in the SMRAM register is set.

Bit	Access & Default	Description
63:32	RO 00000000h	Reserved
31:20	R/W/L 000h	**Graphics Base of Stolen Memory (GBSM):** This register contains bits 31:20 of the base address of stolen DRAM memory. BIOS determines the base of graphics stolen memory by subtracting the graphics stolen memory size (PCI Device 0, offset 52h, bits 6:4) from TOLUD (PCI Device 0, offset 9Ch, bits 7:2).
19:0	RO 00000h	Reserved

5.1.33 TSEGMB—TSEG Memory Base

B/D/F/Type: 0/0/0/PCI
Address Offset: AC–AFh
Default Value: 00000000h
Access: R/W/L, RO
Size: 32 bits

This register contains the base address of TSEG DRAM memory.

Bit	Access & Default	Description
31:20	R/W/L 000h	**TESG Memory base (TSEGMB):** This register contains bits 31:20 of the base address of TSEG DRAM memory. BIOS determines the base of TSEG memory by subtracting the TSEG size (PCI Device 0, offset 9Eh, bits 2:1) and the graphics stolen memory size (PCI Device 0, offset 52h, bits 6:4) from TOLUD (PCI Device 0, offset 9Ch, bits 7:2). Once D_LCK has been set, these bits become read only.
19:0	RO 00000h	Reserved

5.1.34 TOLUD—Top of Low Usable DRAM

B/D/F/Type:	0/0/0/PCI
Address Offset:	B0–B1h
Default Value:	0010h
Access:	R/W/L, RO
Size:	16 bits

This 16 bit register defines the Top of Low Usable DRAM. TSEG and Graphics Stolen Memory (if below 4 GB) are within the DRAM space defined. From the top, (G)MCH optionally claims 1 to 64 MBs of DRAM for internal graphics if enabled and 1, 2, or 8 MB of DRAM for TSEG if enabled.

Programming Example (82Q965/92963Q/82G965 GMCH Only)

C1DRB3 is set to 4 GB

TSEG is enabled and TSEG size is set to 1 MB

Internal Graphics is enabled, and Graphics Mode Select is set to 32 MB

BIOS knows the OS requires 1 GB of PCI space.

BIOS also knows the range from FEC0_0000h to FFFF_FFFFh is not usable by the system. This 20 MB range at the very top of addressable memory space is lost to APIC and LT.

According to the above equation, TOLUD is originally calculated to:
4 GB = 1_0000_0000h

The system memory requirements are: 4GB (max addressable space) – 1GB (PCI space) – 20MB (lost memory) = 3GB – 128MB (minimum granularity) = B800_0000h

Since B800_0000h (PCI and other system requirements) is less than 1_0000_0000h, TOLUD should be programmed to B80h.

Bit	Access & Default	Description
15:4	R/W/L 001h	**Top of Low Usable DRAM (TOLUD):** This register contains bits 31:20 of an address one byte above the maximum DRAM memory below 4 GB that is usable by the operating system. Address bits 31:20 programmed to 01h implies a minimum memory size of 1 MB. Configuration software must set this value to the smaller of the following 2 choices: maximum amount memory in the system minus ME stolen memory plus one byte or the minimum address allocated for PCI memory. Address bits 19:0 are assumed to be 0_0000h for the purposes of address comparison. The Host interface positively decodes an address towards DRAM if the incoming address is less than the value programmed in this register. This register must be 64 MB aligned when reclaim is enabled.
3:0	RO 0000b	Reserved

5.1.35 ERRSTS—Error Status

B/D/F/Type: 0/0/0/PCI
Address Offset: C8–C9h
Default Value: 0000h
Access: RO, R/WC/S
Size: 16 bits

This register is used to report various error conditions via the SERR DMI messaging mechanism. A SERR DMI message is generated on a 0-to-1 transition of any of these flags (if enabled by the ERRCMD and PCICMD registers).

These bits are set regardless of whether SERR is enabled and generated. After the error processing is complete, the error logging mechanism can be unlocked by clearing the appropriate status bit by software writing a 1 to it.

Bit	Access & Default	Description
15:13	RO 000b	Reserved
12	R/WC/S 0b	**(G)MCH Software Generated Event for SMI (GSGESMI):** 1 = The source of the SMI was a Device 2 Software Event.
11	R/WC/S 0b	**(G)MCH Thermal Sensor Event for SMI / SCI / SERR (GTSE):** The status bit is set only if a message is sent based on Thermal event enables in Error command, SMI command and SCI command registers. A trip point can generate one of SMI, SCI, or SERR interrupts (two or more per event is invalid). Multiple trip points can generate the same interrupt, if software chooses this mode, subsequent trips may be lost. If this bit is already set, then an interrupt message will not be sent on a new thermal sensor event. 1 = (G)MCH Thermal Sensor trip has occurred and an SMI, SCI or SERR has been generated.
10	RO 0b	Reserved
9	R/WC/S 0b	**LOCK to non-DRAM Memory Flag (LCKF):** 1 = (G)MCH has detected a lock operation to memory space that did not map into DRAM.
8	RO 0b	Reserved
7	R/WC/S 0b	**DRAM Throttle Flag (DTF):** 1 = Indicates that a DRAM Throttling condition occurred. 0 = Software has cleared this flag since the most recent throttling event.
6:0	RO 000h	Reserved

5.1.36 ERRCMD—Error Command

B/D/F/Type: 0/0/0/PCI
Address Offset: CA–CBh
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

This register controls the (G)MCH responses to various system errors. Since the (G)MCH does not have an SERR# signal, SERR messages are passed from the (G)MCH to the ICH8 over DMI.

When a bit in this register is set, a SERR message will be generated on DMI whenever the corresponding flag is set in the ERRSTS register. The actual generation of the SERR message is globally enabled for Device 0 via the PCI Command register.

Bit	Access & Default	Description
15:12	RO 0h	Reserved
11	R/W 0b	**GMCH Thermal Sensor Event for SMI / SCI / SERR (GTSE):** Indicates that a GMCH Thermal Sensor trip has occurred and an SMI, SCI or SERR has been generated. The status bit is set only if a message is sent based on Thermal event enables in Error command, SMI command and SCI command registers. A trip point can generate one of SMI, SCI, or SERR interrupts (two or more per event is invalid). Multiple trip points can generate the same interrupt, if software chooses this mode, subsequent trips may be lost. If this bit is already set, then an interrupt message will not be sent on a new thermal sensor event.
10	RO 0b	Reserved
9	R/W 0b	**LOCK to non-DRAM Memory Flag (LCKF):** When this bit is set to 1, the GMCH has detected a lock operation to memory space that did not map into DRAM.
8:0	RO 000h	Reserved

5.1.37 SMICMD—SMI Command

B/D/F/Type: 0/0/0/PCI
Address Offset: CC–CDh
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

This register enables the Thermal Sensor trip on the Hot trip point to generate an SMI DMI special cycle.

Note: Bit 11 of this register must be programmed to a 1.

Bit	Access & Default	Description
15:12	RO 0h	Reserved
11	R/W 0b	**SMI on GMCH Thermal Sensor Trip (TSTSMI):** 0 = Disable. Reporting of this condition via SMI messaging is disabled. 1 = Enable. A SMI DMI special cycle is generated by the MCH when the thermal sensor trip requires a SMI. A thermal sensor trip point cannot generate more than one special cycle.
10:0	RO 000h	Reserved

5.1.38 SKPD—Scratchpad Data

B/D/F/Type: 0/0/0/PCI
Address Offset: DC–DFh
Default Value: 00000000h
Access: R/W
Size: 32 bits

This register holds 32 writable bits with no functionality behind them. It is for the convenience of BIOS and graphics drivers.

Bit	Access & Default	Description
31:0	R/W 0s	**Scratchpad Data (SKPD):** 1 DWord of data storage.

5.1.39 CAPID0—Capability Identifier

B/D/F/Type: 0/0/0/PCI
Address Offset: E0–E9h
Default Value: 00000000000001090009h
Access: RO
Size: 80 bits

Bit	Access & Default	Description
79:26	RO 0000000000 0000h	Reserved
27:24	RO 1h	**CAPID Version (CAPIDV):** This field has the value 0001b to identify the first revision of the CAPID register definition.
23:16	RO 09h	**CAPID Length (CAPIDL):** This field has the value 09h to indicate the structure length (9 bytes).
15:8	RO 00h	**Next Capability Pointer (NCP):** This field is hardwired to 00h indicating the end of the capabilities linked list.
7:0	RO 09h	**Capability Identifier (CAP_ID):** This field has the value 1001b to identify the CAP_ID assigned by the PCI SIG for vendor dependent capability pointers.

5.2 MCHBAR Registers

The MCHBAR registers are offset from the MCHBAR base address. Table 5-2 provides an address map of the registers listed by address offset in ascending order. Detailed register bit descriptions follow the table.

Table 5-2. MCHBAR Register Address Map

Address Offset	Symbol	Register Name	Default Value	Access
111h	CHDECMISC	Channel Decode Miscellaneous	00h	R/W
200–201h	C0DRB0	Channel 0 DRAM Rank Boundary Address 0	0000h	R/W, RO
202–203h	C0DRB1	Channel 0 DRAM Rank Boundary Address 1	0000h	R/W, RO
204–205h	C0DRB2	Channel 0 DRAM Rank Boundary Address 2	0000h	RO, R/W
206–207h	C0DRB3	Channel 0 DRAM Rank Boundary Address 3	0000h	R/W, RO
208–209h	C0DRA01	Channel 0 DRAM Rank 0,1 Attribute	0000h	R/W
20A–20Bh	C0DRA23	Channel 0 DRAM Rank 2,3 Attribute	0000h	R/W
250–251h	C0CYCTRKPCHG	Channel 0 CYCTRK PCHG	0000h	R/W
252–255h	C0CYCTRKACT	Channel 0 CYCTRK ACT	00000000h	RO, R/W
256–257h	C0CYCTRKWR	Channel 0 CYCTRK WR	0000h	R/W
258–25Ah	C0CYCTRKRD	Channel 0 CYCTRK READ	000000h	RO, R/W
25B–25Ch	C0CYCTRKREFR	Channel 0 CYCTRK REFR	0000h	RO, R/W
260–263h	C0CKECTRL	Channel 0 CKE Control	00000800h	R/W
269–26Eh	C0REFRCTRL	Channel 0 DRAM Refresh Control	021830000 C30h	R/W, RO
29C–29Fh	C0ODTCTRL	Channel 0 ODT Control	00100000h	RO, R/W
600–601h	C1DRB0	Channel 1 DRAM Rank Boundary Address 0	0000h	R/W, RO
602–603h	C1DRB1	Channel 1 DRAM Rank Boundary Address 1	0000h	RO, R/W
604–605h	C1DRB2	Channel 1 DRAM Rank Boundary Address 2	0000h	R/W, RO
606–607h	C1DRB3	Channel 1 DRAM Rank Boundary Address 3	0000h	R/W, RO
608–609h	C1DRA01	Channel 1 DRAM Rank 0,1 Attributes	0000h	R/W

Address Offset	Symbol	Register Name	Default Value	Access
60A–60Bh	C1DRA23	Channel 1 DRAM Rank 2,3 Attributes	0000h	R/W
650–651h	C1CYCTRKPCHG	Channel 1 CYCTRK PCHG	0000h	R/W
652–655h	C1CYCTRKACT	Channel 1 CYCTRK ACT	00000000h	RO, R/W
656–657h	C1CYCTRKWR	Channel 1 CYCTRK WR	0000h	R/W,
658–65Ah	C1CYCTRKRD	Channel 1 CYCTRK READ	000000h	R/W, RO
660–663h	C1CKECTRL	Channel 1 CKE Control	00000800h	R/W
669–66Eh	C1REFRCTRL	Channel 1 DRAM Refresh Control	021830000 C30h	R/W, RO
69C–69Fh	C1ODTCTRL	Channel 1 ODT Control	00100000h	R/W, RO
A00–A01h	EPC0DRB0	ME Channel 0 DRAM Rank Boundary Address 0	0000h	R/W, RO
A02–A03h	EPC0DRB1	ME Channel 0 DRAM Rank Boundary Address 1	0000h	R/W, RO
A04–A05h	EPC0DRB2	ME Channel 0 DRAM Rank Boundary Address 2	0000h	R/W, RO
A06–A07h	EPC0DRB3	ME Channel 0 DRAM Rank Boundary Address 3	0000h	R/W, RO
A08–A09h	EPC0DRA01	ME Channel 0 DRAM Rank 0,1 Attribute	0000h	R/W
A0A–A0Bh	EPC0DRA23	ME Channel 0 DRAM Rank 2,3 Attribute	0000h	R/W
A19–A1Ah	EPDCYCTRKWRTPRE	MED CYCTRK WRT PRE	0000h	R/W, RO
A1C–A1Fh	EPDCYCTRKWRTACT	MED CYCTRK WRT ACT	00000000h	RO, R/W
A20–A21h	EPDCYCTRKWRTWR	MED CYCTRK WRT WR	0000h	R/W, RO
A24–A26h	EPDCYCTRKWRTRD	MED CYCTRK WRT READ	000000h	R/W,
A98h	EPDSRCTL	MEDunit Self refresh control	00h	R/W/SC, R/W/L
A28–A2Ch	EPDCKECONFIGREG	MED CKE related configuration registers	00E000000 0h	R/W
A2Eh	EPMEMSPACE	ME Memory space configuration	00h	R/W, RO
CD8h	TSC1	Thermal Sensor Control 1	00h	R/W/L, R/W, RS/WC
CD9h	TSC2	Thermal Sensor Control 2	00h	R/W/L, RO
CDAh	TSS	Thermal Sensor Status	00h	RO

Address Offset	Symbol	Register Name	Default Value	Access
CDCh–CDFh	TSTTP	Thermal Sensor Temperature Trip Point	00000000h	RO, R/W, R/W/L
CE2h	TCO	Thermal Calibration Offset	00h	R/W/L/K, R/W/L
CE4h	THERM1	Hardware Protection	00h	R/W/L, RO, R/W/L/K
CE6h	THERM3	TCO Fuses	00h	RS/WC, RO
CEA–CEBh	TIS	Thermal Interrupt Status	0000h	RO, R/WC
CF1h	TSMICMD	Thermal SMI Command	00h	RO, R/W
F14–F17h	PMSTS	Power Management Status	00000000h	R/WC/S, RO

5.2.1 CHDECMISC—Channel Decode Miscellaneous

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 111h
Default Value: 00h
Access: R/W
Size: 8 bits
BIOS Optimal Default 0h

This register has Miscellaneous CHDEC/MAGEN configuration bits.

Bit	Access & Default	Description
7:7	RO 0h	Reserved
6:5	R/W 00b	**Enhanced Mode Select (ENHMODESEL):** 00 = Swap Enabled for Bank Selects and Rank Selects 01 = Reserved 10 = Swap Enabled for Bank Selects only 11 = Reserved
4	RO 0b	Reserved
3	R/W 0b	**Ch1 Enhanced Mode (CH1 ENHMODE):** This bit enables Enhanced addressing mode of operation is enabled for Ch 1. 0 = Disable. 1 = Enable.
2	R/W 0b	**Ch0 Enhanced Mode (CH0 ENHMODE):** This bit indicates that enhanced addressing mode of operation is enabled of Ch 0. 0 = Disable. 1 = Enable.
1	R/W 0b	**Flex Memory (FLXMEM):** This bit disables Flex mode memory configuration. 0 = Disable. 1 = Enable.
0	R/W 0b	**ME Present (EPPRSNT):** This bit indicates whether ME UMA is present in the system. 0 = Not Present. 1 = Present.

5.2.2 C0DRB0—Channel 0 DRAM Rank Boundary Address 0

B/D/F/Type:	0/0/0/MCHBAR
Address Offset:	200–201h
Default Value:	0000h
Access:	R/W, RO
Size:	16 bits

The DRAM Rank Boundary Registers define the upper boundary address of each DRAM rank with a granularity of 64 MB. Each rank has its own single-word DRB register. These registers are used to determine which chip select will be active for a given address. Channel and rank map:

Ch 0, Rank 0 = 200h
Ch 0, Rank 1 = 202h
Ch 0, Rank 2 = 204h
Ch 0, Rank 3 = 206h
Ch 1, Rank 0 = 600h
Ch 1, Rank 1 = 602h
Ch 1, Rank 2 = 604h
Ch 1, Rank 3 = 606h

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If Channel 0 is empty, all of the C0DRBs are programmed with 00h.

C0DRB0 = Total memory in Ch 0, Rank 0 (in 64 MB increments)
C0DRB1 = Total memory in Ch 0, Rank 0 + Ch 0, Rank 1 (in 64 MB increments)
…

If Channel 1 is empty, all of the C1DRBs are programmed with 00h

C1DRB0= Total memory in Ch 1, Rank 0 (in 64 MB increments)
C1DRB1= Total memory in Ch 1, Rank 0 + Ch 1, Rank 1 (in 64 MB increments)
...

For Flex Memory Mode

C1DRB0, C1DRB1, and C1DRB2:

They are also programmed similar to non-Flex mode. Only exception is, the DRBs corresponding to the top most populated rank and higher ranks in Channel 1 must be programmed with the value of the total Channel 1 population plus the value of total Channel 0 population (C0DRB3).

Example: If only Ranks 0 and 1 are populated in Ch1 in Flex mode, then:

C1DRB0 = Total memory in Ch 1, Rank 0 (in 64MB increments)

C1DRB1 = C0DRB3 + Total memory in Ch 1, Rank 0 + Ch 1, Rank 1 (in 64 MB increments) (Rank 1 is the topmost populated rank)

C1DRB2 = C1DRB1

C1DRB3 = C1DRB1

C1DRB3:

C1DRB3 = C0DRB3 + Total memory in Channel 1.

Bit	Access & Default	Description
15:10	RO 000000b	Reserved
9:0	R/W 000h	**Channel 0 Dram Rank Boundary Address 0 (C0DRBA0):** This register defines the DRAM rank boundary for rank0 of Channel 0 (64 MB granularity) = R0 R0 = Total Rank 0 memory size is 64 MB R1 = Total Rank 1 memory size is 64 MB R2 = Total Rank 2 memory size is 64 MB R3 = Total Rank 3 memory size is 64 MB

5.2.3 C0DRB1—Channel 0 DRAM Rank Boundary Address 1

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 202–203h
Default Value: 0000h
Access: R/W, RO
Size: 16 bits

See C0DRB0 register for programming information.

Bit	Access & Default	Description
15:10	RO 000000b	Reserved
9:0	R/W 000h	**Channel 0 Dram Rank Boundary Address 1 (C0DRBA1):** This register defines the DRAM rank boundary for rank1 of Channel 0 (64 MB granularity) = (R1 + R0) R0 = Total Rank 0 memory size is 64 MB R1 = Total Rank 1 memory size is 64 MB R2 = Total Rank 2 memory size is 64 MB R3 = Total Rank 3 memory size is 64 MB

5.2.4 C0DRB2—Channel 0 DRAM Rank Boundary Address 2

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 204–205h
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

See C0DRB0 register for programming information.

Bit	Access & Default	Description
15:10	RO 000000b	Reserved
9:0	R/W 000h	**Channel 0 DRAM Rank Boundary Address 2 (C0DRBA2):** This register defines the DRAM rank boundary for rank2 of Channel 0 (64 MB granularity) = (R2 + R1 + R0) R0 = Total Rank 0 memory size is 64 MB R1 = Total Rank 1 memory size is 64 MB R2 = Total Rank 2 memory size is 64 MB R3 = Total Rank 3 memory size is 64 MB

5.2.5 C0DRB3—Channel 0 DRAM Rank Boundary Address 3

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 206–207h
Default Value: 0000h
Access: R/W, RO
Size: 16 bits

See C0DRB0 register for programming information.

Bit	Access & Default	Description
15:10	RO 000000b	Reserved
9:0	R/W 000h	**Channel 0 DRAM Rank Boundary Address 3 (C0DRBA3):** This register defines the DRAM rank boundary for rank3 of Channel 0 (64 MB granularity) = (R3 + R2 + R1 + R0) R0 = Total Rank 0 memory size is 64 MB R1 = Total Rank 1 memory size is 64 MB R2 = Total Rank 2 memory size is 64 MB R3 = Total Rank 3 memory size is 64 MB

5.2.6 C0DRA01—Channel 0 DRAM Rank 0,1 Attribute

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 208–209h
Default Value: 0000h
Access: R/W
Size: 16 bits

The DRAM Rank Attribute Registers define the page sizes/number of banks to be used when accessing different ranks. These registers should be left with their default value (all zeros) for any rank that is unpopulated, as determined by the corresponding CxDRB registers. Each byte of information in the CxDRA registers describes the page size of a pair of ranks. Channel and rank map:

Ch 0, Rank 0, 1= 208h–209h
Ch 0, Rank 2, 3 = 20Ah–20Bh
Ch 1, Rank 0, 1= 608h–609h
Ch 1, Rank 2, 3= 60Ah–60Bh

DRA[7:0] = "00" means Cfg 0 , DRA[7:0] ="01" means Cfg 1 .... DRA[7:0] = "09" means Cfg 9 and so on.

Table 5-3. DRAM Rank Attribute Register Programming

Cfg	Tech	DDRx	Depth	Width	Row	Col	Bank	Row Size	Page Size
0	256Mb	2	32M	8	13	10	2	256 MB	8K
1	256Mb	2	16M	16	13	9	2	128 MB	4K
2	512Mb	2	64M	8	14	10	2	512 MB	8k
3	512Mb	2	32M	16	13	10	2	256 MB	8k
4	512Mb	3	64M	8	13	10	3	512 MB	8k
5	512Mb	3	32M	16	12	10	3	256 MB	8k
6	1 Gb	2,3	128M	8	14	10	3	1 GB	8k
7	1 Gb	2,3	64M	16	13	10	3	512 MB	8k

Bit	Access & Default	Description
15:8	R/W 00h	**Channel 0 DRAM Rank-1 Attributes (C0DRA1):** This field defines DRAM pagesize/number-of-banks for rank1 for given channel. See Table 5-3 for programming.
7:0	R/W 00h	**Channel 0 DRAM Rank-0 Attributes (C0DRA0):** This field defines DRAM page size/number-of-banks for rank0 for given channel. See Table 5-3 for programming.

5.2.7 C0DRA23—Channel 0 DRAM Rank 2,3 Attribute

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 20A–20Bh
Default Value: 0000h
Access: R/W
Size: 16 bits

See C0DRA01 register for programming information.

Bit	Access & Default	Description
15:8	R/W 00h	**Channel 0 DRAM Rank-3 Attributes (CODRA3):** This register defines DRAM pagesize/number-of-banks for rank3 for given channel. See Table 5-3 for programming.
7:0	R/W 00h	**Channel 0 DRAM Rank-2 Attributes (CODRA2):** This register defines DRAM pagesize/number-of-banks for rank2 for given channel. See Table 5-3 for programming.

5.2.8 C0CYCTRKPCHG—Channel 0 CYCTRK Precharge

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 250–251h
Default Value: 0000h
Access: R/W
Size: 16 bits

This register provides Channel 0 CYCTRK Precharge.

Bit	Access & Default	Description
15:11	R/W 00000b	**ACT To PRE Delayed (C0sd_cr_act_pchg):** This configuration register indicates the minimum allowed spacing (in DRAM clocks) between the ACT and PRE commands to the same rank-bank. This field corresponds to t_{RAS} in the DDR specification.
10:6	R/W 00000b	**Write To PRE Delayed (C0sd_cr_wr_pchg):** This configuration register indicates the minimum allowed spacing (in DRAM clocks) between the WRITE and PRE commands to the same rank-bank. This register corresponds to t_{WR} in the DDR specification.
5:2	R/W 0000b	**READ To PRE Delayed (C0sd_cr_rd_pchg):** This configuration register indicates the minimum allowed spacing (in DRAM clocks) between the READ and PRE commands to the same rank-bank.
1:0	R/W 00b	**PRE To PRE Delayed (C0sd_cr_pchg_pchg):** This configuration register indicates the minimum allowed spacing (in DRAM clocks) between two PRE commands to the same rank.

5.2.9 C0CYCTRKACT—Channel 0 CYCTRK ACT

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 252–255h
Default Value: 00000000h
Access: RO, R/W
Size: 32 bits

This register provides Channel 0 CYCTRK Activate.

Bit	Access & Default	Description
31:28	RO 0h	Reserved
27:22	R/W 000000b	**ACT Window Count (C0sd_cr_act_windowcnt):** This field indicates the window duration (in DRAM clocks) during which the controller counts the # of activate commands that are launched to a particular rank. If the number of activate commands launched within this window is greater than 4, then a check is implemented to block launch of further activates to this rank for the rest of the duration of this window.
21	R/W 0b	**Max ACT Check (C0sd_cr_maxact_dischk):** This bit enables the check that ensures that there are no more than four activates to a particular rank in a given window. 0 = Disable 1 = Enable.
20:17	R/W 0000b	**ACT to ACT Delayed (C0sd_cr_act_act[):** This field indicates the minimum allowed spacing (in DRAM clocks) between two ACT commands to the same rank. This field corresponds to t_{RRD} in the DDR Specification.
16:13	R/W 0000b	**PRE to ACT Delayed (C0sd_cr_pre_act):** This field indicates the minimum allowed spacing (in DRAM clocks) between the PRE and ACT commands to the same rank-bank. This field indicates the minimum allowed spacing (in DRAM clocks) between the PRE-ALL and ACT commands to the same rank. This field corresponds to t_{RP} in the DDR specification.
12:9	R/W 0h	**ALLPRE to ACT Delay (C0sd0_cr_preall_act):** From the launch of a precharge all command wait for this many memory clocks before launching an Activate command. This field corresponds to t_{PALL_RP}.
8:0	R/W 000000000b	**REF to ACT Delayed (C0sd_cr_rfsh_act):** This configuration register indicates the minimum allowed spacing (in DRAM clocks) between REF and ACT commands to the same rank. This field corresponds to t_{RFC} in the DDR specification.

5.2.10 C0CYCTRKWR—Channel 0 CYCTRK WR

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 256–257h
Default Value: 0000h
Access: R/W
Size: 16 bits

This register provides Channel 0 CYCTRK WR control.

Bit	Access & Default	Description
15:12	R/W 0h	**ACT To Write Delay (C0sd_cr_act_wr):** This field indicates the minimum allowed spacing (in DRAM clocks) between the ACT and WRITE commands to the same rank-bank. This field corresponds to t_{RCD_wr} in the DDR specification.
11:8	R/W 0h	**Same Rank Write To Write Delayed (C0sd_cr_wrsr_wr):** This field indicates the minimum allowed spacing (in DRAM clocks) between two WRITE commands to the same rank.
7:4	R/W 0h	**Different Rank Write to Write Delay (C0sd_cr_wrdr_wr):** This field indicates the minimum allowed spacing (in DRAM clocks) between two WRITE commands to different ranks. This field corresponds to t_{WR_WR} in the DDR specification.
3:0	R/W 0h	**READ To WRTE Delay (C0sd_cr_rd_wr):** This field indicates the minimum allowed spacing (in DRAM clocks) between the READ and WRITE commands. This field corresponds to t_{RD_WR}.

5.2.11 C0CYCTRKRD—Channel 0 CYCTRK READ

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 258–25Ah
Default Value: 000000h
Access: RO, R/W
Size: 24 bits

This register provides Channel 0 CYCTRK RD control.

Bit	Access & Default	Description
23:20	RO 0h	Reserved
19:16	R/W 0h	**Min ACT To READ Delayed (C0sd_cr_act_rd):** This field indicates the minimum allowed spacing (in DRAM clocks) between the ACT and READ commands to the same rank-bank. This field corresponds to t_{RCD_rd} in the DDR specification.
15:11	R/W 00000b	**Same Rank Write To READ Delayed (C0sd_cr_wrsr_rd):** This field indicates the minimum allowed spacing (in DRAM clocks) between the WRITE and READ commands to the same rank. This field corresponds to t_{WTR} in the DDR Specification.

Bit	Access & Default	Description
10:8	R/W 000b	**Different Ranks Write To READ Delayed (C0sd_cr_wrdr_rd):** This field indicates the minimum allowed spacing (in DRAM clocks) between the WRITE and READ commands to different ranks. This field corresponds to t_{WR_RD} in the DDR specification.
7:4	R/W 0000b	**Same Rank Read To Read Delayed (C0sd_cr_rdsr_rd):** This configuration register indicates the minimum allowed spacing (in DRAM clocks) between two READ commands to the same rank.
3:0	R/W 0000b	**Different Ranks Read To Read Delayed (C0sd_cr_rddr_rd):** This configuration register indicates the minimum allowed spacing (in DRAM clocks) between two READ commands to different ranks. This field corresponds to t_{RD_RD}.

5.2.12 C0CYCTRKREFR—Channel 0 CYCTRK REFR

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 25B–25Ch
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

This register provides Channel 0 CYCTRK Refresh.

Bit	Access & Default	Description
15:13	RO 000b	Reserved.
12:9	R/W 0000b	**Same Rank PALL to REF Delayed (C0sd_cr_pchgall_rfsh):** This field indicates the minimum allowed spacing (in DRAM clocks) between the PRE-ALL and REF commands to the same rank.
8:0	R/W 000000000b	**Different Rank REF to REF Delayed (C0sd_cr_rfsh_rfsh):** This field indicates the minimum allowed spacing (in DRAM clocks) between two REF commands to same ranks.

5.2.13 C0CKECTRL—Channel 0 CKE Control

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 260–263h
Default Value: 00000800h
Access: R/W
Size: 32 bits

This register provides CKE controls for Channel 0.

Bit	Access & Default	Description
31:30	R/W 00b	**Number of Clocks from Internal ODT Command Start that ODT Read Safe will be Asserted (sd0_cr_odt_rdsafe):** Number of clocks from internal ODT command start that ODT Read Safe will be asserted.
29:28	R/W 00b	**Number of Clocks from Internal ODT Command Start that ODT Write Safe will be Asserted (sd0_cr_odt_wrsafe):** Number of clocks from internal ODT command start that ODT Write Safe will be asserted.
27	R/W 0b	**Start the Self-Refresh Exit Sequence (sd0_cr_srcstart):** This bit indicates the request to start the self-refresh exit sequence.
26:24	R/W 000b	**CKE Pulse Width Requirement in High Phase (sd0_cr_cke_pw_hl_safe):** This configuration register indicates CKE pulse width requirement in high phase. This field corresponds to tCKE (high) in the DDR specification.
23	R/W 0b	**Rank 3 Population (sd0_cr_rankpop3):** 0 = Not populated 1 = Populated
22	R/W 0b	**Rank 2 Population (sd0_cr_rankpop2):** 0 = Not populated 1 = Populated
21	R/W 0b	**Rank 1 Population (sd0_cr_rankpop1):** 0 = Not populated 1 = Populated
20	R/W 0b	**Rank 0 Population (sd0_cr_rankpop0):** 0 = Not populated 1 = Populated
19:17	R/W 000b	**CKE Pulse Width Requirement in Low Phase (sd0_cr_cke_pw_lh_safe):** This configuration register indicates CKE pulse width requirement in low phase. This field corresponds to t_{CKE} (low) in the DDR specification.
16	R/W 0b	**Enable CKE Toggle for PDN Entry/Exit (sd0_cr_pdn_enable):** This bit indicates that the toggling of CKEs (for PDN entry/exit) is enabled.
15	R/W 0b	**Read ODT Not Always Safe (sd0_cr_rdodtnas):** Internal Read ODT to CS is not always safe. Setting this bit selects the delay (programmable) in the ODT Read Safe register field.

Bit	Access & Default	Description
14	R/W 0b	**Write ODT Not Always Safe (sd0_cr_wrodtnas):** Internal Write ODT to CS is not always safe. Setting this bit selects the delay (programmable) in the ODT Write Safe register field.
13:10	R/W 0010b	**Minimum Power Down exit to Non-Read Command Spacing (sd0_cr_txp):** This field indicates the minimum number of clocks to wait following assertion of CKE before issuing a non-read command. 1010–1111 = Reserved 0010–1001 = 2–9 clocks 0000–0001 = Reserved
9:1	R/W 000000000b	**Self Refresh Exit Count (sd0_cr_slfrfsh_exit_cnt):** This field indicates the Self refresh exit count. (Program to 255). This field corresponds to t_{XSNR}/t_{XSRD} in the DDR specification.
0	R/W 0b	**Indicates only 1 DIMM Populated (sd0_cr_singledimmpop):** This bit, when set, indicates that only 1 DIMM is populated.

5.2.14 C0REFRCTRL—Channel 0 DRAM Refresh Control

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 269–26Eh
Default Value: 021830000C30h
Access: R/W, RO
Size: 48 bits

This register provides settings to configure the DRAM refresh controller.

Bit	Access & Default	Description
47:42	RO 00h	Reserved
41:37	R/W 10000b	**Direct Rcomp Quiet Window (DIRQUIET):** This field indicates the amount of refresh_tick events to wait before the service of rcomp request in non-default mode of independent rank refresh.
36:32	R/W 11000b	**Indirect Rcomp Quiet Window (INDIRQUIET):** This field indicates the amount of refresh_tick events to wait before the service of rcomp request in non-default mode of independent rank refresh.
31:27	R/W 00110b	**Rcomp Wait (RCOMPWAIT):** This field indicates the amount of refresh_tick events to wait before the service of rcomp request in non-default mode of independent rank refresh.
26	RO 0b	Reserved**:**
25	R/W 0b	**Refresh Counter Enable (REFCNTEN):** This bit enables the refresh counter to count during times that DRAM is not in self-refresh, but refreshes are not enabled. Such a condition may occur due to the need to reprogram DIMMs following a DRAM controller switch. This bit has no effect when Refresh is enabled (i.e., there is no mode where Refresh is enabled but the counter does not run). Thus, in conjunction with bit 23 REFEN, the modes are: **REFEN:REFCNTEN — Description** 0:0 — Normal refresh disable 0:1 — Refresh disabled, but counter is accumulating refreshes. 1:X — Normal refresh enable
24	R/W 0b	**All Rank Refresh (ALLRKREF):** This bit enables (by default) that all the ranks are refreshed in a staggered/atomic fashion. 0 = All the ranks are refreshed in a staggered/atomic fashion. 1 = Ranks are refreshed in an independent fashion.
23	R/W 0b	**Refresh Enable (REFEN):** 0 = Disabled 1 = Enabled
22	R/W 0b	**DDR Initialization Done (INITDONE):** This bit indicates that DDR initialization is complete. 0 = Not Done 1= Done

Bit	Access & Default	Description
21:20	RO 00b	Reserved
19:18	R/W 00b	**DRAM Refresh Panic Watermark (REFPANICWM):** When the refresh count exceeds this level, a refresh request is launched to the scheduler and the dref_panic flag is set. 00 = 5 01 = 6 10 = 7 11 = 8
17:16	R/W 00b	**DRAM Refresh High Watermark (REFHIGHWM):** When the refresh count exceeds this level, a refresh request is launched to the scheduler and the dref_high flag is set. 00 = 3 01 = 4 10 = 5 11 = 6
15:14	R/W 00b	**DRAM Refresh Low Watermark (REFLOWWM):** When the refresh count exceeds this level, a refresh request is launched to the scheduler and the dref_low flag is set. 00 = 1 01 = 2 10 = 3 11 = 4
13:0	R/W 001100001 10000b	**Refresh Counter Time Out Value (REFTIMEOUT):** Program this field with a value that will provide 7.8 us at the memory clock frequency. At various memory clock frequencies this results in the following values: 266 MHz -> 820 hex 333 MHz -> A28 hex 400 MHz -> C30 hex

5.2.15 C0ODTCTRL—Channel 0 ODT Control

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 29C–29Fh
Default Value: 00100000h
Access: RO, R/W
Size: 32 bits

This register provides ODT controls.

Bit	Access & Default	Description
31:24	RO 00h	Reserved
23:20	R/W 0001b	**MCH ODT Latency (sd0_cr_modtl):** Delay from CS# to (G)MCH ODT assertion. 0000 = Reserved 0001–1100 = 1–12clocks 1101–1111 = Reserved
19:17	R/W 000	**CAS latency (sd0_cr_casl):** Reserved (for CAS Latency) This field indicates the CAS latency of the memory population. This field is also termed as SDRAM to CAS latency. 000 = 3 memory clocks 001 = 4 memory clocks … 111 = 10 memory clocks
16:0	RO 00h	Reserved

5.2.16 C1DRB0—Channel 1 DRAM Rank Boundary Address 0

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 600–601h
Default Value: 0000h
Access: R/W, RO
Size: 16 bits

The operation of this register is detailed in the C0DRB0 register description.

Bit	Access & Default	Description
15:10	RO 000000b	Reserved
9:0	R/W 000h	**Channel 1 DRAM Rank Boundary Address 0 (C1DRBA0):** See C0DRB0 register. In Flex mode this is the topmost populated rank in Channel 1; program this value to be cumulative of Ch0 DRB3.

5.2.17 C1DRB1—Channel 1 DRAM Rank Boundary Address 1

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 602–603h
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

The operation of this register is detailed in the C0DRB0 register description.

Bit	Access & Default	Description
15:10	RO 000000b	Reserved
9:0	R/W 000h	**Channel 1 DRAM Rank Boundary Address 1 (C1DRBA1):** See C0DRB1 register. In Flex mode this is the topmost populated rank in Channel 1; program this value to be cumulative of Ch0 DRB3.

5.2.18 C1DRB2—Channel 1 DRAM Rank Boundary Address 2

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 604–605h
Default Value: 0000h
Access: R/W, RO
Size: 16 bits

The operation of this register is detailed in the C0DRB0 register description.

Bit	Access & Default	Description
15:10	RO 000000b	Reserved
9:0	R/W 000h	**Channel 1 DRAM Rank Boundary Address 2 (C1DRBA2):** See C0DRB2 register. In Flex mode this is the topmost populated rank in Channel 1; program this value to be cumulative of Ch0 DRB3.

5.2.19 C1DRB43—Channel 1 DRAM Rank Boundary Address 3

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 606–607h
Default Value: 0000h
Access: R/W, RO
Size: 16 bits

The operation of this register is detailed in the C0DRB0 register description.

Bit	Access & Default	Description
15:10	RO 000000b	Reserved
9:0	R/W 000h	**Channel 1 DRAM Rank Boundary Address 3 (C1DRBA3):** See C0DRB3 register. In Flex mode this is the topmost populated rank in Channel 1; program this value to be cumulative of Ch0 DRB3

5.2.20 C1DRA01—Channel 1 DRAM Rank 0,1 Attributes

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 608–609h
Default Value: 0000h
Access: R/W
Size: 16 bits

The operation of this register is detailed in the C0DRA01 register description.

Bit	Access & Default	Description
15:8	R/W 00h	**Channel 1 DRAM Rank-1 Attributes (C1DRA1):** See C0DRA1 register.
7:0	R/W 00h	**Channel 1 DRAM Rank-0 Attributes (C1DRA0):** See C0DRA0 register.

5.2.21 C1DRA23—Channel 1 DRAM Rank 2,3 Attributes

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 60A–60Bh
Default Value: 0000h
Access: R/W
Size: 16 bits

The operation of this register is detailed in the description for register C0DRA01.

Bit	Access & Default	Description
15:8	R/W 00h	**Channel 1 DRAM Rank-3 Attributes (C1DRA3):** See C0DRA3 register.
7:0	R/W 00h	**Channel 1 DRAM Rank-2 Attributes (C1DRA2):** See C0DRA2 register.

5.2.22 C1CYCTRKPCHG—Channel 1 CYCTRK PreCharge

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 650–651h
Default Value: 0000h
Access: R/W
Size: 16 bits

This register provides control for Channel 1 CYCTRK Precharge.

Bit	Access & Default	Description
15:11	R/W 00000b	**ACT To PRE Delayed (C1sd_cr_act_pchg):** This field indicates the minimum allowed spacing (in DRAM clocks) between the ACT and PRE commands to the same rank-bank. This field corresponds to t_{RAS} in the DDR Specification.
10:6	R/W 00000b	**Write To PRE Delayed (C1sd_cr_wr_pchg):** This field indicates the minimum allowed spacing (in DRAM clocks) between the WRITE and PRE commands to the same rank-bank. This field corresponds to t_{WR} in the DDR Specification.
5:2	R/W 0000b	**READ To PRE Delayed (C1sd_cr_rd_pchg):** This configuration register indicates the minimum allowed spacing (in DRAM clocks) between the READ and PRE commands to the same rank-bank.
1:0	R/W 00b	**PRE To PRE Delayed (C1sd_cr_pchg_pchg):** This configuration register indicates the minimum allowed spacing (in DRAM clocks) between two PRE commands to the same rank.

5.2.23 C1CYCTRKACT—Channel 1 CYCTRK ACT

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 652–655h
Default Value: 00000000h
Access: RO, R/W
Size: 32 bits

This register provides control for Channel 1 CYCTRK ACT.

Bit	Access & Default	Description
31:28	RO 0h	Reserved
27:22	R/W 000000b	**ACT Window Count (C1sd_cr_act_windowcnt):** This field indicates the window duration (in DRAM clocks) during which the controller counts the # of activate commands that are launched to a particular rank. If the number of activate commands launched within this window is greater than 4, then a check is implemented to block launch of further activates to this rank for the rest of the duration of this window.
21	R/W 0b	**Max ACT Check (C1sd_cr_maxact_dischk):** This field enables the check that ensures that there are no more than four activates to a particular rank in a given window. 0 = Disable 1 = Enable
20:17	R/W 0000b	**ACT to ACT Delayed (C1sd_cr_act_act[):** This field indicates the minimum allowed spacing (in DRAM clocks) between two ACT commands to the same rank. This field corresponds to t_{RRD} in the DDR specification.
16:13	R/W 0000b	**PRE to ACT Delayed (C1sd_cr_pre_act):** This field indicates the minimum allowed spacing (in DRAM clocks) between the PRE and ACT commands to the same rank-bank:12:9R/W0000bPRE-ALL to ACT Delayed (C1sd_cr_preall_act):This configuration register indicates the minimum allowed spacing (in DRAM clocks) between the PRE-ALL and ACT commands to the same rank. This field corresponds to tRP in the DDR specification.
12:9	R/W 0h	**ALLPRE to ACT Delay (C1sd_cr_preall_act):** From the launch of a precharge all command wait for this many memory clocks before launching an Activate command. This field corresponds to t_{PALL_RP}.
8:0	R/W 00000000 0b	**REF to ACT Delayed (C1sd_cr_rfsh_act):** This configuration register indicates the minimum allowed spacing (in DRAM clocks) between REF and ACT commands to the same rank. This field corresponds to t_{RFC} in the DDR specification.

5.2.24 C1CYCTRKWR—Channel 1 CYCTRK Write

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 656–657h
Default Value: 0000h
Access: R/W
Size: 16 bits

This register provides Channel 1 CYCTRK Write control.

Bit	Access & Default	Description
15:12	R/W 0h	**ACT To Write Delay (C1sd_cr_act_wr):** This field indicates the minimum allowed spacing (in DRAM clocks) between the ACT and WRITE commands to the same rank-bank This field corresponds to t_{RCD_wr} in the DDR Specification.
11:8	R/W 0h	**Same Rank Write To Write Delayed (C1sd_cr_wrsr_wr):** This field indicates the minimum allowed spacing (in DRAM clocks) between two WRITE commands to the same rank.
7:4	R/W 0h	**Different Rank Write to Write Delay (C1sd_cr_wrdr_wr):** This field indicates the minimum allowed spacing (in DRAM clocks) between two WRITE commands to different ranks. This field corresponds to t_{WR_WR} in the DDR specification.
3:0	R/W 0h	**READ To WRTE Delay (C1sd_cr_rd_wr):** This configuration register indicates the minimum allowed spacing (in DRAM clocks) between the READ and WRITE commands. This field corresponds to t_{RD_WR}.

5.2.25 C1CYCTRKRD—Channel 1 CYCTRK Read

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 658–65Ah
Default Value: 000000h
Access: R/W, RO
Size: 24 bits

This register provides Channel 1 CYCTRK Read control.

Bit	Access & Default	Description
23:20	RO 0h	Reserved
19:16	R/W 0h	**Min ACT To READ Delayed (C1sd_cr_act_rd):** This field indicates the minimum allowed spacing (in DRAM clocks) between the ACT and READ commands to the same rank-bank. This field corresponds to t_{RCD_rd} in the DDR Specification
15:11	R/W 00000b	**Same Rank Write To READ Delayed (C1sd_cr_wrsr_rd):** This field indicates the minimum allowed spacing (in DRAM clocks) between the WRITE and READ commands to the same rank. This field corresponds to t_{WTR} in the DDR specification.

Bit	Access & Default	Description
10:8	R/W 000b	**Different Ranks Write To READ Delayed (C1sd_cr_wrdr_rd):** This field indicates the minimum allowed spacing (in DRAM clocks) between the WRITE and READ commands to different ranks. This field corresponds to t_{WR_RD} in the DDR specification.
7:4	R/W 0000b	**Same Rank Read To Read Delayed (C1sd_cr_rdsr_rd):** This field indicates the minimum allowed spacing (in DRAM clocks) between two READ commands to the same rank.
3:0	R/W 0000b	**Different Ranks Read To Read Delayed (C1sd_cr_rddr_rd):** This field indicates the minimum allowed spacing (in DRAM clocks) between two READ commands to different ranks. This field corresponds to t_{RD_RD}.

5.2.26 C1CKECTRL—Channel 1 CKE Control

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 660–663h
Default Value: 00000800h
Access: R/W
Size: 32 bits

This register provides Channel 1 CKE control.

Bit	Access & Default	Description
31:30	R/W 00b	**Number of clocks from internal ODT command start that ODT Read Safe will be asserted (sd1_cr_odt_rdsafe):** This field determines the number of clocks from internal ODT command start that ODT Read Safe will be asserted.
29:28	R/W 00b	**Number of clocks from internal ODT command start that ODT Read Safe will be asserted (sd1_cr_odt_wrsafe):** This field determines the number of clocks from internal ODT command start that ODT Write Safe will be asserted.
27	R/W 0b	**start the self-refresh exit sequence (sd1_cr_srcstart):** This bit indicates the request to start the self-refresh exit sequence.
26:24	R/W 000b	**CKE pulse width requirement in high phase (sd1_cr_cke_pw_hl_safe):** This field indicates CKE pulse width requirement in high phase. This field corresponds to t_{CKE} (high) in the DDR specification.
23	R/W 0b	**Rank 3 Population (sd1_cr_rankpop3):** 0 = Rank 3 not populated 1 = Rank 3 populated
22	R/W 0b	**Rank 2 Population (sd1_cr_rankpop2):** 0 = Rank 2 not populated 1 = Rank 2 populated

Bit	Access & Default	Description
21	R/W 0b	**Rank 1 Population (sd1_cr_rankpop1):** 0 = Rank 1 not populated 1 = Rank 1 populated
20	R/W 0b	**Rank 0 Population (sd1_cr_rankpop0):** 0 = Rank 0 not populated 1 = Rank 0 populated
19:17	R/W 000b	**CKE pulse width requirement in low phase (sd1_cr_cke_pw_lh_safe):** This field indicates CKE pulse width requirement in low phase. This field corresponds to t_{CKE} (low) in the DDR specification.
16	R/W 0b	**Enable CKE toggle for PDN entry / exit (sd1_cr_pdn_enable):** This configuration bit indicates that the toggling of CKEs (for PDN entry/exit) is enabled.
15	R/W 0b	**Read ODT Not Always Safe (sd1_cr_rdodtnas):** Internal Read ODT to CS is not always safe. Setting this bit selects the delay (programmable) in the ODT Read Safe register field.
14	R/W 0b	**Write ODT Not Always Safe (sd1_cr_wrodtnas):** Internal Write ODT to CS is not always safe. Setting this bit selects the delay (programmable) in the ODT Write Safe register field.
13:10	R/W 0010b	**Minimum Power down Exit to Non-Read command spacing (sd1_cr_txp):** This field indicates the minimum number of clocks to wait following assertion of CKE before issuing a non-read command. 0000–0001=Reserved. 0010–1001=2-9 clocks 1010–1111= Reserved.
9:1	R/W 000000000b	**Self refresh exit count (sd1_cr_slfrfsh_exit_cnt):** This field indicates the Self refresh exit count. (Program to 255). This field corresponds to t_{XSNR}/t_{XSRD} in the DDR specification.
0	R/W 0b	**Indicates only 1 DIMM populated (sd1_cr_singledimmpop):** This field indicates the that only 1 DIMM is populated.

5.2.27 C1REFRCTRL—Channel 1 DRAM Refresh Control

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 669–66Eh
Default Value: 021830000C30h
Access: R/W, RO
Size: 48 bits

This register provides settings to configure the DRAM refresh controller.

Bit	Access & Default	Description
47:42	RO 00h	Reserved
41:37	R/W 10000b	**Direct Rcomp Quiet Window (DIRQUIET):** This configuration setting indicates the amount of refresh_tick events to wait before the service of rcomp request in non-default mode of independent rank refresh.
36:32	R/W 11000b	**Indirect Rcomp Quiet Window (INDIRQUIET):** This configuration setting indicates the amount of refresh_tick events to wait before the service of rcomp request in non-default mode of independent rank refresh.
31:27	R/W 00110b	**Rcomp Wait (RCOMPWAIT):** This configuration setting indicates the amount of refresh_tick events to wait before the service of rcomp request in non-default mode of independent rank refresh.
26	RO 0b	Reserved**:**
25	R/W 0b	**Refresh Counter Enable (REFCNTEN):** This bit is used to enable the refresh counter to count during times that DRAM is not in self-refresh, but refreshes are not enabled. Such a condition may occur due to need to reprogram DIMMs following DRAM controller switch. This bit has no effect when Refresh is enabled (i.e. there is no mode where Refresh is enabled but the counter does not run) So, in conjunction with bit 23 REFEN, the modes are: **REFEN:REFCNTEN** — **Description** 0:0 — Normal refresh disable 0:1 — Refresh disabled, but counter is accumulating refreshes 1:X — Normal refresh enable
24	R/W 0b	**All Rank Refresh (ALLRKREF):** This bit enables (by default) that all the ranks are refreshed in a staggered/atomic fashion. If set, the ranks are refreshed in an independent fashion.
23	R/W 0b	**Refresh Enable (REFEN):** Refresh is enabled. 0 = Disabled 1 = Enabled

Bit	Access & Default	Description
22	R/W 0b	**DDR Initialization Done (INITDONE):** This bit indicates that DDR initialization is complete. 0 = Not Done 1 = Done
21:20	RO 0b	Reserved
19:18	R/W 00b	**DRAM Refresh Panic Watermark (REFPANICWM):** When the refresh count exceeds this level, a refresh request is launched to the scheduler and the dref_panic flag is set. 00 = 5 01 = 6 10 = 7 11 = 8
17:16	R/W 00b	**DRAM Refresh High Watermark (REFHIGHWM):** When the refresh count exceeds this level, a refresh request is launched to the scheduler and the dref_high flag is set. 00 = 3 01 = 4 10 = 5 11 = 6
15:14	R/W 00b	**DRAM Refresh Low Watermark (REFLOWWM):** When the refresh count exceeds this level, a refresh request is launched to the scheduler and the dref_low flag is set. 00 = 1 01 = 2 10 = 3 11 = 4
13:0	R/W 001100001 10000b	**Refresh Counter Time Out Value (REFTIMEOUT):** Program this field with a value that will provide 7.8 us at the memory clock frequency. At various memory clock frequencies this results in the following values: 266 MHz -> 820h 333 MHz -> A28h 400 MHz -> C30h

5.2.28 C1ODTCTRL—Channel 1 ODT Control

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 69C–69Fh
Default Value: 00100000h
Access: R/W, RO
Size: 32 bits

This register provides ODT controls.

Bit	Access & Default	Description
31:24	RO 00h	Reserved
23:20	R/W 0001b	**MCH ODT Latency (sd1_cr_modtl):** Delay from CS# to (G)MCH ODT assertion. 0000 = Reserved 0001–1100 = 1–12 clocks 1101–1111 = Reserved
19:17	R/W 000b	**CAS latency (sd1_cr_casl):** This field indicates the CAS latency of the memory population. 000 = 3 memory clocks 001 = 4 memory clocks … 111 = 10 memory clocks Also, termed as SDRAM to CAS latency.
16:0	RO 00h	Reserved

5.2.29 EPC0DRB0—ME Channel 0 DRAM Rank Boundary Address 0

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: A00–A01h
Default Value: 0000h
Access: R/W, RO
Size: 16 bits

Bit	Access & Default	Description
15:10	RO 000000b	Reserved
9:0	R/W 000h	**Channel 0 Dram Rank Boundary Address 0 (C0DRBA0):**

5.2.30 EPC0DRB1—ME Channel 0 DRAM Rank Boundary Address 1

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: A02–A03h
Default Value: 0000h
Access: R/W, RO
Size: 16 bits

See the C0DRB0 register for programming details.

Bit	Access & Default	Description
15:10	RO 000000b	Reserved
9:0	R/W 000h	**Channel 0 Dram Rank Boundary Address 1 (C0DRBA1):**

5.2.31 EPC0DRB2—ME Channel 0 DRAM Rank Boundary Address 2

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: A04–A05h
Default Value: 0000h
Access: R/W, RO
Size: 16 bits

See the C0DRB0 register for programming details.

Bit	Access & Default	Description
15:10	RO 000000b	Reserved
9:0	R/W 000h	**Channel 0 DRAM Rank Boundary Address 2 (C0DRBA2):**

5.2.32 EPC0DRB3—ME Channel 0 DRAM Rank Boundary Address 3

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: A06–A07h
Default Value: 0000h
Access: R/W, RO
Size: 16 bits

See C0DRB0 register for programming details.

Bit	Access & Default	Description
15:10	RO 000000b	Reserved
9:0	R/W 000h	**Channel 0 DRAM Rank Boundary Address 3 (C0DRBA3):**

5.2.33 EPC0DRA01—ME Channel 0 DRAM Rank 0,1 Attribute

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: A08–A09h
Default Value: 0000h
Access: R/W,
Size: 16 bits

The DRAM Rank Attribute Registers define the page sizes/number of banks to be used when accessing different ranks. These registers should be left with their default value (all zeros) for any rank that is unpopulated, as determined by the corresponding CxDRB registers. Each byte of information in the CxDRA registers describes the page size of a pair of ranks. Channel and rank map:

Ch0, Rank0, 1 = 108h–109h
Ch0, Rank2, 3 = 10Ah–10Bh
Ch1, Rank0, 1 = 188h–189h
Ch1, Rank2, 3 = 18Ah–18Bh

Bit	Access & Default	Description
15:8	R/W 00h	**Channel 0 DRAM Rank-1 Attributes (C0DRA1):** This field defines DRAM pagesize/number-of-banks for rank1 for given channel
7:0	R/W 00h	**Channel 0 DRAM Rank-0 Attributes (C0DRA0):** This field defines DRAM pagesize/number-of-banks for rank0 for given channel

5.2.34 EPC0DRA23—ME Channel 0 DRAM Rank 2,3 Attribute

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: A0A–A0Bh
Default Value: 0000h
Access: R/W
Size: 16 bits

See C0DRA01 register for programming details.

Bit	Access & Default	Description
15:8	R/W 00h	**Channel 0 DRAM Rank-3 Attributes (CODRA3):** This field defines DRAM pagesize/number-of-banks for rank3 for given channel
7:0	R/W 00h	**Channel 0 DRAM Rank-2 Attributes (CODRA2):** This field defines DRAM pagesize/number-of-banks for rank2 for given channel
26	R/W 0b	**DDR Initialization Done (INITDONE):** This bit indicates that DDR initialization is complete. 0 = Not Done 1 = Done
25:0	RO 0000h	Reserved

5.2.35 EPDCYCTRKWRTPRE—MED CYCTRK WRT PRE

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: A19–A1Ah
Default Value: 0000h
Access: R/W, RO
Size: 16 bits

This is the EPD CYCTRK WRT PRE Status register.

Bit	Access & Default	Description
15:11	R/W 00000b	**ACT To PRE Delayed (C0sd_cr_act_pchg):** This field indicates the minimum allowed spacing (in DRAM clocks) between the ACT and PRE commands to the same rank-bank
10:6	R/W 00000b	**Write To PRE Delayed (C0sd_cr_wr_pchg):** This field indicates the minimum allowed spacing (in DRAM clocks) between the WRITE and PRE commands to the same rank-bank
5:2	R/W 0000b	**READ To PRE Delayed (C0sd_cr_rd_pchg):** This field indicates the minimum allowed spacing (in DRAM clocks) between the READ and PRE commands to the same rank-bank
1:0	RO 00b	Reserved:

5.2.36 EPDCYCTRKWRTACT—MED CYCTRK WRT ACT

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: A1C–A1Fh
Default Value: 00000000h
Access: RO, R/W
Size: 32 bits

This is the MED CYCTRK WRT ACT Status register.

Bit	Access & Default	Description
31:21	RO 000h	Reserved
20:17	R/W 0000b	**ACT to ACT Delayed (C0sd_cr_act_act[):** This field indicates the minimum allowed spacing (in DRAM clocks) between two ACT commands to the same rank.
16:13	R/W 0000b	**PRE to ACT Delayed (C0sd_cr_pre_act):** This field indicates the minimum allowed spacing (in DRAM clocks) between the PRE and ACT commands to the same rank-bank:
12:9	RO 0h	Reserved
8:0	R/W 000000000b	**REF to ACT Delayed (C0sd_cr_rfsh_act):** This field indicates the minimum allowed spacing (in DRAM clocks) between REF and ACT commands to the same rank.

5.2.37 EPDCYCTRKWRTWR—MED CYCTRK WRT WR

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: A20–A21h
Default Value: 0000h
Access: R/W, RO
Size: 16 bits

This is the EPD CYCTRK WRT WR status register.

Bit	Access & Default	Description
15:12	R/W 0h	**ACT To Write Delay (C0sd_cr_act_wr):** This field indicates the minimum allowed spacing (in DRAM clocks) between the ACT and WRITE commands to the same rank-bank.
11:8	R/W 0h	**Same Rank Write To Write Delayed (C0sd_cr_wrsr_wr):** This field indicates the minimum allowed spacing (in DRAM clocks) between two WRITE commands to the same rank.
7:4	RO 0h	Reserved
3:0	R/W 0h	**READ To WRTE Delay (C0sd_cr_rd_wr):** This field indicates the minimum allowed spacing (in DRAM clocks) between the READ and WRITE commands.

5.2.38 EPDCYCTRKWRTRD—MED CYCTRK WRT READ

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: A24–A26h
Default Value: 000000h
Access: R/W
Size: 24 bits
BIOS Optimal Default 000h

This is the MED CYCTRK WRT RD status register.

Bit	Access & Default	Description
23:23	RO 0h	Reserved
22:20	R/W 000b	**MEDunit DQS Slave DLL Enable to Read Safe (EPDSDLL2RD):** This field provides the setting for Read command safe from the point of enabling the slave DLLs.
19:18	RO 0h	Reserved
17:14	R/W 0h	**Min ACT To READ Delayed (C0sd_cr_act_rd):** This field indicates the minimum allowed spacing (in DRAM clocks) between the ACT and READ commands to the same rank-bank
13:9	R/W 00000b	**Same Rank Write To READ Delayed (C0sd_cr_wrsr_rd):** This field indicates the minimum allowed spacing (in DRAM clocks) between the WRITE and READ commands to the same rank.
8:6	RO 0h	Reserved
5:3	R/W 000b	**Same Rank Read To Read Delayed (C0sd_cr_rdsr_rd):** This field indicates the minimum allowed spacing (in DRAM clocks) between two READ commands to the same rank.
2:0	RO 0h	Reserved

5.2.39 EPDCKECONFIGREG—MED CKE Related Configuration Register

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: A28–A2Ch
Default Value: 00E0000000h
Access: R/W
Size: 40 bits
BIOS Optimal Default 0h

This is the CKE related configuration register for MED.

Bit	Access & Default	Description
39:35	R/W 00000b	**MEDunit TXPDLL Count (EPDTXPDLL):** This field specifies the delay from precharge power down exit to a command that requires the DRAM DLL to be operational. The commands are read/write.
34:32	R/W 000b	**MEDunit TXP Count (EPDCKETXP):** This field specifies the timing requirement for Active power down exit or fast exit pre-charge power down exit to any command or slow exit pre-charge power down to Non-DLL (rd/wr/odt) command.
31:29	R/W 111b	**Mode Select (sd0_cr_sms):** This field setting indicates the mode in which the controller is operating in. 111 = Normal mode of operation, else special mode of operation.
28:27	R/W 00b	**MEDunit EMRS Command Select. (EPDEMRSSEL):** This field provides EMRS mode to select BANK address. 01 = EMRS 10 = EMRS2 11 = EMRS3
26:24	R/W 000b	**CKE Pulse Width Requirement in High Phase (sd0_cr_cke_pw_hl_safe):** This field indicates CKE pulse width requirement in high phase..
23:20	R/W 0h	**One-hot Active Rank Population (ep_scr_actrank):** This field indicates the active rank in a one hot manner
19:17	R/W 000b	**CKE Pulse Width Requirement in Low Phase (sd0_cr_cke_pw_lh_safe):** This field indicates CKE pulse width requirement in low phase..
16:15	RO 0h	Reserved
14	R/W 0b	**MEDunit MPR mode (EPDMPR):** MPR Read Mode 1 = MPR mode 0 = Normal mode

Bit	Access & Default	Description
13	R/W 0b	**MEDunit Power Down enable for ODT Rank (EPDOAPDEN):** This bit enables the ODT ranks to dynamically enter power down. 0 = Disable active power down. 1 = Enable active power down.
12	R/W 0b	**MEDunit Power Down Enable for Active Rank (EPDAAPDEN):** This bit enables the active rank to dynamically enter power down. 0 = Disable active power down. 1 = Enable active power down.
11:10	RO 0h	Reserved
9:1	R/W 00000000 0b	**Self Refresh Exit Count (sd0_cr_slfrfsh_exit_cnt):** This field indicates the Self refresh exit count. (Program to 255)
0	R/W 0b	**Indicates Only 1 DIMM Populated (sd0_cr_singledimmpop):** This field indicates that only 1 DIMM is populated.

5.2.40 MEMEMSPACE—ME Memory Space configuration

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: A2Eh
Default Value: 00h
Access: R/W, RO
Size: 8 bits

This register provides settings to enable the ME memory space and define the size of EP memory if enabled.

Bit	Access & Default	Description
7:5	RO 000b	Reserved
4:0	R/W 00000b	**ME-UMA(Sx) Region Size (EXRS):** These bits are written by firmware to indicate the desired size of ME-UMA(Sx) memory region. This is done prior to bring up core power and allowing BIOS to initialize memory. Within channel 0 DDR, the physical base address for ME-UMA(Sx) will be determined by: ME-UMA(Sx)BASE = C0DRB3 - EXRS. This forces the ME-UMA(Sx) region to always be positioned at the top of the memory populated in channel 0. The approved sizes for ME-UMA(Sx) are values between 0000b (0MB, no ME-UMA(Sx) region) and 10000b (16MB ME-UMA(Sx) region)

5.2.41 EPDREFCONFIG—ME DRAM Refresh Configuration

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: A30–A33h
Default Value: 40000C30h
Access: R/W, RO
Size: 32 bits

This register provides settings to configure the MED refresh controller.

Bit	Access & Default	Description
31	RO 0b	Reserved
30:29	R/W 10b	**MEDunit Refresh Count Addition for Self Refresh Exit. (EPDREF4SR):** This field indicates the number of additional refreshes that need to be added to the refresh request count after exiting self refresh. Typical value is to add 2 refreshes. 00 = Add 0 Refreshes 01 = Add 1 Refreshes 10 = Add 2 Refreshes 11 = Add 3 Refreshes
28	R/W 0b	**Refresh Counter Enable (REFCNTEN):** This bit is used to enable the refresh counter to count during times that DRAM is not in self-refresh, but refreshes are not enabled. Such a condition may occur due to need to reprogram DIMMs following DRAM controller switch. This bit has no effect when Refresh is enabled (i.e., there is no mode where Refresh is enabled but the counter does not run). Thus, in conjunction with bit 23 REFEN, the modes are: **REFEN:REFCNTEN** **Description** 0:0 Normal refresh disable 0:1 Refresh disabled, but counter is accumulating refreshes. 1:X Normal refresh enable
27	R/W 0b	**Refresh Enable (REFEN):** 0 = Disabled 1 = Enabled
26	R/W 0b	**DDR Initialization Done (INITDONE):** This bit indicates that DDR initialization is complete. 0 = Not Done 1 = Done
25:22	RO 0000b	Reserved

Bit	Access & Default	Description
21:18	R/W 0000b	**DRAM Refresh High Watermark (REFHIGHWM):** When the refresh count exceeds this level, a refresh request is launched to the scheduler and the dref_high flag is set. 0000 = 0 0001 = 1 ..... 1000 = 8
17:14	R/W 0000b	**DRAM Refresh Low Watermark (REFLOWWM):** When the refresh count exceeds this level, a refresh request is launched to the scheduler and the dref_low flag is set. 0000 = 0 0001 = 1 ..... 1000 = 8
13:0	R/W 00110000 110000b	**Refresh Counter Time Out Value (REFTIMEOUT):** Program this field with a value that will provide 7.8 us at the memory clock frequency. At various memory clock frequencies this results in the following values: 266 MHz -> 820h 333 MHz -> A28h 400 MHz -> C30h

5.2.42 TSC1—Thermal Sensor Control 1

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: CD8h
Default Value: 00h
Access: RW/L, R/W, RS/WC
Size: 8 bits

This register controls the operation of the thermal sensor. Bits 7:1 of this register are reset to their defaults by CLPWROK. Bit 0 is reset to its default by PLTRST#.

Bit	Access & Default	Description
7	R/W/L 0b	**Thermal Sensor Enable (TSE):** This bit enables power to the thermal sensor. Lockable via TCO bit 7. 0 = Disabled 1 = Enabled
6	RO 0b	Reserved

Bit	Access & Default	Description
5:2	R/W 0000b	**Digital Hysteresis Amount (DHA):** This field determines whether no offset, 1 LSB, 2... 15 are used for hysteresis for the trip points. 0000 = digital hysteresis disabled, no offset added to trip temperature 0001 = offset is 1 LSB added to each trip temperature when tripped ... 0110 = ~3.0 °C (Recommended setting) ... 1110 = added to each trip temperature when tripped 1111 = added to each trip temperature when tripped
1	RO 0b	Reserved
0	RS/WC 0b	**In Use (IU):** Software semaphore bit. After a full MCH RESET, a read to this bit returns a 0. After the first read, subsequent reads will return a 1. A write of a 1 to this bit will reset the next read value to 0. Writing a 0 to this bit has no effect. Software can poll this bit until it reads a 0, and will then own the usage of the thermal sensor. This bit has no other effect on the hardware, and is only used as a semaphore among various independent software threads that may need to use the thermal sensor. Software that reads this register but does not intend to claim exclusive access of the thermal sensor must write a one to this bit if it reads a 0, in order to allow other software threads to claim it.

5.2.43 TSC2—Thermal Sensor Control 2

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: CD9h
Default Value: 00h
Access: R/W/L, RO
Size: 8 bits

This register controls the operation of the thermal sensor. All bits in this register are reset to their defaults by CLPWROK.

Bit	Access & Default	Description
7:4	RO 0h	Reserved
3:0	R/W/L 0h	**Thermometer Mode Enable and Rate (TE):** These bits enable the thermometer mode functions and set the Thermometer controller rate. The trip points (Catastrophic and Hot) will all operate using the programmed trip points and Thermometer mode rate. **NOTE:** During boot, all other thermometer mode registers (except lock bits) should be programmed appropriately before enabling the Thermometer Mode. Lockable via TCO bit 7. 0000 = Disabled. Thermometer mode disabled 0100 = Enabled, 2048 clock mode (normal Thermometer mode operation) - provides ~7.68 us settling time @ 266 MHz - provides ~6.14 us settling time @ 333 MHz - provides ~5.12 us settling time @ 400 MHz 0101 = Enabled, 3072 clock mode 0110 = Enabled, 4096 clock mode 0111 = Enabled, 6144 clock mode - provides ~23.1 us settling time @ 266 MHz - provides ~18.5 us settling time @ 333 MHz - provides ~15.4 us settling time @ 400 MHz all other permutations reserved **NOTE:** The settling time for DAC and Thermal Diode is between 2 us and 5 us. To meet this requirement the SE value must be programmed to be 5 micro-seconds or more. Recommendation is to use 0100h setting.

5.2.44 TSS—Thermal Sensor Status

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: CDAh
Default Value: 00h
Access: RO
Size: 8 bits

This register provides trip point and other status of the thermal sensor. All bits in this register are reset to their defaults by CLPWROK.

Bit	Access & Default	Description
7	RO 0b	**Catastrophic Trip Indicator (CTI):** 1 = Internal thermal sensor temperature is above the catastrophic setting.
6	RO 0b	**Hot Trip Indicator (HTI):** 1 = Internal thermal sensor temperature is above the Hot setting.
5:0	RO 00000b	Reserved

5.2.45 TSTTP—Thermal Sensor Temperature Trip Point

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: CDC–CDFh
Default Value: 00000000h
Access: RO, R/W, R/W/L
Size: 32 bits

This register sets the target values for the trip points. All bits in this register are reset to their defaults by CLPWROK.

Bit	Access & Default	Description
31:16	RO 00h	Reserved
15:8	R/W/L 00h	**Hot Trip Point Setting (HTPS):** This field sets the target value for the Hot trip point. Lockable via TCO bit 7.
7:0	R/W/L 00h	**Catastrophic Trip Point Setting (CTPS):** This field sets the target for the Catastrophic trip point. See also TST[Direct DAC Connect Test Enable]. Lockable via TCO bit 7.

5.2.46 TCO—Thermal Calibration Offset

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: CE2h
Default Value: 00h
Access: R/W/L/K, R/W/L
Size: 8 bits

Bit 7 reset to its default by PLTRST#. Bits 6:0 reset to their defaults by CLPWROK.

Bit	Access & Default	Description
7	R/W/L/K 0b	**Thermal Sensor Lock Bit (TSLB):** This bit, when written to a 1, locks the Catastrophic programming interface, including bits 7:0 of this register and bits 15:0 of TSTTP, bits 1,7 of TSC 1, bits 3:0 of TSC 2, bits 4:0 of TSC 3, and bits 0,7 of TST. This bit may only be set to a 0 by a hardware reset (PLTRST#). Writing a 0 to this bit has no effect.
6:0	R/W/L 00h	**Calibration Offset (CO):** This field contains the current calibration offset for the Thermal Sensor DAC inputs. The calibration offset is a twos complement signed number which is added to the temperature counter value to help generate the final value going to the thermal sensor DAC. This register is loaded by the HW from fuses that are blown during test. This field is Read/Write, but should be kept at its default value as programmed by the fuses in the part. Note for TCO operation: While this is a seven-bit field, the 7th bit is sign extended to 9 bits for TCO operation. The range of 00h to 3Fh corresponds to 0_0000_0000h to 0_0011_1111h. The range of 41h to 7Fh corresponds to 1 1100 001 (i.e., negative 3fh) to 1_1111_1111h (i.e., negative 1), respectively.

5.2.47 THERM1—Hardware Protection

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: CE4h
Default Value: 00h
Access: R/W/L, RO, R/W/L/K
Size: 8 bits

All bits in this register are reset to their defaults by PLTRST#.

Bit	Access & Default	Description
7:4	RO 0000b	**Reserved**
3	R/W/L 0b	**Halt on Catastrophic (HOC):** 0 = Continue to toggle clocks when the catastrophic sensor trips. 1 = All clocks are disabled when the catastrophic sensor trips. A system reset is required to bring the system out of a halt from the thermal sensor.
2:1	RO 00b	**Reserved**
0	R/W/L/K 0b	**Hardware Protection Lock Bit (HTL):** This bit locks bits 7:0 of this register. 0 = The register bits are unlocked. 1 = The register bits are locked. It may only be set to a 0 by a hardware reset. Writing a 0 to this bit has no effect.

5.2.48 TIS—Thermal Interrupt Status

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: CEA–CEBh
Default Value: 0000h
Access: RO, R/W/C
Size: 16 bits

This register is used to report if the temperature is rising or falling past the Hot Trip Point. After an SMI# is asserted by the Hot Trip Point, SW can examine the current state of the thermal zones by examining the TSS.

Software must write a 1 to clear the status bits in this register.

Following scenario is possible: An interrupt is initiated on a rising temperature trip, the appropriate DMI cycles are generated, and eventually the software services the interrupt and sees a rising temperature trip as the cause in the status bits for the interrupts. Assume that the software then clears the local interrupt status bit in the TIS register for that trip event. It is possible at this point that a falling temperature trip event occurs before the software has had the time to clear the global interrupts status bit. But since software has already looked at the status register before this

event happened, software may not clear the local status flag for this event. Therefore, after the global interrupt is cleared by software, software must look at the instantaneous status in the TSS register.

All bits in this register are reset to their defaults by PLTRST#.

Bit	Access & Default	Description
15:10	RO 00h	Reserved
9	R/WC 0b	**Was Catastrophic Thermal Sensor Interrupt Event (WCTSIE):** Software must write a 1 to clear this status bit. 0 = No trip for this event 1 = Catastrophic Thermal Sensor trip based on a higher to lower temperature transition thru the trip point
8	R/WC 0b	**Was Hot Thermal Sensor Interrupt Event (WHTSIE):** Software must write a 1 to clear this status bit. 0 = No trip for this event 1 = Hot Thermal Sensor trip based on a higher to lower temperature transition thru the trip point
7:5	RO 000b	Reserved
4	R/WC 0b	**Catastrophic Thermal Sensor Interrupt Event (CTSIE):** Software must write a 1 to clear this status bit. 0 = No trip for this event. 1 = Catastrophic Thermal Sensor trip event occurred based on a lower to higher temperature transition thru the trip point.
3	R/WC 0b	**Hot Thermal Sensor Interrupt Event (HTSIE):** Software must write a 1 to clear this status bit. 0 = No trip for this event. 1 = Hot Thermal Sensor trip event occurred based on a lower to higher temperature transition thru the trip point.
2:0	RO 000b	Reserved

5.2.49 TSMICMD—Thermal SMI Command

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: CF1h
Default Value: 00h
Access: RO, R/W
Size: 8 bits

This register selects specific errors to generate a SMI DMI special cycle, as enabled by the Device 0 SMI Error Command Register [SMI on MCH Thermal Sensor Trip]. All bits in this register are reset to their defaults by PLTRST#.

Bit	Access & Default	Description
7:2	RO 000h	Reserved
1	R/W 0b	**SMI on (G)MCH Hot Thermal Sensor Trip (SMGHTST):** 0 = Disable reporting of this condition via SMI messaging. 1 = Does not mask the generation of an SMI# DMI special cycle on a Hot thermal sensor trip.
0	RO 0b	Reserved

5.2.50 PMSTS—Power Management Status

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: F14–F17h
Default Value: 00000000h
Access: R/WC/S, RO
Size: 32 bits

This register is reset by PWROK only.

Bit	Access & Default	Description
31:9	RO 00000h	Reserved
8	R/WC/S 0b	**Warm Reset Occurred (WRO):** This bit is set when a ResetWarn is received, and cleared by PWROK=0. 0 = No Warm Reset occurred. 1 = Warm Reset occurred. **BIOS Requirement:** BIOS can check and clear this bit when executing POST code. This way BIOS knows that if the bit is set, then the PMSTS bits [1:0] must also be set, and if not BIOS needs to power-cycle the platform.

Bit	Access & Default	Description
7:2	RO 00h	Reserved
1	R/WC/S 0b	**Channel 1 in Self-Refresh (C1SR):** This bit is set by power management hardware after Channel 1 is placed in self refresh as a result of a Power State or a Reset Warn sequence. • Cleared by Power management hardware before starting Channel 1 self refresh exit sequence initiated by a power management exit. • Cleared by the BIOS by writing a "1" in a warm reset (Reset# asserted while PWROK is asserted) exit sequence. 0 = Channel 1 not ensured to be in self refresh. 1 = Channel 1 in Self Refresh.
0	R/WC/S 0b	**Channel 0 in Self-Refresh (C0SR):** This bit is set by power management hardware after Channel 0 is placed in self refresh as a result of a Power State or a Reset Warn sequence. • Cleared by Power management hardware before starting Channel 0 self refresh exit sequence initiated by a power management exit. • Cleared by the BIOS by writing a "1" in a warm reset (Reset# asserted while PWROK is asserted) exit sequence. 0 = Channel 0 not ensured to be in self refresh. 1 = Channel 0 in Self Refresh.

5.3 MEBAR Registers

Table 5-4. MEBAR Register Address Map

Address Offset	Symbol	Register Name	Default Value	Access
44–47h	EPESD	ME Element Self Description	00000201h	RO, R/WO
50–53h	EPLE1D	Controller Link Entry 1 Description	01000000h	RO, R/WO
58–57h	EPLE1A	Controller Link Entry 1 Address	000000000000000h	RO, R/WO
60–63h	EPLE2D	Controller Link Entry 2 Description	02000002h	RO, R/WO
68–6Fh	EPLE2A	Controller Link Entry 2 Address	000000000008000h	RO

5.3.1 EPESD—ME Element Self Description

B/D/F/Type: 0/0/0/PXPEPBAR
Address Offset: 44–47h
Default Value: 00000201h
Access: RO, R/WO
Size: 32 bits

This register provides information about the root complex element containing this Link Declaration Capability.

Bit	Access & Default	Description
31:24	RO 00h	**Port Number (PN):** This field specifies the port number associated with this element with respect to the component that contains this element. A value of 00h indicates to configuration software that this is the default egress port.
23:16	R/WO 00h	**Component ID (CID):** This field identifies the physical component that contains this Root Complex Element.
15:8	RO 02h	**Number of Link Entries (NLE):** This field indicates the number of link entries following the Element Self Description. This field reports 2 link entries (one each for PEG and DMI).
7:4	RO 0h	Reserved
3:0	RO 1h	**Element Type (ET):** This field indicates the type of the Root Complex Element. Value of 1 h represents a port to system memory.

5.3.2 EPLE1D—Controller Link Entry 1 Description

B/D/F/Type: 0/0/0/PXPEPBAR
Address Offset: 50–53h
Default Value: 01000000h
Access: RO, R/WO
Size: 32 bits

This register provides the first part of a link entry that declares an internal link to another Root Complex Element.

Bit	Access & Default	Description
31:24	RO 01h	**Target Port Number (TPN):** This field specifies the port number associated with the element targeted by this link entry (DMI). The target port number is with respect to the component that contains this element as specified by the target component ID.
23:16	R/WO 00h	**Target Component ID (TCID):** This field identifies the physical or logical component that is targeted by this link entry.
15:2	RO 0000h	Reserved
1	RO 0b	**Link Type (LTYP):** This bit indicates that the link points to memory-mapped space (for RCRB). The link address specifies the 64-bit base address of the target RCRB.
0	R/WO 0b	**Link Valid (LV):** 0 = Link Entry is not valid and will be ignored. 1 = Link Entry specifies a valid link.

5.3.3 EPLE1A—Controller Link Entry 1 Address

B/D/F/Type: 0/0/0/PXPEPBAR
Address Offset: 58–5Fh
Default Value: 0000000000000000h
Access: RO, R/WO
Size: 64 bits

This register provides the second part of a link entry that declares an internal link to another Root Complex Element.

Bit	Access & Default	Description
63:32	RO 00000000h	Reserved
31:12	R/WO 00000h	**Link Address (LA):** This field contains the memory-mapped base address of the RCRB that is the target element (DMI) for this link entry.
11:0	RO 000h	Reserved

5.3.4 EPLE2D—Controller Link Entry 2 Description

B/D/F/Type: 0/0/0/PXPEPBAR
Address Offset: 60–63h
Default Value: 02000002h
Access: RO, R/WO
Size: 32 bits

This register provides the first part of a link entry that declares an internal link to another Root Complex Element.

Bit	Access & Default	Description
31:24	RO 02h	**Target Port Number (TPN):** This field specifies the port number associated with the element targeted by this link entry (PEG). The target port number is with respect to the component that contains this element as specified by the target component ID.
23:16	R/WO 00h	**Target Component ID (TCID):** This field identifies the physical or logical component that is targeted by this link entry. A value of 0 is reserved. Component IDs start at 1. This value is a mirror of the value in the Component ID field of all elements in this component.
15:2	RO 0000h	Reserved
1	RO 1b	**Link Type (LTYP):** This bit is hardwired to I indicating that the link points to configuration space of the integrated device that controls the x16 root port. The link address specifies the configuration address (segment, bus, device, function) of the target root port.
0	R/WO 0b	**Link Valid (LV):** 0 = Link entry is not valid and will be ignored. 1 = Link entry specifies a valid link.

5.3.5 EPLE2A—Controller Link Entry 2 Address

B/D/F/Type: 0/0/0/PXPEPBAR
Address Offset: 68–6Fh
Default Value: 0000000000008000h
Access: RO
Size: 64 bits

This register provides the second part of a link entry that declares an internal link to another Root Complex Element.

Bit	Access & Default	Description
63:28	RO 000000000h	Reserved
27:20	RO 00h	**Bus Number (BUSN):**
19:15	RO 00001b	**Device Number (DEVN):** Target for this link is PCI Express x16 port (Device 1). (82Q965, 82G965, 82P965 (G)MCH Only)
14:12	RO 000b	**Function Number (FUNN):**
11:0	RO 000h	Reserved

§

6 PCI Express* Registers (Device 1, Function 0) (Intel® 82Q965/82G965/82P965 Only)

Device 1 contains the controls associated with the PCI Express x16 root port that is the intended to attach as the point for external graphics. It also functions as the virtual PCI-to-PCI bridge.

Warning: When reading the PCI Express "conceptual" registers such as this, you may not get a valid value unless the register value is stable.

The *PCI Express* Specification* defines two types of reserved bits.

Reserved and Preserved:

1. Reserved for future R/W implementations; software must preserve value read for writes to bits.
2. Reserved and Zero: Reserved for future R/WC/S implementations; software must use 0 for writes to bits.

Unless explicitly documented as Reserved and Zero, all bits marked as reserved are part of the Reserved and Preserved type, which have historically been the typical definition for Reserved.

Note: Most (if not all) control bits in this device cannot be modified unless the link is down. Software is required to first Disable the link, then program the registers, and then re-enable the link (which will cause a full-retrain with the new settings).

Table 6-1. PCI Express* Register Address Map (Device 1, Function 0)

Address Offset	Symbol	Register Name	Default Value	Access
00–01h	VID1	Vendor Identification	8086h	RO
02–03h	DID1	Device Identification	2981h	RO
04–05h	PCICMD1	PCI Command	0000h	RO, R/W
06–07h	PCISTS1	PCI Status	0010h	RO, R/WC
08h	RID1	Revision Identification	See register description	RO
09–0Bh	CC1	Class Code	060400h	RO
0Ch	CL1	Cache Line Size	00h	R/W

Address Offset	Symbol	Register Name	Default Value	Access
0Eh	HDR1	Header Type	01h	RO
18h	PBUSN1	Primary Bus Number	00h	RO
19h	SBUSN1	Secondary Bus Number	00h	R/W
1Ah	SUBUSN1	Subordinate Bus Number	00h	R/W
1Ch	IOBASE1	I/O Base Address	F0h	R/W, RO
1Dh	IOLIMIT1	I/O Limit Address	00h	R/W, RO
1E–1Fh	SSTS1	Secondary Status	0000h	R/WC, RO
20–21h	MBASE1	Memory Base Address	FFF0h	R/W, RO
22–22h	MLIMIT1	Memory Limit Address	0000h	R/W, RO
24–25h	PMBASE1	Prefetchable Memory Base Address	FFF1h	R/W, RO
26–27h	PMLIMIT1	Prefetchable Memory Limit Address	0001h	R/W, RO
28–2Bh	PMBASEU1	Prefetchable Memory Base Address	00000000h	R/W
2C–2Fh	PMLIMITU1	Prefetchable Memory Limit Address	00000000h	R/W
34h	CAPPTR1	Capabilities Pointer	88h	RO
3Ch	INTRLINE1	Interrupt Line	00h	R/W
3Dh	INTRPIN1	Interrupt Pin	01h	RO
3E–3Fh	BCTRL1	Bridge Control	0000h	RO, R/W
80–83h	PM_CAPID1	Power Management Capabilities	C8039001h	RO
84–87h	PM_CS1	Power Management Control/Status	00000000h	RO, R/W/S, R/W
88–8Bh	SS_CAPID	Subsystem ID and Vendor ID Capabilities	0000800Dh	RO
8C–8Fh	SS	Subsystem ID and Subsystem Vendor ID	00008086h	R/WO
90–91h	MSI_CAPID	Message Signaled Interrupts Capability ID	A005h	RO
92–93h	MC	Message Control	0000h	R/W, RO
94–97h	MA	Message Address	00000000h	R/W, RO
98–99h	MD	Message Data	0000h	R/W
A0–A1h	PEG_CAPL	PCI Express-G Capability List	0010h	RO
A2–A3h	PEG_CAP	PCI Express-G Capabilities	0141h	RO, R/WO
A4–A7h	DCAP	Device Capabilities	00008000h	RO
A8–A9h	DCTL	Device Control	0000h	RO, R/W
AA–ABh	DSTS	Device Status	0000h	RO, R/WC
AC–AFh	LCAP	Link Capabilities	02014D01h	RO, R/WO

Address Offset	Symbol	Register Name	Default Value	Access
B0–B1h	LCTL	Link Control	0000h	RO, R/W, R/W/SC
B2–B3h	LSTS	Link Status	1001h	RO
B4–B7h	SLOTCAP	Slot Capabilities	00040000h	R/WO, RO
B8–B9h	SLOTCTL	Slot Control	01C0h	RO, R/W
BA–BBh	SLOTSTS	Slot Status	0000h	RO, R/WC
BC–BDh	RCTL	Root Control	0000h	RO, R/W
C0–C3h	RSTS	Root Status	00000000h	RO, R/WC
EC–EFh	PEGLC	PCI Express-G Legacy Control	00000000h	R/W, RO
100–103h	VCECH	Virtual Channel Enhanced Capability Header	14010002h	RO
104–107h	PVCCAP1	Port VC Capability Register 1	00000000h	RO
108–10Bh	PVCCAP2	Port VC Capability Register 2	00000000h	RO
10C–10Dh	PVCCTL	Port VC Control	0000h	RO, R/W
110–113h	VC0RCAP	VC0 Resource Capability	00000000h	RO
114–117h	VC0RCTL	VC0 Resource Control	800000FFh	RO, R/W
11A–11Bh	VC0RSTS	VC0 Resource Status	0002h	RO
140–143h	RCLDECH	Root Complex Link Declaration Enhanced	00010005h	RO
144–147h	ESD	Element Self Description	02000100h	RO, R/WO
150–153h	LE1D	Link Entry 1 Description	00000000h	RO, R/WO
158–15Fh	LE1A	Link Entry 1 Address	000000000000000h	RO, R/WO
218–21Fh	PEGSSTS	PCI Express-G Sequence Status	0000000000000FFFh	RO

6.1 PCI Express* Configuration Register Details (Device 1, Function 0)

6.1.1 VID1—Vendor Identification

B/D/F/Type: 0/1/0/PCI
Address Offset: 0–1h
Default Value: 8086h
Access: RO
Size: 16 bits

This register, combined with the Device Identification register, uniquely identify any PCI device.

Bit	Access & Default	Description
15:0	RO 8086h	**Vendor Identification (VID1):** PCI standard identification for Intel.

6.1.2 DID1—Device Identification

B/D/F/Type: 0/1/0/PCI
Address Offset: 2–3h
Default Value: 2981h
Access: RO
Size: 16 bits

This register, combined with the Vendor Identification register, uniquely identifies any PCI device.

Bit	Access & Default	Description
15:8	RO 29h	**Device Identification Number (DID1(UB)):** Identifier assigned to the (G)MCH device 1 (virtual PCI-to-PCI bridge, PCI Express Graphics port).
7:4	RO 7h	**Device Identification Number (DID1(HW)):** Identifier assigned to the (G)MCH device 1 (virtual PCI-to-PCI bridge, PCI Express Graphics port).
3:0	RO 1h	**Device Identification Number (DID1(LB)):** Identifier assigned to the (G)MCH device 1 (virtual PCI-to-PCI bridge, PCI Express Graphics port).

6.1.3 PCICMD1—PCI Command

B/D/F/Type: 0/1/0/PCI
Address Offset: 4–5h
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

Bit	Access & Default	Description
15:11	RO 00h	Reserved
10	R/W 0b	**INTA Assertion Disable (INTAAD):** This bit only affects interrupts generated by the device (PCI INTA from a PME or Hot Plug event) controlled by this command register. It does not affect upstream MSIs, upstream PCI INTA-INTD assert and de-assert messages. 0 = This device is permitted to generate INTA interrupt messages. 1 = This device is prevented from generating interrupt messages. Any INTA emulation interrupts already asserted must be de-asserted when this bit is set.
9	RO 0b	**Fast Back-to-Back Enable (FB2B):** Not Applicable or Implemented. Hardwired to 0.
8	R/W 0b	**SERR# Message Enable (SERRE1):** This bit controls Device 1 SERR# messaging. The (G)MCH communicates the SERR# condition by sending a SERR message to the ICH. This bit, when set, enables reporting of non-fatal and fatal errors detected by the device to the Root Complex. Note that errors are reported if enabled either through this bit or through the PCI-Express specific bits in the Device Control Register. 0 = The SERR message is generated by the (G)MCH for Device 1 only under conditions enabled individually through the Device Control register. 1 = The (G)MCH is enabled to generate SERR messages that will be sent to the ICH for specific Device 1 error conditions generated/detected on the primary side of the virtual PCI to PCI bridge (not those received by the secondary side). The status of SERRs generated is reported in the PCISTS1 register.
7	RO 0b	Reserved: Hardwired to 0.
6	R/W 0b	**Parity Error Response Enable (PERRE):** This bit controls whether the Master Data Parity Error bit in the PCI Status register can bet set. 0 = Disable. Master Data Parity Error bit in PCI Status register can NOT be set. 1 = Enable. Master Data Parity Error bit in PCI Status register CAN be set.
5	RO 0b	**VGA Palette Snoop (VGAPS):** Hardwired to 0.

Bit	Access & Default	Description
4	RO 0b	**Memory Write and Invalidate Enable (MWIE):** Hardwired to 0.
3	RO 0b	**Special Cycle Enable (SCE):** Hardwired to 0.
2	R/W 0b	**Bus Master Enable (BME):** This bit controls the ability of the PEG port to forward Memory and I/O Read/Write Requests in the upstream direction. This bit does not affect forwarding of Completions from the primary interface to the secondary interface. 0 = This device is prevented from making memory or I/O requests to its primary bus. Note that according to PCI Specification, as MSI interrupt messages are in-band memory writes, disabling the bus master enable bit prevents this device from generating MSI interrupt messages or passing them from its secondary bus to its primary bus. Upstream memory writes/reads, I/O writes/reads, peer writes/reads, and MSIs will all be treated as invalid cycles. Writes are forwarded to memory address with byte enables de-asserted. Reads will be forwarded to memory address and will return Unsupported Request status (or Master abort) in its completion packet. 1 = This device is allowed to issue requests to its primary bus. Completions for previously issued memory read requests on the primary bus will be issued when the data is available.
1	R/W 0b	**Memory Access Enable (MAE):** 0 = Disable. All of device 1's memory space is disabled. 1 = Enable the Memory and Pre-fetchable memory address ranges defined in the MBASE1, MLIMIT1, PMBASE1, and PMLIMIT1 registers.
0	R/W 0b	**IO Access Enable (IOAE):** 0 = Disable. All of device 1's I/O space is disabled. 1 = Enable the I/O address range defined in the IOBASE1, and IOLIMIT1 registers.

6.1.4 PCISTS1—PCI Status

B/D/F/Type: 0/1/0/PCI
Address Offset: 6–7h
Default Value: 0010h
Access: RO, R/WC
Size: 16 bits

This register reports the occurrence of error conditions associated with primary side of the "virtual" Host-PCI Express bridge in the (G)MCH.

Bit	Access & Default	Description
15	RO 0b	**Detected Parity Error (DPE):** Hardwired to 0. Parity (generating poisoned TLPs) is not supported on the primary side of this device.
14	R/WC 0b	**Signaled System Error (SSE):** This bit is set when this Device sends an SERR due to detecting an ERR_FATAL or ERR_NONFATAL condition and the SERR Enable bit in the Command register is '1'. Both received (if enabled by BCTRL1[1]) and internally detected error messages do not affect this field.
13	RO 0b	**Received Master Abort Status (RMAS):** Hardwired to 0. The concept of a master abort does not exist on primary side of this device.
12	RO 0b	**Received Target Abort Status (RTAS):** Hardwired to 0. The concept of a target abort does not exist on primary side of this device.
11	RO 0b	**Signaled Target Abort Status (STAS):** Hardwired to 0. The concept of a target abort does not exist on primary side of this device.
10:9	RO 00b	**DEVSELB Timing (DEVT):** This device is not the subtractively decoded device on bus 0. This bit field is therefore hardwired to 00 to indicate that the device uses the fastest possible decode.
8	RO 0b	**Master Data Parity Error (PMDPE):** Because the primary side of the PEG's virtual PCI-to-PCI bridge is integrated with the (G)MCH functionality, there is no scenario where this bit will get set.
7	RO 0b	**Fast Back-to-Back (FB2B):** Hardwired to 0.
6	RO 0b	Reserved
5	RO 0b	**66/60 MHz capability (CAP66):** Hardwired to 0.
4	RO 1b	**Capabilities List (CAPL):** Hardwired to 1 to indicate that a capabilities list is present.
3	RO 0b	**INTA Status (INTAS):** This bit indicates that an interrupt message is pending internally to the device. Only PME and Hot Plug sources feed into this status bit (not PCI INTA–INTD assert and de-assert messages). The INTA Assertion Disable bit, PCICMD1[10], has no effect on this bit.
2:0	RO 000b	Reserved

6.1.5 RID1—Revision Identification

B/D/F/Type: 0/1/0/PCI
Address Offset: 8h
Default Value: See table
Access: RO
Size: 8 bits

This register contains the revision number of the (G)MCH device 1. These bits are read only and writes to this register have no effect.

Bit	Access & Default	Description
7:0	RO 00h	**Revision Identification Number (RID1):** This is an 8-bit value that indicates the revision identification number for the (G)MCH Device 0. Refer to the *Intel® 965 Express Chipset Specification Update* for the value of the Revision ID register.

6.1.6 CC1—Class Code

B/D/F/Type: 0/1/0/PCI
Address Offset: 9–Bh
Default Value: 060400h
Access: RO
Size: 24 bits

This register identifies the basic function of the device, a more specific sub-class, and a register- specific programming interface.

Bit	Access & Default	Description
23:16	RO 06h	**Base Class Code (BCC):** This field indicates the base class code for this device. This code has the value 06h, indicating a Bridge device.
15:8	RO 04h	**Sub-Class Code (SUBCC):** This field indicates the sub-class code for this device. The code is 04h indicating a PCI to PCI Bridge.
7:0	RO 00h	**Programming Interface (PI):** This field indicates the programming interface of this device. This value does not specify a particular register set layout and provides no practical use for this device.

6.1.7 CL1—Cache Line Size

B/D/F/Type: 0/1/0/PCI
Address Offset: Ch
Default Value: 00h
Access: R/W
Size: 8 bits

Bit	Access & Default	Description
7:0	R/W 00h	**Cache Line Size (Scratch pad):** This field is implemented by PCI Express devices as a read/write field for legacy compatibility purposes but has no impact on any PCI Express device functionality.

6.1.8 HDR1—Header Type

B/D/F/Type: 0/1/0/PCI
Address Offset: Eh
Default Value: 01h
Access: RO
Size: 8 bits

This register identifies the header layout of the configuration space. No physical register exists at this location.

Bit	Access & Default	Description
7:0	RO 01h	**Header Type Register (HDR):** This field returns 01h to indicate that this is a single function device with bridge header layout.

6.1.9 PBUSN1—Primary Bus Number

B/D/F/Type: 0/1/0/PCI
Address Offset: 18h
Default Value: 00h
Access: RO
Size: 8 bits

This register identifies that this "virtual" Host-PCI Express bridge is connected to PCI bus 0.

Bit	Access & Default	Description
7:0	RO 00h	**Primary Bus Number (BUSN):** Configuration software typically programs this field with the number of the bus on the primary side of the bridge. Since device 1 is an internal device and its primary bus is always 0, these bits are read only and are hardwired to 0.

6.1.10 SBUSN1—Secondary Bus Number

B/D/F/Type: 0/1/0/PCI
Address Offset: 19h
Default Value: 00h
Access: R/W
Size: 8 bits

This register identifies the bus number assigned to the second bus side of the "virtual" bridge (i.e., to PCI Express-G). This number is programmed by the PCI configuration software to allow mapping of configuration cycles to PCI Express-G.

Bit	Access & Default	Description
7:0	R/W 00h	**Secondary Bus Number (BUSN):** This field is programmed by configuration software with the bus number assigned to PCI Express.

6.1.11 SUBUSN1—Subordinate Bus Number

B/D/F/Type: 0/1/0/PCI
Address Offset: 1Ah
Default Value: 00h
Access: R/W
Size: 8 bits

This register identifies the subordinate bus (if any) that resides at the level below PCI Express-G. This number is programmed by the PCI configuration software to allow mapping of configuration cycles to PCI Express-G.

Bit	Access & Default	Description
7:0	R/W 00h	**Subordinate Bus Number (BUSN):** This register is programmed by configuration software with the number of the highest subordinate bus that lies behind the device 1 bridge. When only a single PCI device resides on the PCI Express-G segment, this register will contain the same value as the SBUSN1 register.

6.1.12 IOBASE1—I/O Base Address

B/D/F/Type: 0/1/0/PCI
Address Offset: 1Ch
Default Value: F0h
Access: R/W, RO
Size: 8 bits

This register controls the processor to PCI Express-G I/O access routing based on the following formula:

IO_BASE ≤ address ≤ IO_LIMIT

Only the upper 4 bits are programmable. For the purpose of address decode address bits 11:0 are treated as 0. Thus, the bottom of the defined I/O address range will be aligned to a 4 KB boundary.

Bit	Access & Default	Description
7:4	R/W Fh	**I/O Address Base (IOBASE): This field c**orresponds to address bits 15:12 of the I/O addresses passed by bridge 1 to PCI Express-G.
3:0	RO 0h	Reserved

6.1.13 IOLIMIT1—I/O Limit Address

B/D/F/Type: 0/1/0/PCI
Address Offset: 1Dh
Default Value: 00h
Access: R/W, RO
Size: 8 bits

This register controls the processor to PCI Express-G I/O access routing based on the following formula:

IO_BASE ≤ address ≤ IO_LIMIT

Only the upper 4 bits are programmable. For the purpose of address decode, address bits 11:0 are assumed to be FFFh. Thus, the top of the defined I/O address range will be at the top of a 4 KB aligned address block.

Bit	Access & Default	Description
7:4	R/W 0h	**I/O Address Limit (IOLIMIT):** This field corresponds to address bits 15:12 of the I/O address limit of device 1. Devices between this upper limit and IOBASE1 will be passed to the PCI Express hierarchy associated with this device.
3:0	RO 0h	Reserved

6.1.14 SSTS1—Secondary Status

B/D/F/Type: 0/1/0/PCI
Address Offset: 1E–1Fh
Default Value: 0000h
Access: R/WC, RO
Size: 16 bits

SSTS1 is a 16-bit status register that reports the occurrence of error conditions associated with secondary side (i.e., PCI Express-G side) of the "virtual" PCI-PCI bridge in the (G)MCH.

Bit	Access & Default	Description
15	R/WC 0b	**Detected Parity Error (DPE):** This bit is set by the Secondary Side for a Type 1 Configuration Space header device whenever it receives a Poisoned TLP, regardless of the state of the Parity Error Response Enable bit in the Bridge Control register.
14	R/WC 0b	**Received System Error (RSE):** This bit is set when the Secondary Side for a Type 1 configuration space header device receives an ERR_FATAL or ERR_NONFATAL.
13	R/WC 0b	**Received Master Abort (RMA):** This bit is set when the Secondary Side for Type 1 Configuration Space Header Device (for requests initiated by the Type 1 Header Device itself) receives a Completion with Unsupported Request Completion Status.
12	R/WC 0b	**Received Target Abort (RTA):** This bit is set when the Secondary Side for Type 1 Configuration Space Header Device (for requests initiated by the Type 1 Header Device itself) receives a Completion with Completer Abort Completion Status.
11	RO 0b	**Signaled Target Abort (STA):** Hardwired to 0. The (G)MCH does not generate Target Aborts (the (G)MCH will never complete a request using the Completer Abort Completion status).
10:9	RO 00b	**DEVSEL# Timing (DEVT):** Hardwired to 0.
8	R/WC 0b	**Master Data Parity Error (SMDPE):** When set, this bit indicates that the (G)MCH received across the link (upstream) a Read Data Completion Poisoned TLP (EP=1). This bit can only be set when the Parity Error Enable bit in the Bridge Control register is set.
7	RO 0b	**Fast Back-to-Back (FB2B):** Hardwired to 0.
6	RO 0b	Reserved
5	RO 0b	**66/60 MHz capability (CAP66):** Hardwired to 0.
4:0	RO 00000b	Reserved

6.1.15 MBASE1—Memory Base Address

B/D/F/Type: 0/1/0/PCI
Address Offset: 20–21h
Default Value: FFF0h
Access: R/W, RO
Size: 16 bits

This register controls the processor to PCI Express non-prefetchable memory access routing based on the following formula:

MEMORY_BASE ≤ address ≤ MEMORY_LIMIT

The upper 12 bits of the register are read/write and correspond to the upper 12 address bits 31:20 of the 32 bit address. The bottom 4 bits of this register are read-only and return zeroes when read. This register must be initialized by the configuration software. For the purpose of address decode, address bits 19:0 are assumed to be 0. Thus, the bottom of the defined memory address range will be aligned to a 1 MB boundary.

Bit	Access & Default	Description
15:4	R/W FFFh	**Memory Address Base (MBASE):** This field corresponds to address bits 31:20 of the lower limit of the memory range that will be passed to PCI Express-G.
3:0	RO 0h	Reserved

6.1.16 MLIMIT1—Memory Limit Address

B/D/F/Type: 0/1/0/PCI
Address Offset: 22–23h
Default Value: 0000h
Access: R/W, RO
Size: 16 bits

This register controls the processor to PCI Express-G non-prefetchable memory access routing based on the following formula:

MEMORY_BASE ≤ address ≤ MEMORY_LIMIT

The upper 12 bits of the register are read/write and correspond to the upper 12 address bits 31:20 of the 32 bit address. The bottom 4 bits of this register are read-only and return zeroes when read. This register must be initialized by the configuration software. For the purpose of address decode address bits 19:0 are assumed to be FFFFFh. Thus, the top of the defined memory address range will be at the top of a 1 MB aligned memory block.

Note: Memory range covered by MBASE and MLIMIT registers are used to map non-prefetchable PCI Express-G address ranges (typically where control/status memory-mapped I/O data structures of the graphics controller will reside) and PMBASE and PMLIMIT are used to map prefetchable address ranges (typically graphics local memory). This segregation allows application of USWC space attribute to be performed in a true plug-and-play manner to the prefetchable address range for improved processor- PCI Express memory access performance.

Note: Configuration software is responsible for programming all address range registers (prefetchable, non-prefetchable) with the values that provide exclusive address ranges (i.e., prevent overlap with each other and/or with the ranges covered with the main memory). There is no provision in the (G)MCH hardware to enforce prevention of overlap and operations of the system in the case of overlap are not assured.

Bit	Access & Default	Description
15:4	R/W 000h	**Memory Address Limit (MLIMIT):** This field corresponds to address bits 31:20 of the upper limit of the address range passed to PCI Express.
3:0	RO 0h	Reserved

6.1.17 PMBASE1—Prefetchable Memory Base Address

B/D/F/Type: 0/1/0/PCI
Address Offset: 24–25h
Default Value: FFF1h
Access: R/W, RO
Size: 16 bits

This register, in conjunction with the corresponding Upper Base Address register, controls the processor to PCI Express-G prefetchable memory access routing based on the following formula:

PREFETCHABLE_MEMORY_BASE ≤ address ≤ PREFETCHABLE_MEMORY_LIMIT

The upper 12 bits of this register are read/write and correspond to address bits 31:20 of the 40-bit address. The lower 8 bits of the Upper Base Address register are read/write and correspond to address bits 39:32 of the 40-bit address. This register must be initialized by the configuration software. For the purpose of address decode, address bits 19:0 are assumed to be 0. Thus, the bottom of the defined memory address range will be aligned to a 1 MB boundary.

Bit	Access & Default	Description
15:4	R/W FFFh	**Prefetchable Memory Base Address (MBASE):** This field corresponds to address bits 31:20 of the lower limit of the memory range that will be passed to PCI Express.
3:0	RO 1h	**64-bit Address Support:** This field indicates that the upper 32 bits of the prefetchable memory region base address are contained in the Prefetchable Memory base Upper Address register at 28h.

6.1.18 PMLIMIT1—Prefetchable Memory Limit Address

B/D/F/Type: 0/1/0/PCI
Address Offset: 26–27h
Default Value: 0001h
Access: R/W, RO
Size: 16 bits

This register in conjunction with the corresponding Upper Limit Address register controls the processor to PCI Express-G prefetchable memory access routing based on the following formula:

PREFETCHABLE_MEMORY_BASE ≤ address ≤ PREFETCHABLE_MEMORY_LIMIT

The upper 12 bits of this register are read/write and correspond to address bits 31:20 of the 40-bit address. The lower 8 bits of the Upper Limit Address register are read/write and correspond to address bits 39:32 of the 40-bit address. This register must be initialized by the configuration software. For the purpose of address decode, address bits 19:0 are assumed to be FFFFFh. Thus, the top of the defined memory address range will be at the top of a 1 MB aligned memory block. Note that prefetchable memory range is supported to allow segregation by the configuration software between the memory ranges that must be defined as UC and the ones that can be designated as a USWC (i.e., prefetchable) from the processor perspective.

Bit	Access & Default	Description
15:4	R/W 000h	**Prefetchable Memory Address Limit (PMLIMIT):** This field corresponds to address bits 31:20 of the upper limit of the address range passed to PCI Express.
3:0	RO 1h	**64-bit Address Support:** Indicates that the upper 32 bits of the prefetchable memory region limit address are contained in the Prefetchable Memory Base Limit Address register at 2Ch

6.1.19 PMBASEU1—Prefetchable Memory Base Address

B/D/F/Type: 0/1/0/PCI
Address Offset: 28–2Bh
Default Value: 00000000h
Access: R/W
Size: 32 bits

The functionality associated with this register is present in the PEG design implementation. This register in conjunction with the corresponding Upper Base Address register controls the processor to PCI Express-G prefetchable memory access routing based on the following formula:

PREFETCHABLE_MEMORY_BASE ≤ address ≤ PREFETCHABLE_MEMORY_LIMIT

The upper 12 bits of this register are read/write and correspond to address bits 31:20 of the 40-bit address. The lower 8 bits of the Upper Base Address register are read/write and correspond to address bits 39:32 of the 40-bit address. This register must be initialized by the configuration software. For the purpose of address decode, address bits 19:0 are assumed to be 0. Thus, the bottom of the defined memory address range will be aligned to a 1 MB boundary.

Bit	Access & Default	Description
31:0	R/W 00000000h	**Prefetchable Memory Base Address (MBASEU):** This field corresponds to address bits 63:32 of the lower limit of the prefetchable memory range that will be passed to PCI Express.

6.1.20 PMLIMITU1—Prefetchable Memory Limit Address

B/D/F/Type: 0/1/0/PCI
Address Offset: 2C–2Fh
Default Value: 00000000h
Access: R/W
Size: 32 bits

The functionality associated with this register is present in the PEG design implementation. This register, in conjunction with the corresponding Upper Limit Address register, controls the processor to PCI Express-G prefetchable memory access routing based on the following formula:

PREFETCHABLE_MEMORY_BASE ≤ address ≤ PREFETCHABLE_MEMORY_LIMIT

The upper 12 bits of this register are read/write and correspond to address bits 31:20 of the 40- bit address. The lower 8 bits of the Upper Limit Address register are read/write and correspond to address bits 39:32 of the 40-bit address. This register must be initialized by the configuration software. For the purpose of address decode, address bits 19:0 are assumed to be FFFFFh. Thus, the top of the defined memory address range will be at the top of a 1 MB aligned memory block.

Note that prefetchable memory range is supported to allow segregation by the configuration software between the memory ranges that must be defined as UC and the ones that can be designated as a USWC (i.e., prefetchable) from the processor perspective.

Bit	Access & Default	Description
31:0	R/W 00000000h	**Prefetchable Memory Address Limit (MLIMITU):** This field corresponds to address bits 63:32 of the upper limit of the prefetchable memory range that will be passed to PCI Express.

6.1.21 CAPPTR1—Capabilities Pointer

B/D/F/Type: 0/1/0/PCI
Address Offset: 34h
Default Value: 88h
Access: RO
Size: 8 bits

The capabilities pointer provides the address offset to the location of the first entry in this device's linked list of capabilities.

Bit	Access & Default	Description
7:0	RO 88h	**First Capability (CAPPTR1):** The first capability in the list is the Subsystem ID and Subsystem Vendor ID Capability.

6.1.22 INTRLINE1—Interrupt Line

B/D/F/Type: 0/1/0/PCI
Address Offset: 3Ch
Default Value: 00h
Access: R/W
Size: 8 bits

This register contains interrupt line routing information. The device itself does not use this value; rather, it is used by device drivers and operating systems to determine priority and vector information.

Bit	Access & Default	Description
7:0	R/W 00h	**Interrupt Connection (INTCON):** This field is used to communicate interrupt line routing information.

6.1.23 INTRPIN1—Interrupt Pin

B/D/F/Type: 0/1/0/PCI
Address Offset: 3Dh
Default Value: 01h
Access: RO
Size: 8 bits

This register specifies which interrupt pin this device uses.

Bit	Access & Default	Description
7:0	RO 01h	**Interrupt Pin (INTPIN):** As a single function device, the PCI Express device specifies INTA as its interrupt pin. 01h=INTA.

6.1.24 BCTRL1—Bridge Control

B/D/F/Type: 0/1/0/PCI
Address Offset: 3E–3Fh
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

This register provides extensions to the PCICMD1 register that are specific to PCI-PCI bridges. The BCTRL1 register provides additional control for the secondary interface (i.e., PCI Express-G) as well as some bits that affect the overall behavior of the "virtual" Host-PCI Express bridge in the (G)MCH (e.g., VGA compatible address ranges mapping).

Bit	Access & Default	Description
15:12	RO 0h	Reserved
11	RO 0b	**Discard Timer SERR# Enable (DTSERRE):** Not Applicable or Implemented. Hardwired to 0.
10	RO 0b	**Discard Timer Status (DTSTS):** Not Applicable or Implemented. Hardwired to 0.
9	RO 0b	**Secondary Discard Timer (SDT):** Not Applicable or Implemented. Hardwired to 0.
8	RO 0b	**Primary Discard Timer (PDT):** Not Applicable or Implemented. Hardwired to 0.
7	RO 0b	**Fast Back-to-Back Enable (FB2BEN):** Not Applicable or Implemented. Hardwired to 0.
6	R/W 0b	**Secondary Bus Reset (SRESET):** 0 = No secondary bus reset initiated 1 = Initiates a hot reset on the corresponding PCI Express Port. This will force the LTSSM to transition to the Hot Reset state (via Recovery) from L0, L0s, or L1 states.
5	RO 0b	**Master Abort Mode (MAMODE):** Does not apply to PCI Express. Hardwired to 0.
4	R/W 0b	**VGA 16-bit Decode (VGA16D):** Enables the PCI-to-PCI bridge to provide 16-bit decoding of VGA I/O address precluding the decoding of alias addresses every 1 KB. This bit only has meaning if bit 3 (VGA Enable) of this register is also set to 1, enabling VGA I/O decoding and forwarding by the bridge. 0 = Execute 10-bit address decodes on VGA I/O accesses. 1 = Execute 16-bit address decodes on VGA I/O accesses.

Bit	Access & Default	Description
3	R/W 0b	**VGA Enable (VGAEN):** This bit controls the routing of processor-initiated transactions targeting VGA compatible I/O and memory address ranges. 0 = Disable 1 = Enable
2	R/W 0b	**ISA Enable (ISAEN):** This bit is needed to exclude legacy resource decode to route ISA resources to legacy decode path. Modifies the response by the (G)MCH to an I/O access issued by the processor that target ISA I/O addresses. This applies only to I/O addresses that are enabled by the IOBASE and IOLIMIT registers. 0 = All addresses defined by the IOBASE and IOLIMIT for processor I/O transactions will be mapped to PCI Express-G. 1 = (G)MCH does not forward to PCI Express-G any I/O transactions addressing the last 768 bytes in each 1 KB block, even if the addresses are within the range defined by the IOBASE and IOLIMIT registers.
1	R/W 0b	**SERR Enable (SERREN):** 0 = No forwarding of error messages from secondary side to primary side that could result in an SERR. 1 = ERR_COR, ERR_NONFATAL, and ERR_FATAL messages result in SERR message when individually enabled by the Root Control register.
0	R/W 0b	**Parity Error Response Enable (PEREN):** This bit controls whether the Master Data Parity Error bit in the Secondary Status register is set when the (G)MCH receives across the link (upstream) a Read Data Completion Poisoned TLP 0 = Master Data Parity Error bit in Secondary Status register can **NOT** be set. 1 = Master Data Parity Error bit in Secondary Status register CAN be set.

6.1.25 PM_CAPID1—Power Management Capabilities

B/D/F/Type: 0/1/0/PCI
Address Offset: 80–83h
Default Value: C8039001h
Access: RO
Size: 32 bits

Bit	Access & Default	Description
31:27	RO 19h	**PME Support (PMES):** This field indicates the power states in which this device may indicate PME wake via PCI Express messaging. D0, D3hot, and D3cold. This device is not required to do anything to support D3hot and D3cold; it simply must report that those states are supported. Refer to the PCI Power Management 1.1 specification for encoding explanation and other power management details.
26	RO 0b	**D2 Power State Support (D2PSS):** Hardwired to 0 to indicate that the D2 power management state is NOT supported.
25	RO 0b	**D1 Power State Support (D1PSS):** Hardwired to 0 to indicate that the D1 power management state is NOT supported.
24:22	RO 000b	**Auxiliary Current (AUXC):** Hardwired to 0 to indicate that there are no 3.3Vaux auxiliary current requirements.
21	RO 0b	**Device Specific Initialization (DSI):** Hardwired to 0 to indicate that special initialization of this device is NOT required before generic class device driver is to use it.
20	RO 0b	**Auxiliary Power Source (APS):** Hardwired to 0.
19	RO 0b	**PME Clock (PMECLK):** Hardwired to 0 to indicate this device does NOT support PMEB generation.
18:16	RO 011b	**PCI PM CAP Version (PCIPMCV):** A value of 011b indicates that this function complies with revision 1.2 of the PCI Power Management Interface Specification.
15:8	RO 90h	**Pointer to Next Capability (PNC):** This contains a pointer to the next item in the capabilities list. If MSICH (CAPL[0] @ 7Fh) is 0, then the next item in the capabilities list is the Message Signaled Interrupts (MSI) capability at 90h
7:0	RO 01h	**Capability ID (CID):** Value of 01h identifies this linked list item (capability structure) as being for PCI Power Management registers.

6.1.26 PM_CS1—Power Management Control/Status

B/D/F/Type: 0/1/0/PCI
Address Offset: 84–87h
Default Value: 00000000h
Access: RO, R/W/S, R/W
Size: 32 bits

Bit	Access & Default	Description
31:16	RO 0000h	Reserved:
15	RO 0b	**PME Status (PMESTS):** This bit indicates that this device does not support PMEB generation from D3cold.
14:13	RO 00b	**Data Scale (DSCALE):** This field indicates that this device does not support the power management data register.
12:9	RO 0h	**Data Select (DSEL):** This field indicates that this device does not support the power management data register.
8	R/W/S 0b	**PME Enable (PMEE):** This bit indicates that this device does not generate PME# assertion from any D-state. 0 = PME# generation not possible from any D State 1 = PME# generation enabled from any D State The setting of this bit has no effect on hardware. See PM_CAP[15:11]
7:2	RO 00h	Reserved

Bit	Access & Default	Description
1:0	R/W 00b	**Power State (PS):** This field indicates the current power state of this device and can be used to set the device into a new power state. If software attempts to write an unsupported state to this field, write operation must complete normally on the bus, but the data is discarded and no state change occurs. 00 = D0 01 = D1 (Not supported in this device.) 10 = D2 (Not supported in this device.) 11 = D3 Support of D3cold does not require any special action. While in the D3hot state, this device can only act as the target of PCI configuration transactions (for power management control). This device also cannot generate interrupts or respond to MMR cycles in the D3 state. The device must return to the D0 state in order to be fully-functional. When the Power State is other than D0, the bridge will Master Abort (i.e., not claim) any downstream cycles (with exception of type 0 configuration cycles). Consequently, these unclaimed cycles will go down DMI and come back up as Unsupported Requests, which the (G)MCH logs as Master Aborts in Device 0 PCISTS[13] There is no additional hardware functionality required to support these Power States.

6.1.27 SS_CAPID—Subsystem ID and Vendor ID Capabilities

B/D/F/Type: 0/1/0/PCI
Address Offset: 88–8Bh
Default Value: 0000800Dh
Access: RO
Size: 32 bits

This capability is used to uniquely identify the subsystem where the PCI device resides. Because this device is an integrated part of the system and not an add-in device, it is anticipated that this capability will never be used. However, it is necessary because Microsoft will test for its presence.

Bit	Access & Default	Description
31:16	RO 0000h	Reserved
15:8	RO 80h	**Pointer to Next Capability (PNC):** This contains a pointer to the next item in the capabilities list which is the PCI Power Management capability.
7:0	RO 0Dh	**Capability ID (CID):** Value of 0Dh identifies this linked list item (capability structure) as being for SSID/SSVID registers in a PCI-to-PCI Bridge.

6.1.28 SS—Subsystem ID and Subsystem Vendor ID

B/D/F/Type: 0/1/0/PCI
Address Offset: 8C–8Fh
Default Value: 00008086h
Access: R/WO
Size: 32 bits

System BIOS can be used as the mechanism for loading the SSID/SVID values. These values must be preserved through power management transitions and a hardware reset.

Bit	Access & Default	Description
31:16	R/WO 0000h	**Subsystem ID (SSID):** This field indicates the particular subsystem and is assigned by the vendor.
15:0	R/WO 8086h	**Subsystem Vendor ID (SSVID):** This field indicates the manufacturer of the subsystem and is the same as the vendor ID which is assigned by the PCI Special Interest Group.

6.1.29 MSI_CAPID—Message Signaled Interrupts Capability ID

B/D/F/Type: 0/1/0/PCI
Address Offset: 90–91h
Default Value: A005h
Access: RO
Size: 16 bits

When a device supports MSI, it can generate an interrupt request to the processor by writing a predefined data item (a message) to a predefined memory address.

Bit	Access & Default	Description
15:8	RO A0h	**Pointer to Next Capability (PNC):** This field contains a pointer to the next item in the capabilities list which is the PCI Express capability.
7:0	RO 05h	**Capability ID (CID):** This field contains 05h that identifies this linked list item (capability structure) as being for MSI registers.

6.1.30 MC—Message Control

B/D/F/Type: 0/1/0/PCI
Address Offset: 92–93h
Default Value: 0000h
Access: R/W, RO
Size: 16 bits

System software can modify bits in this register, but the device is prohibited from doing so.

If the device writes the same message multiple times, only one of those messages is ensured to be serviced. If all of them must be serviced, the device must not generate the same message again until the driver services the earlier one.

Bit	Access & Default	Description
15:8	RO 00h	Reserved
7	RO 0b	**64-bit Address Capable (64AC):** Hardwired to 0 to indicate that the function does not implement the upper 32 bits of the Message Address register and is incapable of generating a 64-bit memory address.
6:4	R/W 000b	**Multiple Message Enable (MME):** System software programs this field to indicate the actual number of messages allocated to this device. This number will be equal to or less than the number actually requested. The encoding is the same as for the MMC field below.
3:1	RO |000b	**Multiple Message Capable (MMC):** System software reads this field to determine the number of messages being requested by this device. 000 = 1 (Number of Messages Requested) All other values are reserved.

Bit	Access & Default	Description
0	R/W 0b	**MSI Enable (MSIEN):** This bit controls the ability of this device to generate MSIs. 0 = Disable. MSI will **not** be generated. 1 = Enable. MSI will be generated when PME or HotPlug messages are received by the (G)MCH. INTA will not be generated and INTA Status (PCISTS1[3]) will not be set.

6.1.31 MA—Message Address

B/D/F/Type: 0/1/0/PCI
Address Offset: 94–97h
Default Value: 00000000h
Access: R/W, RO
Size: 32 bits

Bit	Access & Default	Description
31:2	R/W 00000000h	**Message Address (MA):** System software uses this field to assign an MSI address to the device. The device handles an MSI by writing the padded contents of the MD register to this address.
1:0	RO 00b	**Force DWord Align (FDWA):** Hardwired to 0 so that addresses assigned by system software are always aligned on a DWord address boundary.

6.1.32 MD—Message Data

B/D/F/Type: 0/1/0/PCI
Address Offset: 98–99h
Default Value: 0000h
Access: R/W
Size: 16 bits

Bit	Access & Default	Description
15:0	R/W 0000h	**Message Data (MD):** This field is the base message data pattern assigned by system software and used to handle an MSI from the device. When the device must generate an interrupt request, it writes a 32-bit value to the memory address specified in the MA register. The upper 16 bits are always set to 0. The lower 16 bits are supplied by this register.

6.1.33 PEG_CAPL—PCI Express* Capability List

B/D/F/Type: 0/1/0/PCI
Address Offset: A0–A1h
Default Value: 0010h
Access: RO
Size: 16 bits

This register enumerates the PCI Express capability structure.

Bit	Access & Default	Description
15:8	RO 00h	**Pointer to Next Capability (PNC):** This value terminates the capabilities list. The Virtual Channel capability and any other PCI Express specific capabilities that are reported via this mechanism are in a separate capabilities list located entirely within PCI Express Extended Configuration Space.
7:0	RO 10h	**Capability ID (CID):** This field identifies this linked list item (capability structure) as being for PCI Express registers.

6.1.34 PEG_CAP—PCI Express* Capabilities

B/D/F/Type: 0/1/0/PCI
Address Offset: A2–A3h
Default Value: 0141h
Access: RO, R/WO
Size: 16 bits

This register indicates PCI Express device capabilities.

Bit	Access & Default	Description
15:14	RO	Reserved
13:9	RO 00b	**Interrupt Message Number (IMN):** Not Applicable or Implemented. Hardwired to 0.
8	R/WO 1b	**Slot Implemented (SI):** 0 = The PCI Express Link associated with this port is connected to an integrated component or is disabled. 1 = The PCI Express Link associated with this port is connected to a slot.
7:4	RO 4h	**Device/Port Type (DPT):** Hardwired to 4h to indicate root port of PCI Express Root Complex.
3:0	RO 1h	**PCI Express Capability Version (PCI EXPRESS*CV):** Hardwired to 1h as it is the first version.

6.1.35 DCAP—Device Capabilities

B/D/F/Type: 0/1/0/PCI
Address Offset: A4–A7h
Default Value: 00008000h
Access: RO
Size: 32 bits

This register indicates PCI Express device capabilities.

Bit	Access & Default	Description
31:16	RO 0000h	Reserved
15	RO 1b	**Role Based Error Reporting (RBER):** Hardwired to 1 indicating that this device implements the functionality defined in the Error Reporting ECN as required by the PCI Express 1.1 spec.
14:6	RO 000h	Reserved:
5	RO 0b	**Extended Tag Field Supported (ETFS):** Hardwired to 0 indicating support for 5-bit Tags as a Requestor.
4:3	RO 00b	**Phantom Functions Supported (PFS):** Not Applicable or Implemented. Hardwired to 0.
2:0	RO 000b	**Max Payload Size (MPS):** Hardwired to indicate 128B maximum supported payload for Transaction Layer Packets (TLP).

6.1.36 DCTL—Device Control

B/D/F/Type: 0/1/0/PCI
Address Offset: A8–A9h
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

This register provides control for PCI Express device specific capabilities. The error reporting enable bits are in reference to errors detected by this device, not error messages received across the link. The reporting of error messages (ERR_CORR, ERR_NONFATAL, ERR_FATAL) received by Root Port is controlled exclusively by Root Port Command Register.

Bit	Access & Default	Description
15:8	RO 000h	Reserved
7:5	R/W 000b	**Max Payload Size (MPS):** Hardware ignores this field. It is writeable only to support compliance testing. 000 = 128B maximum supported payload for Transaction Layer Packets (TLP). As a receiver, the Device must handle TLPs as large as the set value; as transmitter, the Device must not generate TLPs exceeding the set value. All other encodings are reserved.
4	RO 0b	Reserved for Enable Relaxed Ordering
3	R/W 0b	**Unsupported Request Reporting Enable (URRE):** 0 = Disable. 1 = Enable. Allows signaling ERR_NONFATAL, ERR_FATAL, or ERR_CORR to the Root Control register when detecting an unmasked Unsupported Request (UR). An ERR_CORR is signaled when an unmasked Advisory Non-Fatal UR is received. An ERR_FATAL or ERR_NONFATAL is sent to the Root Control register when an uncorrectable non-Advisory UR is received with the severity bit set in the Uncorrectable Error Severity register.
2	R/W 0b	**Fatal Error Reporting Enable (FERE):** 0 = Disable 1 = Enables signaling of ERR_FATAL to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.
1	R/W 0b	**Non-Fatal Error Reporting Enable (NERE):** 0 = Disable 1 = Enables signaling of ERR_NONFATAL to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.

Bit	Access & Default	Description
0	R/W 0b	**Correctable Error Reporting Enable (CERE):** 0 = Disable 1 = Enables signaling of ERR_CORR to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.

6.1.37 DSTS—Device Status

B/D/F/Type: 0/1/0/PCI
Address Offset: AA–ABh
Default Value: 0000h
Access: RO, R/WC
Size: 16 bits

This register reflects status corresponding to controls in the Device Control register. The error reporting bits are in reference to errors detected by this device, not errors messages received across the link.

Bit	Access & Default	Description
15:6	RO 000h	Reserved and Zero: For future R/WC/S implementations; software must use 0 for writes to bits.
5	RO 0b	**Transactions Pending (TP):** 0 = All pending transactions (including completions for any outstanding non-posted requests on any used virtual channel) have been completed. 1 = Device has transaction(s) pending (including completions for any outstanding non-posted requests for all used Traffic Classes).
4	RO 0b	Reserved
3	R/WC 0b	**Unsupported Request Detected (URD):** 0 = Unsupported request **Not** detected. 1 = Device received an Unsupported Request. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control Register. Additionally, the Non-Fatal Error Detected bit or the Fatal Error Detected bit is set according to the setting of the Unsupported Request Error Severity bit. In production systems setting the Fatal Error Detected bit is not an option as support for AER will not be reported.

Bit	Access & Default	Description
2	R/WC 0b	**Fatal Error Detected (FED):** 0 = Fatal error **Not** detected. 1 = Fatal error(s) were detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. When Advanced Error Handling is enabled, errors are logged in this register regardless of the settings of the uncorrectable error mask register.
1	R/WC 0b	**Non-Fatal Error Detected (NFED):** 0 = Non-Fatal error **Not** detected. 1 = Non-fatal error(s) were detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. When Advanced Error Handling is enabled, errors are logged in this register regardless of the settings of the uncorrectable error mask register.
0	R/WC 0b	**Correctable Error Detected (CED):** 0 = Correctable error **Not** detected. 1 = Correctable error(s) were detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. When Advanced Error Handling is enabled, errors are logged in this register regardless of the settings of the correctable error mask register.

6.1.38 LCAP—Link Capabilities

B/D/F/Type: 0/1/0/PCI
Address Offset: AC–AFh
Default Value: 02014D01h
Access: RO, R/WO
Size: 32 bits

This register Indicates PCI Express device specific capabilities.

Bit	Access & Default	Description
31:24	RO 02h	**Port Number (PN):** This field indicates the PCI Express port number for the given PCI Express link. Matches the value in Element Self Description[31:24].
23:21	RO 000b	Reserved
20	RO 0b	**Data Link Layer Link Active Reporting Capable (DLLLARC):** For a Downstream Port, this bit must be set to 1b if the component supports the optional capability of reporting the DL_Active state of the Data Link Control and Management State Machine. For a hot-plug capable Downstream Port (as indicated by the Hot-Plug Capable field of the Slot Capabilities register), this bit must be set to 1b. For Upstream Ports and components that do not support this optional capability, this bit must be hardwired to 0b.
19	RO 0b	**Surprise Down Error Reporting Capable (SDERC):** For a Downstream Port, this bit must be set to 1b if the component supports the optional capability of detecting and reporting a Surprise Down error condition. For Upstream Ports and components that do not support this optional capability, this bit must be hardwired to 0b.
18	RO 0b	**Clock Power Management (CPM):** A value of 1b in this bit indicates that the component tolerates the removal of any reference clock(s) when the link is in the L1 and L2/3 Ready link states. A value of 0b indicates the component does not have this capability and that reference clock(s) must not be removed in these link states. This capability is applicable only in form factors that support "clock request" (CLKREQ#) capability. For a multi-function device, each function indicates its capability independently. Power Management configuration software must only permit reference clock removal if all functions of the multifunction device indicate a 1b in this bit.
17:15	R/WO 010b	**L1 Exit Latency (L1ELAT):** This field indicates the length of time this port requires to complete the transition from L1 to L0. The value 010 b indicates the range of 2 us to less than 4 us. Both bytes of this register that contain a portion of this field must be written simultaneously in order to prevent an intermediate (and undesired) value from ever existing.

Bit	Access & Default	Description
14:12	RO 100b	**L0s Exit Latency (L0SELAT):** This field indicates the length of time this Port requires to complete the transition from L0s to L0. 000 = Less than 64 ns 001 = 64ns to less than 128ns 010 = 128ns to less than 256 ns 011 = 256ns to less than 512ns 100 = 512ns to less than 1us 101 = 1 us to less than 2 us 110 = 2 us - 4 us 111 = More than 4 us The actual value of this field depends on the common Clock Configuration bit (LCTL[6]) and the Common and Non-Common clock L0s Exit Latency values in PEGL0SLAT (Offset 22Ch)
11:10	R/WO 11b	**Active State Link PM Support (ASLPMS):** BIOS Requirement: Desktop chipsets do not support ASPM L1, so BIOS should program this field to 01.
9:4	RO 10h	**Max Link Width (MLW):** This field indicates the maximum number of lanes supported for this link.
3:0	RO 1h	**Max Link Speed (MLS):** Hardwired to indicate 2.5 Gb/s.

6.1.39 LCTL—Link Control

B/D/F/Type: 0/1/0/PCI
Address Offset: B0–B1h
Default Value: 0000h
Access: RO, R/W, R/W/SC
Size: 16 bits
BIOS Optimal Default 0h

This register allows control of PCI Express link.

Bit	Access & Default	Description
15:9	RO 0000000b	Reserved
8	RO 0b	**Enable Clock Power Management (ECPM):** Applicable only for form factors that support a "Clock Request" (CLKREQ#) mechanism, this enable functions as follows 0 = Disable. Clock power management is disabled and device must hold CLKREQ# signal low. (default) 1 = Enable. Device is permitted to use CLKREQ# signal to power manage link clock according to protocol defined in appropriate form factor specification. Components that do not support Clock Power Management (as indicated by a 0b value in the Clock Power Management bit of the Link Capabilities Register) must hardwire this bit to 0b.
7	R/W 0b	**Extended Synch (ES):** 0 = Standard Fast Training Sequence (FTS). 1= Forces the transmission of additional ordered sets when exiting the L0s state and when in the Recovery state. This mode provides external devices (e.g., logic analyzers) monitoring the Link time to achieve bit and symbol lock before the link enters L0 and resumes communication. This is a test mode only and may cause other undesired side effects such as buffer overflows or underruns.
6	R/W 0b	**Common Clock Configuration (CCC):** The state of this bit affects the L0s Exit Latency reported in LCAP[14:12] and the N_FTS value advertised during link training. See PEGL0SLAT at offset 22Ch. 0 = This component and the component at the opposite end of this Link are operating with asynchronous reference clock. 1 = This component and the component at the opposite end of this Link are operating with a distributed common reference clock.
5	R/W/SC 0b	**Retrain Link (RL):** This bit always returns 0 when read. This bit is cleared automatically (no need to write a 0). 0 = Normal operation. 1 = Full Link retraining is initiated by directing the Physical Layer LTSSM from L0, L0s, or L1 states to the Recovery state.

Bit	Access & Default	Description
4	R/W 0b	**Link Disable (LD):** Writes to this bit are immediately reflected in the value read from the bit, regardless of actual Link state. 0 = Normal operation 1 = Link is disabled. Forces the LTSSM to transition to the Disabled state (via Recovery) from L0, L0s, or L1 states. Link retraining happens automatically on 0-to-1 transition, just like when coming out of reset.
3	RO 0b	**Read Completion Boundary (RCB):** Hardwired to 0 to indicate 64 byte.
2	RO 0b	Reserved.
1:0	R/W 00b	**Active State PM (ASPM):** This field controls the level of active state power management supported on the given link. 00 = Disabled 01 = L0s Entry Supported 10 = Reserved 11 = L0s and L1 Entry Supported

6.1.40 LSTS—Link Status

B/D/F/Type: 0/1/0/PCI
Address Offset: B2–B3h
Default Value: 1001h
Access: RO
Size: 16 bits

This register indicates PCI Express link status.

Bit	Access & Default	Description
15:14	RO 00b	Reserved and Zero: For future R/WC/S implementations; software must use 0 for writes to bits.
13	RO 0b	**Data Link Layer Link Active (Optional) (DLLLA):** This bit indicates the status of the Data Link Control and Management State Machine. It returns a 1b to indicate the DL_Active state, 0b otherwise. This bit must be implemented if the corresponding Data Link Layer Active Capability bit is implemented. Otherwise, this bit must be hardwired to 0b.
12	RO 1b	**Slot Clock Configuration (SCC):** 0 = The device uses an independent clock irrespective of the presence of a reference on the connector. 1 = The device uses the same physical reference clock that the platform provides on the connector.
11	RO 0b	**Link Training (LTRN):** This bit indicates that the Physical Layer LTSSM is in the Configuration or Recovery state, or that 1b was written to the Retrain Link bit but Link training has not yet begun. Hardware clears this bit when the LTSSM exits the Configuration/Recovery state once Link training is complete.
10	RO 0b	**Undefined:** The value read from this bit is undefined. In previous versions of this specification, this bit was used to indicate a Link Training Error. System software must ignore the value read from this bit. System software is permitted to write any value to this bit.
9:4	RO 00h	**Negotiated Width (NW):** This bit indicates negotiated link width. This field is valid only when the link is in the L0, L0s, or L1 states (after link width negotiation is successfully completed). 00h = Reserved 01h = X1 02h = Reserved 04h = Reserved 08h = Reserved 10h = X16 All other encodings are reserved.
3:0	RO 1h	**Negotiated Speed (NS):** This field indicates negotiated link speed. 1h = 2.5 Gb/s All other encodings are reserved.

6.1.41 SLOTCAP—Slot Capabilities

B/D/F/Type: 0/1/0/PCI
Address Offset: B4–B7h
Default Value: 00040000h
Access: R/WO, RO
Size: 32 bits

PCI Express Slot related registers allow for the support of Hot Plug.

Bit	Access & Default	Description
31:19	R/WO 0000h	**Physical Slot Number (PSN):** This field indicates the physical slot number attached to this Port.
18	R/WO 1b	**No Command Completed Support (NCCS):** 1 = This slot does not generate software notification when an issued command is completed by the Hot-Plug Controller. This bit is only permitted to be set to 1b if the hotplug capable port is able to accept writes to all fields of the Slot Control register without delay between successive writes.
17	RO 0b	Reserved: Reserved for Electromechanical Interlock Present (EIP).
16:15	R/WO 00b	**Slot Power Limit Scale (SPLS):** This field specifies the scale used for the Slot Power Limit Value. 00 = 1.0x 01 = 0.1x 10 = 0.01x 11 = 0.001x If this field is written, the link sends a Set_Slot_Power_Limit message.
14:7	R/WO 00h	**Slot Power Limit Value (SPLV):** In combination with the Slot Power Limit Scale value, this field specifies the upper limit on power supplied by slot. Power limit (in Watts) is calculated by multiplying the value in this field by the value in the Slot Power Limit Scale field. If this field is written, the link sends a Set_Slot_Power_Limit message.
6	RO 0b	**Hot-plug Capable (HPC):** 0 = Not Hot-plug capable 1 = Slot is capable of supporting hot-lug operations.
5	RO 0b	**Hot-plug Surprise (HPS):** 0 = No Hot-plug surprise 1 = An adapter present in this slot might be removed from the system without any prior notification. This is a form factor specific capability. This bit is an indication to the operating system to allow for such removal without impacting continued software operation.

Bit	Access & Default	Description
4	RO 0b	**Power Indicator Present (PIP):** 0 = No power indicator 1 = A Power Indicator is electrically controlled by the chassis for this slot.
3	RO 0b	**Attention Indicator Present (AIP):** 0 = No Attention indicator 1 = An Attention Indicator is electrically controlled by the chassis.
2	RO 0b	**MRL Sensor Present (MSP):** 0 = No MRL sensor 1 = MRL Sensor is implemented on the chassis for this slot.
1	RO 0b	**Power Controller Present (PCP):** 0 = No power controller 1 = A software programmable Power Controller is implemented for this slot/adapter (depending on form factor).
0	RO 0b	**Attention Button Present (ABP):** 0 = No attention button 1 = An Attention Button for this slot is electrically controlled by the chassis.

6.1.42 SLOTCTL—Slot Control

B/D/F/Type: 0/1/0/PCI
Address Offset: B8–B9h
Default Value: 01C0h
Access: RO, R/W
Size: 16 bits

PCI Express Slot related registers allow for the support of Hot Plug.

Bit	Access & Default	Description
15:13	RO 000b	Reserved
12	RO 0b	**Data Link Layer State Changed Enable (DLLSCE):** If the Data Link Layer Link Active capability is implemented, when set to 1b, this field enables software notification when Data Link Layer Link Active field is changed.
11	RO 0b	**Electromechanical Interlock Control (EIC):** If an Electromechanical Interlock is implemented, a write of 1b to this field causes the state of the interlock to toggle. A write of 0b to this field has no effect. A read to this register always returns a 0.
10	RO 0b	**Power Controller Control (PCC):** If a Power Controller is implemented, this field when written sets the power state of the slot per the defined encodings. Reads of this field must reflect the value from the latest write, even if the corresponding hotplug command is not complete, unless software issues a write without waiting for the previous command to complete in which case the read value is undefined. Depending on the form factor, the power is turned on/off either to the slot or within the adapter. Note that in some cases the power controller may autonomously remove slot power or not respond to a power-up request based on a detected fault condition, independent of the Power Controller Control setting. 0 = Power On 1 = Power Off If the Power Controller Implemented field in the Slot Capabilities register is set to 0b, then writes to this field have no effect and the read value of this field is undefined.
9:8	RO 01b	**Power Indicator Control (PIC):** If a Power Indicator is implemented, writes to this field set the Power Indicator to the written state. Reads of this field must reflect the value from the latest write, even if the corresponding hot-plug command is not complete, unless software issues a write without waiting for the previous command to complete in which case the read value is undefined. 00 = Reserved 01 = On 10 = Blink 11 = Off

Bit	Access & Default	Description
7:6	RO 11b	**Attention Indicator Control (AIC):** If an Attention Indicator is implemented, writes to this field set the Attention Indicator to the written state. Reads of this field must reflect the value from the latest write, even if the corresponding hot-plug command is not complete, unless software issues a write without waiting for the previous command to complete in which case the read value is undefined. If the indicator is electrically controlled by chassis, the indicator is controlled directly by the downstream port through implementation specific mechanisms. 00 = Reserved 01 = On 10 = Blink 11 = Off
5	RO 0b	**Hot-plug Interrupt Enable (HPIE):** 0 = Disable 1 = Enables generation of an interrupt on enabled hot-plug events Default value of this field is 0b. If the Hot Plug Capable field in the Slot Capabilities register is set to 0b, this bit is permitted to be read-only with a value of 0b.
4	RO 0b	**Command Completed Interrupt Enable (CCI):** If Command Completed notification is supported (as indicated by No Command Completed Support field of Slot Capabilities Register), when set to 1b, this bit enables software notification when a hot-plug command is completed by the Hot-Plug Controller. If Command Completed notification is not supported, this bit must be hardwired to 0b.
3	R/W 0b	**Presence Detect Changed Enable (PDCE):** 0 = Disable 1 = Enables software notification on a presence detect changed event.
2	RO 0b	**MRL Sensor Changed Enable (MSCE):** If the MRL Sensor Present field in the Slot Capabilities register is set to 0b, this bit is permitted to be read-only with a value of 0b. 0 = Disable (default) 1 = Enables software notification on a MRL sensor changed event.
1	RO 0b	**Power Fault Detected Enable (PFDE):** If Power Fault detection is not supported, this bit is permitted to be read-only with a value of 0b 0 = Disable (default) 1 = Enables software notification on a power fault event.
0	RO 0b	**Attention Button Pressed Enable (ABPE):** 0 = Disable (default) 1 = Enables software notification on an attention button pressed event.

6.1.43 SLOTSTS—Slot Status

B/D/F/Type: 0/1/0/PCI
Address Offset: BA–BBh
Default Value: 0000h
Access: RO, R/WC
Size: 16 bits

PCI Express Slot related registers allow for the support of Hot Plug.

Bit	Access & Default	Description
15:7	RO 0000000b	Reserved and Zero: For future R/WC/S implementations; software must use 0 for writes to bits.
6	RO 0b	**Presence Detect State (PDS):** This bit indicates the presence of an adapter in the slot, reflected by the logical "OR" of the Physical Layer in-band presence detect mechanism and, if present, any out-of-band presence detect mechanism defined for the slot's corresponding form factor. Note that the in-band presence detect mechanism requires that power be applied to an adapter for its presence to be detected. Consequently, form factors that require a power controller for hot-plug must implement a physical pin presence detect mechanism. 0 = Slot Empty 1 = Card Present in slot This register must be implemented on all Downstream Ports that implement slots. For Downstream Ports not connected to slots (where the Slot Implemented bit of the PCI Express Capabilities Register is 0b), this bit must return 1b.
5	RO 0b	Reserved
4	RO	**Command Completed (CC):** If Command Completed notification is supported (as indicated by No Command Completed Support field of Slot Capabilities Register), this bit is set when a hot-plug command has completed and the Hot-Plug Controller is ready to accept a subsequent command. The Command Completed status bit is set as an indication to host software that the Hot-Plug Controller has processed the previous command and is ready to receive the next command; it provides no assurance that the action corresponding to the command is complete. If Command Completed notification is not supported, this bit must be hardwired to 0b.
3	R/WC 0b	**Detect Changed (PDC):** This bit is set when the value reported in Presence Detect State is changed.
2	RO 0b	**MRL Sensor Changed (MSC):** If an MRL sensor is implemented, this bit is set when a MRL Sensor state change is detected. If an MRL sensor is not implemented, this bit must not be set.

Bit	Access & Default	Description
1	RO 0b	**Power Fault Detected (PFD):** If a Power Controller that supports power fault detection is implemented, this bit is set when the Power Controller detects a power fault at this slot. Note that, depending on hardware capability, it is possible that a power fault can be detected at any time, independent of the Power Controller Control setting or the occupancy of the slot. If power fault detection is not supported, this bit must not be set.
0	RO 0b	**Attention Button Pressed (ABP):** If an Attention Button is implemented, this bit is set when the attention button is pressed. If an Attention Button is not supported, this bit must not be set.

6.1.44 RCTL—Root Control

B/D/F/Type: 0/1/0/PCI
Address Offset: BC–BDh
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

This register allows control of PCI Express Root Complex specific parameters. The system error control bits in this register determine if corresponding SERRs are generated when our device detects an error (reported in this device's Device Status register) or when an error message is received across the link. Reporting of SERR as controlled by these bits takes precedence over the SERR Enable in the PCI Command Register.

Bit	Access & Default	Description
15:4	RO 000h	Reserved
3	R/W 0b	**PME Interrupt Enable (PMEIE):** 0 = No interrupts are generated as a result of receiving PME messages. 1 = Enables interrupt generation upon receipt of a PME message as reflected in the PME Status bit of the Root Status Register. A PME interrupt is also generated if the PME Status bit of the Root Status Register is set when this bit is set from a cleared state.
2	R/W 0b	**System Error on Fatal Error Enable (SEFEE):** This bit controls the Root Complex's response to fatal errors. 0 = No SERR generated on receipt of fatal error. 1 = SERR should be generated if a fatal error is reported by any of the devices in the hierarchy associated with this Root Port, or by the Root Port itself.
1	R/W 0b	**System Error on Non-Fatal Uncorrectable Error Enable (SENFUEE):** This bit controls the Root Complex's response to non-fatal errors. 0 = No SERR generated on receipt of non-fatal error. 1 = SERR should be generated if a non-fatal error is reported by any of the devices in the hierarchy associated with this Root Port, or by the Root Port itself.
0	R/W 0b	**System Error on Correctable Error Enable (SECEE):** This bit controls the Root Complex's response to correctable errors. 0 = No SERR generated on receipt of correctable error. 1 = SERR should be generated if a correctable error is reported by any of the devices in the hierarchy associated with this Root Port, or by the Root Port itself.

6.1.45 RSTS—Root Status

B/D/F/Type: 0/1/0/PCI
Address Offset: C0–C3h
Default Value: 00000000h
Access: RO, R/WC
Size: 32 bits

This register provides information about PCI Express Root Complex specific parameters.

Bit	Access & Default	Description
31:18	RO 0000h	Reserved
17	RO 0b	**PME Pending (PMEP):** 1 = Another PME is pending when the PME Status bit is set. When the PME Status bit is cleared by software; the PME is delivered by hardware by setting the PME Status bit again and updating the Requestor ID appropriately. The PME pending bit is cleared by hardware if no more PMEs are pending.
16	R/WC 0b	**PME Status (PMES):** 1 = PME was asserted by the requestor ID indicated in the PME Requestor ID field. Subsequent PMEs are kept pending until the status register is cleared by writing a 1 to this field.
15:0	RO 0000h	**PME Requestor ID (PMERID):** This field indicates the PCI requestor ID of the last PME requestor.

6.1.46 PEGLC—PCI Express*-G Legacy Control

B/D/F/Type: 0/1/0/PCI
Address Offset: EC–EFh
Default Value: 00000000h
Access: R/W, RO
Size: 32 bits

This register controls functionality that is needed by Legacy (non-PCI Express aware) operating systems during run time.

Bit	Access & Default	Description
31:3	RO 00000000h	Reserved
2	R/W 0b	**PME GPE Enable (PMEGPE):** 0 = Do Not generate GPE PME message when PME is received. 1 = Generate a GPE PME message when PME is received (Assert_PMEGPE and De-assert_PMEGPE messages on DMI). This enables the (G)MCH to support PMEs on the PEG port under legacy operating systems.
1	R/W 0b	**Hot-Plug GPE Enable (HPGPE):** 0 = Do Not generate GPE Hot-Plug message when Hot-Plug event is received. 1 = Generate a GPE Hot-Plug message when Hot-Plug Event is received (Assert_HPGPE and Deassert_HPGPE messages on DMI). This enables the (G)MCH to support Hot-Plug on the PEG port under legacy operating systems.
0	R/W 0b	**General Message GPE Enable (GENGPE):** 0 = Do Not forward received GPE assert/de-assert messages. 1 = Forward received GPE assert/de-assert messages. These general GPE message can be received via the PEG port from an external Intel device (i.e., PxH) and will be subsequently forwarded to the ICH (via Assert_GPE and Deassert_GPE messages on DMI). For example, PxH might send this message if a PCI Express device is hot plugged into a PxH downstream port.

6.1.47 VCECH—Virtual Channel Enhanced Capability Header

B/D/F/Type: 0/1/0/MMR
Address Offset: 100–103h
Default Value: 14010002h
Access: RO
Size: 32 bits

This register indicates PCI Express device Virtual Channel capabilities. Extended capability structures for PCI Express devices are located in PCI Express extended configuration space and have different field definitions than standard PCI capability structures.

Bit	Access & Default	Description
31:20	RO 140h	**Pointer to Next Capability (PNC):** The Link Declaration Capability is the next in the PCI Express extended capabilities list.
19:16	RO 1h	**PCI Express Virtual Channel Capability Version (PCI EXPRESS*VCCV):** Hardwired to 1 to indicate compliances with the 1.1 version of the PCI Express specification.
15:0	RO 0002h	**Extended Capability ID (ECID):** Value of 0002h identifies this linked list item (capability structure) as being for PCI Express Virtual Channel registers.

6.1.48 PVCCAP1—Port VC Capability Register 1

B/D/F/Type: 0/1/0/MMR
Address Offset: 104–107h
Default Value: 00000000h
Access: RO
Size: 32 bits

This register describes the configuration of PCI Express Virtual Channels associated with this port.

Bit	Access & Default	Description
31:7	RO 0000000h	Reserved
6:4	RO 000b	**Low Priority Extended VC Count (LPEVCC):** This field indicates the number of (extended) Virtual Channels in addition to the default VC belonging to the low-priority VC (LPVC) group that has the lowest priority with respect to other VC resources in a strict-priority VC Arbitration. The value of 0 in this field implies strict VC arbitration.
3	RO 0b	Reserved
2:0	RO 000b	**Extended VC Count (EVCC):** This field indicates the number of (extended) Virtual Channels in addition to the default VC supported by the device.

6.1.49 PVCCAP2—Port VC Capability Register 2

B/D/F/Type: 0/1/0/MMR
Address Offset: 108–10Bh
Default Value: 00000000h
Access: RO
Size: 32 bits

This register describes the configuration of PCI Express Virtual Channels associated with this port.

Bit	Access & Default	Description
31:24	RO 00h	**VC Arbitration Table Offset (VCATO):** This field indicates the location of the VC Arbitration Table. This field contains the zero-based offset of the table in DQWORDS (16 bytes) from the base address of the Virtual Channel Capability Structure. A value of 0 indicates that the table is not present (due to fixed VC priority).
23:8	RO 0000h	Reserved
7:0	RO 00h	Reserved

6.1.50 PVCCTL—Port VC Control

B/D/F/Type: 0/1/0/MMR
Address Offset: 10C–10Dh
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

Bit	Access & Default	Description
15:4	RO 000h	Reserved
3:1	R/W 000b	**VC Arbitration Select (VCAS):** This field will be programmed by software to the only possible value as indicated in the VC Arbitration Capability field. Since there is no other VC supported than the default, this field is reserved.
0	RO 0b	Reserved

6.1.51 VC0RCAP—VC0 Resource Capability

B/D/F/Type: 0/1/0/MMR
Address Offset: 110–113h
Default Value: 00000000h
Access: RO
Size: 32 bits

Bit	Access & Default	Description
31:16	RO 0000h	Reserved
15	RO 0b	**Reject Snoop Transactions (RSNPT):** 0 = Transactions with or without the No Snoop bit set within the TLP header are allowed on this VC. 1 = Any transaction without the No Snoop bit set within the TLP header will be rejected as an Unsupported Request.
14:0	RO 0000h	Reserved

6.1.52 VC0RCTL—VC0 Resource Control

B/D/F/Type: 0/1/0/MMR
Address Offset: 114–117h
Default Value: 800000FFh
Access: RO, R/W
Size: 32 bits

This register controls the resources associated with PCI Express Virtual Channel 0.

Bit	Access & Default	Description
31	RO 1b	**VC0 Enable (VC0E):** For VC0, this bit is hardwired to 1 and read only as VC0 can never be disabled.
30:27	RO 0h	Reserved
26:24	RO 000b	**VC0 ID (VC0ID):** This field assigns a VC ID to the VC resource. For VC0, this field is hardwired to 0s and read only.
23:8	RO 0000h	Reserved
7:1	R/W 7Fh	**TC/VC0 Map (TCVC0M):** This field indicates the TCs (Traffic Classes) that are mapped to the VC resource. Bit locations within this field correspond to TC values. For example, when bit 7 is set in this field, TC7 is mapped to this VC resource. When more than one bit in this field is set, it indicates that multiple TCs are mapped to the VC resource. To remove one or more TCs from the TC/VC Map of an enabled VC, software must ensure that no new or outstanding transactions with the TC labels are targeted at the given Link.
0	RO 1b	**TC0/VC0 Map (TC0VC0M):** Traffic Class 0 is always routed to VC0.

6.1.53 VC0RSTS—VC0 Resource Status

B/D/F/Type: 0/1/0/MMR
Address Offset: 11A–11Bh
Default Value: 0002h
Access: RO
Size: 16 bits

This register reports the Virtual Channel specific status.

Bit	Access & Default	Description
15:2	RO 0000h	Reserved
1	RO 1b	**VC0 Negotiation Pending (VC0NP):** 0 = The VC negotiation is complete. 1 = The VC resource is still in the process of negotiation (initialization or disabling). This bit indicates the status of the process of Flow Control initialization. It is set by default on Reset, as well as whenever the corresponding Virtual Channel is Disabled or the Link is in the DL_Down state. It is cleared when the link successfully exits the FC_INIT2 state. Before using a Virtual Channel, software must check whether the VC Negotiation Pending fields for that Virtual Channel are cleared in both Components on a Link.
0	RO 0b	Reserved

6.1.54 RCLDECH—Root Complex Link Declaration Enhanced

B/D/F/Type: 0/1/0/MMR
Address Offset: 140–143h
Default Value: 00010005h
Access: RO
Size: 32 bits

This capability declares links from this element (PEG) to other elements of the root complex component to which it belongs. See PCI Express specification for link/topology declaration requirements.

Bit	Access & Default	Description
31:20	RO 000h	**Pointer to Next Capability (PNC):** This is the last capability in the PCI Express extended capabilities list
19:16	RO 1h	**Link Declaration Capability Version (LDCV):** Hardwired to 1 to indicate compliances with the 1.1 version of the PCI Express specification.
15:0	RO 0005h	**Extended Capability ID (ECID):** The value of 0005h identifies this linked list item (capability structure) as being for PCI Express Link Declaration Capability.

6.1.55 ESD—Element Self Description

B/D/F/Type: 0/1/0/MMR
Address Offset: 144–147h
Default Value: 02000100h
Access: RO, R/WO
Size: 32 bits

This register provides information about the root complex element containing this Link Declaration Capability.

Bit	Access & Default	Description
31:24	RO 02h	**Port Number (PN):** This field specifies the port number associated with this element with respect to the component that contains this element. This port number value is used by the egress port of the component to provide arbitration to this Root Complex Element.
23:16	R/WO 00h	**Component ID (CID):** This field identifies the physical component that contains this Root Complex Element.
15:8	RO 01h	**Number of Link Entries (NLE):** This field identifies the number of link entries following the Element Self Description. This field reports 1 (to Egress port only as we don't report any peer-to-peer capabilities in our topology).
7:4	RO 0h	Reserved
3:0	RO 0h	**Element Type (ET):** This field identifies the type of the Root Complex Element. Value of 0 h represents a root port.

6.1.56 LE1D—Link Entry 1 Description

B/D/F/Type: 0/1/0/MMR
Address Offset: 150–153h
Default Value: 00000000h
Access: RO, R/WO
Size: 32 bits

This register provides the first part of a Link Entry which declares an internal link to another Root Complex Element.

Bit	Access & Default	Description
31:24	RO 00h	**Target Port Number (TPN):** This field specifies the port number associated with the element targeted by this link entry (Egress Port). The target port number is with respect to the component that contains this element as specified by the target component ID.
23:16	R/WO 00h	**Target Component ID (TCID):** This field identifies the physical or logical component that is targeted by this link entry.
15:2	RO 0000h	Reserved
1	RO 0b	**Link Type (LTYP):** This field identifies that the link points to memory-mapped space (for RCRB). The link address specifies the 64-bit base address of the target RCRB.
0	R/WO 0b	**Link Valid (LV):** 0 = Link Entry is not valid and will be ignored. 1 = Link Entry specifies a valid link.

6.1.57 LE1A—Link Entry 1 Address

B/D/F/Type: 0/1/0/MMR
Address Offset: 158–15Fh
Default Value: 0000000000000000h
Access: RO, R/WO
Size: 64 bits

This register provides the second part of a Link Entry which declares an internal link to another Root Complex Element.

Bit	Access & Default	Description
63:32	RO 00000000h	Reserved
31:12	R/WO 00000h	**Link Address (LA):** This field contains the memory-mapped base address of the RCRB that is the target element (Egress Port) for this link entry.
11:0	RO 000h	Reserved

6.1.58 PEGSSTS—PCI Express*-G Sequence Status

B/D/F/Type: 0/1/0/MMR
Address Offset: 218–21Fh
Default Value: 0000000000000FFFh
Access: RO
Size: 64 bits

This register provides PCI Express status reporting that is required by the PCI Express specification.

Bit	Access & Default	Description
63:60	RO 0h	Reserved
59:48	RO 000h	**Next Transmit Sequence Number (NTSN):** This field indicates the value of the NXT_TRANS_SEQ counter. This counter represents the transmit Sequence number to be applied to the next TLP to be transmitted onto the Link for the first time.
47:44	RO 0h	Reserved
43:32	RO 000h	**Next Packet Sequence Number (NPSN):** This field indicates the packet sequence number to be applied to the next TLP to be transmitted or re-transmitted onto the Link.
31:28	RO 0h	Reserved
27:16	RO 000h	**Next Receive Sequence Number (NRSN):** This is the sequence number associated with the TLP that is expected to be received next.
15:12	RO 0h	Reserved
11:0	RO FFFh	**Last Acknowledged Sequence Number (LASN):** This is the sequence number associated with the last acknowledged TLP.

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7 Direct Memory Interface (DMI) Registers

This Root Complex Register Block (RCRB) controls the (G)MCH-ICH8 serial interconnect. The base address of this space is programmed in DMIBAR in D0:F0 configuration space. Table 7-1 provides an address map of the DMI registers listed by address offset in ascending order.
Section 7.1 provides register bit descriptions.

Table 7-1. DMI Register Address Map

Address Offset	Symbol	Register Name	Default Value	Access
00–03h	DMIVCECH	DMI Virtual Channel Enhanced Capability	04010002h	RO
04–07h	DMIPVCCAP1	DMI Port VC Capability Register 1	00000001h	R/WO, RO
08–0Bh	DMIPVCCAP2	DMI Port VC Capability Register 2	00000000h	RO
0C–0Dh	DMIPVCCTL	DMI Port VC Control	0000h	RO, R/W
10–13h	DMIVC0RCAP	DMI VC0 Resource Capability	00000001h	RO
14–17h	DMIVC0RCTL0	DMI VC0 Resource Control	800000FFh	RO, R/W
1A–1Bh	DMIVC0RSTS	DMI VC0 Resource Status	0002h	RO
1C–1Fh	DMIVC1RCAP	DMI VC1 Resource Capability	00008001h	RO
20–23h	DMIVC1RCTL1	DMI VC1 Resource Control	01000000h	R/W, RO
26–27h	DMIVC1RSTS	DMI VC1 Resource Status	0002h	RO
84–87h	DMILCAP	DMI Link Capabilities	00012C41h	RO, R/WO
88–89h	DMILCTL	DMI Link Control	0000h	R/W, RO
8A–8Bh	DMILSTS	DMI Link Status	0001h	RO

7.1 Direct Memory Interface (DMI) Configuration Register Details

7.1.1 DMIVCECH—DMI Virtual Channel Enhanced Capability

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: 0–3h
Default Value: 04010002h
Access: RO
Size: 32 bits

This register indicates DMI Virtual Channel capabilities.

Bit	Access & Default	Description
31:20	RO 040h	**Pointer to Next Capability (PNC) :** This field contains the offset to the next PCI Express capability structure in the linked list of capabilities (Link Declaration Capability).
19:16	RO 1h	**PCI Express* Virtual Channel Capability Version (PCI EXPRESS*VCCV):** Hardwired to 1 to indicate compliances with the 1.1 version of the PCI Express specification.
15:0	RO 0002h	**Extended Capability ID (ECID):** Value of 0002h identifies this linked list item (capability structure) as being for PCI Express Virtual Channel registers.

7.1.2 DMIPVCCAP1—DMI Port VC Capability Register 1

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: 4–7h
Default Value: 00000001h
Access: R/WO, RO
Size: 32 bits

This register describes the configuration of PCI Express Virtual Channels associated with this port.

Bit	Access & Default	Description
31:7	RO 0000000h	Reserved
6:4	RO 000b	**Low Priority Extended VC Count (LPEVCC):** This field indicates the number of (extended) Virtual Channels in addition to the default VC belonging to the low-priority VC (LPVC) group that has the lowest priority with respect to other VC resources in a strict-priority VC Arbitration. The value of 0 in this field implies strict VC arbitration.
3	RO 0b	Reserved
2:0	R/WO 001b	**Extended VC Count (EVCC):** This field indicates the number of (extended) Virtual Channels in addition to the default VC supported by the device. The Private Virtual Channel is not included in this count.

7.1.3 DMIPVCCAP2—DMI Port VC Capability Register 2

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: 8–Bh
Default Value: 00000000h
Access: RO
Size: 32 bits

This register describes the configuration of PCI Express Virtual Channels associated with this port.

Bit	Access & Default	Description
31:0	RO 00000000h	Reserved

7.1.4 DMIPVCCTL—DMI Port VC Control

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: C–Dh
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

Bit	Access & Default	Description
15:4	RO 000h	Reserved
3:1	R/W 000b	**VC Arbitration Select (VCAS):** This field will be programmed by software to the only possible value as indicated in the VC Arbitration Capability field. See the PCI express specification for more details.
0	RO 0b	Reserved

7.1.5 DMIVC0RCAP—DMI VC0 Resource Capability

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: 10–13h
Default Value: 00000001h
Access: RO
Size: 32 bits

Bit	Access & Default	Description
31:16	RO 00000h	Reserved
15	RO 0b	**Reject Snoop Transactions (REJSNPT):** 0 = Transactions with or without the No Snoop bit set within the TLP header are allowed on this VC. 1 = Any transaction without the No Snoop bit set within the TLP header will be rejected as an Unsupported Request.
14:8	RO 00h	Reserved
7:0	RO 01h	**Port Arbitration Capability (PAC):** Having only bit 0 set indicates that the only supported arbitration scheme for this VC is non-configurable hardware-fixed.

7.1.6 DMIVC0RCTL0—DMI VC0 Resource Control

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: 14–17h
Default Value: 800000FFh
Access: RO, R/W
Size: 32 bits

This register controls the resources associated with PCI Express Virtual Channel 0.

Bit	Access & Default	Description
31	RO 1b	**Virtual Channel 0 Enable (VC0E):** For VC0, this bit is hardwired to 1 and read only as VC0 can never be disabled.
30:27	RO 0h	Reserved
26:24	RO 000b	**Virtual Channel 0 ID (VC0ID):** Assigns a VC ID to the VC resource. For VC0, this field is hardwired to 000 and read only.
23:20	RO 0h	Reserved
19:17	R/W 000b	**Port Arbitration Select (PAS):** This field configures the VC resource to provide a particular Port Arbitration service. Valid value for this field is a number corresponding to one of the asserted bits in the Port Arbitration Capability field of the VC resource. Because only bit 0 of that field is asserted. This field will always be programmed to 1.
16:8	RO 000h	Reserved
7:1	R/W 7Fh	**Traffic Class / Virtual Channel 0 Map (TCVC0M):** This field indicates the TCs (Traffic Classes) that are mapped to the VC resource. Bit locations within this field correspond to TC values. For example, when bit 7 is set in this field, TC7 is mapped to this VC resource. When more than one bit in this field is set, it indicates that multiple TCs are mapped to the VC resource. To remove one or more TCs from the TC/VC Map of an enabled VC, software must ensure that no new or outstanding transactions with the TC labels are targeted at the given Link.
0	RO 1b	**Traffic Class 0 / Virtual Channel 0 Map (TC0VC0M):** Traffic Class 0 is always routed to VC0.

7.1.7 DMIVC0RSTS—DMI VC0 Resource Status

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: 1A–1Bh
Default Value: 0002h
Access: RO
Size: 16 bits

This register reports the Virtual Channel specific status.

Bit	Access & Default	Description
15:2	RO 0000h	Reserved.
1	RO 1b	**Virtual Channel 0 Negotiation Pending (VC0NP):** This bit indicates the status of the process of Flow Control initialization. It is set by default on Reset, as well as whenever the corresponding Virtual Channel is Disabled or the Link is in the DL_Down state. It is cleared when the link successfully exits the FC_INIT2 state. 0 = The VC negotiation is complete. 1 = The VC resource is still in the process of negotiation (initialization or disabling). **BIOS Requirement:** Before using a Virtual Channel, software must check whether the VC Negotiation Pending fields for that Virtual Channel are cleared in both Components on a Link.
0	RO 0b	Reserved

7.1.8 DMIVC1RCAP—DMI VC1 Resource Capability

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: 1C–1Fh
Default Value: 00008001h
Access: RO
Size: 32 bits

Bit	Access & Default	Description
31:16	RO 00000h	Reserved
15	RO 1b	**Reject Snoop Transactions (REJSNPT):** 0 = Transactions with or without the No Snoop bit set within the TLP header are allowed on this VC. 1 = Any transaction without the No Snoop bit set within the TLP header will be rejected as an Unsupported Request.
14:8	RO 00h	Reserved
7:0	RO 01h	**Port Arbitration Capability (PAC):** Having only bit 0 set indicates that the only supported arbitration scheme for this VC is non-configurable hardware-fixed.

7.1.9 DMIVC1RCTL1—DMI VC1 Resource Control

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: 20–23h
Default Value: 01000000h
Access: R/W, RO
Size: 32 bits

Controls the resources associated with PCI Express Virtual Channel 1.

Bit	Access & Default	Description
31	R/W 0b	**Virtual Channel 1 Enable (VC1E):** 0 = Virtual Channel is disabled. 1 = Virtual Channel is enabled.
30:27	RO 0h	Reserved
26:24	R/W 001b	**Virtual Channel 1 ID (VC1ID):** This field assigns a VC ID to the VC resource. Assigned value must be non-zero. This field can not be modified when the VC is already enabled.
23:20	RO 0h	Reserved
19:17	R/W 000b	**Port Arbitration Select (PAS):** This field configures the VC resource to provide a particular Port Arbitration service. Valid value for this field is a number corresponding to one of the asserted bits in the Port Arbitration Capability field of the VC resource.
16:8	RO 000h	Reserved
7:1	R/W 00h	**Traffic Class / Virtual Channel 1 Map (TCVC1M):** This field indicates the TCs (Traffic Classes) that are mapped to the VC resource. Bit locations within this field correspond to TC values. For example, when bit 7 is set in this field, TC7 is mapped to this VC resource. When more than one bit in this field is set, it indicates that multiple TCs are mapped to the VC resource. In order to remove one or more TCs from the TC/VC Map of an enabled VC, software must ensure that no new or outstanding transactions with the TC labels are targeted at the given Link.
0	RO 0b	**Traffic Class 0 / Virtual Channel 1 Map (TC0VC1M):** Traffic Class 0 is always routed to VC0.

7.1.10 DMIVC1RSTS—DMI VC1 Resource Status

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: 26–27h
Default Value: 0002h
Access: RO
Size: 16 bits

This register reports the Virtual Channel specific status.

Bit	Access & Default	Description
15:2	RO 0000h	Reserved
1	RO 1b	**Virtual Channel 1 Negotiation Pending (VC1NP):** 0 = The VC negotiation is complete. 1 = The VC resource is still in the process of negotiation (initialization or disabling).
0	RO 0b	Reserved

7.1.11 DMILCAP—DMI Link Capabilities

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: 84–87h
Default Value: 00012C41h
Access: RO, R/WO
Size: 32 bits

This field indicates DMI specific capabilities.

Bit	Access & Default	Description
31:18	RO 0000h	Reserved
17:15	R/WO 010b	**L1 Exit Latency (L1SELAT):** This field indicates the length of time this Port requires to complete the transition from L1 to L0. 010 = 2 us to less than 4 us.
14:12	R/WO 010b	**L0s Exit Latency (L0SELAT):** This field indicates the length of time this Port requires to complete the transition from L0s to L0. 010 = 128 ns to less than 256 ns
11:10	RO 11b	**Active State Link PM Support (ASLPMS):** L0s and L1 entry supported.
9:4	RO 04h	**Max Link Width (MLW):** This field indicates the maximum number of lanes supported for this link.
3:0	RO 1h	**Max Link Speed (MLS):** Hardwired to indicate 2.5 Gb/s.

7.1.12 DMILCTL—DMI Link Control

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: 88–89h
Default Value: 0000h
Access: R/W, RO
Size: 16 bits

This register allows control of DMI.

Bit	Access & Default	Description
15:8	RO 00h	Reserved
7	R/W 0b	**Extended Synch (EXTSYNC):** 0 = Standard Fast Training Sequence (FTS). 1 = Forces the transmission of additional ordered sets when exiting the L0s state and when in the Recovery state.
6:3	RO 0h	Reserved
2	R/W 0b	**Far-End Digital Loopback (FEDLB):**
1:0	R/W 00b	**Active State Power Management Support (ASPMS):** This field controls the level of active state power management supported on the given link. 00 = Disabled 01 = L0s Entry Supported 10 = Reserved 11 = L0s and L1 Entry Supported

7.1.13 DMILSTS—DMI Link Status

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: 8A–8Bh
Default Value: 0001h
Access: RO
Size: 16 bits

This register indicates DMI status.

Bit	Access & Default	Description
15:10	RO 00h	Reserved and Zero for future R/WC/S implementations. Software must use 0 for writes to these bits.
9:4	RO 00h	**Negotiated Width (NWID):** This field indicates negotiated link width. This field is valid only when the link is in the L0, L0s, or L1 states (after link width negotiation is successfully completed). 04h = X4 All other encodings are reserved.
3:0	RO 1h	**Negotiated Speed (NSPD):** This field indicates negotiated link speed. 1h = 2.5 Gb/s All other encodings are reserved.

§

8 Integrated Graphics Device Registers (Device 2) (Intel® 82Q965/82Q963/82G965 Only)

The Integrated Graphics Device (IGD) registers are located in Device 2 (D0), Function 0 (F0) and Function 1 (F1). This chapter provides the descriptions for these registers. Section 8.1 provides the register descriptions for Device 2, Function 0. Section 8.2 provides the register descriptions for Device 2, Function 1.

8.1 IGD Configuration Register Details (Device 2, Function 0)

Device 2, Function 0 contains registers for the internal graphics functions. Table 8-1 lists the PCI configuration registers in order of ascending offset address.

Function 0 can be VGA compatible or not; this is selected through bit 1 of the GGC register (Device 0, offset 52h)

Table 8-1. Integrated Graphics Device Register Address Map (Device 2, Function 0)

Address Offset	Symbol	Register Name	Default Value	Access
00–01h	VID2	Vendor Identification	8086h	RO
02–03h	DID2	Device Identification	2982h	RO
04–05h	PCICMD2	PCI Command	0000h	RO, R/W
06–07h	PCISTS2	PCI Status	0090h	RO, R/WC
08h	RID2	Revision Identification	See register description	RO
09–0Bh	CC	Class Code	030000h	RO
0Ch	CLS	Cache Line Size	00h	RO
0Dh	MLT2	Master Latency Timer	00h	RO
0Eh	HDR2	Header Type	80h	RO
10–17h	GTTMMADR	Graphics Translation Table, Memory Mapped Range Address	0000000000000002h	RO, R/W
18–1Fh	GMADR	Graphics Memory Range Address	0000000000000000Ah	R/W/L, RO, R/W

Address Offset	Symbol	Register Name	Default Value	Access
20–23h	IOBAR	IO Base Address	00000001h	RO, R/W
2C–2Dh	SVID2	Subsystem Vendor Identification	0000h	R/WO
2E–2Fh	SID2	Subsystem Identification	0000h	R/WO
30–33h	ROMADR	Video BIOS ROM Base Address	00000000h	RO
34h	CAPPOINT	Capabilities Pointer	D0h	RO
3Ch	INTRLINE	Interrupt Line	00h	R/W
3Dh	INTRPIN	Interrupt Pin	01h	RO
3Eh	MINGNT	Minimum Grant	00h	RO
3Fh	MAXLAT	Maximum Latency	00h	RO
44h	MCAPPTR	Mirror of Device 0 Capabilities Pointer	E0h	RO
48–51h	CAPID0	Mirror of Device 0 Capability Identifier	0000000000 0001090009 h	RO
52–53h	MGGC	Mirror of Device 0 GMCH Graphics Control Register	0030h	RO
54–57h	DEVEN	Mirror of Device 0 Device Enable	000003DBh	RO, R/W/L
58–5Bh	SSRW	Software Scratch Read Write	00000000h	R/W
5C–5Fh	BSM	Base of Stolen Memory	07800000h	RO
90–91h	MSI_CAPID	Message Signaled Interrupts Capability ID	D005h	RO
92–93h	MC	Message Control	0000h	RO, R/W
94–97h	MA	Message Address	00000000h	R/W, RO
98–98h	MD	Message Data	0000h	R/W
D0–D1h	PMCAPID	Power Management Capabilities ID	0001h	RO
D2–D3h	PMCAP	Power Management Capabilities	0022h	RO
D4–D5h	PMCS	Power Management Control/Status	0000h	RO, R/W
E0–E0h	SWSMI	Software SMI	0000h	R/W

8.1.1 VID2—Vendor Identification

B/D/F/Type: 0/2/0/PCI
Address Offset: 0–1h
Default Value: 8086h
Access: RO
Size: 16 bits

This register combined with the Device Identification register uniquely identifies any PCI device.

Bit	Access & Default	Description
15:0	RO 8086h	**Vendor Identification Number (VID):** PCI standard identification for Intel.

8.1.2 DID2—Device Identification

B/D/F/Type: 0/2/0/PCI
Address Offset: 2–3h
Default Value: 2982h
Access: RO
Size: 16 bits

This register, combined with the Vendor Identification register, uniquely identifies any PCI device.

Bit	Access & Default	Description
15:0	RO 2982h	**Device Identification Number (DID):** This is a 16 bit value assigned to the GMCH Graphic device

8.1.3 PCICMD2—PCI Command

B/D/F/Type: 0/2/0/PCI
Address Offset: 4–5h
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

This 16-bit register provides basic control over the IGD's ability to respond to PCI cycles. The PCICMD Register in the IGD disables the IGD PCI compliant master accesses to main memory.

Bit	Access & Default	Description
15:11	RO 00h	Reserved
10	R/W 0b	**Interrupt Disable (INTDIS):** This bit disables the device from asserting INTx#. 0 = Enable the assertion of this device's INTx# signal. 1 = Disable the assertion of this device's INTx# signal. DO_INTx messages will not be sent to DMI.
9	RO 0b	**Fast Back-to-Back (FB2B):** Not Implemented. Hardwired to 0.
8	RO 0b	**SERR Enable (SERRE):** Not Implemented. Hardwired to 0.
7	RO 0b	**Address/Data Stepping Enable (ADSTEP):** Not Implemented. Hardwired to 0.
6	RO 0b	**Parity Error Enable (PERRE):** Not Implemented. Hardwired to 0. Since the IGD belongs to the category of devices that does not corrupt programs or data in system memory or hard drives, the IGD ignores any parity error that it detects and continues with normal operation.
5	RO 0b	**Video Palette Snooping (VPS):** This bit is hardwired to 0 to disable snooping.
4	RO 0b	**Memory Write and Invalidate Enable (MWIE):** Hardwired to 0. The IGD does not support memory write and invalidate commands.
3	RO 0b	**Special Cycle Enable (SCE):** This bit is hardwired to 0. The IGD ignores Special cycles.
2	R/W 0b	**Bus Master Enable (BME):** 0 = Disable IGD bus mastering. 1 = Enable the IGD to function as a PCI compliant master.
1	R/W 0b	**Memory Access Enable (MAE):** This bit controls the IGD's response to memory space accesses. 0 = Disable. 1 = Enable.
0	R/W 0b	**I/O Access Enable (IOAE):** This bit controls the IGD's response to I/O space accesses. 0 = Disable. 1 = Enable.

8.1.4 PCISTS2—PCI Status

B/D/F/Type: 0/2/0/PCI
Address Offset: 6–7h
Default Value: 0090h
Access: RO, R/WC
Size: 16 bits

PCISTS is a 16-bit status register that reports the occurrence of a PCI compliant master abort and PCI compliant target abort. PCISTS also indicates the DEVSEL# timing that has been set by the IGD.

Bit	Access & Default	Description
15	RO 0b	**Detected Parity Error (DPE):** Hardwired to 0. The IGD does not detect parity.
14	RO 0b	**Signaled System Error (SSE):** Hardwired to 0. The IGD never asserts SERR#.
13	RO 0b	**Received Master Abort Status (RMAS):** Hardwired to 0. The IGD never gets a master abort.
12	RO 0b	**Received Target Abort Status (RTAS):** Hardwired to 0. The IGD never gets a target abort.
11	RO 0b	**Signaled Target Abort Status (STAS):** Hardwired to 0. The IGD does not use target abort semantics.
10:9	RO 00b	**DEVSEL Timing (DEVT):** N/A. Hardwired to 00.
8	RO 0b	**Master Data Parity Error Detected (DPD):** Since Parity Error Response is hardwired to disabled (and the IGD does not do any parity detection), this bit is hardwired to 0.
7	RO 1b	**Fast Back-to-Back (FB2B):** Hardwired to 1. The IGD accepts fast back-to-back when the transactions are not to the same agent.
6	RO 0b	**User Defined Format (UDF):** Hardwired to 0.
5	RO 0b	**66 MHz PCI Capable (66C):** Hardwired to 0.
4	RO 1b	**Capability List (CLIST):** This bit is set to 1 to indicate that the register at 34h provides an offset into the function's PCI Configuration Space containing a pointer to the location of the first item in the list.
3	R/WC 0b	**Interrupt Status (INTSTS):** This bit reflects the state of the interrupt in the device. Only when the Interrupt Disable bit in the PCICMD2 register (offset 04h) is a 0 and this Interrupt Status bit is a 1, will the devices INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit. This bit is set by hardware; software must write a 1 to clear this bit.
2:0	RO 000b	Reserved

8.1.5 RID2—Revision Identification

B/D/F/Type: 0/2/0/PCI
Address Offset: 8h
Default Value: See table below
Access: RO
Size: 8 bits

This register contains the revision number for Device #2 Functions 0 and 1.

Bit	Access & Default	Description
7:0	RO 00h	**Revision Identification Number (RID):** This is an 8-bit value that indicates the revision identification number for the GMCH Device 0. Refer to the *Intel® 965 Express Chipset Family Specification Update* for the value of the Revision ID register.

8.1.6 CC—Class Code

B/D/F/Type: 0/2/0/PCI
Address Offset: 9–Bh
Default Value: 030000h
Access: RO
Size: 24 bits

This register contains the device programming interface information related to the Sub-Class Code and Base Class Code definition for the IGD. This register also contains the Base Class Code and the function sub-class in relation to the Base Class Code.

Bit	Access & Default	Description
23:16	RO 03h	**Base Class Code (BCC):** This is an 8-bit value that indicates the base class code for the GMCH. 03h = Display controller.
15:8	RO 00h	**Sub-Class Code (SUBCC):** Value will be determined based on Device 0 GGC register, GMS and IVD fields. 00h = VGA compatible 80h = Non VGA (GMS = "000" or IVD = "1")
7:0	RO 00h	**Programming Interface (PI):** 00h = Display controller.

8.1.7 CLS—Cache Line Size

B/D/F/Type: 0/2/0/PCI
Address Offset: Ch
Default Value: 00h
Access: RO
Size: 8 bits

The IGD does not support this register as a PCI slave.

Bit	Access & Default	Description
7:0	RO 00h	**Cache Line Size (CLS):** This field is hardwired to 0s. The IGD as a PCI compliant master does not use the Memory Write and Invalidate command and, in general, does not perform operations based on cache line size.

8.1.8 MLT2—Master Latency Timer

B/D/F/Type: 0/2/0/PCI
Address Offset: Dh
Default Value: 00h
Access: RO
Size: 8 bits

The IGD does not support the programmability of the master latency timer because it does not perform bursts.

Bit	Access & Default	Description
7:0	RO 00h	**Master Latency Timer Count Value (MLTCV):** Hardwired to 0s.

8.1.9 HDR2—Header Type

B/D/F/Type: 0/2/0/PCI
Address Offset: Eh
Default Value: 80h
Access: RO
Size: 8 bits

This register contains the Header Type of the IGD.

Bit	Access & Default	Description
7	RO 1b	**Multi Function Status (MFUNC):** This bit indicates if the device is a Multi-Function Device. The Value of this register is determined by DEVEN[4] (Device 0, offset 54h). If DEVEN[4] is set, the MFUNC bit is also set.
6:0	RO 00h	**Header Code (H):** This is a 7-bit value that indicates the Header Code for the IGD. This code has the value 00h, indicating a type 0 configuration space format.

8.1.10 GTTMMADR—Graphics Translation Table, Memory Mapped Range Address

B/D/F/Type: 0/2/0/PCI
Address Offset: 10–17h
Default Value: 0000000000000002h
Access: RO, R/W
Size: 64 bits

This register requests allocation for combined Graphics Translation Table (GTT) and memory-mapped range (1 MB combine for MMIO and Global GTT table aperture; one for 512 KB each)

The allocation is for 1024 KB and the base address is defined by bits [31:20].

Bit	Access & Default	Description
63:36	RO 0000000h	Reserved
35:20	R/W 0000h	**Memory Base Address (GTTMMADR_MBA):** Set by the OS, these bits correspond to address signals 35:20 (1 MB combine for MMIO and Global GTT table aperture; one for 512 KB each).
19:4	RO 0000h	Reserved: Hardwired to 0s to indicate at least 1MB address range.
3	RO 0b	**Prefetchable Memory (PREFMEM):** Hardwired to 0 to prevent prefetching.
2:1	RO 01b	**Memory Type (MEMTYP):** Memory Type (MEMTYP): 0 = 32-bit address. 1 = 64-bit address
0	RO 0b	**Memory / IO Space (MIOS):** Hardwired to 0 to indicate memory space.

8.1.11 GMADR—Graphics Memory Range Address

B/D/F/Type: 0/2/0/PCI
Address Offset: 18–1Fh
Default Value: 000000000000000Ah
Access: R/W/L, RO, R/W
Size: 64 bits

IGD graphics memory base address is specified in this register.

Bit	Access & Default	Description
63:36	RO 0000000h	Reserved
35:29	R/W 0000000b	**Memory Base Address (GMADR_MBA):** Set by the OS, these bits correspond to address signals 35:29.
28	R/W/L 0b	**512MB Address Mask (512ADMSK):** This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO), depending on the value of MSAC[1:0]. See MSAC (Device 2, Function 0, offset 66h) for details.
27	R/W/L 0b	**256 MB Address Mask (256ADMSK):** This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO), depending on the value of MSAC[1:0]. See MSAC (Device 2, Function 0, offset 66h) for details.
26:4	RO 000000h	**Address Mask (ADM):** Hardwired to 0s to indicate at least 128 MB address range.
3	RO 1b	**Prefetchable Memory (PREFMEM):** Hardwired to 1 to enable prefetching.
2:1	RO 01b	**Memory Type (MEMTYP):** 0 = 32-bit address. 1 = 64-bit address
0	RO 0b	**Memory/IO Space (MIOS):** Hardwired to 0 to indicate memory space.

8.1.12 IOBAR—IO Base Address

B/D/F/Type: 0/2/0/PCI
Address Offset: 20–23h
Default Value: 00000001h
Access: RO, R/W
Size: 32 bits

This register provides the Base offset of the I/O registers within Device 2. Bits 15:3 are programmable allowing the I/O Base to be located anywhere in 16-bit I/O address space. Bits 2:1 are fixed and return zero; bit 0 is hardwired to a one indicating that 8 bytes of I/O space are decoded.

Access to the 8Bs of I/O space is allowed in PM state D0 when IO Enable (PCICMD bit 0) set. Access is disallowed in PM states D1–D3 or if IO Enable is clear or if Device 2 is turned off or if Internal graphics is disabled thru the fuse or fuse override mechanisms. Note that access to this I/O BAR is independent of VGA functionality within Device 2. Also, note that this mechanism is available only through Function 0, Device 2 and is not duplicated in Function 1.

If accesses to this I/O bar is allowed, then the GMCH claims all 8, 16, or 32 bit I/O cycles from the processor that falls within the 8B claimed.

Bit	Access & Default	Description
31:16	RO 0000h	Reserved
15:3	R/W 0000h	**IO base Address (IOBASE): O Base Address:** Set by the OS, these bits correspond to address signals 15:3.
2:1	RO 00b	**Memory Type (MEMTYPE): Memory Type:** Hardwired to 0s to indicate 32-bit address.
0	RO 1b	**Memory/IO space type (SPCTYPE): Memory / IO Space:** Hardwired to 1 to indicate I/O space.

8.1.13 SVID2—Subsystem Vendor Identification

B/D/F/Type: 0/2/0/PCI
Address Offset: 2C–2Dh
Default Value: 0000h
Access: R/WO
Size: 16 bits

Bit	Access & Default	Description
15:0	R/WO 0000h	**Subsystem Vendor ID (SUBVID):** This value is used to identify the vendor of the subsystem. This register should be programmed by BIOS during boot-up. Once written, this register becomes Read_Only. This register can only be cleared by a Reset.

8.1.14 SID2—Subsystem Identification

B/D/F/Type: 0/2/0/PCI
Address Offset: 2E–2Fh
Default Value: 0000h
Access: R/WO
Size: 16 bits

Bit	Access & Default	Description
15:0	R/WO 0000h	**Subsystem Identification (SUBID):** This value is used to identify a particular subsystem. This field should be programmed by BIOS during boot-up. Once written, this register becomes read only. This register can only be cleared by a Reset.

8.1.15 ROMADR—Video BIOS ROM Base Address

B/D/F/Type: 0/2/0/PCI
Address Offset: 30–33h
Default Value: 00000000h
Access: RO
Size: 32 bits

The IGD does not use a separate BIOS ROM; therefore, this register is hardwired to 0s.

Bit	Access & Default	Description
31:18	RO 0000h	**ROM Base Address (RBA):** Hardwired to 0s.
17:11	RO 00h	Address Mask (ADMSK): Hardwired to 0s to indicate 256 KB address range.
10:1	RO 000h	Reserved: Hardwired to 0s.
0	RO 0b	**ROM BIOS Enable (RBE):** 0 = ROM not accessible.

8.1.16 CAPPOINT—Capabilities Pointer

B/D/F/Type: 0/2/0/PCI
Address Offset: 34h
Default Value: D0h
Access: RO
Size: 8 bits

Bit	Access & Default	Description
7:0	RO D0h	**Capabilities Pointer Value (CPV):** This field contains an offset into the function's PCI configuration space for the first item in the New Capabilities Linked List, the MSI Capabilities ID registers at address 90h, or the Power Management capability at D0h. This value is determined by the configuration in CAPL[0].

8.1.17 INTRLINE—Interrupt Line

B/D/F/Type: 0/2/0/PCI
Address Offset: 3Ch
Default Value: 00h
Access: R/W
Size: 8 bits

Bit	Access & Default	Description
7:0	R/W 00h	**Interrupt Connection (INTCON):** This field is used to communicate interrupt line routing information. POST software writes the routing information into this register as it initializes and configures the system. The value in this field indicates which input of the system interrupt controller the device's interrupt pin is connected.

8.1.18 INTRPIN—Interrupt Pin

B/D/F/Type: 0/2/0/PCI
Address Offset: 3Dh
Default Value: 01h
Access: RO
Size: 8 bits

Bit	Access & Default	Description
7:0	RO 01h	**Interrupt Pin (INTPIN):** As a single function device, the IGD specifies INTA# as its interrupt pin. 01h = INTA#.

8.1.19 MINGNT—Minimum Grant

B/D/F/Type: 0/2/0/PCI
Address Offset: 3Eh
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access & Default	Description
7:0	RO 00h	**Minimum Grant Value (MGV):** The IGD does not burst as a PCI compliant master.

8.1.20 MAXLAT—Maximum Latency

B/D/F/Type: 0/2/0/PCI
Address Offset: 3Fh
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access & Default	Description
7:0	RO 00h	**Maximum Latency Value (MLV):** The IGD has no specific requirements for how often it needs to access the PCI bus.

8.1.21 MCAPPTR—Mirror of Device 0 Capabilities Pointer

B/D/F/Type: 0/2/0/PCI
Address Offset: 44h
Default Value: E0h
Access: RO
Size: 8 bits

The CAPPTR provides the offset that is the pointer to the location of the first device capability in the capability list.

Bit	Access & Default	Description
7:0	RO E0h	**Mirror of CAPPTR (MCAPPTR):** Pointer to the offset of the first capability ID register block. In this case the first capability is the product-specific Capability Identifier (CAPID0).

8.1.22 CAPID0—Mirror of Device 0 Capability Identifier

B/D/F/Type: 0/2/0/PCI
Address Offset: 48–51h
Default Value: 00000000000001090009h
Access: RO
Size: 80 bits

Bit	Access & Default	Description
79:26	RO 0000000000 0000h	Reserved
27:24	RO 1h	**CAPID Version (CAPIDV):** This field has the value 0001b to identify the first revision of the CAPID register definition.
23:16	RO 09h	**CAPID Length (CAPIDL):** This field has the value 09h to indicate the structure length (9 bytes).
15:8	RO 00h	**Next Capability Pointer (NCP):** This field is hardwired to 00h indicating the end of the capabilities linked list.
7:0	RO 09h	**Capability Identifier (CAP_ID):** This field has the value 1001b to identify the CAP_ID assigned by the PCI SIG for vendor dependent capability pointers.

8.1.23 MGGC—Mirror of Device 0 GMCH Graphics Control Register

B/D/F/Type: 0/2/0/PCI
Address Offset: 52–53h
Default Value: 0030h
Access: RO
Size: 16 bits

Bit	Access & Default	Description
15:7	RO 000h	Reserved
6:4	RO 011b	**Graphics Mode Select (GMS):** This field is used to select the amount of system memory that is pre-allocated to support the Internal Graphics device in VGA (non-linear) and Native (linear) modes. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled. 000 = No memory pre-allocated. Device 2 (IGD) does not claim VGA cycles (Memory and I/O), and the Sub-Class Code field within Device 2, Function 0 Class Code register is 80h. 001 = DVMT (UMA) mode, 1 MB of memory pre-allocated for frame buffer. 010 = Reserved 011 = DVMT (UMA) mode, 8 MB of memory pre-allocated for frame buffer. 100 = Reserved 101 = Reserved 110 = Reserved 111 = Reserved **NOTE:** This register is locked and becomes read only when the D_LCK bit in the SMRAM register is set.
3:2	RO 00b	Reserved
1	RO 0b	**IGD VGA Disable (IVD):** 0 = Enable. Device 2 (IGD) claims VGA memory and I/O cycles; the Sub-Class Code within Device 2 Class Code register is 00. 1 = Disable. Device 2 (IGD) does not claim VGA cycles (memory and I/O), and the Sub-Class Code field within Device 2 function 0 Class Code register is 80h.
0	RO 0b	Reserved

8.1.24 DEVEN—Mirror of Device 0 Device Enable

B/D/F/Type: 0/2/0/PCI
Address Offset: 54–57h
Default Value: 000003DBh
Access: RO
Size: 32 bits

This register allows enabling/disabling of PCI devices and functions that are in the GMCH. The following table bit definitions describes the behavior of all combinations of transactions to devices controlled by this register.

Bit	Access & Default	Description
31:10	RO 0s	Reserved
9	RO 1b	**ME Function 3 (D3F3EN):** If Device 3, Function 0 is disabled and hidden, then Device 3, Function 3 is also disabled and hidden, independent of the state of this bit. 0 = Bus 0, Device 3, Function 3 is disabled and hidden 1 = Bus 0, Device 3, Function 3 is enabled and visible.
8	RO 1b	**ME Function 2 (D3F2EN):** If Device 3, Function 0 is disabled and hidden, then Device 3, Function 2 is also disabled and hidden, independent of the state of this bit. 0 = Bus 0, Device 3, Function 2 is disabled and hidden 1 = Bus 0, Device 3, Function 2 is enabled and visible.
7	RO 1b	Reserved
6	RO 1b	**ME Function 0 (D3F0EN):** If the GMCH does not have ME capability, then Device 3, Function 0 is disabled and hidden, independent of the state of this bit. 0 = Bus 0, Device 3, Function 0 is disabled and hidden 1 = us 0, Device 3, Function 0 is enabled and visible.
5	RO 0b	Reserved
4	RO 1b	**Internal Graphics Engine Function 1 (D2F1EN):** If Device 2, Function 0, is disabled and hidden, then Device 2, Function 1 is also disabled and hidden, independent of the state of this bit. 0 = Bus 0, Device 2, Function 1 is disabled and hidden 1 = Bus 0, Device 2, Function 1 is enabled and visible
3	RO 1b	**Internal Graphics Engine Function 0 (D2F0EN):** 0 = Bus 0, Device 2, Function 0 is disabled and hidden 1 = Bus 0, Device 2, Function 0 is enabled and visible
2	RO 0b	Reserved

Bit	Access & Default	Description
1	RO 1b	**82Q965, 82G965, GMCH** **PCI Express Port (D1EN):** 0 = Bus 0, Device 1, Function 0 is disabled and hidden. 1 = Bus 0, Device 1, Function 0 is enabled and visible. **82Q963 GMCH** Reserved
0	RO 1b	**Host Bridge (D0EN):** Hardwired to 1. Bus 0, Device 0, Function 0 can not be disabled.

8.1.25 SSRW—Software Scratch Read Write

B/D/F/Type: 0/2/0/PCI
Address Offset: 58–5Bh
Default Value: 00000000h
Access: R/W
Size: 32 bits

Bit	Access & Default	Description
31:0	R/W 00000000h	Reserved

8.1.26 BSM—Base of Stolen Memory

B/D/F/Type: 0/2/0/PCI
Address Offset: 5C–5Fh
Default Value: 07800000h
Access: RO
Size: 32 bits

Graphics stolen memory and TSEG are within DRAM space defined under TOLUD. From the top of low used DRAM, GMCH claims 1 to 64 MB of DRAM for internal graphics, if enabled.

The base of stolen memory will always be below 4 GB. This is required to prevent aliasing between stolen range and the reclaim region.

Bit	Access & Default	Description
31:20	RO 078h	**Base of Stolen Memory (BSM):** This register contains bits 31:20 of the base address of stolen DRAM memory. The host interface determines the base of graphics stolen memory by subtracting the graphics stolen memory size from TOLUD. See Device 0 TOLUD for more explanation.
19:0	RO 00000h	Reserved

8.1.27 HSRW—Hardware Scratch Read Write

B/D/F/Type: 0/2/0/PCI
Address Offset: 60–61h
Default Value: 0000h
Access: R/W
Size: 16 bits

Bit	Access & Default	Description
15:0	R/W 0000h	Reserved

8.1.28 MSI_CAPID—Message Signaled Interrupts Capability ID

B/D/F/Type: 0/2/0/PCI
Address Offset: 90–91h
Default Value: D005h
Access: RO
Size: 16 bits

When a device supports MSI, it can generate an interrupt request to the processor by writing a predefined data item (a message) to a predefined memory address. The reporting of the existence of this capability can be disabled by setting MSICH (CAPL[0] @ 7Fh). In that case walking this linked list will skip this capability and instead go directly to the PCI PM capability.

Bit	Access & Default	Description
15:8	RO D0h	**Pointer to Next Capability (POINTNEXT):** This contains a pointer to the next item in the capabilities list which is the Power Management capability.
7:0	RO 05h	**Capability ID (CAPID):** Value of 05h identifies this linked list item (capability structure) as being for MSI registers.

8.1.29 MC—Message Control

B/D/F/Type: 0/2/0/PCI
Address Offset: 92–93h
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

System software can modify bits in this register, but the device is prohibited from doing so. If the device writes the same message multiple times, only one of those messages is assured to be serviced. If all of the messages must be serviced, the device must not generate the same message again until the driver services the earlier one.

Bit	Access & Default	Description
15:8	RO 00h	Reserved
7	RO 0b	**64 Bit Capable (64BCAP):** Hardwired to 0 to indicate that the function does not implement the upper 32 bits of the Message Address register and is incapable of generating a 64-bit memory address.
6:4	R/W 000b	**Multiple Message Enable (MME):** System software programs this field to indicate the actual number of messages allocated to this device. This number will be equal to or less than the number actually requested. The encoding is the same as for the MMC field below.
3:1	RO 000b	**Multiple Message Capable (MMC):** System Software reads this field to determine the number of messages being requested by this device. 000 = 1 request
0	R/W 0b	**MSI Enable (MSIEN):** This bit controls the ability of this device to generate MSIs. 0 = Disable 1 = Enable

8.1.30 MA—Message Address

B/D/F/Type: 0/2/0/PCI
Address Offset: 94–97h
Default Value: 00000000h
Access: R/W, RO
Size: 32 bits

Bit	Access & Default	Description
31:2	R/W 00000000h	**Message Address (MESSADD):** This field is used by system software to assign an MSI address to the device. The device handles a MSI by writing the padded contents of the MD register to this address.
1:0	RO 00b	**Force DWord Align (FDWORD):** Hardwired to 0s so that addresses assigned by system software are always aligned on a DWord address boundary.

8.1.31 MD—Message Data

B/D/F/Type: 0/2/0/PCI
Address Offset: 98–99h
Default Value: 0000h
Access: R/W
Size: 16 bits

Bit	Access & Default	Description
15:0	R/W 0000h	**Message Data (MESSDATA):** This field indicates the Base message data pattern assigned by system software and used to handle an MSI from the device. When the device must generate an interrupt request, it writes a 32-bit value to the memory address specified in the MA register. The upper 16 bits are always set to 0. The lower 16 bits are supplied by this register.

8.1.32 GDRST—Graphics Reset

B/D/F/Type: 0/2/0/PCI
Address Offset: C0h
Default Value: 00h
Access: RO, R/W/L
Size: 8 bits

Bit	Access & Default	Description
7:2	RO 000h	Reserved
1	RO 0b	**Graphics Reset Status (GRS):** This bit is set to 1 when Graphics Reset bit (bit 0 of this register) is set to a 1, and the graphics hardware has completed the debug reset sequence, and all graphics assets are in reset. This bit is cleared when Graphics Reset bit is set to a 0. 0 = Graphics subsystem not in Reset. 1 = Graphics Subsystem in Reset as a result of Graphics Reset.
0	R/W/L 0b	**Graphics Reset (GDR):** 1 = Assert display and render domain reset 0 = De-assert display and render domain reset Render and Display clock domain resets should be asserted for at least 20 us. Once this bit is set to a 1: • All GFX core MMIO registers are returned to power on default state. • All Ring buffer pointers are reset. • Command stream fetches are dropped. • Ongoing render pipeline processing is halted. • State machines and State Variables returned to power on default state. • Display and overlay engines are halted (garbage on screen). • VGA memory is not available. • Store DWords and interrupts are not assured to be completed. • Device 2 IO registers are not available. Device 2 Configuration registers continue to be available while Graphics debug reset is asserted.

8.1.33 PMCAPID—Power Management Capabilities ID

B/D/F/Type: 0/2/0/PCI
Address Offset: D0–D1h
Default Value: 0001h
Access: RO
Size: 16 bits

Bit	Access & Default	Description
15:8	RO 00h	**Next Capability Pointer (NEXT_PTR):** This field contains a pointer to next item in capabilities list. This is the final capability in the list and must be set to 00h.
7:0	RO 01h	**Capability Identifier (CAP_ID):** SIG defines this ID is 01h for power management.

8.1.34 PMCAP—Power Management Capabilities

B/D/F/Type: 0/2/0/PCI
Address Offset: D2–D3h
Default Value: 0022h
Access: RO
Size: 16 bits

Bit	Access & Default	Description
15:11	RO 00h	**PME Support (PMES):** This field indicates the power states in which the IGD may assert PME#. Hardwired to 0 to indicate that the IGD does not assert the PME# signal.
10	RO 0b	**D2 Support (D2):** Hardwired to 0. The D2 power management state is not supported.
9	RO 0b	**D1 Support (D1):** Hardwired to 0 to indicate that the D1 power management state is not supported.
8:6	RO 000b	Reserved
5	RO 1b	**Device Specific Initialization (DSI):** Hardwired to 1 to indicate that special initialization of the IGD is required before generic class device driver is to use it.
4	RO 0b	Reserved
3	RO 0b	**PME Clock (PMECLK):** Hardwired to 0 to indicate IGD does not support PME# generation.
2:0	RO 010b	**Version (VER):** Hardwired to 010b to indicate that there are 4 bytes of power management registers implemented and that this device complies with revision 1.1 of the PCI Power Management Interface Specification.

8.1.35 PMCS—Power Management Control/Status

B/D/F/Type: 0/2/0/PCI
Address Offset: D4–D5h
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

Bit	Access & Default	Description
15	RO 0b	**PME Status (PMESTS):** This bit is 0 to indicate that IGD does not support PME# generation from D3 (cold).
14:13	RO 00b	**Data Scale (DSCALE):** The IGD does not support data register. This bit always returns 00 when read, write operations have no effect.
12:9	RO 0h	**Data Select (DSEL):** The IGD does not support data register. This bit always returns 0h when read, write operations have no effect.
8	RO 0b	**PME Enable (PME_EN):** This bit is 0 to indicate that PME# assertion from D3 (cold) is disabled.
7:2	RO 00h	Reserved
1:0	R/W 00b	**Power State (PWRSTAT):** This field indicates the current power state of the IGD and can be used to set the IGD into a new power state. If software attempts to write an unsupported state to this field, write operation must complete normally on the bus, but the data is discarded and no state change occurs. On a transition from D3-to-D0 the graphics controller is optionally reset to initial values 00 = D0 (Default) 01 = D1 (Not Supported) 10 = D2 (Not Supported) 11= D3

8.1.36 SWSMI—Software SMI

B/D/F/Type: 0/2/0/PCI
Address Offset: E0–E1h
Default Value: 0000h
Access: R/W
Size: 16 bits

As long as there is the potential that DVO port legacy drivers exist in the system that expect this register at this address, Device 2, Function 0address E0h–E1h must be reserved for this register.

Bit	Access & Default	Description
15:8	R/W 00h	**Software Scratch Bits (SWSB):**
7:1	R/W 00h	**Software Flag (SWF):** This field is used to indicate caller and SMI function desired, as well as return result.
0	R/W 0b	**GMCH Software SMI Event (GSSMIE):** When set, this bit triggers an SMI. Software must write a 0 to clear this bit.

8.2 IGD Configuration Register Details (Device 2, Function 1)

The Integrated Graphics Device registers are located in Device 2 (D2), Function 0 (F0) and Function 1 (F1). This section provides the descriptions for the D2:F1 registers. Table 8-2 provides an address map of the D2:F1registers listed in ascending order by address offset. Detailed bit descriptions follow the table.

Table 8-2. Integrated Graphics Device Register Address Map (Device 2, Function 1)

Address Offset	Symbol	Register Name	Default Value	Access
00–01h	VID2	Vendor Identification	8086h	RO
02–03h	DID2	Device Identification	2983h	RO
04–05h	PCICMD2	PCI Command	0000h	RO, R/W
06–07h	PCISTS2	PCI Status	0090h	RO
0808h	RID2	Revision Identification	See register description	RO
09–0Bh	CC	Class Code Register	038000h	RO
0Ch	CLS	Cache Line Size	00h	RO
0Dh	MLT2	Master Latency Timer	00h	RO
0E	HDR2	Header Type	80h	RO
1017–h	MMADR	Memory Mapped Range Address	000000000 0000002h	R/W, RO
2C–2Dh	SVID2	Subsystem Vendor Identification	0000h	R/WO
2E–2Fh	SID2	Subsystem Identification	0000h	R/WO
30–33h	ROMADR	Video BIOS ROM Base Address	00000000h	RO
34–34h	CAPPOINT	Capabilities Pointer	D0h	RO
3Eh	MINGNT	Minimum Grant	00h	RO
3Fh	MAXLAT	Maximum Latency	00h	RO
44h	MCAPPTR	Mirror of Device 0 Capabilities Pointer	E0h	RO
48–51h	CAPID0	Capability Identifier	000000000 000010900 09h	RO
52–53h	MGGC	Mirror of Device 0 GMCH Graphics Control Register	0030h	RO
54–57h	DEVEN	Device Enable	000003DBh	RO
58–5Bh	SSRW	Mirror Function 0 Software Scratch Read Write	00000000h	RO

Address Offset	Symbol	Register Name	Default Value	Access
5C–5Fh	BSM	Mirror of Function 0 Base of Stolen Memory	07800000h	RO
C0h	GDRST	Mirror of Device 2 Func0 Graphics Reset	00h	RO
D0–D1h	PMCAPID	Mirror Function 0 Power Management Capabilities ID	0001h	RO
D2–D3h	PMCAP	Mirror Function 0 Power Management Capabilities	0022h	RO
D4–D5h	PMCS	Power Management Control/Status	0000h	RO, R/W
E0–E1h	SWSMI	Software SMI	0000h	R/W

8.2.1 VID2—Vendor Identification

B/D/F/Type: 0/2/1/PCI
Address Offset: 0–1h
Default Value: 8086h
Access: RO
Size: 16 bits

This register, combined with the Device Identification register, uniquely identifies any PCI device.

Bit	Access & Default	Description
15:0	RO 8086h	**Vendor Identification Number (VID):** PCI standard identification for Intel.

8.2.2 DID2—Device Identification

B/D/F/Type: 0/2/1/PCI
Address Offset: 2–3h
Default Value: 2983h
Access: RO
Size: 16 bits

This register is unique in Function 1 (the Function 0 DID is separate). This difference in Device ID is necessary for allowing distinct Plug and Play enumeration of Function 1 when both Function 0 and Function 1 have the same class code.

Bit	Access & Default	Description
15:0	RO 2983h	**Device Identification Number (DID):** This is a 16 bit value assigned to the GMCH Graphic device Function 1

8.2.3 PCICMD2—PCI Command

B/D/F/Type: 0/2/1/PCI
Address Offset: 4–5h
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

This 16-bit register provides basic control over the IGD's ability to respond to PCI cycles. The PCICMD Register in the IGD disables the IGD PCI compliant master accesses to main memory.

Bit	Access & Default	Description
15:10	RO 00h	Reserved
9	RO 0b	**Fast Back-to-Back (FB2B):** Not Implemented. Hardwired to 0.
8	RO 0b	**SERR Enable (SERRE):** Not Implemented. Hardwired to 0.
7	RO 0b	**Address/Data Stepping Enable (ADSTEP):** Not Implemented. Hardwired to 0.
6	RO 0b	**Parity Error Enable (PERRE):** Not Implemented. Hardwired to 0. Since the IGD belongs to the category of devices that does not corrupt programs or data in system memory or hard drives, the IGD ignores any parity error that it detects and continues with normal operation.
5	RO 0b	**VGA Palette Snoop Enable (VGASNOOP):** Hardwired to 0 to disable snooping.
4	RO 0b	**Memory Write and Invalidate Enable (MWIE):** Hardwired to 0. The IGD does not support memory write and invalidate commands.
3	RO 0b	**Special Cycle Enable (SCE):** Hardwired to 0. The IGD ignores Special cycles.
2	R/W 0b	**Bus Master Enable (BME):** 0 = Disable IGD bus mastering. 1 = Enable the IGD to function as a PCI compliant master.
1	R/W 0b	**Memory Access Enable (MAE):** This bit controls the IGD's response to memory space accesses. 0 = Disable. 1 = Enable.
0	R/W 0b	**I/O Access Enable (IOAE):** This bit controls the IGD's response to I/O space accesses. 0 = Disable. 1 = Enable.

8.2.4 PCISTS2—PCI Status

B/D/F/Type: 0/2/1/PCI
Address Offset: 6–7h
Default Value: 0090h
Access: RO
Size: 16 bits

PCISTS is a 16-bit status register that reports the occurrence of a PCI compliant master abort and PCI compliant target abort. PCISTS also indicates the DEVSEL# timing that has been set by the IGD.

Bit	Access & Default	Description
15	RO 0b	**Detected Parity Error (DPE):** Hardwired to 0. IGD does not detect parity.
14	RO 0b	**Signaled System Error (SSE):** Hardwired to 0. IGD never asserts SERR#.
13	RO 0b	**Received Master Abort Status (RMAS):** Hardwired to 0. IGD never gets a master abort.
12	RO 0b	**Received Target Abort Status (RTAS):** Hardwired to 0. IGD never gets a target abort.
11	RO 0b	**Signaled Target Abort Status (STAS):** Hardwired to 0. IGD does not use target abort semantics.
10:9	RO 00b	**DEVSEL Timing (DEVT):** N/A. These bits are hardwired to 00.
8	RO 0b	**Master Data Parity Error Detected (DPD):** Hardwired to 0. Parity Error Response is hardwired to disabled (and the IGD does not do any parity detection).
7	RO 1b	**Fast Back-to-Back (FB2B):** Hardwired to 1. IGD accepts fast back-to-back when the transactions are not to the same agent.
6	RO 0b	**User Defined Format (UDF):** Hardwired to 0.
5	RO 0b	**66 MHz PCI Capable (66C):** N/A – Hardwired to 0.
4	RO 1b	**Capability List (CLIST):** This bit is set to 1 to indicate that the register at 34h provides an offset into the function's PCI Configuration Space containing a pointer to the location of the first item in the list.
3	RO 0b	**Interrupt Status (INTSTS):** Hardwired to 0.
2:0	RO 000b	Reserved

8.2.5 RID2—Revision Identification

B/D/F/Type: 0/2/1/PCI
Address Offset: 8h
Default Value: See table below
Access: RO
Size: 8 bits

This register contains the revision number for Device 2, Functions 0 and 1.

Bit	Access & Default	Description
7:0	RO 00h	**Revision Identification Number (RID):** This is an 8-bit value that indicates the revision identification number for the GMCH Device 0. Refer to the *Intel® 965 Express Chipset Family Specification Update* for the value of the Revision ID register.

8.2.6 CC—Class Code Register

B/D/F/Type: 0/2/1/PCI
Address Offset: 9–Bh
Default Value: 038000h
Access: RO
Size: 24 bits

This register contains the device programming interface information related to the Sub-Class Code and Base Class Code definition for the IGD. This register also contains the Base Class Code and the function sub-class in relation to the Base Class Code.

Bit	Access & Default	Description
23:16	RO 03h	**Base Class Code (BCC):** This is an 8-bit value that indicates the base class code for the GMCH. 03h = Display controller.
15:8	RO 80h	**Sub-Class Code (SUBCC):** 80h = Non VGA
7:0	RO 00h	**Programming Interface (PI):** 00h = Display controller.

8.2.7 CLS—Cache Line Size

B/D/F/Type: 0/2/1/PCI
Address Offset: Ch
Default Value: 00h
Access: RO
Size: 8 bits

The IGD does not support this register as a PCI slave.

Bit	Access & Default	Description
7:0	RO 00h	**Cache Line Size (CLS):** This field is hardwired to 0s. The IGD as a PCI compliant master does not use the Memory Write and Invalidate command and, in general, does not perform operations based on cache line size.

8.2.8 MLT2—Master Latency Timer

B/D/F/Type: 0/2/1/PCI
Address Offset: Dh
Default Value: 00h
Access: RO
Size: 8 bits

The IGD does not support the programmability of the master latency timer because it does not perform bursts.

Bit	Access & Default	Description
7:0	RO 00h	**Master Latency Timer Count Value (MLTCV):** Hardwired to 0s.

8.2.9 HDR2—Header Type

B/D/F/Type: 0/2/1/PCI
Address Offset: Eh
Default Value: 80h
Access: RO
Size: 8 bits

This register contains the Header Type of the IGD.

Bit	Access & Default	Description
7	RO 1b	**Multi Function Status (MFUNC):** This field indicates if the device is a Multi-Function Device. The Value of this register is determined by Device 0, offset 54h, DEVEN[4]. If Device 0 DEVEN[4] is set, the MFUNC bit is also set.
6:0	RO 00h	**Header Code (H):** This is a 7-bit value that indicates the Header Code for the IGD. This code has the value 00h, indicating a type 0 configuration space format.

8.2.10 MMADR—Memory Mapped Range Address

B/D/F/Type: 0/2/1/PCI
Address Offset: 10–17h
Default Value: 0000000000000002h
Access: R/W, RO
Size: 64 bits

This register requests allocation for the IGD registers and instruction ports. The allocation is for 512 KB and the base address is defined by bits 31:19.

Bit	Access & Default	Description
63:36	RO 0000000h	Reserved
35:20	R/W 0000h	**Memory Base Address (MMADR_MBA):** Set by the OS, these bits correspond to address signals 31:19.
19:4	RO 0000h	**Address Mask (ADMSK):** Hardwired to 0s to indicate 512 KB address range.
3	RO 0b	**Prefetchable Memory (PREFMEM):** Hardwired to 0 to prevent prefetching.
2:1	RO 01b	**Memory Type (MEMTYP):** Hardwired to 01 to indicate 64-bit address.
0	RO 0b	**Memory / IO Space (MIOS):** Hardwired to 0 to indicate memory space.

8.2.11 SVID2—Subsystem Vendor Identification

B/D/F/Type: 0/2/1/PCI
Address Offset: 2C–2Dh
Default Value: 0000h
Access: R/WO
Size: 16 bits

Bit	Access & Default	Description
15:0	R/WO 0000h	**Subsystem Vendor ID (SUBVID):** This value is used to identify the vendor of the subsystem. This register should be programmed by BIOS during boot-up. Once written, this register becomes read only. This register can only be cleared by a Reset.

8.2.12 SID2—Subsystem Identification

B/D/F/Type: 0/2/1/PCI
Address Offset: 2E–2Fh
Default Value: 0000h
Access: R/WO
Size: 16 bits

Bit	Access & Default	Description
15:0	R/WO 0000h	**Subsystem Identification (SUBID):** This value is used to identify a particular subsystem. This field should be programmed by BIOS during boot-up. Once written, this register becomes read only. This register can only be cleared by a Reset.

8.2.13 ROMADR—Video BIOS ROM Base Address

B/D/F/Type: 0/2/1/PCI
Address Offset: 30–33h
Default Value: 00000000h
Access: RO
Size: 32 bits

The IGD does not use a separate BIOS ROM; therefore this register is hardwired to 0s.

Bit	Access & Default	Description
31:18	RO 0000h	**ROM Base Address (RBA):** Hardwired to 0s.
17:11	RO 00h	**Address Mask (ADMSK):** Hardwired to 0s to indicate 256 KB address range.
10:1	RO 000h	Reserved: Hardwired to 0s.
0	RO 0b	**ROM BIOS Enable (RBE):** 0 = ROM not accessible.

8.2.14 CAPPOINT—Capabilities Pointer

B/D/F/Type: 0/2/1/PCI
Address Offset: 34h
Default Value: D0h
Access: RO
Size: 8 bits

Bit	Access & Default	Description
7:0	RO D0h	**Capabilities Pointer Value (CPV):** This field contains an offset into the function's PCI configuration space for the first item in the New Capabilities Linked List, the MSI Capabilities ID registers at address 90h or the Power Management capability at D0h. This value is determined by the configuration in CAPL[0].

8.2.15 MINGNT—Minimum Grant

B/D/F/Type: 0/2/1/PCI
Address Offset: 3Eh
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access & Default	Description
7:0	RO 00h	**Minimum Grant Value (MGV):** The IGD does not burst as a PCI compliant master.

8.2.16 MAXLAT—Maximum Latency

B/D/F/Type: 0/2/1/PCI
Address Offset: 3Fh
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access & Default	Description
7:0	RO 00h	**Maximum Latency Value (MLV):** The IGD has no specific requirements for how often it needs to access the PCI bus.

8.2.17 MCAPPTR—Mirror of Device 0 Capabilities Pointer

B/D/F/Type: 0/2/1/PCI
Address Offset: 44h
Default Value: E0h
Access: RO
Size: 8 bits

The CAPPTR provides the offset that is the pointer to the location of the first device capability in the capability list.

Bit	Access & Default	Description
7:0	RO E0h	**Mirror of CAPPTR (MCAPPTR):** Pointer to the offset of the first capability ID register block. In this case the first capability is the product-specific Capability Identifier (CAPID0).

8.2.18 CAPID0—Capability Identifier

B/D/F/Type: 0/2/1/PCI
Address Offset: 48–51h
Default Value: 00000000000001090009h
Access: RO
Size: 80 bits

Bit	Access & Default	Description
79:26	RO 0000000000 0000h	Reserved
27:24	RO 1h	**CAPID Version (CAPIDV):** This field has the value 0001b to identify the first revision of the CAPID register definition.
23:16	RO 09h	**CAPID Length (CAPIDL):** This field has the value 09h to indicate the structure length (9 bytes).
15:8	RO 00h	**Next Capability Pointer (NCP):** This field is hardwired to 00h indicating the end of the capabilities linked list.
7:0	RO 09h	**Capability Identifier (CAP_ID):** This field has the value 1001b to identify the CAP_ID assigned by the PCI SIG for vendor dependent capability pointers.

8.2.19 MGGC—Mirror of Device 0 GMCH Graphics Control Register

B/D/F/Type: 0/2/1/PCI
Address Offset: 52–53h
Default Value: 0030h
Access: RO
Size: 16 bits

Bit	Access & Default	Description
15:7	RO 000h	Reserved
6:4	RO 011b	**Graphics Mode Select (GMS):** This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics device in VGA (non-linear) and Native (linear) modes. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled. 000 No memory pre-allocated. Device 2 (IGD) does not claim VGA cycles (memory and I/O), and the Sub-Class Code field within Device 2 function 0 Class Code register is 80. 001 = DVMT (UMA) mode, 1 MB of memory pre-allocated for frame buffer. 010 = Reserved 011 = DVMT (UMA) mode, 8 MB of memory pre-allocated for frame buffer. 100 = Reserved 101 = Reserved 110 = Reserved 111 = Reserved **Note:** This register is locked and becomes Read Only when the D_LCK bit in the SMRAM register is set.
3:2	RO 00b	Reserved
1	RO 0b	**IGD VGA Disable (IVD):** 0 = Enable. Device 2 (IGD) claims VGA memory and IO cycles, the Sub-Class Code within Device 2 Class Code register is 00. 1 = Disable. Device 2 (IGD) does not claim VGA cycles (memory and IO), and the Sub- Class Code field within Device 2 function 0 Class Code register is 80h.
0	RO 0b	Reserved

8.2.20 DEVEN—Device Enable

B/D/F/Type: 0/2/1/PCI
Address Offset: 54–57h
Default Value: 000003DBh
Access: RO
Size: 32 bits

This register allows enabling/disabling of PCI devices and functions that are within the GMCH. The following table bit definitions describes the behavior of all combinations of transactions to devices controlled by this register.

Bit	Access & Default	Description
31:10	RO 000000000h	Reserved
9	RO 1b	**ME Function 3 (D3F3EN):** If Device 3, Function 0 is disabled and hidden, then Device 3, Function 3 is also disabled and hidden independent of the state of this bit. 0 = Bus 0, Device 3, Function 3 is disabled and hidden 1 = Bus 0, Device 3, Function 3 is enabled and visible
8	RO 1b	**ME Function 2 (D3F2EN):** If Device 3, Function 0 is disabled and hidden, then Device 3, Function 2 is also disabled and hidden independent of the state of this bit. 0 = Bus 0, Device 3, Function 2, is disabled and hidden 1 = Bus 0, Device 3, Function 2 is enabled and visible
7	RO 1b	Reserved
6	RO 1b	**ME Function 0 (D3F0EN):** If this GMCH does not have ME capability, then Device 3, Function 0 is disabled and hidden independent of the state of this bit. 0 = Bus 0, Device 3, Function 0 is disabled and hidden 1 = Bus 0, Device 3, Function 0 is enabled and visible.
5	RO 0b	Reserved
4	RO 1b	**Internal Graphics Engine Function 1 (D2F1EN):** If Device 2, Function 0 is disabled and hidden, then Device 2, Function 1 is also disabled and hidden independent of the state of this bit. 0 = Bus 0, Device 2, Function 1 is disabled and hidden 1 = Bus 0, Device 2, Function 1 is enabled and visible
3	RO 1b	**Internal Graphics Engine Function 0 (D2F0EN):** 0 = Bus 0, Device 2, Function 0 is disabled and hidden 1 = Bus 0, Device 2, Function 0 is enabled and visible
2	RO 0b	Reserved

Bit	Access & Default	Description
1	RO 1b	**82Q965/82G965 MCH** **PCI Express Port (D1EN):** 0 = Bus 0, Device 1, Function 0 is disabled and hidden. 1 = Bus 0, Device 1, Function 0 is enabled and visible. **82Q963 GMCH** Reserved
0	RO 1b	**Host Bridge (D0EN):** Hardwired to 1. Bus 0, Device 0, Function 0 can not be disabled.

8.2.21 SSRW—Mirror Function 0 Software Scratch Read/Write

B/D/F/Type: 0/2/1/PCI
Address Offset: 58–5Bh
Default Value: 00000000h
Access: RO
Size: 32 bits

Bit	Access & Default	Description
31:0	RO 00000000h	Reserved R/W

8.2.22 BSM—Mirror of Function 0 Base of Stolen Memory

B/D/F/Type: 0/2/1/PCI
Address Offset: 5C–5Fh
Default Value: 07800000h
Access: RO
Size: 32 bits

Graphics stolen memory and TSEG are within DRAM space defined under TOLUD. From the top of low used DRAM, GMCH claims 1 to 64 MB of DRAM for internal graphics, if enabled. The base of stolen memory will always be below 4 GB. This is required to prevent aliasing between stolen range and the reclaim region.

Bit	Access & Default	Description
31:20	RO 078h	**Base of Stolen Memory (BSM):** This register contains bits 31:20 of the base address of stolen DRAM memory. The host interface determines the base of Graphics Stolen memory by subtracting the graphics stolen memory size from TOLUD. See Device 0 TOLUD for more explanation.
19:0	RO 00000h	Reserved

8.2.23 HSRW—Mirror of Device 2, Function 0 Hardware Scratch Read-Write

B/D/F/Type: 0/2/1/PCI
Address Offset: 60–61h
Default Value: 0000h
Access: R/W
Size: 16 bits

Bit	Access & Default	Description
15:0	R/W 0000h	Reserved

8.2.24 PMCAPID—Mirror Function 0 Power Management Capabilities ID

B/D/F/Type: 0/2/1/PCI
Address Offset: D0–D1h
Default Value: 0001h
Access: RO
Size: 16 bits

This register is a mirror of Function 0 with the same R/W attributes. The hardware implements a single physical register common to both Functions 0 and 1.

Bit	Access & Default	Description
15:8	RO 00h	**Next Capability Pointer (NEXT_PTR):** This field contains a pointer to next item in capabilities list. This is the final capability in the list and must be set to 00h.
7:0	RO 01h	**Capability Identifier (CAP_ID):** SIG defines this ID is 01h for power management.

8.2.25 PMCAP—Mirror Function 0 Power Management Capabilities

B/D/F/Type: 0/2/1/PCI
Address Offset: D2–D3h
Default Value: 0022h
Access: RO
Size: 16 bits

This register is a mirror of Function 0 with the same read/write attributes. The hardware implements a single physical register common to both Functions 0 and 1.

Bit	Access & Default	Description
15:11	RO 00h	**PME Support (PMES):** This field indicates the power states in which the IGD may assert PME#. Hardwired to 0 to indicate that the IGD does not assert the PME# signal.
10	RO 0b	**D2 Support (D2):** Hardwired to 0. The D2 power management state is not supported.
9	RO 0b	**D1 Support (D1):** Hardwired to 0 to indicate that the D1 power management state is not supported.
8:6	RO 000b	Reserved
5	RO 1b	**Device Specific Initialization (DSI):** Hardwired to 1 to indicate that special initialization of the IGD is required before generic class device driver is to use it.
4	RO	Reserved
3	RO 0b	**PME Clock (PMECLK):** Hardwired to 0 to indicate IGD does not support PME# generation.
2:0	RO 010b	**Version (VER):** Hardwired to 010b to indicate that there are 4 bytes of power management registers implemented and that this device complies with revision 1.1 of the PCI Power Management Interface Specification.

8.2.26 PMCS—Power Management Control/Status

B/D/F/Type: 0/2/1/PCI
Address Offset: D4–D5h
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

Bit	Access & Default	Description
15	RO 0b	**PME Status (PMESTS):** This bit is 0 to indicate that IGD does not support PME# generation from D3 (cold).
14:13	RO 00b	**Data Scale (DSCALE):** The IGD does not support data register. This bit always returns 0 when read, writes have no effect.
12:9	RO 0h	**Data Select (DATASEL):** The IGD does not support data register. This bit always returns 0 when read, writes have no effect.
8	RO 0b	**PME Enable (PME_EN):** This bit is 0 to indicate that PME# assertion from D3 (cold) is disabled.
7:2	RO 00h	Reserved
1:0	R/W 00b	**Power State (PWRSTAT):** This field indicates the current power state of the IGD and can be used to set the IGD into a new power state. If software attempts to write an unsupported state to this field, write operation must complete normally on the bus, but the data is discarded and no state change occurs. On a transition from D3-to-D0 the graphics controller is optionally reset to initial values. 00 = D0 (Default) 01 = D1 (Not Supported) 10 = D2 (Not Supported) 11 = D3

8.2.27 SWSMI—Mirror of Function 0 Software SMI

B/D/F/Type: 0/2/1/PCI
Address Offset: E0–E1h
Default Value: 0000h
Access: R/W
Size: 16 bits

As long as there is the potential that DVO port legacy drivers are in the system that expect this register at this address, Device 2, Function 0 address E0h–E1h must be reserved for this register.

Bit	Access & Default	Description
15:8	R/W 00h	**Software Scratch Bits (SWSB):**
7:1	R/W 00h	**Software Flag (SWF):** This field indicates caller and SMI function desired, as well as return result.
0	R/W 0b	**GMCH Software SMI Event (GSSMIE):** When Set, this bit will trigger an SMI. Software must write a 0 to clear this bit.

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9 Manageability Engine (ME) Subsystem Registers (Device 3, Functions 0,1,2)

This chapter contains the Manageability Engine registers for BTS '06 Intel® AMT.

9.1 Host Embedded Controller Interface (HECI1) Configuration Register Details (Device 3, Function 0)

Table 9-1. HECI1 Register Address Map (Device 3, Function 0)

Address Offset	Symbol	Register Name	Default Value	Access
00–03h	ID	Identifiers	29848086h	RO
04–05h	CMD	Command	0000h	RO, R/W
06–07h	STS	Device Status	0010h	RO
08h	RID	Revision ID	See register description	RO
09–0Bh	CC	Class Code	000000h	RO
0Ch	CLS	Cache Line Size	00h	RO
0Dh	MLT	Master Latency Timer	00h	RO
0Eh	HTYPE	Header Type	80h	RO
10–17h	HECI_MBAR	HECI MMIO Base Address	0000000000000004h	RO, R/W
2C–2Fh	SS	Sub System Identifiers	00000000h	R/WO
34h	CAP	Capabilities Pointer	50h	RO
3C–3Dh	INTR	Interrupt Information	0100h	RO, R/W
3Eh	MGNT	Minimum Grant	00h	RO
3Fh	MLAT	Maximum Latency	00h	RO
40–43h	HFS	Host Firmware Status	00000000h	RO
50–51h	PID	PCI Power Management Capability ID	8C01h	RO
52–53h	PC	PCI Power Management Capabilities	C803h	RO
54–55h	PMCS	PCI Power Management Control And Status	0008h	R/WC, RO, R/W
8C–8Dh	MID	Message Signaled Interrupt Identifiers	0005h	RO

Address Offset	Symbol	Register Name	Default Value	Access
8E–8Fh	MC	Message Signaled Interrupt Message Control	0080h	RO, R/W
90–93h	MA	Message Signaled Interrupt Message Address	00000000h	R/W, RO
94–97h	MUA	Message Signaled Interrupt Upper Address (Optional)	00000000h	R/W
98–99h	MD	Message Signaled Interrupt Message Data	0000h	R/W
A0h	HIDM	HECI Interrupt Delivery Mode	00h	R/W

9.1.1 ID—Identifiers

B/D/F/Type: 0/3/0/PCI
Address Offset: 0–3h
Default Value: 29848086h
Access: RO
Size: 32 bits

Bit	Access & Default	Description
31:16	RO 2984h	**Device ID (DID):** This register indicates what device number assigned for the ME subsystem.
15:0	RO 8086h	**Vendor ID (VID):** This field indicates Intel is the vendor, assigned by the PCI SIG.

9.1.2 CMD—Command

B/D/F/Type: 0/3/0/PCI
Address Offset: 4–5h
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

Bit	Access & Default	Description
15:11	RO 00000b	Reserved
10	R/W 0b	**Interrupt Disable (ID):** This bit disables this device from generating PCI line based interrupts. This bit does not have any effect on MSI operation. 0 = Enable 1 = Disable

Bit	Access & Default	Description
9	RO 0b	**Fast Back-to-Back Enable (FBE):** Not implemented, hardwired to 0.
8	RO 0b	**SERR# Enable (SEE):** Not implemented, hardwired to 0.
7	RO 0b	**Wait Cycle Enable (WCC):** Not implemented, hardwired to 0.
6	RO 0b	**Parity Error Response Enable (PEE):** Not implemented, hardwired to 0.
5	RO 0b	**VGA Palette Snooping Enable (VGA):** Not implemented, hardwired to 0.
4	RO 0b	**Memory Write and Invalidate Enable (MWIE):** Not implemented, hardwired to 0.
3	RO 0b	**Special Cycle Enable (SCE):** Not implemented, hardwired to 0.
2	R/W 0b	**Bus Master Enable (BME):** This bit controls the HECI host controller's ability to act as a system memory master for data transfers. 0 = Disable. HECI is blocked from generating MSI to the host processor. 1 = Enable When this bit is cleared, HECI bus master activity stops and any active DMA engines return to an idle condition. This bit is made visible to firmware through the H_PCI_CSR register, and changes to this bit may be configured by the H_PCI_CSR register to generate an ME MSI. Note that this bit does not block HECI accesses to ME-UMA (i.e., writes or reads to the host and ME circular buffers through the read window and write window registers still cause ME backbone transactions to ME-UMA).
1	R/W 0b	**Memory Space Enable (MSE):** This bit controls access to the HECI host controller’s memory mapped register space. 0 = Disable 1 = Enable
0	RO 0b	**I/O Space Enable (IOSE):** Not implemented, hardwired to 0.

9.1.3 STS—Device Status

B/D/F/Type: 0/3/0/PCI
Address Offset: 6–7h
Default Value: 0010h
Access: RO
Size: 16 bits

Bit	Access & Default	Description
15	RO 0b	**Detected Parity Error (DPE):** Not implemented, hardwired to 0.
14	RO 0b	**Signaled System Error (SSE):** Not implemented, hardwired to 0.
13	RO 0b	**Received Master-Abort (RMA):** Not implemented, hardwired to 0.
12	RO 0b	**Received Target Abort (RTA):** Not implemented, hardwired to 0.
11	RO 0b	**Signaled Target-Abort (STA):** Not implemented, hardwired to 0.
10:9	RO 00b	**DEVSEL# Timing (DEVT):** These bits are hardwired to 00.
8	RO 0b	**Master Data Parity Error Detected (DPD):** Not implemented, hardwired to 0.
7	RO 0b	**Fast Back-to-Back Capable (FBC):** Not implemented, hardwired to 0.
6	RO 0b	Reserved
5	RO 0b	**66 MHz Capable (C66):** Not implemented, hardwired to 0.
4	RO 1b	**Capabilities List (CL):** Indicates the presence of a capabilities list, hardwired to 1.
3	RO 0b	**Interrupt Status (IS):** Indicates the interrupt status of the device (1 = asserted).
2:0	RO 000b	Reserved

9.1.4 RID—Revision ID

B/D/F/Type: 0/3/0/PCI
Address Offset: 8h
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access & Default	Description
7:0	RO 00h	**Revision ID (RID):** This field indicates stepping of the HECI host controller. Refer to the *Intel® 965 Express Chipset Family Specification Update* for the value of the Revision ID register.

9.1.5 CC—Class Code

B/D/F/Type: 0/3/0/PCI
Address Offset: 9–Bh
Default Value: 000000h
Access: RO
Size: 24 bits

Bit	Access & Default	Description
23:16	RO 00h	**Base Class Code (BCC):** This field indicates the base class code of the HECI host controller device.
15:8	RO 00h	**Sub Class Code (SCC):** This field indicates the sub class code of the HECI host controller device.
7:0	RO 00h	**Programming Interface (PI):** This field indicates the programming interface of the HECI host controller device.

9.1.6 CLS—Cache Line Size

B/D/F/Type: 0/3/0/PCI
Address Offset: Ch
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access & Default	Description
7:0	RO 00h	**Cache Line Size (CLS):** Not implemented, hardwired to 0.

9.1.7 MLT—Master Latency Timer

B/D/F/Type: 0/3/0/PCI
Address Offset: Dh
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access & Default	Description
7:0	RO 00h	**Master Latency Timer (MLT):** Not implemented, hardwired to 0.

9.1.8 HTYPE—Header Type

B/D/F/Type: 0/3/0/PCI
Address Offset: Eh
Default Value: 80h
Access: RO
Size: 8 bits

Bit	Access & Default	Description
7	RO 1b	**Multi-Function Device (MFD):** This bit indicates the HECI host controller is part of a multi-function device.
6:0	RO 0000000b	**Header Layout (HL):** This field indicates that the HECI host controller uses a target device layout.

9.1.9 HECI_MBAR—HECI MMIO Base Address

B/D/F/Type: 0/3/0/PCI
Address Offset: 10–17h
Default Value: 0000000000000004h
Access: RO, R/W
Size: 64 bits

This register allocates space for the HECI memory-mapped registers defined in Section 1.3.7.

Bit	Access & Default	Description
63:4	R/W 00000000 0000000h	**Base Address (BA):** This field provides the base address of register memory space.
3	RO 0b	**Prefetchable (PF):** This bit indicates that this range is not pre-fetchable
2:1	RO 10b	**Type (TP):** This field indicates that this range can be mapped anywhere in 64-bit address space. Note that the (G)MCH only uses bits 35:4 of the base address field as the (G)MCH only decodes FSB address bits 35:4.
0	RO 0b	**Resource Type Indicator (RTE):** This bit indicates a request for register memory space.

9.1.10 SS—Sub System Identifiers

B/D/F/Type: 0/3/0/PCI
Address Offset: 2C–2Fh
Default Value: 00000000h
Access: R/WO
Size: 32 bits

Bit	Access & Default	Description
31:16	R/WO 0000h	**Subsystem ID (SSID):** This field indicates the sub-system identifier. This field should be programmed by BIOS during boot-up. Once written, this register becomes Read Only. This field can only be cleared by PLTRST#.
15:0	R/WO 0000h	**Subsystem Vendor ID (SSVID):** This field indicates the sub-system vendor identifier. This field should be programmed by BIOS during boot-up. Once written, this register becomes Read Only. This field can only be cleared by PLTRST#.

9.1.11 CAP—Capabilities Pointer

B/D/F/Type: 0/3/0/PCI
Address Offset: 34h
Default Value: 50h
Access: RO
Size: 8 bits

Bit	Access & Default	Description
7:0	RO 50h	**Capability Pointer (CP):** This field indicates the first capability pointer offset. It points to the PCI power management capability offset.

9.1.12 INTR—Interrupt Information

B/D/F/Type: 0/3/0/PCI
Address Offset: 3C–3Dh
Default Value: 0100h
Access: RO, R/W
Size: 16 bits

Bit	Access & Default	Description
15:8	RO 01h	**Interrupt Pin (IPIN):** This field indicates the interrupt pin the HECI host controller uses. The value of 01h selects INTA# interrupt pin. Note: As HECI is an internal device in the GMCH, the INTA# pin is implemented as an INTA# message to the ICH8.
7:0	R/W 00h	**Interrupt Line (ILINE):** Software written value to indicate which interrupt line (vector) the interrupt is connected to. No hardware action is taken on this register.

9.1.13 MGNT—Minimum Grant

B/D/F/Type: 0/3/0/PCI
Address Offset: 3Eh
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access & Default	Description
7:0	RO 00h	**Grant (GNT):** Not implemented, hardwired to 0.

9.1.14 MLAT—Maximum Latency

B/D/F/Type: 0/3/0/PCI
Address Offset: 3Fh
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access & Default	Description
7:0	RO 00h	**Latency (LAT):** Not implemented, hardwired to 0.

9.1.15 HFS—Host Firmware Status

B/D/F/Type: 0/3/0/PCI
Address Offset: 40–43h
Default Value: 00000000h
Access: RO
Size: 32 bits

Bit	Access & Default	Description
31:0	RO 00000000h	**Firmware Status Host Access (FS_HA):** This field indicates current status of the firmware for the HECI controller.

9.1.16 PID—PCI Power Management Capability ID

B/D/F/Type: 0/3/0/PCI
Address Offset: 50–51h
Default Value: 8C01h
Access: RO
Size: 16 bits

Bit	Access & Default	Description
15:8	RO 8Ch	**Next Capability (NEXT):** This field indicates the location of the next capability item in the list. This is the Message Signaled Interrupts capability.
7:0	RO 01h	**Cap ID (CID):** This field indicates that this pointer is a PCI power management.

9.1.17 PC—PCI Power Management Capabilities

B/D/F/Type: 0/3/0/PCI
Address Offset: 52–53h
Default Value: C803h
Access: RO
Size: 16 bits

Bit	Access & Default	Description
15:11	RO 11001b	**PME_Support (PSUP):** This field indicates the states that can generate PME#. HECI can assert PME# from any D-state except D1 or D2 which are not supported by HECI.
10	RO 0b	**D2_Support (D2S):** The D2 state is not supported for the HECI host controller.
9	RO 0b	**D1_Support (D1S):** The D1 state is not supported for the HECI host controller.
8:6	RO 000b	**Aux_Current (AUXC):** Reports the maximum Suspend well current required when in the D3COLD state.
5	RO 0b	**Device Specific Initialization (DSI):** This bit indicates whether device-specific initialization is required.
4	RO 0b	Reserved
3	RO 0b	**PME Clock (PMEC):** This bit indicates that PCI clock is not required to generate PME#.
2:0	RO 011b	**Version (VS):** This bit indicates support for Revision 1.2 of the PCI Power Management Specification.

9.1.18 PMCS—PCI Power Management Control And Status

B/D/F/Type: 0/3/0/PCI
Address Offset: 54–55h
Default Value: 0008h
Access: R/WC, RO, R/W
Size: 16 bits

Bit	Access & Default	Description
15	R/WC 0b	**PME Status (PMES):** The PME Status bit in HECI space can be set to 1 by FW performing a write into AUX register to set PMES. This bit is cleared by host processor writing a 1 to it. FW cannot clear this bit. Host processor writes with value 0 have no effect on this bit. This bit is reset to 0 by MRST#
14:9	RO 000000b	Reserved
8	R/W 0b	**PME Enable (PMEE):** This read/write bit is controlled by host SW. It does not directly have an effect on PME events. This bit is reset to 0 by MRST#. 0 = Disable 1 = Enable
7:4	RO 0000b	Reserved
3	RO 1b	**No_Soft_Reset (NSR):** This bit indicates that when the HECI host controller is transitioning from D3hot to D0 due to power state command; it does not perform an internal reset. **0 = No soft reset** **1 = Soft reset**
2	RO 0b	Reserved
1:0	R/W 00b	**Power State (PS):** This field is used both to determine the current power state of the HECI host controller and to set a new power state. The values are: 00 = D0 state 11 = D3HOT state

9.1.19 MID—Message Signaled Interrupt Identifiers

B/D/F/Type: 0/3/0/PCI
Address Offset: 8C–8Dh
Default Value: 0005h
Access: RO
Size: 16 bits

Bit	Access & Default	Description
15:8	RO 00h	**Next Pointer (NEXT):** This field indicates the next item in the list. This can be other capability pointers (such as PCI-Express) or it can be the last item in the list.
7:0	RO 05h	**Capability ID (CID):** Capabilities ID indicates MSI.

9.1.20 MC—Message Signaled Interrupt Message Control

B/D/F/Type: 0/3/0/PCI
Address Offset: 8E–8Fh
Default Value: 0080h
Access: RO, R/W
Size: 16 bits

Bit	Access & Default	Description
15:8	RO 00h	Reserved
7	RO 1b	**64 Bit Address Capable (C64):** This bit indicates whether capable of generating 64-bit messages.
6:4	RO 000b	**Multiple Message Enable (MME):** Not implemented, hardwired to 0.
3:1	RO 000b	**Multiple Message Capable (MMC):** Not implemented, hardwired to 0.
0	R/W 0b	**MSI Enable (MSIE):** If set, MSI is enabled and traditional interrupt pins are not used to generate interrupts. 0 = Disable 1 = Enable

9.1.21 MA—Message Signaled Interrupt Message Address

B/D/F/Type: 0/3/0/PCI
Address Offset: 90–93h
Default Value: 00000000h
Access: R/W, RO
Size: 32 bits

Bit	Access & Default	Description
31:2	R/W 00000000h	**Address (ADDR):** This field indicates the lower 32 bits of the system specified message address; always DW aligned.
1:0	RO 00b	Reserved

9.1.22 MD—Message Signaled Interrupt Message Data

B/D/F/Type: 0/3/0/PCI
Address Offset: 98–99h
Default Value: 0000h
Access: R/W
Size: 16 bits

Bit	Access & Default	Description
15:0	R/W 0000h	**Data (Data):** This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the FSB during the data phase of the MSI memory write transaction.

9.1.23 HIDM—HECI Interrupt Delivery Mode

B/D/F/Type: 0/3/0/PCI
Address Offset: A0h
Default Value: 00h
Access: R/W
Size: 8 bits
BIOS Optimal Default 00h

This register is used to select interrupt delivery mechanism for HECI to Host processor interrupts.

Bit	Access & Default	Description
7:2	RO 0h	Reserved
1:0	R/W 00b	**HECI Interrupt Delivery Mode (HIDM):** These bits control what type of interrupt the HECI will send.: 00 = Generate Legacy or MSI interrupt 01 = Generate SCI 10 = Generate SMI 11 = Reserved

9.2 HECI2 Configuration Register Details (Device 3, Function 1)) (Intel® 82Q965 GMCH Only)

Table 9-2. HECI2 Register Address Map (Device 3, Function 1)

Address Offset	Symbol	Register Name	Default Value	Access
00–03h	ID	Identifiers	29858086h	RO
04–05h	CMD	Command	0000h	RO, R/W
06–07h	STS	Device Status	0010h	RO
08h	RID	Revision ID	See register description	RO
09–0Bh	CC	Class Code	000000h	RO
0Ch	CLS	Cache Line Size	00h	RO
0Dh	MLT	Master Latency Timer	00h	RO
0Eh	HTYPE	Header Type	80h	RO
0Fh	BIST	Built In Self Test	00h	RO
10–17h	HECI_MBAR	HECI MMIO Base Address	000000000 0000004h	RO, R/W
2C–2Fh	SS	Sub System Identifiers	00000000h	R/WO
34h	CAP	Capabilities Pointer	50h	RO
3C–3Dh	INTR	Interrupt Information	0100h	R/W, RO
3Eh	MGNT	Minimum Grant	00h	RO
3Fh	MLAT	Maximum Latency	00h	RO
40–43h	HFS	Host Firmware Status	00000000h	RO
50–51h	PID	PCI Power Management Capability ID	8C01h	RO
52–53h	PC	PCI Power Management Capabilities	C803h	RO
54–55h	PMCS	PCI Power Management Control And Status	0008h	R/W, R/WC, RO
8C–8Dh	MID	Message Signaled Interrupt Identifiers	0005h	RO
8E–8Fh	MC	Message Signaled Interrupt Message Control	0080h	RO, R/W
90–93h	MA	Message Signaled Interrupt Message Address	00000000h	RO, R/W
94–97h	MUA	Message Signaled Interrupt Upper Address (Optional)	00000000h	R/W

Address Offset	Symbol	Register Name	Default Value	Access
98–99h	MD	Message Signaled Interrupt Message Data	0000h	R/W
A0	HIDM	HECI Interrupt Delivery Mode	00h	R/W

9.2.1 ID—Identifiers

B/D/F/Type: 0/3/1/PCI
Address Offset: 0–3h
Default Value: 29858086h
Access: RO
Size: 32 bits

Bit	Access & Default	Description
31:16	RO 2985h	**Device ID (DID):** This field indicates what device number assigned by Intel.
15:0	RO 8086h	**Vendor ID (VID):** This field indicates Intel is the vendor, assigned by the PCI SIG.

9.2.2 CMD—Command

B/D/F/Type: 0/3/1/PCI
Address Offset: 4–5h
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

Bit	Access & Default	Description
15:11	RO 00000b	**RSVD (RSVD):** Reserved
10	R/W 0b	**Interrupt Disable (ID):** This bit disables this device from generating PCI line based interrupts. This bit does not have any effect on MSI operation. 0 = Enable 1 = Disable
9	RO 0b	**Fast Back-to-Back Enable (FBE):** Not implemented, hardwired to 0.
8	RO 0b	**SERR# Enable (SEE):** Not implemented, hardwired to 0.
7	RO 0b	**Wait Cycle Enable (WCC):** Not implemented, hardwired to 0.
6	RO 0b	**Parity Error Response Enable (PEE):** Not implemented, hardwired to 0.

Bit	Access & Default	Description
5	RO 0b	**VGA Palette Snooping Enable (VGA):** Not implemented, hardwired to 0
4	RO 0b	**Memory Write and Invalidate Enable (MWIE):** Not implemented, hardwired to 0.
3	RO 0b	**Special Cycle Enable (SCE):** Not implemented, hardwired to 0.
2	R/W 0b	**Bus Master Enable (BME):** This bit controls the HECI host controller's ability to act as a system memory master for data transfers. 0 = Disable 1 = Enable When this bit is cleared, HECI bus master activity stops and any active DMA engines return to an idle condition. This bit is made visible to firmware through the H_PCI_CSR register, and changes to this bit may be configured by the H_PCI_CSR register to generate an ME MSI. When this bit is 0, HECI is blocked from generating MSI to the host processor. Note: This bit does not block HECI accesses to ME-UMA (i.e., writes or reads to the host and ME circular buffers through the read window and write window registers still cause ME backbone transactions to ME-UMA).
1	R/W 0b	**Memory Space Enable (MSE):** This bit controls access to the HECI host controller's memory mapped register space. 0 = Disable 1 = Enable
0	RO 0b	**I/O Space Enable (IOSE):** Not implemented, hardwired to 0.

9.2.3 STS—Device Status

B/D/F/Type: 0/3/1/PCI
Address Offset: 6–7h
Default Value: 0010h
Access: RO
Size: 16 bits

Bit	Access & Default	Description
15	RO 0b	**Detected Parity Error (DPE):** Not implemented, hardwired to 0.
14	RO 0b	**Signaled System Error (SSE):** Not implemented, hardwired to 0.
13	RO 0b	**Received Master-Abort (RMA):** Not implemented, hardwired to 0.
12	RO	**Received Target Abort (RTA):** Not implemented, hardwired to 0.
11	RO 0b	**Signaled Target-Abort (STA):** Not implemented, hardwired to 0.
10:9	RO 00b	**DEVSEL# Timing (DEVT):** These bits are hardwired to 00.
8	RO 0b	**Master Data Parity Error Detected (DPD):** Not implemented, hardwired to 0.
7	RO 0b	**Fast Back-to-Back Capable (FBC):** Not implemented, hardwired to 0.
6	RO 0b	Reserved
5	RO 0b	**66 MHz Capable (C66):** Not implemented, hardwired to 0.
4	RO 1b	**Capabilities List (CL):** This bit indicates the presence of a capabilities list, hardwired to 1.
3	RO 0b	**Interrupt Status (IS):** This bit indicates the interrupt status of the device 0 = Not asserted 1 = Asserted
2:0	RO 000b	Reserved

9.2.4 RID—Revision ID

B/D/F/Type: 0/3/1/PCI
Address Offset: 8h
Default Value: See table below
Access: RO
Size: 8 bits

Bit	Access & Default	Description
7:0	RO 00h	**Revision ID (RID):** This field indicates stepping of the HECI host controller. Refer to the *Intel® 965 Express Chipset Family Specification Update* for the value of the Revision ID register.

9.2.5 CC—Class Code

B/D/F/Type: 0/3/1/PCI
Address Offset: 9–Bh
Default Value: 000000h
Access: RO
Size: 24 bits

Bit	Access & Default	Description
23:16	RO 00h	**Base Class Code (BCC):** This field indicates the base class code of the HECI host controller device.
15:8	RO 00h	**Sub Class Code (SCC):** This field indicates the sub class code of the HECI host controller device.
7:0	RO 00h	**Programming Interface (PI):** This field indicates the programming interface of the HECI host controller device.

9.2.6 CLS—Cache Line Size

B/D/F/Type: 0/3/1/PCI
Address Offset: Ch
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access & Default	Description
7:0	RO 00h	**Cache Line Size (CLS):** Not implemented, hardwired to 0.

9.2.7 MLT—Master Latency Timer

B/D/F/Type: 0/3/1/PCI
Address Offset: Dh
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access & Default	Description
7:0	RO 00h	**Master Latency Timer (MLT):** Not implemented, hardwired to 0.

9.2.8 HTYPE—Header Type

B/D/F/Type: 0/3/1/PCI
Address Offset: Eh
Default Value: 80h
Access: RO
Size: 8 bits

Bit	Access & Default	Description
7	RO 1b	**Multi-Function Device (MFD):** This bit indicates the HECI host controller is part of a multi-function device.
6:0	RO 0000000b	**Header Layout (HL):** This field indicates that the HECI host controller uses a target device layout.

9.2.9 BIST—Built In Self Test

B/D/F/Type: 0/3/1/PCI
Address Offset: Fh
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access & Default	Description
7	RO 0b	**BIST Capable (BC):** Not implemented, hardwired to 0.
6:0	RO 0000000b	Reserved

9.2.10 HECI_MBAR—HECI MMIO Base Address

B/D/F/Type: 0/3/1/PCI
Address Offset: 10–17h
Default Value: 0000000000000004h
Access: RO, R/W
Size: 64 bits

This register allocates space for the HECI memory mapped registers.

Bit	Access & Default	Description
63:4	R/W 00000000 0000000h	**Base Address (BA):** This field provides the base address of register memory space.
3	RO 0b	**Prefetchable (PF):** This bit indicates that this range is not pre-fetchable
2:1	RO 10b	**Type (TP):** This field indicates that this range can be mapped anywhere in 32-bit address space.
0	RO 0b	**Resource Type Indicator (RTE):** This bit indicates a request for register memory space.

9.2.11 SS—Sub System Identifiers

B/D/F/Type: 0/3/1/PCI
Address Offset: 2C–2Fh
Default Value: 00000000h
Access: R/WO
Size: 32 bits

Bit	Access & Default	Description
31:16	R/WO 0000h	**Subsystem ID (SSID):** This field indicates the sub-system identifier. This field should be programmed by BIOS during boot-up. Once written, this register becomes Read Only. This field can only be cleared by PLTRST#.
15:0	R/WO 0000h	**Subsystem Vendor ID (SSVID):** This field indicates the sub-system vendor identifier. This field should be programmed by BIOS during boot-up. Once written, this register becomes Read Only. This field can only be cleared by PLTRST#.

9.2.12 CAP—Capabilities Pointer

B/D/F/Type: 0/3/1/PCI
Address Offset: 34h
Default Value: 50h
Access: RO
Size: 8 bits

Bit	Access & Default	Description
7:0	RO 50h	**Capability Pointer (CP):** This field indicates the first capability pointer offset. It points to the PCI power management capability offset.

9.2.13 INTR—Interrupt Information

B/D/F/Type: 0/3/1/PCI
Address Offset: 3C–3Dh
Default Value: 0100h
Access: R/W, RO
Size: 16 bits

Bit	Access & Default	Description
15:8	RO 01h	**Interrupt Pin (IPIN):** This field indicates the interrupt pin the HECI host controller uses. 01h = INTA# interrupt pin. **NOTE:** As HECI is an internal device in the GMCH, the INTA# pin is implemented as an INTA# message to the ICH8.
7:0	R/W 00h	**Interrupt Line (ILINE):** This field is a software written value that indicates which interrupt line (vector) the interrupt is connected. No hardware action is taken on this register.

9.2.14 MGNT—Minimum Grant

B/D/F/Type: 0/3/1/PCI
Address Offset: 3Eh
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access & Default	Description
7:0	RO 00h	**Grant (GNT):** Not implemented, hardwired to 0.

9.2.15 MLAT—Maximum Latency

B/D/F/Type: 0/3/1/PCI
Address Offset: 3Fh
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access & Default	Description
7:0	RO 00h	**Latency (LAT):** Not implemented, hardwired to 0.

9.2.16 HFS—Host Firmware Status

B/D/F/Type: 0/3/1/PCI
Address Offset: 40–43h
Default Value: 00000000h
Access: RO
Size: 32 bits

Bit	Access & Default	Description
31:0	RO 00000000h	**Firmware Status Host Access (FS_HA):** This field indicates current status of the firmware for the HECI controller. This field is the host's read only access to the FS field in the ME Firmware Status AUX register.

9.2.17 PID—PCI Power Management Capability ID

B/D/F/Type: 0/3/1/PCI
Address Offset: 50–51h
Default Value: 8C01h
Access: RO
Size: 16 bits

Bit	Access & Default	Description
15:8	RO 8Ch	**Next Capability (NEXT):** This field indicates the location of the next capability item in the list. This is the Message Signaled Interrupts capability.
7:0	RO 01h	**Cap ID (CID):** This field indicates that this pointer is a PCI power management.

9.2.18 PC—PCI Power Management Capabilities

B/D/F/Type: 0/3/1/PCI
Address Offset: 52–53h
Default Value: C803h
Access: RO
Size: 16 bits

Bit	Access & Default	Description
15:11	RO 11001b	**PME_Support (PSUP):** This field indicates the states that can generate PME#. HECI can assert PME# from any D-state except D1 or D2 which are not supported by HECI.
10	RO 0b	**D2_Support (D2S):** The D2 state is not supported for the HECI host controller.
9	RO 0b	**D1_Support (D1S):** The D1 state is not supported for the HECI host controller.
8:6	RO 000b	**Aux_Current (AUXC):** This field reports the maximum Suspend well current required when in the $D3_{COLD}$ state. PME# from $D3_{COLD}$ is not supported; therefore, this field is 000b.
5	RO 0b	**Device Specific Initialization (DSI):** This bit indicates whether device-specific initialization is required.
4	RO 0b	**RSVD (RSVD):** Reserved
3	RO 0b	**PME Clock (PMEC):** This bit indicates that PCI clock is not required to generate PME#.
2:0	RO 011b	**Version (VS):** This field indicates support for Revision 1.2 of the PCI Power Management Specification.

9.2.19 PMCS—PCI Power Management Control and Status

B/D/F/Type: 0/3/1/PCI
Address Offset: 54–55h
Default Value: 0008h
Access: R/W, R/WC, RO
Size: 16 bits

Bit	Access & Default	Description
15	R/WC 0b	**PME Status (PMES):** 0 = This bit is cleared by host processor writing a 1 to it. 1 = The PME Status bit in HECI space can be set to 1 by ARC FW performing a write into AUX register to set PMES. **Notes:** • ARC cannot clear this bit. • Host processor writes with value 0 have no effect on this bit. • This bit is reset to 0 by MRST#.
14:9	RO 000000b	Reserved.
8	R/W 0b	**PME Enable (PMEE):** This bit is read/write, under control of host SW. It does not directly have an effect on PME events. However, this bit is shadowed into AUX space so ARC FW can monitor it. The ARC FW is responsible for ensuring that FW does not cause the PME-S bit to transition to 1 while the PMEE bit is 0, indicating that host SW had disabled PME. This bit is reset to 0 by MRST#
7:4	RO 0000b	Reserved
3	RO 1b	**No_Soft_Reset (NSR):** 1 = This bit indicates that when the HECI host controller is transitioning from D3hot-to-D0 due to power state command, it does not perform an internal reset. Configuration Context is preserved. Upon transition from the D3hot to the D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the PowerState bits. 0 = Devices do perform an internal reset upon transitioning from D3hot to D0 via software control of the PowerState bits. Configuration Context is lost when performing the soft reset. Upon transition from the D3hot to the D0 state, full reinitialization sequence is needed to return the device to D0 Initialized.
2	RO 0b	Reserved

Bit	Access & Default	Description
1:0	R/W 00b	**Power State (PS):** This field is used both to determine the current power state of the HECI host controller and to set a new power state. 00 = D0 state 01 = Reserved 10 = Reserved 11 = D3HOT state The D1 and D2 states are not supported for this HECI host controller. When in the D3HOT state, the HBA's configuration space is available, but the register memory spaces are not. Additionally, interrupts are blocked. This field is visible to firmware through the H_PCI_CSR register, and changes to this field may be configured by the H_PCI_CSR register to generate an ME MSI.

9.2.20 MID—Message Signaled Interrupt Identifiers

B/D/F/Type: 0/3/1/PCI
Address Offset: 8C–8Dh
Default Value: 0005h
Access: RO
Size: 16 bits

Bit	Access & Default	Description
15:8	RO 00h	**Next Pointer (NEXT):** This field indicates the next item in the list. This can be other capability pointers (such as PCI-X or PCI-Express) or it can be the last item in the list.
7:0	RO 05h	**Capability ID (CID):** Capabilities ID indicates MSI.

9.2.21 MC—Message Signaled Interrupt Message Control

B/D/F/Type: 0/3/1/PCI
Address Offset: 8E–8Fh
Default Value: 0080h
Access: RO, R/W
Size: 16 bits

Bit	Access & Default	Description
15:8	RO 00h	**RSVD (RSVD):** Reserved
7	RO 1b	**64 Bit Address Capable (C64):** This field indicates whether capable of generating 64-bit messages.
6:4	RO 000b	**Multiple Message Enable (MME):** Not implemented, hardwired to 0.
3:1	RO 000b	**Multiple Message Capable (MMC):** Not implemented, hardwired to 0.
0	R/W 0b	**MSI Enable (MSIE):** If set, MSI is enabled and traditional interrupt pins are not used to generate interrupts. 0 = Disable 1 = Enable

9.2.22 MA—Message Signaled Interrupt Message Address

B/D/F/Type: 0/3/1/PCI
Address Offset: 90–93h
Default Value: 00000000h
Access: RO, R/W
Size: 32 bits

Bit	Access & Default	Description
31:2	R/W 00000000h	**Address (ADDR):** This field indicates the lower 32 bits of the system specified message address; always DW aligned.
1:0	RO 00b	Reserved

9.2.23 MUA—Message Signaled Interrupt Upper Address (Optional)

B/D/F/Type: 0/3/1/PCI
Address Offset: 94–97h
Default Value: 00000000h
Access: R/W
Size: 32 bits

Bit	Access & Default	Description
31:0	R/W 00000000h	**Upper Address (UADDR):** This field indicates the upper 32 bits of the system specified message address. This register is optional and only implemented if MC.C64=1.

9.2.24 MD—Message Signaled Interrupt Message Data

B/D/F/Type: 0/3/1/PCI
Address Offset: 98–99h
Default Value: 0000h
Access: R/W
Size: 16 bits

Bit	Access & Default	Description
15:0	R/W 0000h	**Data (Data):** This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the FSB during the data phase of the MSI memory write transaction.

9.2.25 HIDM—HECI Interrupt Delivery Mode

B/D/F/Type:	0/3/1/PCI
Address Offset:	A0h
Default Value:	00h
Access:	R/W
Size:	8 bits
BIOS Optimal Default	00h

This register is used to select interrupt delivery mechanism for HECI-to-Host processor interrupts.

Bit	Access & Default	Description
7:2	RO 0h	Reserved
1:0	R/W 00b	**HECI Interrupt Delivery Mode (HIDM):** These bits control what type of interrupt the HECI will send when ARC writes to set the M_IG bit in AUX space. They are interpreted as follows: 00 = Generate Legacy or MSI interrupt 01 = Generate SCI 10 = Generate SMI

9.3 PT IDER Configuration Register Details (Device 3, Function 2) (Intel® 82Q965 GMCH Only)

Table 9-3. PT IDER Register Address Map (Device 3, Function 2)

Address Offset	Symbol	Register Name	Default Value	Access
00–03h	ID	Identification	29868086h	RO
04–05h	CMD	Command Register	0000h	RO, R/W
06–07h	STS	Device Status	00B0h	RO
08h	RID	Revision ID	See register description	RO
09–0Bh	CC	Class Codes	010185h	RO
0Ch	CLS	Cache Line Size	00h	RO
0Dh	MLT	Master Latency Timer	00h	RO
0Eh	HTYPE	Header Type (Not implemented)	Undefined	Undefined
10–13h	PCMDBA	Primary Command Block IO Bar	00000001h	RO, R/W
14–17h	PCTLBA	Primary Control Block Base Address	00000001h	RO, R/W
18–1Bh	SCMDBA	Secondary Command Block Base Address	00000001h	RO, R/W
1C–1Fh	SCTLBA	Secondary Control Block base Address	00000001h	RO, R/W
20–23h	LBAR	Legacy Bus Master Base Address	00000001h	RO, R/W
24–27h	RSVD	Reserved	00000000h	RO
2C–2Fh	SS	Sub System Identifiers	00008086h	R/WO
30–33h	EROM	Expansion ROM Base Address	00000000h	RO
34h	CAP	Capabilities Pointer	C8h	RO
3C–3Dh	INTR	Interrupt Information	0300h	R/W, RO
3Eh	MGNT	Minimum Grant	00h	RO
3Fh	MLAT	Maximum Latency	00h	RO
C8–C9h	PID	PCI Power Management Capability ID	D001h	RO
CA–CBh	PC	PCI Power Management Capabilities	0023h	RO
CC–CFh	PMCS	PCI Power Management Control and Status	00000000h	RO, RO/V, R/W
D0–D1h	MID	Message Signaled Interrupt Capability ID	0005h	RO
D2–D3h	MC	Message Signaled Interrupt Message Control	0080h	RO, R/W
D4–D7h	MA	Message Signaled Interrupt Message Address	00000000h	RO, R/W
D8–DBh	MAU	Message Signaled Interrupt Message Upper Address	00000000h	RO, R/W
DC–DDh	MD	Message Signaled Interrupt Message Data	0000h	R/W

9.3.1 ID—Identification

B/D/F/Type: 0/3/2/PCI
Address Offset: 0–3h
Default Value: 29868086h
Access: RO
Size: 32 bits

This register, combined with the Device Identification register, uniquely identifies any PCI device.

Bit	Access & Default	Description
31:16	RO 2986h	**Device ID (DID):** This field is assigned by Manufacturer; identifies the type of Device
15:0	RO 8086h	**Vendor ID (VID):** This field indicates the company vendor as Intel

9.3.2 CMD—Command Register

B/D/F/Type: 0/3/2/PCI
Address Offset: 4–5h
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

This register provides basic control over the device's ability to respond to and perform Host system related accesses.

Note: Reset: Host System reset or D3->D0 transition of function.

Bit	Access & Default	Description
15:11	RO 00h	Reserved
10	R/W 0b	**Interrupt Disable (ID):** This bit disables pin-based INTx# interrupts. This bit has no effect on MSI operation. 0 = Enable. Internal INTx# messages are generated if there is an interrupt **and** MSI is not enabled. 1 = Disable. Internal INTx# messages will not be generated.
9	RO 0b	**Fast back-to-back enable (FBE):** Hardwired to 0.
8	RO 0b	**SERR# Enable (SEE):** Hardwired to 0. The PT function never generates a SERR#.
7	RO 0b	**Wait Cycle Enable (WCC):** Hardwired to 0.
6	RO 0b	**Parity Error Response Enable (PEE):** Hardwired to 0. No Parity detection in PT functions.

Bit	Access & Default	Description
5	RO 0b	**VGA Palette Snooping Enable (VGA):** Reserved
4	RO 0b	**Memory Write and Invalidate Enable (MWIE):** Reserved
3	RO 0b	**Special Cycle enable (SCE):** Reserved
2	R/W 0b	**Bus Master Enable (BME):** This bit controls the PT function's ability to act as a master for data transfers. This bit does not impact the generation of completions for split transaction commands. 0 = Disable 1 = Enable
1	RO 0b	**Memory Space Enable (MSE):** Hardwired to 0. PT function does not contain target memory space.
0	R/W 0b	**I/O Space Enable (IOSE):** This bit controls access to the PT function's target I/O space 0 = Disable 1 = Enable

9.3.3 STS—Device Status

B/D/F/Type: 0/3/2/PCI
Address Offset: 6–7h
Default Value: 00B0h
Access: RO
Size: 16 bits

This register is used by the function to reflect its PCI status to the host for the functionality that it implements.

Bit	Access & Default	Description
15	RO 0b	**Detected Parity Error (DPE):** Reserved. No parity error on its interface
14	RO 0b	**Signaled System Error (SSE):** Reserved. The PT function will never generate a SERR#
13	RO 0b	**Received Master-Abort Status (RMA):** Reserved
12	RO 0b	**Received Target-Abort Status (RTA):** Reserved
11	RO 0b	**Signaled Target-Abort Status (STA):** Reserved. The PT Function will never generate a target abort.
10:9	RO 00b	**DEVSEL# Timing Status (DEVT):** This bit controls the device select time for the PT function's PCI interface
8	RO 0b	**Master Data Parity Error Detected) (DPD):** Hardwired to 0. PT function (IDER), as a master, does not detect a parity error.

Bit	Access & Default	Description
7	RO 1b	**Fast back to back capable (RSVD):** Reserved
6	RO 0b	Reserved
5	RO 1b	**66 MHz capable:** Reserved
4	RO 1b	**Capabilities List (CL):** This bit indicates that there is a capabilities pointer implemented in the device.
3	RO 0b	**Interrupt Status (IS):** This bit reflects the state of the interrupt in the function. Setting of the Interrupt Disable bit to 1 has no affect on this bit. Only when this bit is a 1 and ID bit is 0 is the INTC interrupt asserted to the Host
2:0	RO 000b	Reserved

9.3.4 RID—Revision ID

B/D/F/Type: 0/3/2/PCI
Address Offset: 8h
Default Value: 00h
Access: RO
Size: 8 bits

This register specifies a device specific revision.

Bit	Access & Default	Description
7:0	RO 00h	**Revision ID (RID):** Refer to the *Intel® 965 Express Chipset Family Specification Update* for the value of the Revision ID register.

9.3.5 CC—Class Codes

B/D/F/Type: 0/3/2/PCI
Address Offset: 9–Bh
Default Value: 010185h
Access: RO
Size: 24 bits

This register identifies the basic functionality of the device is IDE mass storage.

Bit	Access & Default	Description
23:0	RO 010185h	**Programming Interface BCC SCC (PI BCC SCC):**

9.3.6 CLS—Cache Line Size

B/D/F/Type: 0/3/2/PCI
Address Offset: Ch
Default Value: 00h
Access: RO
Size: 8 bits

This register defines the system cache line size in DWord increments. This is mandatory for master that use the Memory-Write and Invalidate command.

Bit	Access & Default	Description
7:0	RO 00h	**Cache Line Size (CLS):** All writes to system memory are Memory Writes.

9.3.7 MLT—Master Latency Timer

B/D/F/Type: 0/3/2/PCI
Address Offset: Dh
Default Value: 00h
Access: RO
Size: 8 bits

This register defines the minimum number of PCI clocks the bus master can retain ownership of the bus whenever it initiates new transactions.

Bit	Access & Default	Description
7:0	RO 00h	**Master Latency Timer (MLT):** Not implemented since the function is in the GMCH

9.3.8 HTYPE—Header Type

B/D/F/Type: 0/3/2/PCI
Address Offset: Eh
Default Value: Undefined
Access: Undefined
Size: 8 bits

This register is Not implemented.

9.3.9 PCMDBA—Primary Command Block IO Bar

B/D/F/Type: 0/3/2/PCI
Address Offset: 10–13h
Default Value: 00000001h
Access: RO, R/W
Size: 32 bits

This 8-byte I/O space is used in Native Mode for the Primary Controller's Command Block.

Reset: Host system Reset or D3->D0 transition of the function.

Bit	Access & Default	Description
31:16	RO 0000h	Reserved
15:3	R/W 0000h	**Base Address (BAR):** This field indicates the base address of the BAR0 I/O space (8 consecutive I/O locations)
2:1	RO 00b	Reserved
0	RO 1b	**Resource Type Indicator (RTE):** Hardwired to 1 indicating a request for I/O space

9.3.10 PCTLBA—Primary Control Block Base Address

B/D/F/Type: 0/3/2/PCI
Address Offset: 14–17h
Default Value: 00000001h
Access: RO, R/W
Size: 32 bits

This 4-byte I/O space is used in Native Mode for the Primary Controller's Control Block.

Reset: Host system Reset or D3->D0 transition of the function.

Bit	Access & Default	Description
31:16	RO 0000h	Reserved
15:2	R/W 0000h	**Base Address (BAR):** This field indicates the Base Address of the BAR1 I/O space (4 consecutive I/O locations).
1	RO 0b	Reserved
0	RO 1b	**Resource Type Indicator (RTE):** This bit indicates a request for I/O space.

9.3.11 SCMDBA—Secondary Command Block Base Address

B/D/F/Type: 0/3/2/PCI
Address Offset: 18–1Bh
Default Value: 00000001h
Access: RO, R/W
Size: 32 bits

This 8-byte I/O space is used in Native Mode for the secondary Controller's Command Block. Secondary Channel is not implemented and reads return 7F7F7F7Fh and all writes are ignored.

Reset: Host System Reset or D3->D0 transition of the function.

Bit	Access & Default	Description
31:16	RO 0000h	Reserved
15:3	R/W 0000h	**Base Address (BAR):** This field indicates the Base Address of the I/O space (8 consecutive I/O locations).
2:1	RO 00b	Reserved
0	RO 1b	**Resource Type Indicator (RTE):** This bit indicates a request for I/O space.

9.3.12 SCTLBA—Secondary Control Block base Address

B/D/F/Type: 0/3/2/PCI
Address Offset: 1C–1Fh
Default Value: 00000001h
Access: RO, R/W
Size: 32 bits

This 4-byte I/O space is used in Native Mode for Secondary Controller's Control block. Secondary Channel is not implemented and reads return 7F7F7F7F and all writes are dropped.

Reset: Host System Reset or D3->D0 transition

Bit	Access & Default	Description
31:16	RO 0000h	Reserved
15:2	R/W 0000h	**Base Address (BAR):** This field indicates the Base Address of the I/O space (4 consecutive I/O locations).
1	RO 0b	Reserved
0	RO 1b	**Resource Type Indicator (RTE):** This bit indicates a request for I/O space.

9.3.13 LBAR—Legacy Bus Master Base Address

B/D/F/Type: 0/3/2/PCI
Address Offset: 20–23h
Default Value: 00000001h
Access: RO, R/W
Size: 32 bits

This Bar is used to allocate I/O space for the SFF-8038i mode of operation (aka Bus Master IDE).

Reset: Host system Reset or D3->D0 transition.

Bit	Access & Default	Description
31:16	RO 0000h	Reserved
15:4	R/W 000h	**Base Address (BA):** This field indicates Base Address of the I/O space (16 consecutive I/O locations).
3:1	RO 000b	Reserved
0	RO 1b	**Resource Type Indicator (RTE):** This bit indicates a request for I/O space.

9.3.14 SS—Sub System Identifiers

B/D/F/Type: 0/3/2/PCI
Address Offset: 2C–2Fh
Default Value: 00008086h
Access: R/WO
Size: 32 bits

These registers are used to uniquely identify the add-in card or the subsystem that the device resides within.

Reset: Host System Reset.

Bit	Access & Default	Description
31:16	R/WO 0000h	**Subsystem ID (SSID):** This field is written by BIOS. No hardware action taken on this value.
15:0	R/WO 8086h	**Subsystem Vendor ID (SSVID):** This field is written by BIOS. No hardware action taken on this value.

9.3.15 EROM—Expansion ROM Base Address

B/D/F/Type: 0/3/2/PCI
Address Offset: 30–33h
Default Value: 00000000h
Access: RO
Size: 32 bits

This optional register is not implemented.

Bit	Access & Default	Description
31:11	RO 000000h	**Expansion ROM Base Address (ERBAR):**
10:1	RO 000h	Reserved
0	RO 0b	**Enable (EN):** Enable expansion ROM Access

9.3.16 CAP—Capabilities Pointer

B/D/F/Type: 0/3/2/PCI
Address Offset: 34h
Default Value: C8h
Access: RO
Size: 8 bits

This optional register is used to point to a linked list of new capabilities implemented by the device.

Bit	Access & Default	Description
7:0	RO C8h	**Capability Pointer (CP):** This field indicates that the first capability pointer offset is offset c8h (the power management capability)

9.3.17 INTR—Interrupt Information

B/D/F/Type: 0/3/2/PCI
Address Offset: 3C–3Dh
Default Value: 0300h
Access: R/W, RO
Size: 16 bits

See definitions in the registers below.

Reset: Host System Reset or D3->D0 reset of the function.

Bit	Access & Default	Description
15:8	RO 03h	**Interrupt Pin (IPIN):** A value of 1h/2h/3h/4h indicates that this function implements legacy interrupt on INTA/INTB/INTC/INTD, respectively. **Function Value INTx** (2 IDE) 03h INTC
7:0	R/W 00h	**Interrupt Line (ILINE):** The value written in this register indicates which input of the system interrupt controller, the device's interrupt pin is connected to. This value is used by the OS and the device driver, and has no affect on the (G)MCH.

9.3.18 MGNT—Minimum Grant

B/D/F/Type: 0/3/2/PCI
Address Offset: 3Eh
Default Value: 00h
Access: RO
Size: 8 bits

This optional register is not implemented.

Bit	Access & Default	Description
7:0	RO 00h	Reserved

9.3.19 MLAT—Maximum Latency

B/D/F/Type: 0/3/2/PCI
Address Offset: 3Fh
Default Value: 00h
Access: RO
Size: 8 bits

This optional register is not implemented.

Bit	Access & Default	Description
7:0	RO 00h	Reserved

9.3.20 PID—PCI Power Management Capability ID

B/D/F/Type: 0/3/2/PCI
Address Offset: C8–C9h
Default Value: D001h
Access: RO
Size: 16 bits

Bit	Access & Default	Description
15:8	RO D0h	**Next Capability (NEXT):** The value of D0h points to the MSI capability
7:0	RO 01h	**Cap ID (CID):** This field indicates that this pointer is a PCI power management.

9.3.21 PC—PCI Power Management Capabilities

B/D/F/Type: 0/3/2/PCI
Address Offset: CA–CBh
Default Value: 0023h
Access: RO
Size: 16 bits

This register implements the power management capabilities of the function.

Bit	Access & Default	Description
15:11	RO 00000b	**PME Support (PME):** This field indicates no PME# in the PT function.
10	RO 0b	**D2 Support (D2S):** The D2 state is not Supported
9	RO 0b	**D1 Support (D1S):** The D1 state is not supported
8:6	RO 000b	**Aux Current (AUXC):** PME# from D3 (cold) state is not supported, therefore this field is 000b
5	RO 1b	**Device Specific Initialization (DSI):** This bit indicates that no device-specific initialization is required.
4	RO 0b	Reserved
3	RO 0b	**PME Clock (PMEC):** This bit indicates that PCI clock is not required to generate PME#.
2:0	RO 011b	**Version (VS):** This field indicates support for revision 1.2 of the PCI power management specification.

9.3.22 PMCS—PCI Power Management Control and Status

B/D/F/Type: 0/3/2/PCI
Address Offset: CC–CFh
Default Value: 00000000h
Access: RO, RO/V, R/W
Size: 32 bits
BIOS Optimal Default 0000h

This register implements the PCI PM Control and Status Register to allow PM state transitions and Wake up.

Note: NSR bit of this register. All registers (PCI configuration and device specific) marked with D3->D0 transition reset will only do so if this bit reads a 0. If this bit is a 1, the D3->D0 transition will not reset the registers.

Reset: Host System Reset or D3->D0 transition.

Bit	Access & Default	Description
31:16	RO 0h	Reserved
15	RO 0b	**PME Status (PMES):** This bit is set when a PME event is to be requested. Not supported
14:9	RO 00h	Reserved
8	RO 0b	**PME Enable (PMEE):** Not Supported
7:2	RO 0s	Reserved
1:0	R/W 00b	**Power State (PS):** This field is used both to determine the current power state of the PT function and to set a new power state. The values are: 00 = D0 state 11 = $D3_{HOT}$ state When in the $D3_{HOT}$ state, the controller's configuration space is available, but the I/O and memory spaces are not. Additionally, interrupts are blocked. If software attempts to write a 10 or 01 to these bits, the write will be ignored.

9.3.23 MID—Message Signaled Interrupt Capability ID

B/D/F/Type: 0/3/2/PCI
Address Offset: D0–D1h
Default Value: 0005h
Access: RO
Size: 16 bits

Message Signaled Interrupt is a feature that allows the device/function to generate an interrupt to the host by performing a DWord memory write to a system specified address with system specified data. This register is used to identify and configure an MSI capable device.

Bit	Access & Default	Description
15:8	RO 00h	**Next Pointer (NEXT):** This value Indicates this is the last item in the capabilities list.
7:0	RO 05h	**Capability ID (CID):** Capabilities ID value indicates device is capable of generating an MSI.

9.3.24 MC—Message Signaled Interrupt Message Control

B/D/F/Type: 0/3/2/PCI
Address Offset: D2–D3h
Default Value: 0080h
Access: RO, R/W
Size: 16 bits

This register provides System Software control over MSI.

Note: Reset: Host System Reset or D3->D0 transition

Bit	Access & Default	Description
15:8	RO 00h	Reserved
7	RO 1b	**64 Bit Address Capable (C64):** This bit indicates the capable of generating 64-bit and 32-bit messages
6:4	R/W 000b	**Multiple Message Enable (MME):** These bits are R/W for software compatibility, but only one message is ever sent by the PT function.
3:1	RO 000b	**Multiple Message Capable (MMC):** Only one message is required.
0	R/W 0b	**MSI Enable (MSIE):** If set, MSI is enabled and traditional interrupt pins are not used to generate interrupts. 0 = Disable 1 = Enable

9.3.25 MA—Message Signaled Interrupt Message Address

B/D/F/Type: 0/3/2/PCI
Address Offset: D4–D7h
Default Value: 00000000h
Access: RO, R/W
Size: 32 bits

This register specifies the DWORD aligned address programmed by system software for sending MSI.

Note: Reset: Host system Reset or D3->D0 transition.

Bit	Access & Default	Description
31:2	R/W 00000000h	**Address (ADDR):** This field indicates the lower 32 bits of the system specified message address; always DWORD aligned
1:0	RO 00b	Reserved

9.3.26 MAU—Message Signaled Interrupt Message Upper Address

B/D/F/Type: 0/3/2/PCI
Address Offset: D8–DBh
Default Value: 00000000h
Access: RO, R/W
Size: 32 bits

Upper 32 bits of the message address for the 64bit address capable device.

Note: Reset: Host system Reset or D3->D0 transition.

Bit	Access & Default	Description
31:4	RO 0000000h	Reserved
3:0	R/W 0000b	**Address (ADDR):** This field indicates the upper 4 bits of the system specified message address.

9.3.27 MD—Message Signaled Interrupt Message Data

B/D/F/Type: 0/3/2/PCI
Address Offset: DC–DDh
Default Value: 0000h
Access: R/W
Size: 16 bits

This 16-bit field is programmed by system software if MSI is enabled.

Note: Reset: Host system Reset or D3->D0 transition.

Bit	Access & Default	Description
15:0	R/W 0000h	**Data (DATA):** This content is driven onto the lower word of the data bus of the MSI memory write transaction.

9.4 (KT) Redirection Configuration Register Details (Device 3, Function 3) (Intel® 82Q965 GMCH Only)

Table 9-4. (KT) Redirection Register Address Map (Device 3, Function3)

Address Offset	Symbol	Register Name	Default Value	Access
00–03h	ID	Identification	29878086h	RO
04–05h	CMD	Command Register	0000h	RO, R/W
06–07h	STS	Device Status	00B0h	RO
08h	RID	Revision ID	See register description	RO
09–0Bh	CC	Class Codes	010185h	RO
0Ch	CLS	Cache Line Size	00h	RO
0Dh	MLT	Master Latency Timer	00h	RO
0Eh	HTYPE	Header Type	Undefined	Undefined
10–13h	KTIBA	KT IO Block Base Address	00000001h	RO, R/W
14–17h	KTMBA	KT Memory Block Base Address	00000000h	RO, R/W
2C–2Fh	SS	Sub System Identifiers	00008086h	R/WO
30–33h	EROM	Expansion ROM Base Address	00000000h	RO
34h	CAP	Capabilities Pointer	C8h	RO
3C–3Dh	INTR	Interrupt Information	0200h	R/W, RO
3Eh	MGNT	Minimum Grant	00h	RO
3Fh	MLAT	Maximum Latency	00h	RO
C8–C9h	PID	PCI Power Management Capability ID	D001h	RO
CA–CBh	PC	PCI Power Management Capabilities	0023h	RO
CC–CFh	PMCS	PCI Power Management Control and Status	00000000h	RO, R/W, RO/V
D0–D1h	MID	Message Signaled Interrupt Capability ID	0005h	RO
D2–D3h	MC	Message Signaled Interrupt Message Control	0080h	RO, R/W
D4–D7h	MA	Message Signaled Interrupt Message Address	00000000h	RO, R/W
D8–DBh	MAU	Message Signaled Interrupt Message Upper Address	00000000h	RO, R/W

Address Offset	Symbol	Register Name	Default Value	Access
DC–DDh	MD	Message Signaled Interrupt Message Data	0000h	R/W

9.4.1 ID—Identification

B/D/F/Type: 0/3/3/PCI
Address Offset: 0–3h
Default Value: 29878086h
Access: RO
Size: 32 bits

This register, combined with the Device Identification register, uniquely identifies any PCI device.

Bit	Access & Default	Description
31:16	RO 2987h	**Device ID (DID):** This field is assigned by manufacturer, identifies the device.
15:0	RO 8086h	**Vendor ID (VID):** This 16-bit field indicates the company vendor as Intel.

9.4.2 CMD—Command Register

B/D/F/Type: 0/3/3/PCI
Address Offset: 4–5h
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

This register provides basic control over the device's ability to respond to and perform Host system related accesses.

Reset: Host System reset or D3->D0 transition.

Bit	Access & Default	Description
15:11	RO 00h	Reserved
10	R/W 0b	**Interrupt Disable (ID):** This disables pin-based INTx# interrupts. This bit has no effect on MSI operation. When set, internal INTx# messages will not be generated. When cleared, internal INTx# messages are generated if there is an interrupt ***and*** MSI is not enabled.
9	RO 0b	**Fast back-to-back enable (FBE):** Hardwired to 0.
8	RO 0b	**SERR# Enable (SEE):** The PT function never generates an SERR#. Hardwired to 0.

Bit	Access & Default	Description
7	RO 0b	**Wait Cycle Enable (WCC):** Hardwired to 0.
6	RO 0b	**Parity Error Response Enable (PEE):** No Parity detection in PT functions. Hardwired to 0.
5	RO 0b	**VGA Palette Snooping Enable (VGA):** Hardwired to 0.
4	RO 0b	**Memory Write and Invalidate Enable (MWIE):** Hardwired to 0.
3	RO 0b	**Special Cycle enable (SCE):** Hardwired to 0.
2	R/W 0b	**Bus Master Enable (BME):** This bit controls the KT function's ability to act as a master for data transfers. This bit does not impact the generation of completions for split transaction commands. For KT, the only bus mastering activity is MSI generation. 0 = Disable 1 = Enable
1	R/W 0b	**Memory Space Enable (MSE):** This bit controls Access to the PT function's target memory space. 0 = Disable 1 = Enable
0	R/W 0b	**I/O Space Enable (IOSE):** This bit controls access to the PT function's target I/O space. 0 = Disable 1 = Enable

9.4.3 STS—Device Status

B/D/F/Type: 0/3/3/PCI
Address Offset: 6–7h
Default Value: 00B0h
Access: RO
Size: 16 bits

This register is used by the function to reflect its PCI status to the host for the functionality that it implements.

Bit	Access & Default	Description
15	RO 0b	**Detected Parity Error (DPE):** No parity error on its interface.
14	RO 0b	**Signaled System Error (SSE):** The PT function will never generate a SERR#.
13	RO 0b	**Received Master-Abort Status (RMA):** Hardwired to 0.

Bit	Access & Default	Description
12	RO 0b	**Received Target-Abort Status (RTA):** Hardwired to 0.
11	RO 0b	**Signaled Target-Abort Status (STA):** The PT Function will never generate a target abort. Hardwired to 0.
10:9	RO 00b	**DEVSEL# Timing Status (DEVT):** This field controls the device select time for the PT function's PCI interface
8	RO 0b	**Master Data Parity Error Detected) (DPD):** PT function (IDER), as a master, does not detect a parity error. Other PT function is not a master and hence this bit is reserved also.
7	RO 1b	**Fast back to back capable (RSVD):** Hardwired to 1.
6	RO 0b	Reserved
5	RO 1b	**66MHz capable (RSVD):**
4	RO 1b	**Capabilities List (CL):** This bit indicates that there is a capabilities pointer implemented in the device.
3	RO 0b	**Interrupt Status (IS):** This bit reflects the state of the interrupt in the function. Setting of the Interrupt Disable bit to 1 has no affect on this bit. Only when this bit is a 1 and ID bit is 0 is the intb interrupt asserted to the Host
2:0	RO 000b	Reserved

9.4.4 RID—Revision ID

B/D/F/Type: 0/3/3/PCI
Address Offset: 8h
Default Value: 00h
Access: RO
Size: 8 bits

This register specifies a device specific revision.

Bit	Access & Default	Description
7:0	RO 00h	**Revision ID (RID):** This field indicates stepping of the silicon. Refer to the *Intel® 965 Express Chipset Family Specification Update* for the value of the Revision ID register.

9.4.5 CC—Class Codes

B/D/F/Type: 0/3/3/PCI
Address Offset: 9–Bh
Default Value: 010185h
Access: RO
Size: 24 bits

This register identifies the basic functionality of the device (i.e., Serial Com Port).

Bit	Access & Default	Description
23:0	RO 010185h	**Programming Interface BCC SCC (PI BCC SCC):**

9.4.6 CLS—Cache Line Size

B/D/F/Type: 0/3/3/PCI
Address Offset: Ch
Default Value: 00h
Access: RO
Size: 8 bits

This register defines the system cache line size in DWord increments. This is mandatory for a master that uses the Memory-Write and Invalidate command.

Bit	Access & Default	Description
7:0	RO 00h	**Cache Line Size (CLS):** All writes to system memory are Memory Writes.

9.4.7 MLT—Master Latency Timer

B/D/F/Type: 0/3/3/PCI
Address Offset: Dh
Default Value: 00h
Access: RO
Size: 8 bits

This register defines the minimum number of PCI clocks the bus master can retain ownership of the bus whenever it initiates new transactions.

Bit	Access & Default	Description
7:0	RO 00h	**Master Latency Timer (MLT):** Not implemented since the function is in the (G)MCH.

9.4.8 HTYPE—Header Type

B/D/F/Type: 0/3/3/PCI
Address Offset: Eh
Default Value: Undefined
Access: Undefined
Size: 8 bits

Register is Not implemented. Reads return 0.

9.4.9 KTIBA—KT IO Block Base Address

B/D/F/Type: 0/3/3/PCI
Address Offset: 10–13h
Default Value: 00000001h
Access: RO, R/W
Size: 32 bits

This register provides the Base Address for the 8 byte I/O space for KT.

Reset: Host system Reset or D3->D0 transition

Bit	Access & Default	Description
31:16	RO 0000h	Reserved
15:3	R/W 0000h	**Base Address (BAR):** This field indicates the base Address of the I/O space (8 consecutive I/O locations)
2:1	RO 00b	Reserved
0	RO 1b	**Resource Type Indicator (RTE):** This bit indicates a request for I/O space.

9.4.10 KTMBA—KT Memory Block Base Address

B/D/F/Type: 0/3/3/PCI
Address Offset: 14–17h
Default Value: 00000000h
Access: RO, R/W
Size: 32 bits

This register provides the Base Address of memory-mapped space.

Reset: Host system Reset or D3->D0 transition

Bit	Access & Default	Description
31:12	R/W 00000h	**Base Address (BAR):** This Memory-mapped I/O BAR field provides address signals 31:12.
11:4	RO 00h	Reserved
3	RO 0b	**Prefetchable (PF):** This bit is hardwired to 0 Indicating that this range is not pre-fetchable.
2:1	RO 00b	**Type (TP):** This bit is hardwired to 00 Indicating that this range can be mapped anywhere in 32-bit address space
0	RO 0b	**Resource Type Indicator (RTE):** This bit is hardwired to 0 Indicating a request for register memory space.

9.4.11 SS—Sub System Identifiers

B/D/F/Type: 0/3/3/PCI
Address Offset: 2C–2Fh
Default Value: 00008086h
Access: R/WO
Size: 32 bits

These registers are used to uniquely identify the add-in card or the subsystem that the device resides within.

Reset: Host system Reset.

Bit	Access & Default	Description
31:16	R/WO 0000h	**Subsystem ID (SSID):** This field is written by BIOS. No hardware action taken on this value
15:0	R/WO 8086h	**Subsystem Vendor ID (SSVID):** This field is written by BIOS. No hardware action taken on this value

9.4.12 EROM—Expansion ROM Base Address

B/D/F/Type: 0/3/3/PCI
Address Offset: 30–33h
Default Value: 00000000h
Access: RO
Size: 32 bits

This optional register is not implemented.

Bit	Access & Default	Description
31:11	RO 000000h	**Expansion ROM Base Address (ERBAR):**
10:1	RO 000h	Reserved
0	RO 0b	**Enable (EN):** This bit enables expansion ROM Access.

9.4.13 CAP—Capabilities Pointer

B/D/F/Type: 0/3/3/PCI
Address Offset: 34h
Default Value: C8h
Access: RO
Size: 8 bits

This optional register is used to point to a linked list of new capabilities implemented by the device.

Bit	Access & Default	Description
7:0	RO C8h	**Capability Pointer (CP):** This field indicates that the first capability pointer offset is offset C8h (the power management capability).

9.4.14 INTR—Interrupt Information

B/D/F/Type: 0/3/3/PCI
Address Offset: 3C–3Dh
Default Value: 0200h
Access: R/W, RO
Size: 16 bits

Reset: Host System Reset or D3->D0 reset of the function.

Bit	Access & Default	Description
15:8	RO 02h	**Interrupt Pin (IPIN):** A value of 1h/2h/3h/4h indicates that this function implements legacy interrupt on INTA/INTB/INTC/INTD, respectively **Function** **Value** **INTx** (3 KT/Serial Port) 02h INTB
7:0	R/W 00h	**Interrupt Line (ILINE):** The value written in this register indicates which input of the system interrupt controller the device's interrupt pin is connected. This value is used by the OS and the device driver, and has no affect on the (G)MCH.

9.4.15 MGNT—Minimum Grant

B/D/F/Type: 0/3/3/PCI
Address Offset: 3Eh
Default Value: 00h
Access: RO
Size: 8 bits

This optional register is not implemented.

Bit	Access & Default	Description
7:0	RO 00h	Reserved

9.4.16 MLAT—Maximum Latency

B/D/F/Type: 0/3/3/PCI
Address Offset: 3Fh
Default Value: 00h
Access: RO
Size: 8 bits

This optional register is not implemented.

Bit	Access & Default	Description
7:0	RO 00h	Reserved

9.4.17 PID—PCI Power Management Capability ID

B/D/F/Type: 0/3/3/PCI
Address Offset: C8–C9h
Default Value: D001h
Access: RO
Size: 16 bits

Bit	Access & Default	Description
15:8	RO D0h	**Next Capability (NEXT):** The value of D0h points to the MSI capability.
7:0	RO 01h	**Cap ID (CID):** This field indicates that this pointer is a PCI power management.

9.4.18 PC—PCI Power Management Capabilities

B/D/F/Type: 0/3/3/PCI
Address Offset: CA–CBh
Default Value: 0023h
Access: RO
Size: 16 bits

This register implements the power management capabilities of the function.

Bit	Access & Default	Description
15:11	RO 00000b	**PME Support (PME):** This field indicates no PME# in the PT function.
10	RO 0b	**D2 Support (D2S):** The D2 state is not Supported.
9	RO 0b	**D1 Support (D1S):** The D1 state is not supported.
8:6	RO 000b	**Aux Current (AUXC):** PME# from D3 (cold) state is not supported' therefore this field is 000b.
5	RO 1b	**Device Specific Initialization (DSI):** This bit indicates that no device-specific initialization is required.
4	RO 0b	Reserved
3	RO 0b	**PME Clock (PMEC):** This bit indicates that PCI clock is not required to generate PME#.
2:0	RO 011b	**Version (VS):** This field indicates support for revision 1.2 of the PCI power management specification.

9.4.19 PMCS—PCI Power Management Control and Status

B/D/F/Type:	0/3/3/PCI
Address Offset:	CC–CFh
Default Value:	00000000h
Access:	RO, R/W, RO/V
Size:	32 bits
BIOS Optimal Default	0000h

This register implements the PCI PM Control and Status Register to allow PM state transitions and Wake up.

Note: NSR bit of this register. All registers (PCI configuration and Device Specific) marked with D3->D0 transition reset will only do so if this bit reads a 0. If this bit is a 1, the D3->D0 transition will not reset the registers.

Reset: Host System Reset or D3->D0 transition.

Bit	Access & Default	Description
31:16	RO 0h	Reserved
15	RO 0b	**PME Status (PMES):** This bit is set when a PME event is to be requested. Not supported.
14:9	RO 00h	Reserved
8	RO 0b	**PME Enable (PMEE):** Not Supported
7:2	RO 0h	Reserved
1:0	R/W 00b	**Power State (PS):** This field is used both to determine the current power state of the PT function and to set a new power state. The values are: 00 = D0 state 11 = $D3_{HOT}$ state When in the $D3_{HOT}$ state, the controller's configuration space is available, but the I/O and memory spaces are not. Additionally, interrupts are blocked. If software attempts to write a 10 or 01 to these bits, the write will be ignored.

9.4.20 MID—Message Signaled Interrupt Capability ID

B/D/F/Type: 0/3/3/PCI
Address Offset: D0–D1h
Default Value: 0005h
Access: RO
Size: 16 bits

Message Signaled Interrupt is a feature that allows the device/function to generate an interrupt to the host by performing a DWord memory write to a system specified address with system specified data. This register is used to identify and configure an MSI capable device.

Bit	Access & Default	Description
15:8	RO 00h	**Next Pointer (NEXT):** This value indicates this is the last item in the list.
7:0	RO 05h	**Capability ID (CID):** The value of Capabilities ID indicates device is capable of generating MSI

9.4.21 MC—Message Signaled Interrupt Message Control

B/D/F/Type: 0/3/3/PCI
Address Offset: D2–D3h
Default Value: 0080h
Access: RO, R/W
Size: 16 bits

This register provides System Software control over MSI.

Reset: Host System Reset or D3->D0 transition.

Bit	Access & Default	Description
15:8	RO 00h	Reserved
7	RO 1b	**64 Bit Address Capable (C64):** This field indicates the capable of generating 64-bit and 32-bit messages
6:4	R/W 000b	**Multiple Message Enable (MME):** These bits are R/W for software compatibility, but only one message is ever sent by the PT function.
3:1	RO 000b	**Multiple Message Capable (MMC):** Only one message is required.
0	R/W 0b	**MSI Enable (MSIE):** If set, MSI is enabled and traditional interrupt pins are not used to generate interrupts. 0 = Disable 1 = Enable

9.4.22 MA—Message Signaled Interrupt Message Address

B/D/F/Type: 0/3/3/PCI
Address Offset: D4–D7h
Default Value: 00000000h
Access: RO, R/W
Size: 32 bits

This register specifies the DWord aligned address programmed by system software for sending MSI.

This register is reset by a Host system Reset or D3->D0 transition.

Bit	Access & Default	Description
31:2	R/W 00000000 h	**Address (ADDR):** This field indicates the lower 32 bits of the system specified message address, always DWORD aligned
1:0	RO 00b	Reserved

9.4.23 MAU—Message Signaled Interrupt Message Upper Address

B/D/F/Type: 0/3/3/PCI
Address Offset: D8–DBh
Default Value: 00000000h
Access: RO, R/W
Size: 32 bits

This register provides the upper 32 bits of the message address for the 64-bit address capable device.

Reset: Host system Reset or D3->D0 transition.

Bit	Access & Default	Description
31:4	RO 0000000h	Reserved
3:0	R/W 0000b	**Address (ADDR):** This field indicates the upper 4 bits of the system specified message address.

9.4.24 MD—Message Signaled Interrupt Message Data

B/D/F/Type: 0/3/3/PCI
Address Offset: DC–DDh
Default Value: 0000h
Access: R/W
Size: 16 bits

This 16-bit field is programmed by system software if MSI is enabled.

Reset: Host system Reset or D3->D0 transition.

Bit	Access & Default	Description
15:0	R/W 0000h	**Data (DATA):** This MSI data is driven onto the lower word of the data bus of the MSI memory write transaction.

§

10 Functional Description

This chapter describes the (G)MCH interfaces and major functional units.

10.1 Host Interface

The (G)MCH supports the Core™2 Duo desktop processor, Pentium® D processor, Pentium 4 processor subset of the Enhanced Mode Scaleable Bus. The cache line size is 64 bytes. Source synchronous transfer is used for the address and data signals. The address signals are double pumped; a new address can be generated every other bus clock. At 133/200/266 MHz bus clock, the address signals run at 266/400/533 MT/s. The data is quad pumped, and an entire 64B cache line can be transferred in two bus clocks. At 133/200/266 MHz bus clock, the data signals run at 533/800/1066 MT/s.

10.1.1 FSB IOQ Depth

The Scalable Bus supports up to 12 simultaneous outstanding transactions.

10.1.2 FSB OOQ Depth

The (G)MCH supports only one outstanding deferred transaction on the FSB.

10.1.3 FSB GTL+ Termination

The (G)MCH integrates GTL+ termination resistors on die. Also, approximately 2.8 pF (fast) – 3.3 pF (slow) per pad of on die capacitance is implemented to provide better FSB electrical performance.

10.1.4 FSB Dynamic Bus Inversion

The (G)MCH supports Dynamic Bus Inversion (DBI) when driving and when receiving data from the processor. DBI limits the number of data signals that are driven to a low voltage on each quad pumped data phase. This decreases the worst-case power consumption of the (G)MCH. HDINV[3:0]# indicate if the corresponding 16 bits of data are inverted on the bus for each quad pumped data phase.

HDINV[3:0]#	Data Bits
HDINV0#	HD[15:0]#
HDINV1#	HD[31:16]#
HDINV2#	HD[47:32]#
HDINV3#	HD[63:48]#

When the processor or the (G)MCH drive data, each 16-bit segment is analyzed. If more than 8 of the 16 signals would normally be driven low on the bus, the corresponding HDINVx# signal will be asserted, and the data will be inverted prior to being driven on the bus. When the processor or the (G)MCH receives data, it monitors HDINV[3:0]# to determine if the corresponding data segment should be inverted.

10.1.4.1 APIC Cluster Mode Support

APIC Cluster mode support is required for backwards compatibility with existing software, including various Operating systems. As one example, with Microsoft Windows 2000, there is a mode (boot.ini) that allows an end user to enable the use of cluster addressing support of the APIC.

- The (G)MCH supports three types of interrupt re-direction:
  - Physical
  - Flat-Logical
  - Clustered-Logical

10.2 System Memory Controller

The (G)MCH integrates a system memory DDR2 controller with two, 64-bit wide interfaces. Only Double Data Rate (DDR2) memory is supported; consequently, the buffers support only SSTL_1.8 V signal interfaces. The memory controller interface is fully configurable through a set of control registers. Rules for populating DIMM slots are included in this chapter.

Note: References to DDR2-800 apply to the 82Q965, 82G965, 82P965 (G)MCH only. The 82Q963 does not support DDR2-800.

The system memory controller supports two styles of memory organization (Interleaved and Asymmetric). Table 10-1 and Table 10-2 show example memory organizations.

Table 10-1. Sample System Memory Organization with Interleaved Channels

	Channel A population	Cumulative top address in Channel A	Channel B population	Cumulative top address in Channel B
Rank 3	0 MB	2560 MB	0 MB	2560 MB
Rank 2	256 MB	2560 MB	256 MB	2560 MB
Rank 1	512 MB	2048 MB	512 MB	2048 MB
Rank 0	512 MB	1024 MB	512 MB	1024 MB

Table 10-2. Sample System Memory Organization with Asymmetric Channels

	Channel A population	Cumulative top address in Channel A	Channel B population	Cumulative top address in Channel B
Rank 3	0 MB	1280 MB	0 MB	2560 MB
Rank 2	256 MB	1280 MB	256 MB	2560 MB
Rank 1	512 MB	1024 MB	512 MB	2304 MB
Rank 0	512 MB	512 MB	512 MB	1792 MB

Interleaved Mode

This mode provides maximum performance on real applications. Addresses are bounced between the channels, and the switch happens after each cache line (64 byte boundary). If two consecutive cache lines are requested, both may be retrieved simultaneously, since they are ensured to be on opposite channels. The drawback of Interleaved Mode is that the system designer must populate both channels of memory such that they have equal capacity, but the technology and device width may vary from one channel to the other.

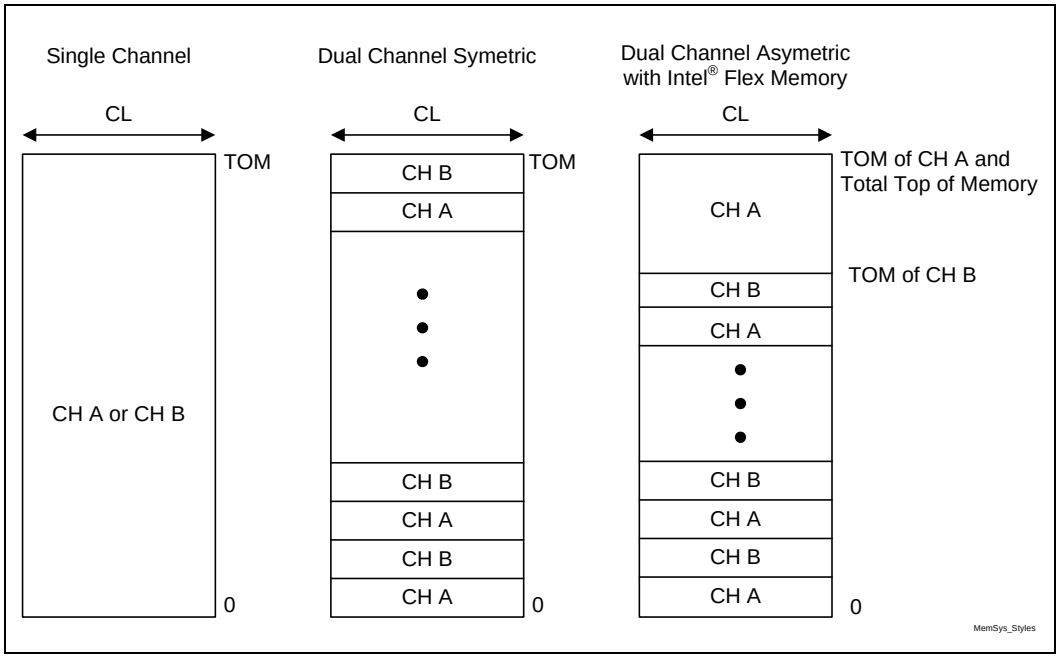
Asymmetric Mode

This mode trades performance for system design flexibility. Unlike the previous mode, addresses start in channel A and stay there until the end of the highest rank in channel A, then addresses continue from the bottom of channel B to the top. Real world applications are unlikely to make requests that alternate between addresses that sit on opposite channels with this memory organization, so in most cases, bandwidth will be limited to that of a single channel. The system designer can populate or not to populate any rank on either channel, including either degenerate single channel case.

Flex Mode

This mode provides the best performance flexibility. The lowest DRAM memory is mapped to two channel operation and the topmost , if any, DRAM memory is mapped to single channel operation. The drawback of Flex mode is that the system designer must populate both channels of memory to get the benefits of flex mode, and there will be multiple zones of dual/single channel operation across the whole of DRAM memory.

Figure 10-1. System Memory Styles



10.2.1 DRAM Technologies and Organization

This section provides information on currently supported DRAM technologies. The following terminology is used:

Single sided	A logical term referring to the number of chip selects attached to the DIMM. A physical DIMM may have the components on both sides of the substrate, but be logically indistinguishable from a single-sided DIMM with all devices on one side, if all components on the DIMM are attached to the same chip select signal.
x8	Each component has 8 data lines.
x16	ECh component has 16 data lines.

All standard 256-Mb, 512-Mb, and 1-Gb technologies and addressing are supported for x16 and x8 devices.

For DDR2
- 533 (PC2 4300)
  - Non-ECC
    - Version A = Single sided x8
    - Version B = Double sided x8
    - Version C = Single sided x16
- 667 (PC2 5300)
  - Non-ECC
    - Version C = Single sided x16
    - Version D = Single sided x8
    - Version E = Double sided x8
- 800 (PC2 6400)
  - Non-ECC
    - Version C = Single sided x16
    - Version D = Single sided x8
    - Version E = Double sided x8

No support for DIMMs with different technologies or capacities on opposite sides of the same DIMM. If one side of a DIMM is populated, the other side is either identical or empty.

Supported components include:

For DDR2 at 533 (PC2 4300) and 667 (PC2 5300)
- 256-Mb technology
  - 32-M cells x8 data bits/cell
    - 1-K columns
    - 4 banks
    - 8-K rows
    - Each component has a 1-KB page.
    - One DIMM has 8 components resulting in an 8-KB page.
    - The capacity of one rank is 256 MB.
  - 16-M cells x16 data bits/cell
    - 512 columns
    - 4 banks
    - 8-K rows
    - Each component has a 1-KB page.
    - One DIMM has 4 components resulting in a 4-KB page.
    - The capacity of one rank is 128 MB.
- 512-Mb technology
  - 64-M cells x8 data bits/cell
    - 1K columns
    - 4 banks
    - 16K rows
    - Each component has a 1-KB page.
    - One DIMM has 8 components resulting in an 8-KB page.
    - The capacity of one rank is 512 MB.
  - 32-M cells x16 data bits/cell
    - 1-K columns
    - 4 banks
    - 8-K rows
    - Each component has a 2-KB page.
    - One DIMM has 4 components resulting in an 8-KB page.
    - The capacity of one rank is 256 MB.
- 1-Gb technology
  - 128-M cells x8 data bits/cell
    - 1-K columns
    - 8 banks
    - 16-K rows
    - Each component has a 1-KB page.
    - One DIMM has 8 components resulting in an 8-KB page.
    - The capacity of one rank is 1 GB.
  - 64-M cells x16 data bits/cell
    - 1-K columns
    - 8 banks
    - 8-K rows
    - Each component has a 2-KB page.
    - One DIMM has 4 components resulting in an 8-KB page.
    - The capacity of one rank is 512 MB.

Note: 800MHz 1Gb technology is not supported

Note: The (G)MCH does not support system memory frequencies that exceed the frequency of the Front Side Bus (FSB). If memory with higher frequency capabilities than that of the FSB is populated, the memory will be under-clocked to align with the FSB.

The DRAM sub-system supports single or dual channels, 64b wide per channel. A maximum of 4 ranks can be populated (2 Double Sided DIMMs) per channel. Mixed mode DDR DS-DIMMs (x8 and x16 on the same DIMM) are not supported (not validated).

By using 1Gb technology, the largest memory capacity is 8 GB (16K rows * 1K columns * 1 cell/(row * column) * 8 b/cell * 8 banks/device * 8 devices/rank * 4 ranks/channel * 2 channel *1M/(K*K) * 1G/1024M * 1B/8b = 8 GB). Using 8 GB of memory is only possible in Interleaved mode with all ranks populated at maximum capacity.

By using 256Mb technology, the smallest memory capacity is 128 MB (8K rows * 512 columns * 1 cell/(row * column) * 16b/cell * 4 banks/device * 4 devices/rank * 1 rank * 1M/1024K * 1B/8b = 128 MB).

10.2.1.1 Rules for Populating DIMM Slots

In all modes, the frequency of system memory will be the lowest frequency of all of the DIMMs in the system, as determined through the SPD registers on the DIMMs.

In Single Channel mode, any DIMM slot within the channel may be populated in any order. Either channel may be used. To save power, do not populate the unused channel.

In Dual Channel Asymmetric mode, any DIMM slot may be populated in any order.

In Dual Channel Interleaved mode, any DIMM slot may be populated in any order, but the total memory in each channel must be the same.

In Flex memory mode, any DIMM slot may be populated in any order per channel, but each channel must have at least 1 DIMM. The matching amount of memory per channel will be run in Dual channel interleaved mode and the remaining unmatched memory will run in Asymmetric mode.

10.2.1.2 System Memory Supported Configurations

The (G)MCH supports the 256 Mbit, 512 Mbit and 1 Gbit technology based DIMMs listed in Table 10-3.

Table 10-3. DDR2 DIMM Supported Configurations

Technology	Configuration	# of Row Address Bits	# of Column Address Bits	# of Bank Address Bits	Page Size	Rank Size
256Mbit	16M X 16	13	9	2	4K	128 MB
256Mbit	32M X 8	13	10	2	8K	256 MB
512Mbit	32M X 16	13	10	2	8K	256 MB
512Mbit	64M X 8	14	10	2	8K	512 MB
1Gbit	128M X 8	14	10	3	8K	1 GB

NOTE: The (G)MCH has a minimum total memory requirement of 256 MB.

10.2.1.3 Main Memory DRAM Address Translation and Decoding

Table 10-4 and Table 10-5 specify the host interface to memory interface address multiplex for the (G)MCH. Refer to the details of the various DIMM configurations as described in Table 10-3.

Table 10-4. DRAM Address Translation (Single Channel / Dual Asymmetric Mode)

Technology (Mb)	256	256	512	512	1024	1024
Row bits	13	13	14	13	14	13
Column bits	10	9	10	10	10	10
Bank bits	2	2	2	2	3	3
Width (b)	8	16	8	16	8	16
Rows	8192	8192	16384	8192	16384	8192
Columns	1024	512	1024	1024	1024	1024
Banks	4	4	4	4	8	8
Page Size (KB)	8	4	8	8	8	8
Devices per rank	8	4	8	4	8	4
Rank Size (MB)	256	128	512	256	1024	512
Depth (M)	32	16	64	32	128	64
Addr bits [n:0]	27	26	28	27	29	28
Available in DDR2	yes	yes	yes	yes	yes	yes
Host Address bit	Memory Address bit					
32	—	—	—	—	—	—
31	—	—	—	—	—	—
30	—	—	—	—	—	—
29	—	—	—	—	r 13	—
28	—	—	r 13	—	r 11	r 11
27	r 12	-	r 12	r 12	r 12	r 12
26	r 10	r 10	r 10	r 10	r 10	r 10
25	r 9	r 9	r 9	r 9	r 9	r 9
24	r 8	r 8	r 8	r 8	r 8	r 8
23	r 7	r 7	r 7	r 7	r 7	r 7
22	r 6	r 6	r 6	r 6	r 6	r 6
21	r 5	r 5	r 5	r 5	r 5	r 5
20	r 4	r 4	r 4	r 4	r 4	r 4
19	r 3	r 3	r 3	r 3	r 3	r 3
18	r 2	r 2	r 2	r 2	r 2	r 2
17	r 1	r 1	r 1	r 1	r 1	r 1
16	r 0	r 0	r 0	r 0	r 0	r 0
15	r 11	r 11	r 11	r 11	b 0	b 0
14	b 1	r 12	b 1	b 1	b 1	b 1
13	b 0	b 0	b 0	b 0	b 2	b 2
12	c 9	b 1	c 9	c 9	c 9	c 9
11	c 8	c 8	c 8	c 8	c 8	c 8
10	c 7	c 7	c 7	c 7	c 7	c 7
9	c 6	c 6	c 6	c 6	c 6	c 6
8	c 5	c 5	c 5	c 5	c 5	c 5
7	c 4	c 4	c 4	c 4	c 4	c 4
6	c 3	c 3	c 3	c 3	c 3	c 3
5	c 2	c 2	c 2	c 2	c 2	c 2
4	c 1	c 1	c 1	c 1	c 1	c 1
3	c 0	c 0	c 0	c 0	c 0	c 0

Table 10-5. DRAM Address Translation (Dual Channel Symmetric Mode)

Technology (Mb)	256	256	512	512	1024	1024
Row bits	13	13	14	13	14	13
Column bits	10	9	10	10	10	10
Bank bits	2	2	2	2	3	3
Width (b)	8	16	8	16	8	16
Rows	8192	8192	16384	8192	16384	8192
Columns	1024	512	1024	1024	1024	1024
Banks	4	4	4	4	8	8
Page Size (KB)	8	4	8	8	8	8
Devices per rank	8	4	8	4	8	4
Rank Size (MB)	256	128	512	256	1024	512
Depth (M)	32	16	64	32	128	64
Addr bits [n:0]	27	26	28	27	29	28
Available in DDR2	yes	yes	yes	yes	yes	yes
Host Address bit	Memory Address bit					
32	—	—	—	—	—	—
31	—	—	—	—	—	—
30	—	—	—	—	r 13	—
29	—	—	r 13	—	r 11	r 11
28	r 12	-	r 12	r 12	r 12	r 12
27	r 10	r 10	r 10	r 10	r 10	r 10
26	r 9	r 9	r 9	r 9	r 9	r 9
25	r 8	r 8	r 8	r 8	r 8	r 8
24	r 7	r 7	r 7	r 7	r 7	r 7
23	r 6	r 6	r 6	r 6	r 6	r 6
22	r 5	r 5	r 5	r 5	r 5	r 5
21	r 4	r 4	r 4	r 4	r 4	r 4
20	r 3	r 3	r 3	r 3	r 3	r 3
19	r 2	r 2	r 2	r 2	r 2	r 2
18	r 1	r 1	r 1	r 1	r 1	r 1
17	r 0	r 0	r 0	r 0	r 0	r 0
16	r 11	r 11	r 11	r 11	b 0	b 0
15	b 1	r 12	b 1	b 1	b 1	b 1
14	b 0	b 0	b 0	b 0	b 2	b 2
13	c 9	b 1	c 9	c 9	c 9	c 9
12	c 8	c 8	c 8	c 8	c 8	c 8
11	c 7	c 7	c 7	c 7	c 7	c 7
10	c 6	c 6	c 6	c 6	c 6	c 6
9	c 5	c 5	c 5	c 5	c 5	c 5
8	c 4	c 4	c 4	c 4	c 4	c 4
7	c 3	c 3	c 3	c 3	c 3	c 3
6	h	h	h	h	h	h
5	c 2	c 2	c 2	c 2	c 2	c 2
4	c 1	c 1	c 1	c 1	c 1	c 1
3	c 0	c 0	c 0	c 0	c 0	c 0

10.2.2 Memory Detection and Initialization

See your Intel representative for the latest BIOS information.

10.2.3 DRAM Clock Generation

The (G)MCH generates three differential clock pairs for every supported DIMM. A total of 6 clock pairs are driven directly by the (G)MCH to 2 DIMMs per channel.

10.2.4 Suspend to RAM and Resume

When entering the Suspend to RAM (STR) state, the SDRAM controller will flush pending cycles and then enter all SDRAM rows into self refresh. In STR, the CKE signals remain LOW so the SDRAM devices will perform self-refresh.

10.2.5 DDR2 On-Die Termination

On-die termination (ODT) is a feature that allows a DRAM to turn on/off internal termination resistance for each DQ, DM, DQS, and DQS# signal for x8 and x16 configurations via the ODT control signals. The ODT feature is designed to improve signal integrity of the memory channel by allowing the termination resistance for the DQ, DM, DQS, and DQS# signals to be located inside the DRAM devices themselves instead of on the motherboard. The (G)MCH drives out the required ODT signals, based on memory configuration and which rank is being written to or read from, to the DRAM devices on a targeted DIMM rank to enable or disable their termination resistance.

10.3 PCI Express* (Intel® 82Q965, 82G965, 82P965 (G)MCH)

See Chapter 1 for a list of PCI Express features, and the PCI Express specification for further details.

This (G)MCH is part of a PCI Express root complex. This means it connects a host processor/memory subsystem to a PCI Express hierarchy. The control registers for this functionality are located in device 1 configuration space and two Root Complex Register Blocks (RCRBs). The DMI RCRB contains registers for control of the Intel ICH8 attach ports.

The PCI Express architecture is specified in layers. Compatibility with the PCI addressing model (a load-store architecture with a flat address space) is maintained to ensure that all existing applications and drivers operate unchanged. The PCI Express configuration uses standard mechanisms as defined in the PCI Plug-and-Play specification. The initial speed of 1.25 GHz (250 MHz internally) results in 2.5 Gb/s/direction; this provides a 250 MB/s communications channel in each direction (500 MB/s total). That is close to twice the data rate of classic PCI per lane.

10.3.1 Transaction Layer

The upper layer of the PCI Express architecture is the Transaction Layer. The Transaction Layer's primary responsibility is the assembly and disassembly of Transaction Layer Packets (TLPs). TLPs are used to communicate transactions, such as read and write, as well as certain types of events. The Transaction Layer also manages flow control of TLPs.

10.3.2 Data Link Layer

The middle layer in the PCI Express stack, the Data Link Layer, serves as an intermediate stage between the Transaction Layer and the Physical Layer. Responsibilities of Data Link Layer include link management, error detection, and error correction.

10.3.3 Physical Layer

The Physical Layer includes all circuitry for interface operation, including driver and input buffers, parallel-to-serial and serial-to-parallel conversion, PLL(s), and impedance matching circuitry.

10.4 Intel® Serial Digital Video Output (SDVO) (Intel® 82Q965, 82Q963, 82G965 GMCH Only)

The SDVO signals on the 82Q965 and 82G965 GMCH are multiplexed with the PCI Express x16 port pins. The SDVO signals on the 82Q963 GMCH are not multiplexed. The Intel® SDVO port is the second generation of digital video output from compliant Intel (G)MCHs. The electrical interface is based on the PCI Express interface, though the protocol and timings are completely unique. Whereas PCI Express runs at a fixed frequency, the frequency of the SDVO interface is dependant upon the active display resolution and timing. The port can be dynamically configured in several modes to support display configurations.

Essentially, an SDVO port transmits display data in a high speed, serial format across differential AC coupled signals. An SDVO port consists of a sideband differential clock pair and a number of differential data pairs.

10.4.1 Intel® SDVO Capabilities

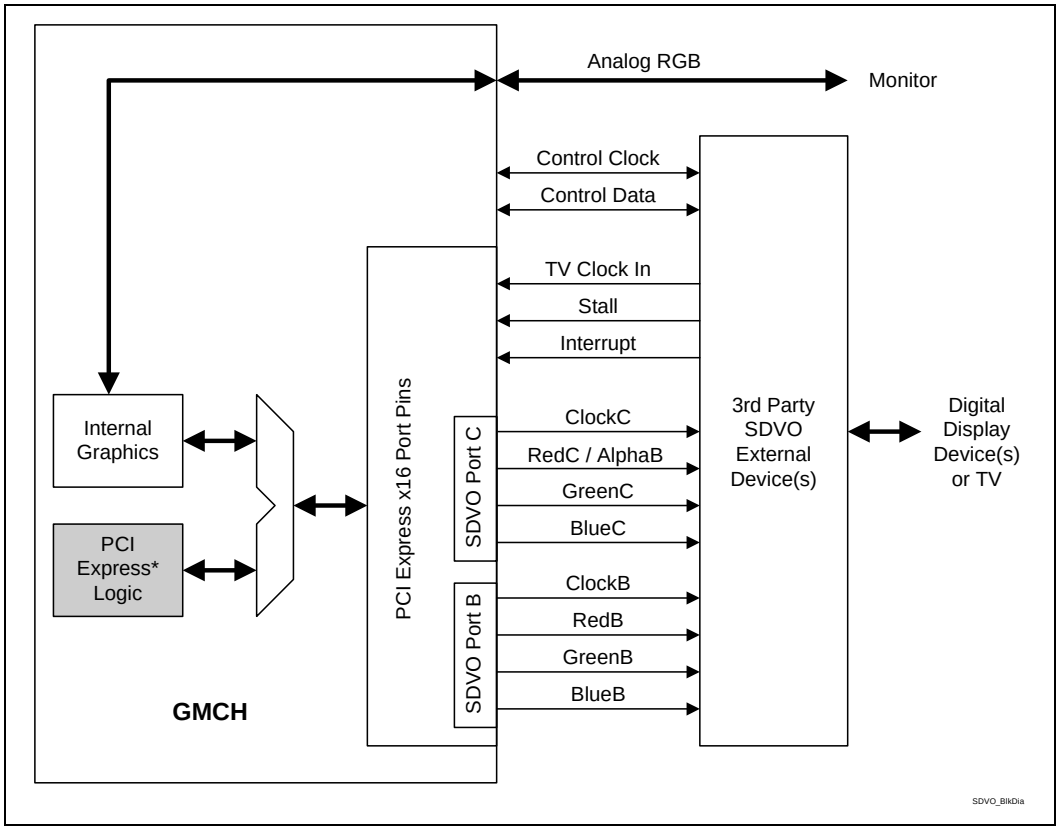
SDVO ports can support a variety of display types including LVDS, DVI, Analog CRT, TV-Out and external CE type devices. The (G)MCH utilizes an external SDVO device to translate from SDVO protocol and timings to the desired display format and timings.

The Internal Graphics Controller can have one or two SDVO ports multiplexed on the x16 PCI Express interface. When an external x16 PCI Express graphics accelerator is not in use, an ADD2 card may be plugged into the x16 connector or if a x16 slot is not present, the SDVO(s) may be located 'down' on the motherboard to access the multiplexed SDVO ports and provide a variety of digital display options.

The ADD2/Media Expansion card is designed to fit in a x16 PCI Express connector. The ADD2/Media Expansion card can support one or two devices. If a single channel SDVO device is utilized, it should be attached to the channel B SDVO pins. The ADD2 card can support two separate SDVO devices when the interface is in Dual Independent or Dual Simultaneous Standard modes. The Media Expansion card adds Video in capabilities.

The SDVO port defines a two-wire point-to-point communication path between the SDVO device and (G)MCH. The SDVO control clock and data provide similar functionality to I^2C. However unlike I^2C, this interface is intended to be point-to-point (from the (G)MCH to the SDVO device) and will require the SDVO device to act as a switch and direct traffic from the SDVO control bus to the appropriate receiver. Additionally, this control bus will be able to run at faster speeds (up to 1 MHz) than a traditional I^2C interface.

Figure 10-2. SDVO Conceptual Block Diagram



10.4.2 Intel® SDVO Modes

The port can be dynamically configured in several modes:

- **Standard.** This mode provides baseline SDVO functionality. It supports pixel rates between 25 MP/s and 270 MP/s. It uses three data pairs to transfer RGB data.
- **Dual Standard.** This mode uses Standard data streams across both SDVOB and SDVOC. Both channels can only run in Standard mode (3 data pairs) and each channel supports pixel rates between 25 MP/s and 270 MP/s.
  - Dual Independent Standard. In Dual Independent Standard mode, each SDVO channel sees a different pixel stream. The data stream across SDVOB is not the same as the data stream across SDVOC.
  - Dual Simultaneous Standard. In Dual Simultaneous Standard mode, both SDVO channels see the same pixel stream. The data stream across SDVOB is the same as the data stream across SDVOC. The display timings will be identical; however, the transfer timings may not be identical (i.e., SDVOB clocks and data may not be perfectly aligned with SDVOC clock and data as seen at the SDVO device). Since this mode uses just a single data stream, it uses a single pixel pipeline within the GMCH.

10.4.3 PCI Express* and Internal Graphics Simultaneous Operation (Intel® 82Q965, 82G965 Only)

10.4.3.1 Standard PCI Express* Cards and Internal Graphics

BIOS control of simultaneous operation is needed to ensure the PCI Express is configured appropriately.

10.4.3.2 Media Expansion Cards (Concurrent SDVO and PCI Express*)

The GMCH supports SDVO lane reversal. This functionality allows current SDVO ADD2 cards to work in current ATX and BTX systems instead of requiring a separate card. The GMCH allows SDVO and PCI Express to operate concurrently on the PCI Express port. The card that plugs into the x16 connector in this case is called a Media Expansion card (MEC). It uses 4 or 8 lanes for SDVO and up to 8 lanes of standard PCI Express.

Note: The only supported PCI Express width, when SDVO is present, is x1.

This concurrency is supported in reversed and non-reversed configurations. Mirroring / Reversing is always about the axis.

Table 10-6. Concurrent SDVO / PCI Express* Configuration Strap Controls

Config #	Description	Slot Reversed Strap	SDVO Present Strap	SDVO/PCI Express* Concurrent Strap
1	PCI Express* not reversed	—	—	—
2	PCI Express* Reversed	Yes	—	—
3	SDVO (ADD2) not reversed	—	Yes	—
4	SDVO (ADD2) Reversed	Yes	Yes	—
5	SDVO & PCI Express* (Media Expansion) not reversed	—	Yes	Yes
6	SDVO & PCI Express* (Media Expansion) Reversed	Yes	Yes	Yes

NOTES:
1. The Configuration #s refer to the following figures (no intentional relation to validation configurations).
2. Configurations 4, 5, and 6 (required addition of SDVO/PCI Express* Concurrent Strap).

Figure 10-3. Concurrent SDVO / PCI Express* Non-Reversed Configurations

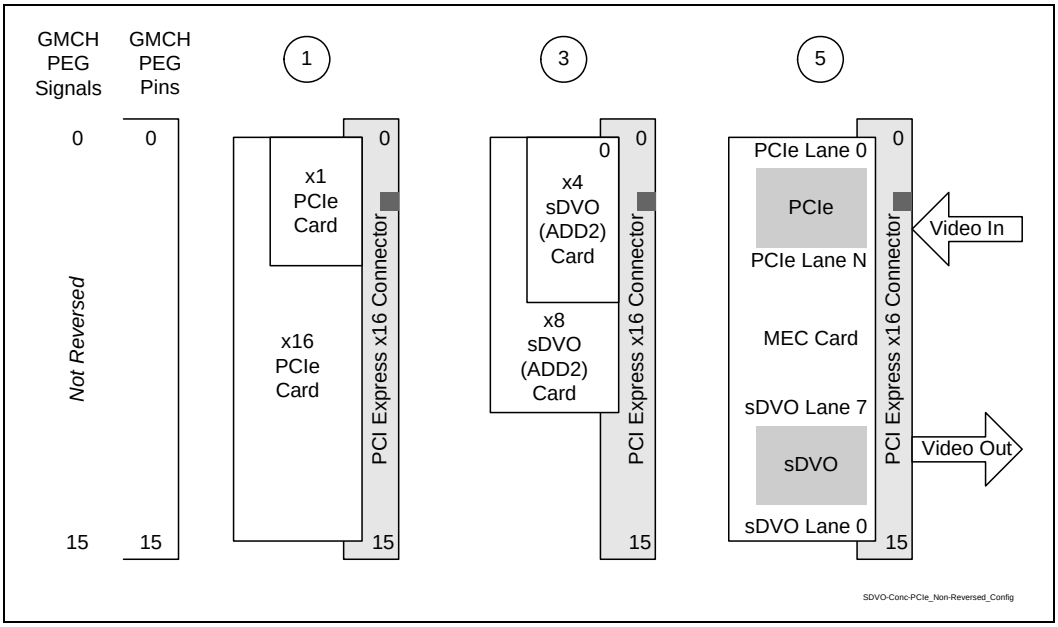
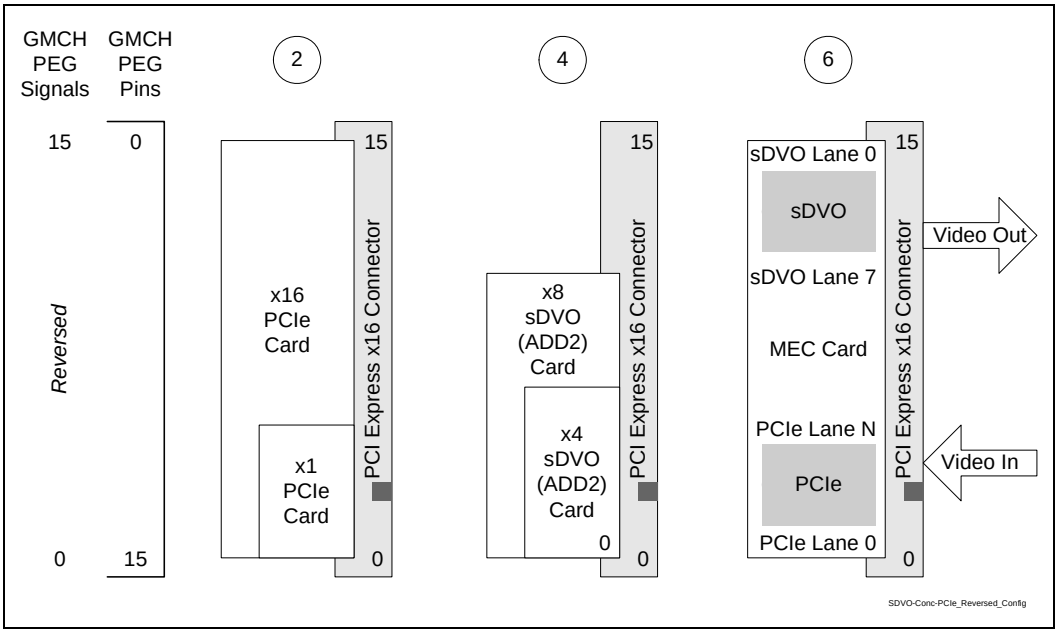


Figure 10-4. Concurrent SDVO / PCI Express* Reversed Configurations



10.5 Integrated Graphics Device (IGD) (Intel® 82Q965, 82Q963, 82G965 GMCH Only)

The 82Q965, 82Q963, 82G965 GMCHs provide a highly integrated graphics accelerator that allows for a flexible Integrated System Graphics solution. High bandwidth access to data is provided through the graphics and system memory ports. The GMCH can access graphics data located in system memory at up to 12.6 GB/s (depending on memory configuration). The GMCH can drive an integrated DAC, and/or two SDVO ports (multiplexed with PCI Express on the 82Q965 and 82G965 GMCH); with the SDVO ports capable of driving an ADD2/Media Expansion card. The external SDVO devices can drive a variety of connections (e.g., TV-Out, TMDS, and LVDS transmitters).

10.5.1 Overview

With the evolution of PC graphics from fixed function parallelizable pipelines to generalized programmable parallel engines, the Internal Graphics Device delivers a highly programmable graphics device capable of rendering 3D, 2D, and video content.

Graphics workloads like 3D, imaging, and video encode/decode are all good examples of parallel applications. The programmable graphics architecture in the GMCH allows the ability for the driver to program the graphics device to operate on parallel workloads in a parallel manor.

10.5.1.1 3D Graphics

The 82G965 GMCH graphics engine supports acceleration for all DX9.0c/DX10 and OGL 1.5 required features and other additional features. Some of the key features supported are:

- Vertex Shader Model 3.0 (HW)
- Hardware Pixel Shader 3.0
- 32-bit and 16-bit Full Precision Floating Point Operations
- Up to 8 Multiple Render Targets (MRTs)
- Occlusion Query
- 128-bit Floating Point Texture Formats
- Bilinear, Trilinear, and Anisotropic MipMap Filtering
- Shadow Maps and Double Sided Stencils

The 82Q965 and 82Q963 GMCH graphics engine supports DX9.0c and OGL 1.4 plus extensions as well as the following:

- Vertex Shader Model 2.0/3.0 (SW Only)
- Hardware Pixel Shader 2.0
- 32-bit and 16-bit Fixed Point Operations
- Up to 8 Multiple Render Targets (MRTs)
- Occlusion Query
- 128-bit Floating Point Texture Formats
- Bilinear, Trilinear, and Anisotropic MipMap Filtering
- Shadow Maps and Double Sided Stencils

The 3D performance of any graphics device is affected by several key factors: memory bandwidth, and numbers of pixels per clock. The 82Q965, 82Q963, and 82G965 GMCH graphic's capability addresses all of these potential bottlenecks by sharing the two channels of memory bandwidth that allows for up to 12.6 GB/s, and the ability to operate on 4 pixels per clock

10.5.1.2 Video Playback — Deinterlacing Support

For display on a progressive computer monitor, interlaced data that has been formatted for display on interlaced monitors (TV), needs to be de-interlaced. The simple approaches to de-interlacing create unwanted display artifacts. More advanced de-interlacing techniques have been developed to provide a high quality, effective solution. The Motion Adaptive Deinterlacing supported in the GMCH greatly reduces the feathering artifacts typical with Weave deinterlacing and the jaggies typically associated to Bob deinterlacing. Clear, sharp text is another benefit on Intel's Motion Adaptive Deinterlacing technique.

10.6 Display Interfaces

The GMCH has three display ports; one analog and two digital. Each port can transmit data according to one or more protocols. The digital ports are connected to an external device that converts one protocol to another. Examples of this are TV encoders, external DACs, LVDS transmitters, and TMDS transmitters. Each display port has control signals that may be used to control, configure and/or determine the capabilities of an external device.

Note: References in this section of multiplexed SDVO ports or PCI Express port apply to the 82Q965 and 82G965 GMCH only. The SDVO ports are dedicated (non-multiplexed) on the 82Q963 GMCH.

The GMCH has one dedicated display port, the analog port. On the 82Q965 and 82G965 GMCH SDVO ports B and C are multiplexed with the PCI Express graphics interface and are not available if an external PCI Express graphics device is in use. When a system uses a PCI Express graphics connector, SDVO ports B and C can be used via an ADD2/Media Expansion (Advanced Digital Display 2) card. Ports B and C can also operate in dual-channel mode, where the data bus is connected to both display ports, allowing a single device to take data at twice the pixel rate.

- The GMCH's analog port uses an integrated 400 MHz RAMDAC that can directly drive a standard progressive scan analog monitor up to a resolution of 2048x1536 pixels with 32-bit color at 75 Hz.
- The GMCH's SDVO ports are each capable of driving a 270-MP pixel rate. Each port is capable of driving a digital display up to 1600x1200 @ 60 Hz. When in dual-channel mode, the GMCH can drive a flat panel up to 2048x1536 @ 75 Hz or dCRT/HDTV up to 1920x1080 @ 85 Hz.

The GMCH is compliant with DVI Specification 1.0. When combined with a DVI compliant external device and connector, the GMCH has a high speed interface to a digital display (e.g., flat panel or digital CRT).

Table 10-7. Display Port Characteristics

		Analog	Digital Port B	Digital Port C
Interface Protocol		RGB DAC	DVO 1.0	DVO 1.0
SIGNALS	HSYNC	Yes Enable/Polarity		
	VSYNC	Yes Enable/Polarity		
	BLANK	No	Yes(1)	Yes(1)
	STALL	No	Yes	Yes
	Field	No	Yes	Yes
	Display_Enable	No		No
Image Aspect Ratio		Programmable and typically 1.33:1 or 1.78:1		
Pixel Aspect Ratio		Square(1)		
Voltage		RGB 0.7 V p-p	PCI Express*	PCI Express
Clock		NA	Differential	
Max Rate		400 Mpixel	270 Mpixel	270 Mpixel
Format		Analog RGB	RGB 8:8:8 YUV 4:4:4	
Control Bus		DDC1/DDC2B	DDC2B	
External Device		No	TMDS/LVDS Transmitter /TV Encoder	
Connector		VGA/DVI-I	DVI/CVBS/S-Video/Component/SCART/HDMI	

NOTES:
1. Single signal software selectable between display enable and Blank#

10.6.1 Analog Display Port Characteristics

The analog display port provides a RGB signal output along with a HSYNC and VSYNC signal. There is an associated DDC signal pair that is implemented using the DDC_CLK and DDC_DATA signals dedicated to the analog port. The intended target device is for a CRT based monitor with a VGA connector. Display devices such as LCD panels with analog inputs may work satisfactory but no functionality has been added to the signals to enhance that capability.

Table 10-8. Analog Port Characteristics

Signal	Port Characteristic	Support
RGB	Voltage Range	0.7 V p-p only
	Monitor Sense	Analog Compare
	Analog Copy Protection	No
	Sync on Green	No
HSYNC VSYNC	Voltage	2.5 V
	Enable/Disable	Port control
	Polarity adjust	VGA or port control
	Composite Sync Support	No
	Special Flat Panel Sync	No
	Stereo Sync	No
DDC	Voltage	Externally buffered to 5 V
	Control	Through GPIO interface

10.6.1.1 Integrated RAMDAC

The display function contains a RAM-based Digital-to-Analog Converter (RAMDAC) that transforms the digital data from the graphics and video subsystems to analog data for the CRT monitor. The GMCH's integrated 400 MHz RAMDAC supports resolutions up to 2048 x 1536 @ 75 Hz. Three 8-bit DACs provide the R, G, and B signals to the monitor.

10.6.1.2 Sync Signals

HSYNC and VSYNC signals are digital and conform to TTL signal levels at the connector. Since these levels cannot be generated internal to the device, external level shifting buffers are required. These signals can be polarity adjusted and individually disabled in one of the two possible states. The sync signals should power up disabled in the high state. No composite sync or special flat panel sync support will be included.

10.6.1.3 VESA / VGA Mode

VESA/VGA mode provides compatibility for pre-existing software that set the display mode using the VGA CRTC registers. Timings are generated based on the VGA register values and the timing generator registers are not used.

10.6.1.4 DDC (Display Data Channel)

DDC is a standard defined by VESA. Its purpose is to allow communication between the host system and display. Both configuration and control information can be exchanged allowing plug- and-play systems to be realized. Support for DDC 1 and 2 is implemented. The GMCH uses the DDC_CLK and DDC_DATA signals to communicate with the analog monitor. The GMCH generates these signals at 2.5 V. External pull-up resistors and level shifting circuitry should be implemented on the board.

The GMCH implements a hardware GMBus controller that can be used to control these signals allowing for transactions speeds up to 400 kHz.

10.6.2 Digital Display Interface

The GMCH has several options for driving digital displays. The GMCH contains two SDVO ports. On the 82Q965 and 82G965 GMCH the ports are multiplexed on the PCI Express* interface. When an external PCI Express* Graphics accelerator is not present, the GMCH can use the multiplexed SDVO ports to provide extra digital display options. These additional digital display capabilities may be provided through an ADD2 card, which is designed to plug in to a PCI Express connector.

10.6.2.1 Multiplexed Digital Display Channels – Intel® SDVOB and Intel® SDVOC (Intel® 82Q965 and 82G965 GMCH Only)

The GMCH has the capability to support digital display devices through two SDVO. When an external graphics accelerator is used via the PCI Express* port, the multiplexed SDVO ports are not available.

The shared SDVO ports each support a pixel clock up to 270 MHz and can support a variety of transmission devices.

SDVO_CTRLDATA is an open-drain signal that acts as a strap during reset to tell the GMCH whether the interface is a PCI Express interface or an SDVO interface. When implementing SDVO, either via ADD2 cards or with a down device, a pull-up is placed on this line to signal to the GMCH to run in SDVO mode and for proper GMBus operation.

10.6.2.1.1 ADD2/Media Expansion Card

When a Q965, G965 Express chipset platform uses a PCI Express* graphics connector, the multiplexed SDVO ports may be used via an ADD2/Media Expansion card. The ADD2/Media Expansion card will be designed to fit a standard PCI Express (x16) connector. Refer to the latest ADD2/Media Expansion EDS and ADD2/Media Expansion card design kits for more details on ADD2/Media Expansion.

10.6.2.1.2 TMDS Capabilities

The GMCH is compliant with DVI Specification 1.0. When combined with a DVI compliant external device and connector, the GMCH has a high speed interface to a digital display (e.g., flat panel or digital CRT). When combining the two multiplexed SDVO ports, the GMCH can drive a flat panel up to 2048x1536 or a dCRT/HDTV up to 1920x1080. Flat Panel is a fixed resolution display. The GMCH supports panel fitting in the transmitter, receiver or an external device, but has no native panel fitting capabilities. The GMCH will however, provide unscaled mode where the display is centered on the panel.

10.6.2.1.3 LVDS Capabilities

The GMCH may use the multiplexed SDVO ports to drive a LVDS transmitter. Flat Panel is a fixed resolution display. The GMCH supports panel fitting in the transmitter, receiver or an external device, as well as using a built in 3x3 panel scalar for a single SDVO port.

10.6.2.1.4 TV-Out Capabilities

Although traditional TVs are not digital displays, the GMCH uses a digital display channel to communicate with a TV-Out transmitter. For that reason, the GMCH considers a TV-Output to be a digital display. The GMCH supports NTSC/PAL/SECAM standard definition formats. The GMCH generates the proper timing for the external encoder. The external encoder is responsible for generation of the proper format signal. Since the multiplexed SDVO interface is a NTSC/PAL/SECAM display on the TV-Out, the port can be configured to be the boot device. It is necessary to ensure that appropriate BIOS support is provided. If EasyLink is supported in the GMCH, then this mechanism could be used to interrogate the display device.

The TV-out interface on the GMCH is addressable as a master device. This allows an external TV encoder device to drive a pixel clock signal on SDVO_TVClk[+/-] that the GMCH uses as a reference frequency. The frequency of this clock is dependent on the output resolution required.

Flicker Filter and Overscan Compensation

The overscan compensation scaling and the flicker filter is done in the external TV encoder chip. Care must be taken to allow for support of TV sets with high performance de-interlacers and progressive scan displays connected to via a non-interlaced signal. Timing is generated with pixel granularity to allow more overscan ratios to be supported.

Direct YUV from Overlay

When source material is in the YUV format and is destined for a device that can take YUV format data in, it is desired to send the data without converting it to RGB. This avoids the truncation errors associated with multiple color conversion steps. The common situation will be that the overlay source data is in the YUV format and bypasses the conversion to RBG as it is sent to the TV port directly.

Sync Lock Support

Sync lock to the TV is done using the external encoders PLL combined with the display phase detector mechanism. The availability of this feature will be determined which external encoder is in use.

Analog Content Protection

Analog content protection will be provided through the external encoder using Macrovision 7.01. DVD software must verify the presence of a Macrovision TV encoder before playback continues. Simple attempts to disable the Macrovision operation must be detected.

Connectors

Target TV connectors support includes the CVBS, S-Video, Component, and SCART connectors. The external TV encoder in use will determine the method of support.

10.6.2.1.5 Control Bus

Communication to SDVO registers and if used, ADD2 PROMs and monitor DDCs, are accomplished by using the SDVO_CTRLDATA and SDVO_CTRLCLK signals through the SDVO device. These signals run up to 1 MHz and connect directly to the SDVO device. The SDVO device is then responsible for routing the DDC and PROM data streams to the appropriate location. Consult SDVO device datasheets for level shifting requirements of these signals.

Intel® SDVO Modes

The port can be dynamically configured in several modes:

- **Standard.** This mode provides baseline SDVO functionality. Supports Pixel Rates between 25 and 270 MP/s. Utilizes three data pairs to transfer RGB data.
- **Extended.** This mode adds Alpha support to data stream. Supports Pixel Rates between 25 and 270 MP/s. Utilizes four data channels and is only supported on SDVOB. Leverages channel C (SDVOC) Red pair as the Alpha pair for channel B (SDVOB).

10.6.3 Multiple Display Configurations

Microsoft Windows* 2000 and Windows* XP operating systems have enabled support for multi-monitor display. Since the GMCH has several display ports available for its two pipes, it can support up to two different images on different display devices. Timings and resolutions for these two images may be different. The GMCH supports Intel® Dual Display Clone, Intel Dual Display Twin, Intel Dual Display Zoom, and Extended Desktop.

Intel Dual Display Clone uses both display pipes to drive the same content, at the same resolution and color depth to two different displays. This configuration allows for different refresh rates on each display.

Intel Dual Display Twin uses one of the display pipes to drive the same content, at the same resolution, color depth, and refresh rates to two different displays.

Intel Dual Display Zoom uses both display pipes to drive different content, at potentially different resolutions, refresh rates, and color depths to two different displays. This configuration results in a portion of the primary display to be zoomed in on and displayed on the secondary display.

Extended Desktop uses both display pipes to drive different content, at potentially different resolutions, refresh rates, and color depths to two different displays. This configuration allows for a larger Windows Desktop by using both displays as a work surface.

Note: The GMCH is also not capable of operating in parallel with an external PCI Express graphics device. The GMCH can, however, work in conjunction with a PCI graphics adapter.

10.7 Power Management

Power management feature list is:

- ACPI 1.0b support
- ACPI S0, S1D, S3 (both Cold and Chipset Hot), S4, S5, C0, and C1 states
- Enhanced power management state transitions for increasing time processor spends in low power states
- Internal Graphics Display Device Control D0, D1, D2, D3 (82Q965, 82Q963, 82G965 GMCH only)
- Graphics Adapter States: D0, D3
- PCI Express Link States: L0, L0s, L1, L2/L3 Ready, L3 (82Q965, 82G965, 82P965 (G)MCH only)

10.8 Thermal Sensor

There are several registers that need to be configured to support the (G)MCH thermal sensor functionality and SMI# generation. Customers must enable the Catastrophic Trip Point at 118 °C as protection for the MCH. If the Catastrophic Trip Point is crossed, the MCH will instantly turn off all clocks inside the device. Users may optionally enable the Hot Trip Point between 85 °C and 105 °C to generate a SMI#. Users are then required to write their own SMI# handler in BIOS that will speed up the (G)MCH (or system) fan to cool the part.

10.8.1 PCI Device 0, Function 0

The SMICMD register requires that a bit be set to generate a SMI# when the Hot trip point is crossed. The ERRSTS register can be inspected for the SMI alert.

Address Offset	Symbol	Register Name	Default Value	Access
C8–C9h	ERRSTS	Error Status	0000h	RO, R/WC/S
CC–CDh	SMICMD	SMI Command	0000h	RO, RW

10.8.2 MCHBAR Thermal Sensor Registers

The Digital Thermometer Configuration Registers reside in the MCHBAR configuration space.

Address Offset	Symbol	Register Name	Default Value	Access
CD8h	TSC1	Thermal Sensor Control 1	00h	R/W/L, R/W, RS/WC
CD9h	TSC2	Thermal Sensor Control 2	00h	R/W/L, RO
CDAh	TSS	Thermal Sensor Status	00h	RO
CDCh–CDFh	TSTTP	Thermal Sensor Temperature Trip Point	00000000h	RO, R/W, R/W/L
CE2h	TCO	Thermal Calibration Offset	00h	R/W/L/K, R/W/L
CE4h	THERM1	Hardware Protection	00h	R/W/L, RO, R/W/L/K
CE6h	THERM3	TCO Fuses	00h	RS/WC, RO
CEA–CEBh	TIS	Thermal Interrupt Status	0000h	RO, R/WC
CF1h	TSMICMD	Thermal SMI Command	00h	RO, R/W

10.8.3 Programming Sequence

The following sequence must be followed in BIOS to properly set up the Hot Trip Point and SMI# assertion.

1. In Thermal Sensor Control 1 Register (TSC1), set thermal sensor enable bit (TSE) and the hysteresis value (DHA) by writing 99h to MCHBAR CD8h
2. Program the Hot Trip Point Register (TSTTP[HTPS]) by writing the appropriate value to MCHBAR CDCh bits [15:8]
3. Program the Catastrophic Trip Point Setting Register (TSTTP[CTPS]) by writing 2Ch to MCHBAR CDCh bits [7:0]
4. In Thermal Sensor Control 2 Register (TSC2), program the Thermometer Mode Enable and Rate (TE) by writing 04h to MCHBAR CD9h bits [3:0]
5. In the Hardware Protection Register (THERM1), program the Halt on Catastrophic bit (HOC) by writing 08h to MCHBAR CE4h bits [7:0]
6. Lock the Hardware Protection by writing a 1 to the Lock bit (HTL) at MCHBAR CE4h bit [0]
7. In Thermal SMI Command Register (TSMICMD), set the SMI# on Hot bit by writing a 02h to MCHBAR CF1h
8. Program the SMI Command register (SMICMD[TSTSMI]) by writing a 1 to bit 11 to PCI CCh
9. Program the TCO Register (TCO[TSLB]) to lock down the other register settings by writing a 1 to bit 7 of MCHBAR CE2h

If the temperature rises above the Hot Trip point:

The TIS[Hot Thermal Sensor Interrupt Event] is set when SMI# interrupt is generated.

10. Clear this bit of the TIS register to allow subsequent interrupts of this type to get registered.
11. Clear the global thermal sensor event bit in the Error Status Register, bit 11.
12. In thermal sensor status register (TSS), the Hot trip indicator (HTI) bit is set if this condition is still valid by the time the software gets to read the register.

10.8.4 Trip Point Temperature Programming

The Catastrophic and Hot trip points are programmed in the TSTTP Register. Bits 7:0 are for the Catastrophic trip point (CTPS), and bits 15:8 are for the Hot trip point (HTPS).

Note: **Based on Intel silicon test and calculations, the Catastrophic trip point must be fixed at 118 °C. The Hot trip point is recommended to be between 95 °C and 105 °C. Programming the Hot Trip Point above this range is not recommended.**

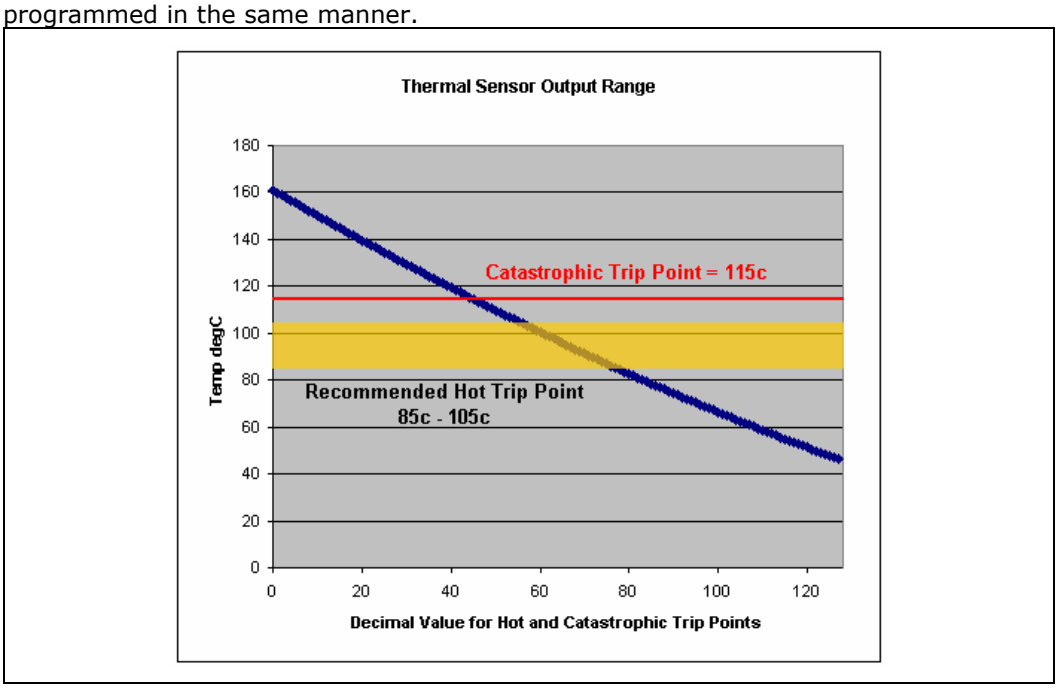
To program both trip point settings, the following polynomial equation should be used.

Programmed temp = (0.0016*value^2) – (1.10707*value) + 161.05

In this case the "value" is a decimal number between 0 and 128. For the Catastrophic Trip Point, a decimal value of 41 (29h) should be used to hit 118 °C.

(0.0016*41^2) – (1.10707*41) + 161.05 = 118.3 °C

The CTPS should then be programmed with 29h. The Hot Trip Point is also programmed in the same manner.

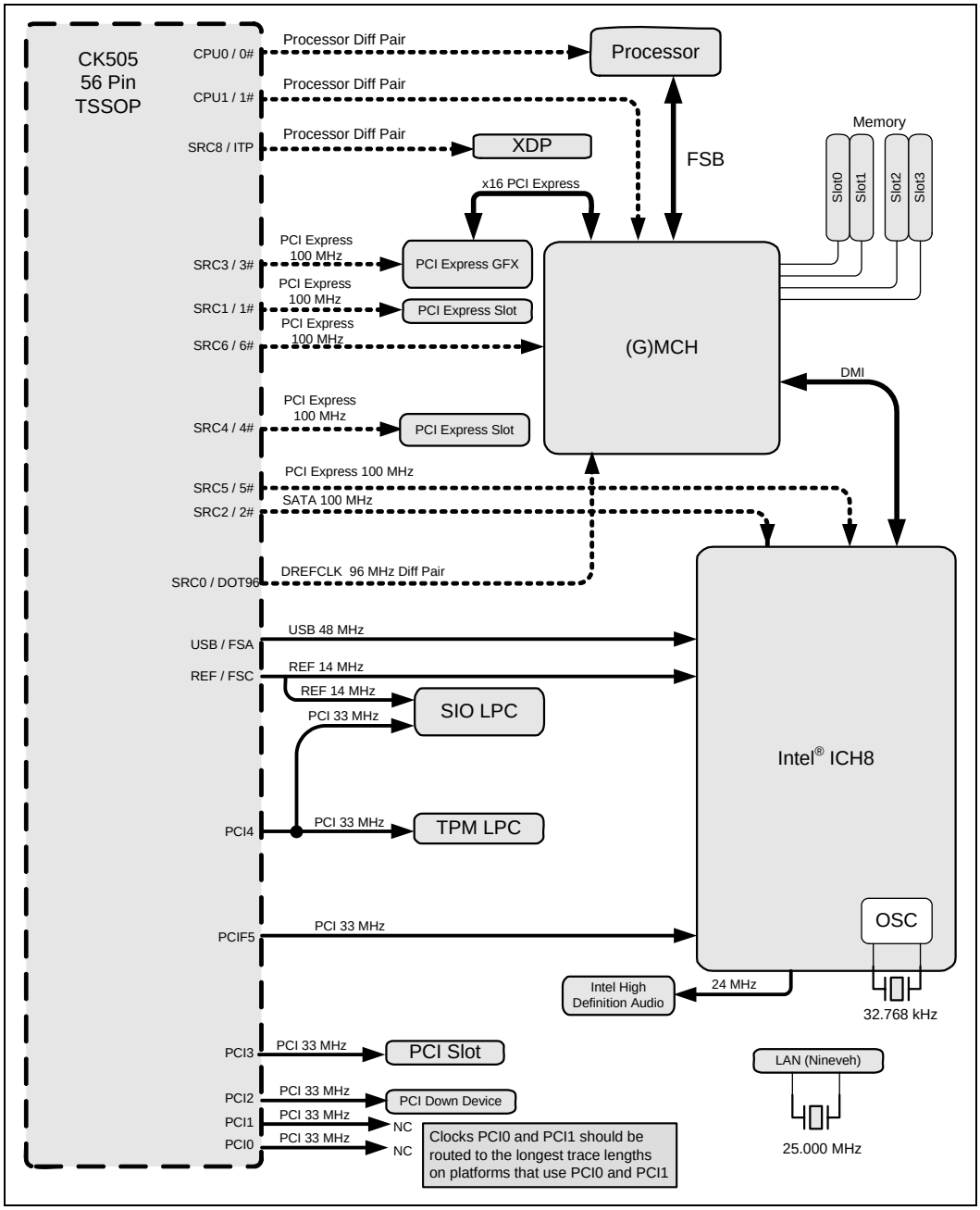


10.9 Clocking

The (G)MCH has a total of 5 PLLs providing many times that many internal clocks. The PLLs are:

- Host PLL. This PLL generates the main core clocks in the host clock domain. It can also be used to generate memory and internal graphics core clocks. It uses the Host clock (H_CLKIN) as a reference.
- Memory IO PLL. This PLL optionally generates low jitter clocks for memory IO interface, as opposed to from Host PLL. Uses the Host FSB differential clock (HPL_CLKINP/HPL_CLKINN) as a reference. Low jitter clock source from Memory IO PLL is required for DDR667 and higher frequencies.
- PCI Express PLL (82Q965, 82G965, 82P965 (G)MCH only). This PLL generates all PCI Express related clocks, including the Direct Media that connect to the ICH8. This PLL uses the 100 MHz clock (G_CLKIN) as a reference.
- Display PLL A. This PLL generates the internal clocks for Display A. It uses D_REFCLKIN as a reference.
- Display PLL B – This PLL generates the internal clocks for Display B. It uses D_REFCLKIN as a reference.
- CK505 is the new clock chip required for the Q965, Q963, G965, P965 Express chipset platforms.

Figure 10-5. Platform Clocking Diagram Example



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11 Electrical Characteristics

This chapter contains the (G)MCH absolute maximum electrical ratings, power dissipation values, and DC characteristics.

Note: References to SDVO apply to the 82Q965, 82Q963, 82G965 GMCH only.

Note: References to DDR2-800 apply to the 82Q965, 82G965 GMCH and 82P965 MCH only.

Note: References to the PCI Express Interface apply to the 82Q965, 82G965 GMCH and 82P965 MCH only.

11.1 Absolute Minimum and Maximum Ratings

Table 11-1 specifies the (G)MCH's absolute maximum and minimum ratings. Within functional operation limits, functionality and long-term reliability can be expected.

At conditions outside functional operation condition limits, but within absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. If a device is returned to conditions within functional operation limits after having been subjected to conditions outside these limits, but within the absolute maximum and minimum ratings, the device may be functional, but with its lifetime degraded depending on exposure to conditions exceeding the functional operation condition limits.

At conditions exceeding absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. Moreover, if a device is subjected to these conditions for any length of time its reliability will be severely degraded or not function when returned to conditions within the functional operating condition limits.

Although the (G)MCH contains protective circuitry to resist damage from static electric discharge, precautions should always be taken to avoid high static voltages or electric fields.

Table 11-1. Absolute Minimum and Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
$T_{storage}$	Storage Temperature	-55	150	°C	1
(G)MCH Core					
VCC	1.25 V Core Supply Voltage with respect to VSS	-0.3	1.375	V	
Host Interface (533 MHz/800 MHz/1066 MHz)					
VTT	System Bus Input Voltage with respect to VSS	-0.3	1.32	V	

Symbol	Parameter	Min	Max	Unit	Notes
VCCA_HPLL	1.25 V Host PLL Analog Supply Voltage with respect to VSS	-0.3	1.375	V	
DDR2 Interface (533 MHz/667 MHz/800MHz)					
VCCSM	1.8 V DDR2 System Memory Supply Voltage with respect to VSS	-0.3	4.0	V	
VCC_SMCLK	1.8 V DDR2 Clock System Memory Supply Voltage with respect to VSS	-0.3	4.0	V	
VCCA_MPLL	1.25 V System Memory PLL Analog Supply Voltage with respect to VSS	-0.3	1.375	V	
PCI Express* / Intel® SDVO / DMI Interface					
VCC_EXP	1.25 V PCI Express* and DMI Supply Voltage with respect to VSS	-0.3	1.375	V	
VCCA_EXP	3.3 V PCI Express* Analog Supply Voltage with respect to VSS	-0.3	3.63	V	
VCCA_EXPPLL	1.25 V PCI Express* PLL Analog Supply Voltage with respect to VSS	-0.3	1.375	V	
R, G, B / CRT DAC Display Interface (8 bit)					
VCCA_DAC	3.3 V Display DAC Analog Supply Voltage with respect to VSS	-0.3	3.63	V	
VCCD_CRT	1.5 V Display DAC Digital Supply Voltage with respect to VSS	-0.3	1.98	V	
VCCDQ_CRT	1.5 V Display DAC Quiet Digital Supply Voltage with respect to VSS	-0.3	1.98	V	
VCCA_DPLLA	1.25 V Display PLL A Analog Supply Voltage with respect to VSS	-0.3	1.375	V	
VCCA_DPLLB	1.25 V Display PLL B Analog Supply Voltage with respect to VSS	-0.3	1.375	V	
Controller Link Interface					
VCC_CL	1.25 V Supply Voltage with respect to VSS	-0.3	1.375	V	
CMOS Interface					
VCC3_3	3.3 V CMOS Supply Voltage with respect to VSS	-0.3	3.63	V	

NOTE:

2. Possible damage to the (G)MCH may occur if the (G)MCH temperature exceeds 150 °C. Intel does not warrant functionality for parts that have exceeded temperatures above 150 °C since this exceeds Intel's specification.

11.1.1 Current Consumption

Table 11-2 shows the current consumption for the (G)MCH in the Advanced Configuration and Power Interface (ACPI) S0 state. I_{CC_MAX} values are determined on a per-interface basis, at the highest frequencies for each interface. Sustained current values or maximum current values cannot occur simultaneously on all interfaces. Sustained values are *measured* sustained RMS maximum current consumption and include leakage estimates. The measurements are made with typical silicon at 45° C. The maximum values are maximum theoretical pre-silicon calculated values. In some cases, the sustained measured values have exceeded the maximum values.

Table 11-2. Current Consumption in S0

Symbol	Parameter	Signal Names	Sustained	Max	Unit	Notes
I_{VCC}	1.25 V Core Supply Current (Discrete Gfx) (82Q965, 82G965 , 82P965 (G)MCH only)	VCC	7.2	9.3	A	1,2
I_{VCC}	1.25 V Core Supply Current (Integrated Gfx) (82Q965, 82G965 , 82Q963 GMCH only)	VCC	15.5	18.9	A	1,2
I_{VCCSM}	DDR2 System Memory Interface (1.8 V) Supply Current	VCCSM	2.26	3.7	A	1,2,3
I_{VCC_SMCLK}	DDR2 System Memory Clock Interface (1.8 V) Supply Current	VCC_SMCLK		250	mA	
I_{VCC_EXP}	1.25 V PCI Express* / Intel® SDVO and DMI Supply Current	VCC_EXP	1.76	2.47	A	2
I_{VCC_CL}	1.25 V Controller Supply Current	VCC_CL	2.64	3.8	A	2
I_{VTT}	System Bus Supply Current	VTT	950	984	mA	1
I_{VCCA_EXP}	3.3 V PCI Express* / Intel® SDVO and DMI Analog Supply Current	VCCA_EXP	0.36	0.36	mA	
I_{VCCA_DAC}	3.3 V Display DAC Analog Supply Current	VCCA_DAC	70	65.8	mA	
I_{VCC3_3}	3.3 V CMOS Supply Current	VCC3_3	21	15.8	mA	
I_{VCCD_CRT}	1.5 V Display Digital Supply Current	VCCD_CRT	100	30	mA	3
I_{VCCDQ_CRT}	1.5 V Display Quiet Digital Supply Current	VCCDQ_CRT		0.033	mA	
I_{VCCA_EXPPLL}	1.25 V PCI Express* / Intel® SDVO and DMI PLL Analog Supply Current	VCCA_EXPPLL	70	71.6	mA	
I_{VCCA_HPLL}	1.25 V Host PLL Supply Current	VCCA_HPLL	20	67.9	mA	
I_{VCCA_DPLLA} I_{VCCA_DPLLB}	1.25 V Display PLL A and PLL B Supply Current	VCCA_DPLLA VCCA_DPLLB	30 40	90.6 90.6	mA	

Symbol	Parameter	Signal Names	Sustained	Max	Unit	Notes
I_{VCCA_MPLL}	System Memory PLL Analog (1.8 V) Supply Current	VCCA_MPLL	90	225	mA	

NOTES:
1. Measurements are for current coming through chipset's supply pins.
2. Rail includes DLLs (and FSB sense amps on VCC).
3. Sustained Measurements are combined because one voltage regulator on the platform supplies both rails on the (G)MCH.

11.2 Signal Groups

The signal description includes the type of buffer used for the particular signal:

PCI Express* / SDVO	PCI Express* / Intel® SDVO interface signals. These signals are compatible with PCI Express* 1.0 Signaling Environment AC Specifications and are AC coupled. The buffers are not 3.3 V tolerant. Differential voltage spec = (|D+ - D-|) * 2 = 1.2Vmax. Single-ended maximum = 1.25 V. Single-ended minimum = 0 V.
DMI	Direct Media Interface signals. These signals are compatible with PCI Express* 1.0 Signaling Environment AC Specifications, but are DC coupled. The buffers are not 3.3 V tolerant. Differential voltage spec = (|D+ - D-|) * 2 = 1.2Vmax. Single-ended maximum = 1.25 V. Single-ended minimum = 0 V.
GTL+	Open Drain GTL+ interface signal. Refer to the GTL+ I/O Specification for complete details. The (G)MCH integrates most GTL+ termination resistors.
HCSL	Host Clock Signal Level buffers. Current mode differential pair. Differential typical swing = (|D+ - D-|) * 2 = 1.4V. Single ended input tolerant from -0.35 V to 1.2 V. Typical crossing voltage 0.35 V.
SSTL-1.8	Stub Series Termination Logic. These are 1.8 V output capable buffers. 1.8 V tolerant.
CMOS	CMOS buffers
Analog	Analog reference or output. May be used as a threshold voltage or for buffer compensation.

Table 11-3. Signal Groups

Signal Type	Signals
Host Interface Signal Groups	
GTL+ Input/Outputs	HADS#, HBNR#, HBREQ0#, HDBSY#, HDRDY#, HDINV[3:0]#, HA[35:3]#, HADSTB[1:0]#, HD[63:0]#, HDSTBP[3:0]#, HDSTBN[3:0]#, HHIT#, HHITM#, HREQ[4:0]#, HLOCK#
GTL+ Common Clock Outputs	HBPRI#, HCPURST#, HDEFER#, HTRDY#, HRS[2:0]#
Analog Host Interface Reference and Compensation Signals	HDVREF, HACCVREF, HSWING, HRCOMP, HSCOMP, HSCOMP#
GTL+ Input	BSEL[2:0]
PCI Express* Graphics and Intel® SDVO Interface Signal Groups	
PCI Express* / Intel® sDVO Input	**PCI Express* Interface[1]:** EXP_RXN[15:0], EXP_RXP[15:0], **SDVO Interface[1]:** SDVO_TVCLKIN+, SDVO_TVCLKIN-, SDVOB_INT+, SDVOB_INT-, SDVO_STALL+, SDVO_STALL-, SDVOC_INT+, SDVOC_INT-
PCI Express* / SDVO Output	**PCI Express* Interface[1]:** EXP_TXN[15:0], EXP_TXP[15:0] **SDVO Interface[1]:** SDVOB_RED+, SDVOB_RED-, SDVOB_GREEN+, SDVOB_GREEN-, SDVOB_BLUE+, SDVOB_BLUE-, SDVOB_CLK+, SDVOB_CLK-, SDVOC_RED+/SDVOB_ALPHA+, SDVOC_RED-/SDVOB_ALPHA-, SDVOC_GREEN+, SDVOC_GREEN-, SDVOC_BLUE+, SDVOC_BLUE-, SDVOC_CLK+, SDVOC_CLK-
CMOS I/O OD	SDVO_CTRLCLK, SDVO_CTRLDATA
Analog PCI Express* / SDVO Interface Compensation Signals	EXP_COMPO, EXP_COMPI
Direct Media Interface Signal Groups	
DMI Input	DMI_RXN[3:0], DMI_RXP[3:0]
DMI Output	DMI_TXN[3:0], DMI_TXP[3:0]
DDR2 Interface Signal Groups	
SSTL – 1.8 DDR2 CMOS I/O	SDQ_A[63:0], SDQ_B[63:0], SDQS_A[7:0], SDQS_A[7:0]#, SDQS_B[7:0], SDQS_B[7:0]#
SSTL – 1.8 DDR2 CMOS Output	SDM_A[7:0], SDM_B[7:0], SMA_A[14:0], SMA_B[14:0], SBS_A[2:0], SBS_B[2:0], SRAS_A#, SRAS_B#, SCAS_A#, SCAS_B#, SWE_A#, SWE_B#, SODT_A[3:0], SODT_B[3:0], SCKE_A[3:0], SCKE_B[3:0], SCS_A[3:0]#, SCS_B[3:0]#, SCLK_A[5:0], SCLK_A[5:0]#, SCLK_B[5:0], SCLK_B[5:0]#
DDR2 Reference and Comp. Voltages	SRCOMP[3:0], SMVREF, SRCOMP_VOL, SRCOMP_VOH

Signal Type	Signals
Controller Link Signal Groups	
CMOS I/O OD	CL_DATA, CL_CLK
CMOS Input	CL_RST#, CL_PWROK
Analog Controller Link Reference Voltage	CL_VREF
R, G, B / CRT DAC Display Signal Groups	
Analog Current Outputs	RED, RED#, GREEN, GREEN#, BLUE, BLUE#
Analog/Ref DAC Miscellaneous	REFSET[2]
CMOS I/O OD	DDC_CLK, DDC_DATA
HVCMOS Output	HSYNC, VSYNC
HCSL	HCLKN, HCLKP, DREFCLKP, DREFCLKN, GCLKP, GCLKN
Reset, and Miscellaneous Signal Groups	
CMOS Input	EXP_EN, EXP_SLR, RSTIN#, PWROK
CMOS Output	ICH_SYNC#
Misc.	TEST[2:0]
I/O Buffer Supply Voltages	
System Bus Input Supply Voltage	VTT
1.25 V PCI Express* / Intel® sDVO Supply Voltages	VCC_EXP
3.3 V PCI Express* / Intel® sDVO Analog Supply Voltage	VCCA_EXP
1.8 V DDR2 Supply Voltage	VCCSM
1.8 V DDR2 Clock Supply Voltage	VCC_SMCLK
1.25 V (G)MCH Core Supply Voltage	VCC
1.25 V Controller Supply Voltage	VCC_CL
3.3 V CMOS Supply Voltage	VCC3_3
3.3 V R, G, B / CRT DAC Display Analog Supply Voltage	VCCA_DAC
1.5 V DAC Digital Supply Voltages	VCCD_CRT, VCCDQ_CRT
PLL Analog Supply Voltages	VCCA_HPLL, VCCA_EXPPLL, VCCA_DPLLA, VCCA_DPLLB, VCCA_MPLL

NOTES:
1. See Chapter 2 for SDVO and PCI Express* Pin Mapping.
2. Current Mode Reference pin. DC Specification is not required

11.3 Buffer Supply and DC Characteristics

11.3.1 I/O Buffer Supply Voltages

The I/O buffer supply voltage is measured at the (G)MCH package pins. The tolerances shown in Table 11-4 are inclusive of all noise from DC up to 20 MHz. In the lab, the voltage rails should be measured with a bandwidth limited oscilloscope with a roll off of 3 dB/decade above 20 MHz under all operating conditions.

Table 11-4 indicates which supplies are connected directly to a voltage regulator or to a filtered voltage rail. For voltages that are connected to a filter, they should me measured at the *input* of the filter.

If the recommended platform decoupling guidelines cannot be met, the system designer will have to make tradeoffs between the voltage regulator output DC tolerance and the decoupling performance of the capacitor network to stay within the voltage tolerances listed in Table 11-4.

Table 11-4. I/O Buffer Supply Voltage

Symbol	Parameter	Min	Nom	Max	Unit	Notes
VCCSM	DDR2 I/O Supply Voltage	1.7	1.8	1.9	V	
VCC_SMCLK	DDR2 I/O Supply Voltage	1.7	1.8	1.9	V	2
VCC_EXP	SDVO, PCI-Express* Supply Voltage	1.188	1.25	1.313	V	
VCCA_EXP	SDVO, PCI-Express* Analog Supply Voltage	3.135	3.3	3.465	V	2
VTT	System Bus Input Supply Voltage	1.14	1.2	1.26	V	
VCC	(G)MCH Core Supply Voltage	1.188	1.25	1.313	V	
VCC_CL	Controller Supply Voltage	1.188	1.25	1.313	V	
VCC3_3	CMOS Supply Voltage	3.135	3.3	3.465	V	
VCCA_DAC	Display DAC Analog Supply Voltage	3.135	3.3	3.465	V	
VCCD_CRT	Display Digital Supply Voltage	1.425	1.5	1.575	V	1
VCCDQ_CRT	Display Quiet Digital Supply Voltage	1.425	1.5	1.575	V	1
VCCA_HPLL, VCCA_EXPPLL, VCCA_DPLLA, VCCA_DPLLB, VCCA_MPLL	Various PLLs' Analog Supply Voltages	1.188	1.25	1.313	V	2

NOTES:
1. The VCCD_CRT and VCCDQ_CRT can also operate at a nominal 1.8 V ± 5% input voltage. Only the 1.5 V nominal voltage setting will be validated internally.
2. These rails are filtered from other voltage rails on the platform and should be measured at the *input* of the filter.

11.3.2 General DC Characteristics

Table 11-5. DC Characteristics

Symbol	Parameter	Min	Nom	Max	Unit	Notes
Reference Voltages						
HDVREF, HACCVREF	Host Data, Address, and Common Clock Signal Reference Voltages	0.63 x VTT –2%	0.63 x VTT	0.63 x VTT +2%	V	
HSWING	Host Compensation Reference Voltage	0.25 x VTT –2%	0.25 x VTT	0.25 x VTT+2%	V	
CL_VREF	Controller Link Reference Voltage	0.274 x VCC_CL	0.279 x VCC_CL	0.284 x VCC_CL		
SMVREF	DDR2 Reference Voltage	0.49 x VCCSM	0.50 x VCCSM	0.51 x VCCSM	V	
Host Interface						
V_{IL_H}	Host GTL+ Input Low Voltage	-0.10	0	(0.63 x VTT) – 0.1	V	
V_{IH_H}	Host GTL+ Input High Voltage	(0.63 x VTT)+0.1	VTT	VTT +0.1	V	
V_{OL_H}	Host GTL+ Output Low Voltage	—	—	(0.25 x VTT)+0.1	V	
V_{OH_H}	Host GTL+ Output High Voltage	VTT – 0.1	—	VTT	V	
I_{OL_H}	Host GTL+ Output Low Current	—	—	VTTmax * (1–0.25) / Rttmin	mA	Rtt_{min} = 47.5 Ω
I_{LEAK_H}	Host GTL+ Input Leakage Current	—	—	20	µA	V_{OL}< Vpad< V_{TT}
C_{PAD}	Host GTL+ Input Capacitance	2	—	2.5	pF	
C_{PCKG}	Host GTL+ Input Capacitance (common clock)	0.90	—	2.5	pF	
DDR2 Interface						
$V_{IL(DC)}$	DDR2 Input Low Voltage	—	—	SMVREF – 0.125	V	
$V_{IH(DC)}$	DDR2 Input High Voltage	SMVREF + 0.125	—		V	
$V_{IL(AC)}$	DDR2 Input Low Voltage	—	—	SMVREF – 0.250	V	
$V_{IH(AC)}$	DDR2 Input High Voltage	SMVREF + 0.250	—		V	
V_{OL}	DDR2 Output Low Voltage	—	—	0.3	V	1
V_{OH}	DDR2 Output High Voltage	1.5	—		V	1
I_{Leak}	Input Leakage Current	—	—	±20	µA	4
I_{Leak}	Input Leakage Current	—	—	±550	µA	5

Symbol	Parameter	Min	Nom	Max	Unit	Notes
$C_{I/O}$	DDR2 Input/Output Pin Capacitance	3.0	—	6.0	pF	
1.25 V PCI Express* Interface 1.1 (includes PCI Express* and Intel® SDVO)						
$V_{TX\text{-}DIFF\ P\text{-}P}$	Differential Peak to Peak Output Voltage	0.800	—	1.2	V	2
$V_{TX\_CM\text{-}ACp}$	AC Peak Common Mode Output Voltage	—	—	20	mV	
$Z_{TX\text{-}DIFF\text{-}DC}$	DC Differential TX Impedance	80	100	120	Ω	
$V_{RX\text{-}DIFF\ p\text{-}p}$	Differential Peak to Peak Input Voltage	0.175	—	1.2	V	3
$V_{RX\_CM\text{-}ACp}$	AC Peak Common Mode Input Voltage	—	—	150	mV	
Input Clocks						
V_{IL}	Input Low Voltage	-0.150	0	N/A	V	
V_{IH}	Input High Voltage	0.660	0.710	0.850	V	
$V_{CROSS(ABS)}$	Absolute Crossing Voltage	0.300	N/A	0.550	V	6,7,8,9
$\Delta V_{CROSS(REL)}$	Range of Crossing Points	N/A	N/A	0.140	V	9
C_{IN}	Input Capacitance	1	—	3	pF	
SDVO_CTRLDATA, SDVO_CTRLCLK						
V_{IL}	Input Low Voltage	—	—	0.75	V	
V_{IH}	Input High Voltage	1.75	—		V	
I_{LEAK}	Input Leakage Current	—	—	± 10	µA	
C_{IN}	Input Capacitance	—	—	10.0	pF	
I_{OL}	Output Low Current (CMOS Outputs)	—	—	7.8	mA	@ 50% swing
I_{OH}	Output High Current (CMOS Outputs)	-1	—	—	mA	@ 50% swing
V_{OL}	Output Low Voltage (CMOS Outputs)	—	—	0.4	V	
V_{OH}	Output High Voltage (CMOS Outputs)	2.25	—	—	V	
DDC_DATA, DDC_CLK						
V_{IL}	Input Low Voltage	—	—	0.9	V	
V_{IH}	Input High Voltage	2.1	—	—	V	
I_{LEAK}	Input Leakage Current	—	—	± 10	µA	
C_{IN}	Input Capacitance	—	—	10.0	pF	
I_{OL}	Output Low Current (CMOS Outputs)	—	—	27.0	mA	@ 50% swing
I_{OH}	Output High Current (CMOS Outputs)	-1	—	—	mA	@ 50% swing

Symbol	Parameter	Min	Nom	Max	Unit	Notes
V_{OL}	Output Low Voltage (CMOS Outputs)	—	—	0.4	V	
V_{OH}	Output High Voltage (CMOS Outputs)	2.7	—	—	V	
CL_DATA, CL_CLK						
V_{IL}	Input Low Voltage	—	—	0.277	V	
V_{IH}	Input High Voltage	0.477	—	—	V	
I_{LEAK}	Input Leakage Current	—	—	± 20	µA	
C_{IN}	Input Capacitance	—	—	1.5	pF	
I_{OL}	Output Low Current (CMOS Outputs)	—	—	1.0	mA	@V_{OL_HI} max
I_{OH}	Output High Current (CMOS Outputs)	6.0	—	—	mA	@V_{OH_HI} min
V_{OL}	Output Low Voltage (CMOS Outputs)	—	—	0.06	V	
V_{OH}	Output High Voltage (CMOS Outputs)	0.6	—	—	V	
PWROK, CL_PWROK, RSTIN#						
V_{IL}	Input Low Voltage	—	—	0.3	V	
V_{IH}	Input High Voltage	3.0	—	—	V	
I_{LEAK}	Input Leakage Current	—	—	±100	µA	
C_{IN}	Input Capacitance	—	—	6.0	pF	
CL_RST#						
V_{IL}	Input Low Voltage	—	—	0.13	V	
V_{IH}	Input High Voltage	1.17	—		V	
I_{LEAK}	Input Leakage Current	—	—	±20	µA	
C_{IN}	Input Capacitance	—	—	5.0	pF	
ICH_SYNC#						
I_{OL}	Output Low Current (CMOS Outputs)	—	—	2.0	mA	@V_{OL_HI} max
I_{OH}	Output High Current (CMOS Outputs)	-2.0	—		mA	@V_{OH_HI} min
V_{OL}	Output Low Voltage (CMOS Outputs)	—	—	0.33	V	
V_{OH}	Output High Voltage (CMOS Outputs)	2.97	—		V	
EXP_SLR, EXP_EN						
V_{IL}	Input Low Voltage	-0.10	0	(0.63 x VTT) – 0.1	V	
V_{IH}	Input High Voltage	(0.63 x VTT)+0.1	VTT	VTT +0.1	V	

Symbol	Parameter	Min	Nom	Max	Unit	Notes
I_{LEAK}	Input Leakage Current	—	—	20	µA	V_{OL}< Vpad< V_{TT}
C_{IN}	Input Capacitance	2	—	2.5	pF	
HSYNC, VSYNC						
I_{OL}	Output Low Current (CMOS Outputs)	—	—	35.0	mA	@V_{OL_HI} max
I_{OH}	Output High Current (CMOS Outputs)	-1	—		mA	@V_{OH_HI} min
V_{OL}	Output Low Voltage (CMOS Outputs)	—	—	0.5	V	
V_{OH}	Output High Voltage (CMOS Outputs)	2.4	—		V	

NOTES:

1. Determined with 2x (G)MCH DDR2 Buffer Strength Settings into a 50 Ω to 0.5xVCCSM test load.
2. Specified at the measurement point into a timing and voltage compliance test load as shown in Transmitter compliance eye diagram of PCI Express* specification and measured over any 250 consecutive TX UIs.
3. Specified at the measurement point over any 250 consecutive UIs. The test load shown in Receiver compliance eye diagram of PCI Express* spec should be used as the RX device when taking measurements.
4. Applies to pin to VCC or VSS leakage current for the SDQ_A[63:0]# and SDQ_B[63:0]# signals.
5. Applies to pin to pin leakage current between SDQS_A[7:0], SDQS_A[7:0]#, SDQS_B[7:0]#, and SDQS_B[7:0]# signals.
6. Crossing voltage defined as instantaneous voltage when rising edge of BCLK0 equals falling edge of BCLK1.
7. V_{Havg} is the statistical average of the V_H measured by the oscilloscope.
8. The crossing point must meet the absolute and relative crossing point specifications simultaneously.

11.3.3 R, G, B / CRT DAC Display DC Characteristics (Intel® 82Q965, 82Q963, 82G965 GMCH Only)

Table 11-6. R, G, B / CRT DAC Display DC Characteristics: Functional Operating Range (VCCA_DAC = 3.3 V ± 5%)

Parameter	Min	Typical	Max	Units	Notes
DAC Resolution	8	—	—	Bits	1
Max Luminance (full-scale)	0.665	0.700	0.770	V	1, 2, 4 (white video level voltage)
Min Luminance	—	0.000	—	V	1, 3, 4 (black video level voltage)
LSB Current	—	73.2	—	μA	4,5
Integral Linearity (INL)	-1.0	—	+1.0	LSB	1,6
Differential Linearity (DNL)	-1.0	—	+1.0	LSB	1,6
Video channel-channel voltage amplitude mismatch	—	—	6	%	7
Monotonicity	Ensured				

NOTES:
1. Measured at each R, G, B termination according to the VESA Test Procedure – Evaluation of Analog Display Graphics Subsystems Proposal (Version 1, Draft 4, December 1, 2000).
2. Maximum steady-state amplitude
3. Minimum steady-state amplitude
4. Defined for a double 75 Ω termination.
5. Set by external reference resistor value.
6. INL and DNL measured and calculated according to VESA Video Signal Standards.
7. Maximum full-scale voltage difference among R, G, B outputs (percentage of steady-state full-scale voltage).

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12 Ballout and Package Information

This chapter provides the ballout and package information.

12.1 Ballout

Figure 12-1, Figure 12-2, and Figure 12-3 show the (G)MCH ballout from a top-of-package view. Table 12-1 provides ballout list ordered by signal name.

Note: Notes for Figure 12-1, Figure 12-2, and Figure 12-3, and Table 12-1.

1. Balls that are listed as RSVD are reserved.
2. Some balls marked as reserved (RSVD) are used in XOR testing. See Chapter 13 for details.
3. Balls that are listed as NC are No Connects.
4. Analog Display Signals (RED, RED#, GREEN, GREEN#, BLUE, BLUE#, REFSET, HSYNC, VSYNC, DDC_CLK, DDC_DATA) and the SDVO_CTRLCLK and SDVO_CTRLDATA signals are not used on the 82P965 MCH. Contact your Intel field representative for proper termination of the corresponding balls.
5. For the 82Q965 and 82G965 GMCH, the PCI Express and SDVO signals are multiplexed. However, only the PCI Express signal name is included in the following ballout figures and table. See Section 2.10 for the PCI Express to SDVO signal name mapping.
6. The 82Q963 GMCH does not have a PCI Express Interface. Thus, these balls are dedicated to the SDVO interface. See Section 2.10 for the PCI Express to SDVO signal name mapping.

Figure 12-1. (G)MCH Ballout Diagram Ballout Diagram (Top View Left – Columns 43–30)

	43	42	41	40	39	38	37	36	35	34	33	32	31	30	
BC	TEST0	NC	VSS		VCCSM		VSS			VCCSM		VSS		VCCSM	BC
BB	NC	VCC_ SMCLK	VCC_ SMCLK	SRCOMP2	VCCSM	SCS_A3#	VCCSM		SODT_A2	SWE_A#	SRAS_A#	VCCSM	SODT_B3	SCS_B1#	BB
BA	VCC_ SMCLK	VCC_ SMCLK		SRCOMP3	SODT_A3	SODT_A1			SCS_A1#	SCS_A2#	SBS_A0		SMA_A0	SODT_B1	BA
AY		VCC_ SMCLK	VSS	VSS		SMA_A13	SODT_A0		SCAS_A#		SMA_A10	VCCSM	SCS_B3#		AY
AW	VSS	RSVD	VSS		SDQS_B4		SDQ_B32		SCS_A0#		SCLK_A2#	SBS_A1	SCLK_B0#		AW
AV		SDQ_A32	SDQ_A37	SDQ_A36		SDQ_B33	VSS		VSS		SCLK_A2	SCLK_B2	SCLK_B0		AV
AU	SDM_A4	VSS		SDQ_A33	SDQS_B4#	VSS	SDM_B4		SDQ_B36		SCLK_A5#	VSS	SCLK_A0		AU
AT											SCLK_A5	SCLK_B2#	VSS		AT
AR		SDQ_A38	SDQS_A4	SDQS_A4#	SDQ_B44	VSS	SDQ_B39		SDQ_B37		VSS	VSS	SCLK_A0#		AR
AP	VSS	SDQ_A34	SDQ_A39									SCLK_B5#	SCLK_A3#		AP
AN		SDQ_A45	SDQ_A40	SDQ_A44	SDQ_A35	VSS	SDQ_B35	SDQ_B34	SDQ_B38		SCLK_B5	RSVD	VSS		AN
AM	SDM_A5	VSS		VSS	SDQ_A41	SDQ_B41	SDM_B5	VSS	SDQ_B40	SDQ_B45	VSS		RSVD		AM
AL		SDQ_A46	SDQS_A5	SDQS_A5#	SDQ_A47	SDQ_B43	SDQ_B46	VSS	SDQS_B5	SDQS_B5#	VSS	SDQ_B47	RSVD		AL
AK	VSS	SDQ_A42	SDQ_A43											VCC_CL	AK
AJ		SDQ_A52	SDQ_A53	SDQ_A48	VSS	SDQ_B49	SDQ_B52	VSS	SDQ_B53	SDQ_B42	VSS	RSVD	VCC_CL	VCC_CL	AJ
AH	SDQ_A49	VSS													AH
AG		SDQS_A6	SDQS_A6#	SDM_A6	SDM_B6	SDQ_B48	VSS	SDQS_B6#	SDQS_B6	VSS	SDQ_B54	RSVD	VCC_CL	VCC_CL	AG
AF	VSS	SDQ_A55	SDQ_A54		SDQ_A50	SDQ_B61	VSS	VSS	SDQ_B50	SDQ_B55	SDQ_B51	RSVD	VCC_CL	VCC_CL	AF
AE		SDQ_A60	SDQ_A61	SDQ_A51											AE
AD	SDQ_A57	VSS		SDQ_A56	VSS	SDM_B7	VSS	SDQ_B56	VSS	SDQ_B60	VSS	VCC_CL	VCC_CL	VCC_CL	AD
AC		SDQS_A7	SDQS_A7#	SDM_A7	SDQ_A62	VSS	SDQS_B7#	SDQS_B7	VSS	SDQ_B62	SDQ_B57	VCC_CL	VCC_CL	VCC_CL	AC
AB	VSS	SDQ_A63	SDQ_A58												AB
AA		HBREQ0#	HRS1#	SDQ_A59	SM_ SLEWIN1	VSS	HA35#	SDQ_B59	VSS	SDQ_B58	SDQ_B63	VCC_CL	VCC_CL	VCC_CL	AA
Y	HHITM#	VSS		HTRDY#	HA34#	HA33#	VSS	HA32#	VSS	HA29#	VSS	VCC_CL_ PLL	VCC_CL	VCC_CL	Y
W		HBNR#	HDRDY#	HADS#											W
V	VSS	HA30#	HLOCK#		VSS	HA31#	VSS	HA22#	HA28#	VSS	HA27#	VSS	RSVD	VCC_CL	V
U		HHIT#	HRS0#	HDBSY#	HRS2#	VSS	HA17#	HA24#	VSS	HADSTB1#	HA25#	HCLKN	RSVD	RSVD	U
T	HDEFER#	VSS													T
R		HD4	HD2#	HD0#	HA21#	HA23#	HA19#	VSS	HA26#	HA14#	VSS	HCLKP	VSS	RSVD	R
P	VSS	HA20#	HD1#											VSS	P
N		HD7	HD6#	HD3#	HA18#	HA16#	HA12#	VSS	HA15#	HA10#	VSS	HA9#	VSS		N
M	HDSTBN0#	VSS		HDINV0#	HD5#	HA11#	VSS	HA13#	VSS	HADSTB0#	VSS		HD34#		M
L		HD10#	HD8#	HDSTBP0#	HA4#	HREQ2#	HA6#	HA7#	HREQ1#		VSS	VSS	VSS		L
K	VSS	HA8#	HD12#									HD29#	HD36#		K
J		HA3#	HD11#	HA5#	HD9#	VSS	HREQ4#		VSS		HDINV1#	VSS	HD32#		J
H											HDSTBN1#	HD30#	VSS		H
G	HREQ3#	VSS		HD13#	HBPRI#	VSS	HD19#		HDSTBP1#		HD25#	VSS	HD37#		G
F		HD15#	HD14#	HREQ0#		HD18#	VSS		VSS		HD27#	HD33#	HD39#		F
E	VSS	HD20#	HD50#		HD21#		HD22#		HD28#		HDINV3#	VSS	HD35#		E
D		HD52#	HD17#	VSS		HDSTBN3#	HD57#		HD54#		HD59#	HD63#	VSS		D
C	VSS	HD16#		HD53#	HD23#	HD56#			HD49#	HD60#	HD48#		HCPURST#	VTT	C
B	NC	NC	HD51#	HD55#	HD24#	HDSTBP3#	VSS		HD61#	HD31#	HD58#	VSS	VSS	VTT	B
A	TEST2	NC	VSS		VSS		HD26#			VSS		HD62#		VTT	A
	43	42	41	40	39	38	37	36	35	34	33	32	31	30	

Figure 12-2. (G)MCH Ballout Diagram (Top View Middle– Columns 29–15)

	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	
BC		VSS		VCCSM		VSS		VCCSM		SCKE_A0		VCCSM		SMA_B3		BC
BB	SODT_B2	VCCSM	SCS_B0#	VCCSM	SMA_A1	VCCSM	SMA_A8	SMA_A11	SBS_A2	VCCSM	RSVD	VCCSM	SMA_B0	VCCSM	SMA_B6	BB
BA	SODT_B0		SWE_B#	SMA_A2	SMA_A3		SMA_A5	SMA_A9	SMA_A14		SCKE_A3	SBS_B1	SMA_B2		SMA_B5	BA
AY	SMA_B13		SCS_B2#		SMA_A4	SMA_A6	SMA_A7		SCKE_A2	SCKE_A1	SBS_B0		SMA_B1		SMA_B8	AY
AW	SCAS_B#		SCLK_B4#	SRAS_B#		VCCSM	SDQ_B29		SMA_A12	VCCSM		SMA_B10	SDQ_B23		SMA_B4	AW
AV	SCLK_B4		VSS	VCCSM		SDQ_B24	VSS		VSS	SDQ_A31		VCCSM	VSS		SDQ_B22	AV
AU	SCLK_B3		SCLK_B1	SDQS_B3#		VSS	SDQ_B28		SDQ_A26	VSS		SDQS_A3#	SDQ_B18		SDQ_B16	AU
AT	VSS		SCLK_B1#	SDQ_B26		SDQS_B3	SDQ_B25		SDQ_A27	SDQS_A3		SDQ_A24	SDQ_B19		VSS	AT
AR	SCLK_B3#		VSS	VSS		SDQ_B30	VSS		VSS	VSS		SDQ_A25	VSS		SDQS_B2#	AR
AP	SCLK_A3		SCLK_A1	SDQ_B27		VSS	SDM_B3		SM_SLEWIN0	SDQ_A30		VSS	SDQ_A28		SDQS_B2	AP
AN	VSS		SCLK_A1#	SDQ_B31		VSS	VSS		RSVD	VSS		SDM_A3	SDQ_A29		VSS	AN
AM	VSS		SCLK_A4#	SCLK_A4		VSS	VSS		RSVD	VSS		RSTIN#	PWROK		CL_PWROK	AM
AL	VCC_CL		VCC_CL	VCC_CL		VCC_CL	VCC_CL		VCC_CL	VCC_CL		VCC_CL	VCC_CL		VCC_CL	AL
AK	VCC_CL		VCC_CL	VCC_CL		VCC_CL	VCC_CL		VCC_CL	VCC_CL		VCC_CL	VCC_CL		VCC_CL	AK
AJ	VCC_CL		VCC_CL	VCC_CL		VCC_CL	VCC_CL		VCC_CL	VCC_CL		VCC_CL	VCC_CL		VCC_CL	AJ
AH																AH
AG	VCC_CL		VCC_CL	VCC_CL	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC		VCC	AG
AF	VCC_CL		VCC_CL	VCC	VCC	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VCC		VCC	AF
AE			VCC	VCC	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC			AE
AD	VCC_CL		VCC	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VCC		VCC	AD
AC	VCC_CL		VCC	VCC	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC		VCC	AC
AB			VCC	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VCC			AB
AA	VCC_CL		VCC	VCC	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC		VCC	AA
Y	VCC_CL		VCC	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VCC		VCC	Y
W			VCC	VCC	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VCC	VCC			W
V	VCC_CL		VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC		VCC	V
U	VCC_CL		VCC_CL	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC		VCC	U
T																T
R	RSVD		VTT	VTT		VTT	VTT		VSS	VCC		VCC	VCC		VCC	R
P	VTT		VTT	VTT		VTT	VTT		VSS	VCC		VSS	VSS		VCC	P
N	VTT		VSS	VTT		VTT	VTT		VSS	NC		RSVD	RSVD		RSVD	N
M	VTT		VSS	HD47#		VTT	VTT		VSS	RSVD		RSVD	VSS		VSS	M
L	VSS		HD42#	HD45#		VTT	VTT		VSS	VSS		RSVD	RSVD		RSVD	L
K	HD38#		HD43#	VSS		VTT	VTT		VSS	ALLZTEST		VSS	RSVD		EXP_RXP1	K
J	HD40#		VSS	HD46#		VTT	VTT		VSS	BSEL1		BSEL2	EXP_EN		EXP_RXN1	J
H	VSS		HDSTBN2#	HD44#		VTT	VTT		VSS	VSS		RSVD	VSS		VSS	H
G	HDINV2#		HDSTBP2#	VTT		VTT	VTT		VSS	BSEL0		RSVD	SDVO_CTRLDATA		EXP_RXN0	G
F	HD41#		VSS	VTT		VTT	VTT		VSS	XORTEST		VSS	RSVD		EXP_RXP0	F
E	VTT		VTT	VTT		VSS	VTT		VSS	VSS		EXP_SLR	SDVO_CTRLCLK		VSS	E
D	VTT	VTT	VTT		HSCOMP#	HDVREF	HRCOMP		VSS	BLUE#	GREEN#		VSS	VSS	VSYNC	D
C	VTT		VTT	VSS	HSCOMP		VCCA_HPLL	VCCA_DPLLB	VCCD_CRT		GREEN	RED#	VCCA_DAC		HSYNC	C
B	VTT	VTT	VTT	VSS	HSWING	HACCVREF	VSS	VSS	VCCDQ_CRT	BLUE	VSS	RED	VCC3_3	VCCA_DAC	VCCA_EXPPLL	B
A		VTT		VSS		VCCA_MPLL		VCCA_DPLLA		REFSET		VSS		VCCA_EXP		A
	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	

Figure 12-3. (G)MCH Ballout Diagram (Top View Right – Columns 14–0)

	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
BC	VCCSM		SBS_B2		VSS			SDQ_A17		VSS		VSS	NC	TEST1	BC
BB	SMA_B9	SMA_B11	VCCSM	SCKE_B2	SDQ_A23	SDQS_A2		VSS	SDQ_A20	SDQ_A10	SDQ_A15	SDQS_A1	RSVD	NC	BB
BA	SMA_B7	SMA_B12		SCKE_B3	SDQ_A22	SDQS_A2#			SDQ_A21	SDQ_A14	SDQS_A1#		SDM_A1	VSS	BA
AY		SMA_B14	SCKE_B0	SDQ_A19		SDM_A2		SDQ_A16	SDQ_A11		VSS	SDQ_A9	SDQ_A8		AY
AW		SDM_B2	SCKE_B1	SDQ_A18		SDM_B1		SDQ_B3		SDQ_B2		SDQ_A13	SDQ_A12	VSS	AW
AV		SDQ_B17	SDQ_B14	VSS		VSS		VSS	SDQS_B0		SDQ_A7	SDQ_A2	SDQ_A3		AV
AU		SDQ_B20	SDQ_B15	SDQ_B9		SDQ_B13		SDQ_B7	VSS	SDQS_B0#	SDQS_A0		VSS	SDQ_A6	AU
AT		VSS	VSS	SDQ_B8											AT
AR		SDQ_B11	SDQS_B1	SDQ_B12		VSS		SDM_B0	VSS	SDQ_A0	SDQ_A1	SDQS_A0#	SDM_A0		AR
AP		SDQ_B10	SDQS_B1#									SDQ_A4	SDQ_A5	VSS	AP
AN		VSS	VSS	VSS		SDQ_B6	SDQ_B1	SDQ_B0	SDQ_B5	SDQ_B4	VSS	SRCOMP1	SRCOMP0		AN
AM		SDQ_B21		VSS	SMRCOMPVOH	VSS	SMRCOMPVOL	VSS	SVREF	CL_VREF	VSS		VSS	VSS	AM
AL		VCC_CL	VCC_CL	VCC_CL	VCC_CL	VCC_CL	VCC_CL	VCC_CL	VCC_CL	VCC_CL	VCC_CL	VCC_CL	VCC_CL		AL
AK	VCC_CL											VCC_CL	VCC_CL	VCC_CL	AK
AJ	VCC_CL	VCC_CL	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC		AJ
AH											VCC		VCC	VCC	AH
AG	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC		AG
AF	VCC	VCC	VCC	VCC	VSS	VSS	VSS	VSS	VSS	VSS		VSS	VSS	VSS	AF
AE											VCC_EXP	VCC_EXP	VCC_EXP		AE
AD	VCC	CL_CLK	CL_DATA	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP		VCC_EXP	VCC_EXP	AD
AC	VCC	VCC	EXP_COMPI	EXP_COMPO	VSS	DMI_TXN2	DMI_TXP2	VSS	VCC	VSS	VCC_EXP	VCC_EXP	VCC_EXP		AC
AB												DMI_RXP3	VSS	VSS	AB
AA	VCC	VCC	CL_RST#	RSVD	RSVD	RSVD	VSS	DMI_RXP2	DMI_RXN2	VSS	DMI_RXN3	VCC	DMI_TXN3		AA
Y	VCC	VCC	RSVD	VCC	VSS	DMI_RXN1	DMI_RXP1	VSS	VCC	VSS	DMI_TXN1		DMI_TXP3	VSS	Y
W											DMI_TXP1	VSS	DMI_RXP0		W
V	VCC	VCC	VCC	VSS	VCC	VCC	VSS	DMI_TXP0	DMI_TXN0	VSS		EXP_TXP15	VSS	DMI_RXN0	V
U	VCC	VCC	RSVD	RSVD	VCC	VCC	VSS	VSS	VCC	VSS	EXP_TXN15	VCC	EXP_TXP14		U
T											EXP_RXP14		EXP_TXN14	VSS	T
R	VCC	RSVD	RSVD	VSS	EXP_RXN13	EXP_RXP13	VSS	EXP_RXN15	EXP_RXP15	VSS	EXP_RXN14	VSS	EXP_TXP13		R
P	VCC											EXP_TXP12	VSS	EXP_TXN13	P
N		VSS	VCC	VCC	VSS	VCC	VCC	VSS	VCC	VSS	EXP_TXN12	VCC	EXP_TXP11		N
M		DDC_CLK		VSS	VSS	EXP_RXN10	EXP_RXP10	VSS	EXP_RXN12	EXP_RXP12	EXP_RXP11		EXP_TXN11	VSS	M
L		DDC_DATA	VCC	VSS		EXP_RXP9	EXP_RXN9	VSS	VCC	VSS	EXP_RXN11	VSS	EXP_TXP10		L
K		VSS	VSS									EXP_TXN9	VSS	EXP_TXN10	K
J		ICH_SYNC#	EXP_RXP3	EXP_RXP4		VSS		VSS	VCC	VSS	EXP_TXP9	VCC	VCC		J
H		VSS	EXP_RXN3	EXP_RXN4											H
G		VSS	VSS	VSS		VSS		VSS	EXP_RXP8	EXP_RXN8	EXP_TXN8		VCC	VSS	G
F		RSVD	EXP_RXP2	VCC		VCC		EXP_RXP5	EXP_RXN6		EXP_TXP8	VSS	EXP_TXP7		F
E		VSS	EXP_RXN2	VSS		VSS		EXP_RXN5		EXP_RXP6		VSS	EXP_TXN7	VSS	E
D		DREFCLKN	EXP_TXN0	EXP_TXP0		EXP_TXN2		EXP_TXP4	EXP_TXN4		VCC	VSS	EXP_RXN7		D
C	DREFCLKP	VCC		VSS	EXP_TXP2	VCC			VSS	VSS	VSS		EXP_RXP7	VSS	C
B	VSS	GCLKN	GCLKP	EXP_TXP1	VSS	EXP_TXP3		EXP_TXN3	EXP_TXN5	EXP_TXP5	EXP_TXN6	EXP_TXP6	NC		B
A	RSVD		VSS		EXP_TXN1			VSS		VSS		VSS			A
	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

Table 12-1. (G)MCH Ballout Sorted by Signal Name

Signal Name	Ball #
ALLZTEST	K20
BLUE	B20
BLUE#	D20
BSEL0	G20
BSEL1	J20
BSEL2	J18
CL_CLK	AD13
CL_DATA	AD12
CL_PWROK	AM15
CL_RST#	AA12
CL_VREF	AM5
DDC_CLK	M13
DDC_DATA	L13
DMI_RXN0	V1
DMI_RXN1	Y9
DMI_RXN2	AA6
DMI_RXN3	AA4
DMI_RXP0	W2
DMI_RXP1	Y8
DMI_RXP2	AA7
DMI_RXP3	AB3
DMI_TXN0	V6
DMI_TXN1	Y4
DMI_TXN2	AC9
DMI_TXN3	AA2
DMI_TXP0	V7
DMI_TXP1	W4
DMI_TXP2	AC8
DMI_TXP3	Y2
DREFCLKN	D13
DREFCLKP	C14
EXP_COMPI	AC12
EXP_COMPO	AC11
EXP_EN	J17
EXP_RXN0	G15
EXP_RXN1	J15
EXP_RXN2	E12
EXP_RXN3	H12
EXP_RXN4	H11
EXP_RXN5	E7
EXP_RXN6	F6
EXP_RXN7	D2
EXP_RXN8	G5
EXP_RXN9	L8
EXP_RXN10	M9
EXP_RXN11	L4
EXP_RXN12	M6
EXP_RXN13	R10
EXP_RXN14	R4
EXP_RXN15	R7
EXP_RXP0	F15
EXP_RXP1	K15
EXP_RXP2	F12
EXP_RXP3	J12
EXP_RXP4	J11
EXP_RXP5	F7
EXP_RXP6	E5
EXP_RXP7	C2
EXP_RXP8	G6
EXP_RXP9	L9
EXP_RXP10	M8
EXP_RXP11	M4
EXP_RXP12	M5
EXP_RXP13	R9
EXP_RXP14	T4
EXP_RXP15	R6
EXP_SLR	E18
EXP_TXN0	D12
EXP_TXN1	A10
EXP_TXN2	D9
EXP_TXN3	B7
EXP_TXN4	D6
EXP_TXN5	B6
EXP_TXN6	B4
EXP_TXN7	E2
EXP_TXN8	G4
EXP_TXN9	K3
EXP_TXN10	K1
EXP_TXN11	M2
EXP_TXN12	N4
EXP_TXN13	P1
EXP_TXN14	T2
EXP_TXN15	U4
EXP_TXP0	D11
EXP_TXP1	B11
EXP_TXP2	C10
EXP_TXP3	B9
EXP_TXP4	D7
EXP_TXP5	B5
EXP_TXP6	B3
EXP_TXP7	F2
EXP_TXP8	F4
EXP_TXP9	J4
EXP_TXP10	L2
EXP_TXP11	N2
EXP_TXP12	P3
EXP_TXP13	R2
EXP_TXP14	U2
EXP_TXP15	V3
GCLKN	B13
GCLKP	B12
GREEN	C19

Signal Name	Ball #
GREEN#	D19
HA3#	J42
HA4#	L39
HA5#	J40
HA6#	L37
HA7#	L36
HA8#	K42
HA9#	N32
HA10#	N34
HA11#	M38
HA12#	N37
HA13#	M36
HA14#	R34
HA15#	N35
HA16#	N38
HA17#	U37
HA18#	N39
HA19#	R37
HA20#	P42
HA21#	R39
HA22#	V36
HA23#	R38
HA24#	U36
HA25#	U33
HA26#	R35
HA27#	V33
HA28#	V35
HA29#	Y34
HA30#	V42
HA31#	V38
HA32#	Y36
HA33#	Y38
HA34#	Y39
HA35#	AA37
HACCVREF	B24

Signal Name	Ball #
HADS#	W40
HADSTB0#	M34
HADSTB1#	U34
HBNR#	W42
HBPRI#	G39
HBREQ0#	AA42
HCLKN	U32
HCLKP	R32
HCPURST#	C31
HD0#	R40
HD1#	P41
HD2#	R41
HD3#	N40
HD5#	M39
HD6#	N41
HD7#	N42
HD8#	L41
HD9#	J39
HD10#	L42
HD11#	J41
HD12#	K41
HD13#	G40
HD14#	F41
HD15#	F42
HD16#	C42
HD17#	D41
HD18#	F38
HD19#	G37
HD20#	E42
HD21#	E39
HD22#	E37
HD23#	C39
HD24#	B39
HD25#	G33
HD26#	A37

Signal Name	Ball #
HD27#	F33
HD28#	E35
HD29#	K32
HD30#	H32
HD31#	B34
HD32#	J31
HD33#	F32
HD34#	M31
HD35#	E31
HD36#	K31
HD37#	G31
HD38#	K29
HD39#	F31
HD4#	R42
HD40#	J29
HD41#	F29
HD42#	L27
HD43#	K27
HD44#	H26
HD45#	L26
HD46#	J26
HD47#	M26
HD48#	C33
HD49#	C35
HD50#	E41
HD51#	B41
HD52#	D42
HD53#	C40
HD54#	D35
HD55#	B40
HD56#	C38
HD57#	D37
HD58#	B33
HD59#	D33
HD60#	C34

Signal Name	Ball #
HD61#	B35
HD62#	A32
HD63#	D32
HDBSY#	U40
HDEFER#	T43
HDINV0#	M40
HDINV1#	J33
HDINV2#	G29
HDINV3#	E33
HDRDY#	W41
HDSTBN0#	M43
HDSTBN1#	H33
HDSTBN2#	H27
HDSTBN3#	D38
HDSTBP0#	L40
HDSTBP1#	G35
HDSTBP2#	G27
HDSTBP3#	B38
HDVREF	D24
HHIT#	U42
HHITM#	Y43
HLOCK#	V41
HRCOMP	D23
HREQ0#	F40
HREQ1#	L35
HREQ2#	L38
HREQ3#	G43
HREQ4#	J37
HRS0#	U41
HRS1#	AA41
HRS2#	U39
HSCOMP	C25
HSCOMP#	D25
HSWING	B25
HSYNC	C15

Signal Name	Ball #
HTRDY#	Y40
ICH_SYNC#	J13
NC	BC42
NC	BC2
NC	BB43
NC	BB1
NC	B43
NC	B42
NC	B2
NC	N20
NC	A42
PWROK	AM17
RED	B18
RED#	C18
REFSET	A20
RSVD	AJ32
RSVD	V31
RSVD	AL31
RSVD	A14
RSVD	F13
RSVD	F17
RSVD	H18
RSVD	K17
RSVD	G18
RSVD	M18
RSVD	L18
RSVD	L15
RSVD	M20
RSVD	N15
RSVD	N18
RSVD	N17
RSVD	L17
RSVD	Y12
RSVD	AA9
RSVD	AA10

Signal Name	Ball #
RSVD	AA11
RSVD	R29
RSVD	R30
RSVD	U30
RSVD	U31
RSVD	R13
RSVD	R12
RSVD	U11
RSVD	U12
RSVD	AA39
RSVD	AP21
RSVD	AW42
RSVD	BB2
RSVD	AF32
RSVD	AG32
RSVD	BB19
RSVD	AM21
RSVD	AM31
RSVD	AN32
RSVD	AN21
RSTIN#	AM18
SBS_A0	BA33
SBS_A1	AW32
SBS_A2	BB21
SBS_B0	AY19
SBS_B1	BA18
SBS_B2	BC12
SCAS_A#	AY35
SCAS_B#	AW29
SCKE_A0	BC20
SCKE_A1	AY20
SCKE_A2	AY21
SCKE_A3	BA19
SCKE_B0	AY12
SCKE_B1	AW12

Signal Name	Ball #
SCKE_B2	BB11
SCKE_B3	BA11
SCLK_A0	AU31
SCLK_A0#	AR31
SCLK_A1	AP27
SCLK_A1#	AN27
SCLK_A2	AV33
SCLK_A2#	AW33
SCLK_A3	AP29
SCLK_A3#	AP31
SCLK_A4	AM26
SCLK_A4#	AM27
SCLK_A5	AT33
SCLK_A5#	AU33
SCLK_B0	AV31
SCLK_B0#	AW31
SCLK_B1	AU27
SCLK_B1#	AT27
SCLK_B2	AV32
SCLK_B2#	AT32
SCLK_B3	AU29
SCLK_B3#	AR29
SCLK_B4	AV29
SCLK_B4#	AW27
SCLK_B5	AN33
SCLK_B5#	AP32
SCS_A0#	AW35
SCS_A1#	BA35
SCS_A2#	BA34
SCS_A3#	BB38
SCS_B0#	BB27
SCS_B1#	BB30
SCS_B2#	AY27
SCS_B3#	AY31
SDM_A0	AR2

Signal Name	Ball #
SDM_A1	BA2
SDM_A2	AY9
SDM_A3	AN18
SDM_A4	AU43
SDM_A5	AM43
SDM_A6	AG40
SDM_A7	AC40
SDM_B0	AR7
SDM_B1	AW9
SDM_B2	AW13
SDM_B3	AP23
SDM_B4	AU37
SDM_B5	AM37
SDM_B6	AG39
SDM_B7	AD38
SDQ_A0	AR5
SDQ_A1	AR4
SDQ_A2	AV3
SDQ_A3	AV2
SDQ_A4	AP3
SDQ_A5	AP2
SDQ_A6	AU1
SDQ_A7	AV4
SDQ_A8	AY2
SDQ_A9	AY3
SDQ_A10	BB5
SDQ_A11	AY6
SDQ_A12	AW2
SDQ_A13	AW3
SDQ_A14	BA5
SDQ_A15	BB4
SDQ_A16	AY7
SDQ_A17	BC7
SDQ_A18	AW11
SDQ_A19	AY11

Signal Name	Ball #
SDQ_A20	BB6
SDQ_A21	BA6
SDQ_A22	BA10
SDQ_A23	BB10
SDQ_A24	AT18
SDQ_A25	AR18
SDQ_A26	AU21
SDQ_A27	AT21
SDQ_A28	AP17
SDQ_A29	AN17
SDQ_A30	AP20
SDQ_A31	AV20
SDQ_A32	AV42
SDQ_A33	AU40
SDQ_A34	AP42
SDQ_A35	AN39
SDQ_A36	AV40
SDQ_A37	AV41
SDQ_A38	AR42
SDQ_A39	AP41
SDQ_A40	AN41
SDQ_A41	AM39
SDQ_A42	AK42
SDQ_A43	AK41
SDQ_A44	AN40
SDQ_A45	AN42
SDQ_A46	AL42
SDQ_A47	AL39
SDQ_A48	AJ40
SDQ_A49	AH43
SDQ_A50	AF39
SDQ_A51	AE40
SDQ_A52	AJ42
SDQ_A53	AJ41
SDQ_A54	AF41

Signal Name	Ball #
SDQ_A55	AF42
SDQ_A56	AD40
SDQ_A57	AD43
SDQ_A58	AB41
SDQ_A59	AA40
SDQ_A60	AE42
SDQ_A61	AE41
SDQ_A62	AC39
SDQ_A63	AB42
SDQ_B0	AN7
SDQ_B1	AN8
SDQ_B2	AW5
SDQ_B3	AW7
SDQ_B4	AN5
SDQ_B5	AN6
SDQ_B6	AN9
SDQ_B7	AU7
SDQ_B8	AT11
SDQ_B9	AU11
SDQ_B10	AP13
SDQ_B11	AR13
SDQ_B12	AR11
SDQ_B13	AU9
SDQ_B14	AV12
SDQ_B15	AU12
SDQ_B16	AU15
SDQ_B17	AV13
SDQ_B18	AU17
SDQ_B19	AT17
SDQ_B20	AU13
SDQ_B21	AM13
SDQ_B22	AV15
SDQ_B23	AW17
SDQ_B24	AV24
SDQ_B25	AT23

Signal Name	Ball #
SDQ_B26	AT26
SDQ_B27	AP26
SDQ_B28	AU23
SDQ_B29	AW23
SDQ_B30	AR24
SDQ_B31	AN26
SDQ_B32	AW37
SDQ_B33	AV38
SDQ_B34	AN36
SDQ_B35	AN37
SDQ_B36	AU35
SDQ_B37	AR35
SDQ_B38	AN35
SDQ_B39	AR37
SDQ_B40	AM35
SDQ_B41	AM38
SDQ_B42	AJ34
SDQ_B43	AL38
SDQ_B44	AR39
SDQ_B45	AM34
SDQ_B46	AL37
SDQ_B47	AL32
SDQ_B48	AG38
SDQ_B49	AJ38
SDQ_B50	AF35
SDQ_B51	AF33
SDQ_B52	AJ37
SDQ_B53	AJ35
SDQ_B54	AG33
SDQ_B55	AF34
SDQ_B56	AD36
SDQ_B57	AC33
SDQ_B58	AA34
SDQ_B59	AA36
SDQ_B60	AD34

Signal Name	Ball #
SDQ_B61	AF38
SDQ_B62	AC34
SDQ_B63	AA33
SDQS_A0	AU4
SDQS_A0#	AR3
SDQS_A1	BB3
SDQS_A1#	BA4
SDQS_A2	BB9
SDQS_A2#	BA9
SDQS_A3	AT20
SDQS_A3#	AU18
SDQS_A4	AR41
SDQS_A4#	AR40
SDQS_A5	AL41
SDQS_A5#	AL40
SDQS_A6	AG42
SDQS_A6#	AG41
SDQS_A7	AC42
SDQS_A7#	AC41
SDQS_B0	AV6
SDQS_B0#	AU5
SDQS_B1	AR12
SDQS_B1#	AP12
SDQS_B2	AP15
SDQS_B2#	AR15
SDQS_B3	AT24
SDQS_B3#	AU26
SDQS_B4	AW39
SDQS_B4#	AU39
SDQS_B5	AL35
SDQS_B5#	AL34
SDQS_B6	AG35
SDQS_B6#	AG36
SDQS_B7	AC36
SDQS_B7#	AC37

Signal Name	Ball #
SDVO_CTRLCLK	E17
SDVO_CTRLDATA	G17
SMA_A0	BA31
SMA_A1	BB25
SMA_A2	BA26
SMA_A3	BA25
SMA_A4	AY25
SMA_A5	BA23
SMA_A6	AY24
SMA_A7	AY23
SMA_A8	BB23
SMA_A9	BA22
SMA_A10	AY33
SMA_A11	BB22
SMA_A12	AW21
SMA_A13	AY38
SMA_A14	BA21
SMA_B0	BB17
SMA_B1	AY17
SMA_B2	BA17
SMA_B3	BC16
SMA_B4	AW15
SMA_B5	BA15
SMA_B6	BB15
SMA_B7	BA14
SMA_B8	AY15
SMA_B9	BB14
SMA_B10	AW18
SMA_B11	BB13
SMA_B12	BA13
SMA_B13	AY29
SMA_B14	AY13
SMRCOMPVOH	AM10
SMRCOMPVOL	AM8

Signal Name	Ball #
SODT_A0	AY37
SODT_A1	BA38
SODT_A2	BB35
SODT_A3	BA39
SODT_B0	BA29
SODT_B1	BA30
SODT_B2	BB29
SODT_B3	BB31
SRAS_A#	BB33
SRAS_B#	AW26
SRCOMP0	AN2
SRCOMP1	AN3
SRCOMP2	BB40
SRCOMP3	BA40
SVREF	AM6
SWE_A#	BB34
SWE_B#	BA27
TEST0	BC43
TEST1	BC1
TEST2	A43
VCC	P20
VCC	Y11
VCC	AG25
VCC	AG24
VCC	AG23
VCC	AG22
VCC	AG21
VCC	AG20
VCC	AG19
VCC	AG18
VCC	AG17
VCC	AG15
VCC	AG14
VCC	AF26
VCC	AF25

Signal Name	Ball #
VCC	AF24
VCC	AF22
VCC	AF20
VCC	AF18
VCC	AF17
VCC	AF15
VCC	AF14
VCC	AE27
VCC	AE26
VCC	AE25
VCC	AE23
VCC	AE21
VCC	AE19
VCC	AE17
VCC	AD27
VCC	AD26
VCC	AD18
VCC	AD17
VCC	AD15
VCC	AD14
VCC	AC27
VCC	AC26
VCC	AC17
VCC	AC15
VCC	AC14
VCC	AB27
VCC	AB26
VCC	AB18
VCC	AB17
VCC	AA27
VCC	AA26
VCC	AA17
VCC	AA15
VCC	AA14
VCC	Y27

Signal Name	Ball #
VCC	Y26
VCC	Y18
VCC	Y17
VCC	Y15
VCC	Y14
VCC	W27
VCC	W26
VCC	W25
VCC	W23
VCC	W21
VCC	W19
VCC	W18
VCC	W17
VCC	V27
VCC	V26
VCC	V25
VCC	V24
VCC	V23
VCC	V22
VCC	V21
VCC	V20
VCC	V19
VCC	V18
VCC	V17
VCC	V15
VCC	V14
VCC	U26
VCC	U25
VCC	U24
VCC	U23
VCC	U22
VCC	U21
VCC	U20
VCC	U19
VCC	U18

Signal Name	Ball #
VCC	U17
VCC	U15
VCC	U14
VCC	R20
VCC	R18
VCC	R17
VCC	R15
VCC	R14
VCC	P15
VCC	P14
VCC	AJ12
VCC	AJ11
VCC	AJ10
VCC	AJ9
VCC	AJ8
VCC	AJ7
VCC	AJ6
VCC	AJ5
VCC	AJ4
VCC	AJ3
VCC	AJ2
VCC	AH4
VCC	AH2
VCC	AH1
VCC	AG13
VCC	AG12
VCC	AG11
VCC	AG10
VCC	AG9
VCC	AG8
VCC	AG7
VCC	AG6
VCC	AG5
VCC	AG4
VCC	AG3

Signal Name	Ball #
VCC	AG2
VCC	AF13
VCC	AF12
VCC	AF11
VCC	AD24
VCC	AD22
VCC	AD20
VCC	AC25
VCC	AC23
VCC	AC21
VCC	AC19
VCC	AC13
VCC	AC6
VCC	AB24
VCC	AB22
VCC	AB20
VCC	AA25
VCC	AA23
VCC	AA21
VCC	AA19
VCC	AA13
VCC	AA3
VCC	Y24
VCC	Y22
VCC	Y20
VCC	Y13
VCC	Y6
VCC	V13
VCC	V12
VCC	V10
VCC	V9
VCC	U13
VCC	U10
VCC	U9
VCC	U6

Signal Name	Ball #
VCC	U3
VCC	N12
VCC	N11
VCC	N9
VCC	N8
VCC	N6
VCC	N3
VCC	L6
VCC	J6
VCC	J3
VCC	J2
VCC	G2
VCC	F11
VCC	F9
VCC	D4
VCC	C13
VCC	C9
VCC	L12
VCC_CL	AJ26
VCC_CL	AJ24
VCC_CL	AJ23
VCC_CL	AJ21
VCC_CL	AJ20
VCC_CL	AJ18
VCC_CL	AJ17
VCC_CL	AJ15
VCC_CL	AJ14
VCC_CL	AA30
VCC_CL	AA29
VCC_CL	Y30
VCC_CL	Y29
VCC_CL	V30
VCC_CL	V29
VCC_CL	U29
VCC_CL	U27

Signal Name	Ball #
VCC_CL	AL12
VCC_CL	AL11
VCC_CL	AL10
VCC_CL	AL9
VCC_CL	AL8
VCC_CL	AL7
VCC_CL	AL6
VCC_CL	AL5
VCC_CL	AL4
VCC_CL	AL3
VCC_CL	AL2
VCC_CL	AK26
VCC_CL	AK24
VCC_CL	AK23
VCC_CL	AK21
VCC_CL	AK20
VCC_CL	AK18
VCC_CL	AK17
VCC_CL	AK15
VCC_CL	AK3
VCC_CL	AK2
VCC_CL	AK1
VCC_CL	AJ13
VCC_CL	AD31
VCC_CL	AC31
VCC_CL	AA31
VCC_CL	Y31
VCC_CL	AJ30
VCC_CL	AJ29
VCC_CL	AJ27
VCC_CL	AG30
VCC_CL	AG29
VCC_CL	AG27
VCC_CL	AG26
VCC_CL	AF30

Signal Name	Ball #
VCC_CL	AF29
VCC_CL	AF27
VCC_CL	AD30
VCC_CL	AD29
VCC_CL	AC30
VCC_CL	AC29
VCC_CL	AL26
VCC_CL	AL24
VCC_CL	AL23
VCC_CL	AL21
VCC_CL	AL20
VCC_CL	AL18
VCC_CL	AL17
VCC_CL	AL15
VCC_CL	AK30
VCC_CL	AK29
VCC_CL	AK27
VCC_CL	AJ31
VCC_CL	AG31
VCC_CL	AF31
VCC_CL	AD32
VCC_CL	AC32
VCC_CL	AA32
VCC_CL	AL29
VCC_CL	AL27
VCC_CL	AL13
VCC_CL	AK14
VCC_CL_PLL	Y32
VCC_EXP	AD11
VCC_EXP	AD10
VCC_EXP	AD9
VCC_EXP	AD8
VCC_EXP	AD7
VCC_EXP	AD6
VCC_EXP	AD5

Signal Name	Ball #
VCC_EXP	AD4
VCC_EXP	AD2
VCC_EXP	AD1
VCC_EXP	AC4
VCC_EXP	AC3
VCC_EXP	AC2
VCC_EXP	AE4
VCC_EXP	AE3
VCC_EXP	AE2
VCC_SMCLK	BB42
VCC_SMCLK	BA43
VCC_SMCLK	BB41
VCC_SMCLK	BA42
VCC_SMCLK	AY42
VCC3_3	B17
VCCA_DAC	C17
VCCA_DAC	B16
VCCA_DPLLA	A22
VCCA_DPLLB	C22
VCCA_EXP	A16
VCCA_EXPPLL	B15
VCCA_HPLL	C23
VCCA_MPLL	A24
VCCD_CRT	C21
VCCDQ_CRT	B21
VCCSM	BC39
VCCSM	BC34
VCCSM	BC30
VCCSM	BC26
VCCSM	BC22
VCCSM	BC18
VCCSM	BC14
VCCSM	BB39
VCCSM	BB37
VCCSM	BB32

Signal Name	Ball #
VCCSM	BB28
VCCSM	BB26
VCCSM	BB24
VCCSM	BB20
VCCSM	BB18
VCCSM	BB16
VCCSM	BB12
VCCSM	AY32
VCCSM	AW24
VCCSM	AW20
VCCSM	AV26
VCCSM	AV18
VSS	D16
VSS	BC41
VSS	BC3
VSS	BA1
VSS	AY40
VSS	AF23
VSS	AF21
VSS	AF19
VSS	AE24
VSS	AE22
VSS	AE20
VSS	AE18
VSS	AC18
VSS	AA18
VSS	W24
VSS	W22
VSS	W20
VSS	R21
VSS	E1
VSS	C43
VSS	C1
VSS	A41
VSS	A5

Signal Name	Ball #
VSS	A3
VSS	BC37
VSS	BC32
VSS	BC28
VSS	BC24
VSS	BC10
VSS	BC5
VSS	BB7
VSS	AY41
VSS	AY4
VSS	AW43
VSS	AW41
VSS	AW1
VSS	AV37
VSS	AV35
VSS	AV27
VSS	AV23
VSS	AV21
VSS	AV17
VSS	AV11
VSS	AV9
VSS	AV7
VSS	AU42
VSS	AU38
VSS	AU32
VSS	AU24
VSS	AU20
VSS	AU6
VSS	AU2
VSS	AT31
VSS	AT29
VSS	AT15
VSS	AT13
VSS	AT12
VSS	AR38

Signal Name	Ball #
VSS	AR33
VSS	AR32
VSS	AR27
VSS	AR26
VSS	AR23
VSS	AR21
VSS	AR20
VSS	AR17
VSS	AR9
VSS	AR6
VSS	AP43
VSS	AP24
VSS	AP18
VSS	AP1
VSS	AN38
VSS	AN31
VSS	AN29
VSS	AN24
VSS	AN23
VSS	AN20
VSS	AN15
VSS	AN13
VSS	AN12
VSS	AN11
VSS	AN4
VSS	AM42
VSS	AM40
VSS	AM36
VSS	AM33
VSS	AM29
VSS	AM24
VSS	AM23
VSS	AM20
VSS	AM11
VSS	AM9

Signal Name	Ball #
VSS	AM7
VSS	AM4
VSS	AM2
VSS	AM1
VSS	AL36
VSS	AL33
VSS	AK43
VSS	AJ39
VSS	AJ36
VSS	AJ33
VSS	AH42
VSS	AG37
VSS	AG34
VSS	AF43
VSS	AF37
VSS	AF36
VSS	AF10
VSS	AF9
VSS	AF8
VSS	AF7
VSS	AF6
VSS	AF5
VSS	AF3
VSS	AF2
VSS	AF1
VSS	AD42
VSS	AD39
VSS	AD37
VSS	AD35
VSS	AD33
VSS	AD25
VSS	AD23
VSS	AD21
VSS	AD19
VSS	AC38

Signal Name	Ball #
VSS	AC35
VSS	AC24
VSS	AC22
VSS	AC20
VSS	AC10
VSS	AC7
VSS	AC5
VSS	AB43
VSS	AB25
VSS	AB23
VSS	AB21
VSS	AB19
VSS	AB2
VSS	AB1
VSS	AA38
VSS	AA35
VSS	AA24
VSS	AA22
VSS	AA20
VSS	AA8
VSS	AA5
VSS	Y42
VSS	Y37
VSS	Y35
VSS	Y33
VSS	Y25
VSS	Y23
VSS	Y21
VSS	Y19
VSS	Y10
VSS	Y7
VSS	Y5
VSS	Y1
VSS	W3
VSS	V43

Signal Name	Ball #
VSS	V39
VSS	V37
VSS	V34
VSS	V32
VSS	V11
VSS	V8
VSS	V5
VSS	V2
VSS	U38
VSS	U35
VSS	U8
VSS	U7
VSS	U5
VSS	T42
VSS	T1
VSS	R36
VSS	R33
VSS	R31
VSS	R11
VSS	R8
VSS	R5
VSS	R3
VSS	P43
VSS	P30
VSS	P21
VSS	P18
VSS	P17
VSS	P2
VSS	N36
VSS	N33
VSS	N31
VSS	N27
VSS	N21
VSS	N13
VSS	N10

Signal Name	Ball #
VSS	N7
VSS	N5
VSS	M42
VSS	M37
VSS	M35
VSS	M33
VSS	M27
VSS	M21
VSS	M17
VSS	M15
VSS	M10
VSS	M7
VSS	M1
VSS	L33
VSS	L32
VSS	L31
VSS	L29
VSS	L21
VSS	L20
VSS	L11
VSS	L7
VSS	L5
VSS	L3
VSS	K43
VSS	K26
VSS	K21
VSS	K18
VSS	K13
VSS	K12
VSS	K2
VSS	J38
VSS	J35
VSS	J32
VSS	J27
VSS	J21

Signal Name	Ball #
VSS	J9
VSS	J7
VSS	J5
VSS	H31
VSS	H29
VSS	H21
VSS	H20
VSS	H17
VSS	H15
VSS	H13
VSS	G42
VSS	G38
VSS	G32
VSS	G21
VSS	G13
VSS	G12
VSS	G11
VSS	G9
VSS	G7
VSS	G1
VSS	F37
VSS	F35
VSS	F27
VSS	F21
VSS	F18
VSS	F3
VSS	E43
VSS	E32
VSS	E24
VSS	E21
VSS	E20
VSS	E15
VSS	E13
VSS	E11
VSS	E9

Signal Name	Ball #
VSS	E3
VSS	D40
VSS	D31
VSS	D21
VSS	D17
VSS	D3
VSS	C26
VSS	C11
VSS	C6
VSS	C5
VSS	C4
VSS	B37
VSS	B32
VSS	B31
VSS	B26
VSS	B23
VSS	B22
VSS	B19
VSS	B14
VSS	B10
VSS	A39
VSS	A34
VSS	A26
VSS	A18
VSS	A12

Signal Name	Ball #
VSS	A7
VSS	M11
VSYNC	D15
VTT	R27
VTT	R26
VTT	R24
VTT	R23
VTT	P29
VTT	P27
VTT	P26
VTT	P24
VTT	P23
VTT	N29
VTT	N26
VTT	N24
VTT	N23
VTT	M29
VTT	M24
VTT	M23
VTT	L24
VTT	L23
VTT	K24
VTT	K23
VTT	J24
VTT	J23

Signal Name	Ball #
VTT	H24
VTT	H23
VTT	G26
VTT	G24
VTT	G23
VTT	F26
VTT	F24
VTT	F23
VTT	E29
VTT	E27
VTT	E26
VTT	E23
VTT	D29
VTT	D28
VTT	D27
VTT	C30
VTT	C29
VTT	C27
VTT	B30
VTT	B29
VTT	B28
VTT	B27
VTT	A30
VTT	A28
XORTEST	F20

12.2 Package Dimensions

The (G)MCH package measures 34 mm × 34 mm (see Figure 12-4). The 1226 balls are located in a non-grid pattern (see Figure 12-5). For additional details, refer to the *Intel® 965 and Q963 Express Chipset Family Thermal and Mechanical Design Guide*.

Figure 12-4. (G)MCH Package Dimensions

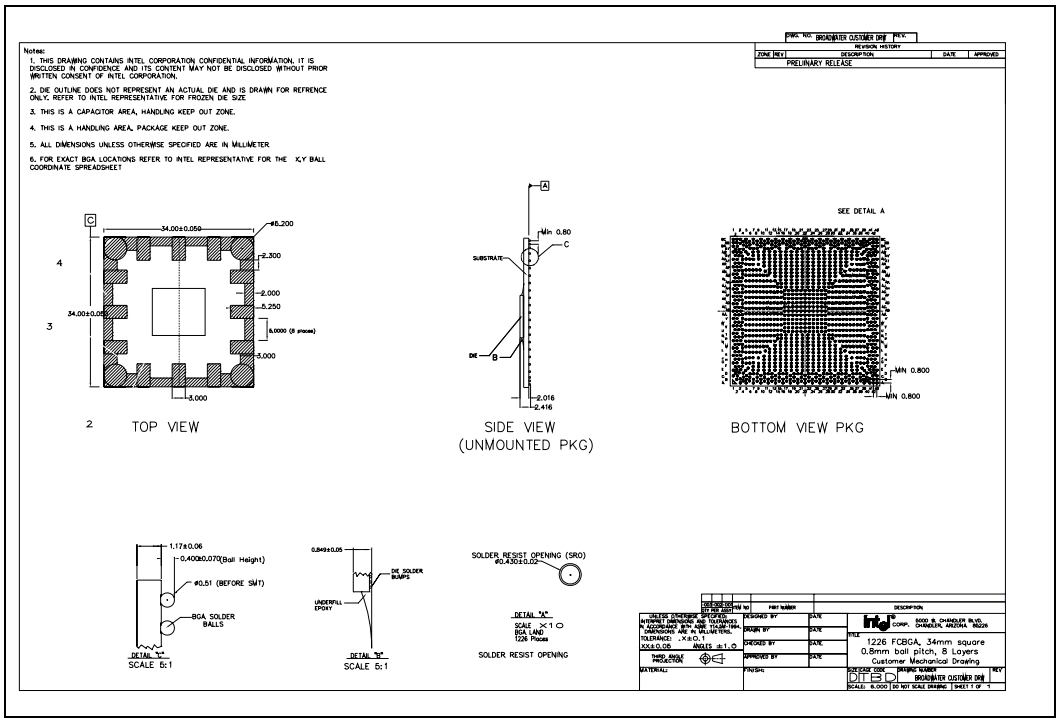
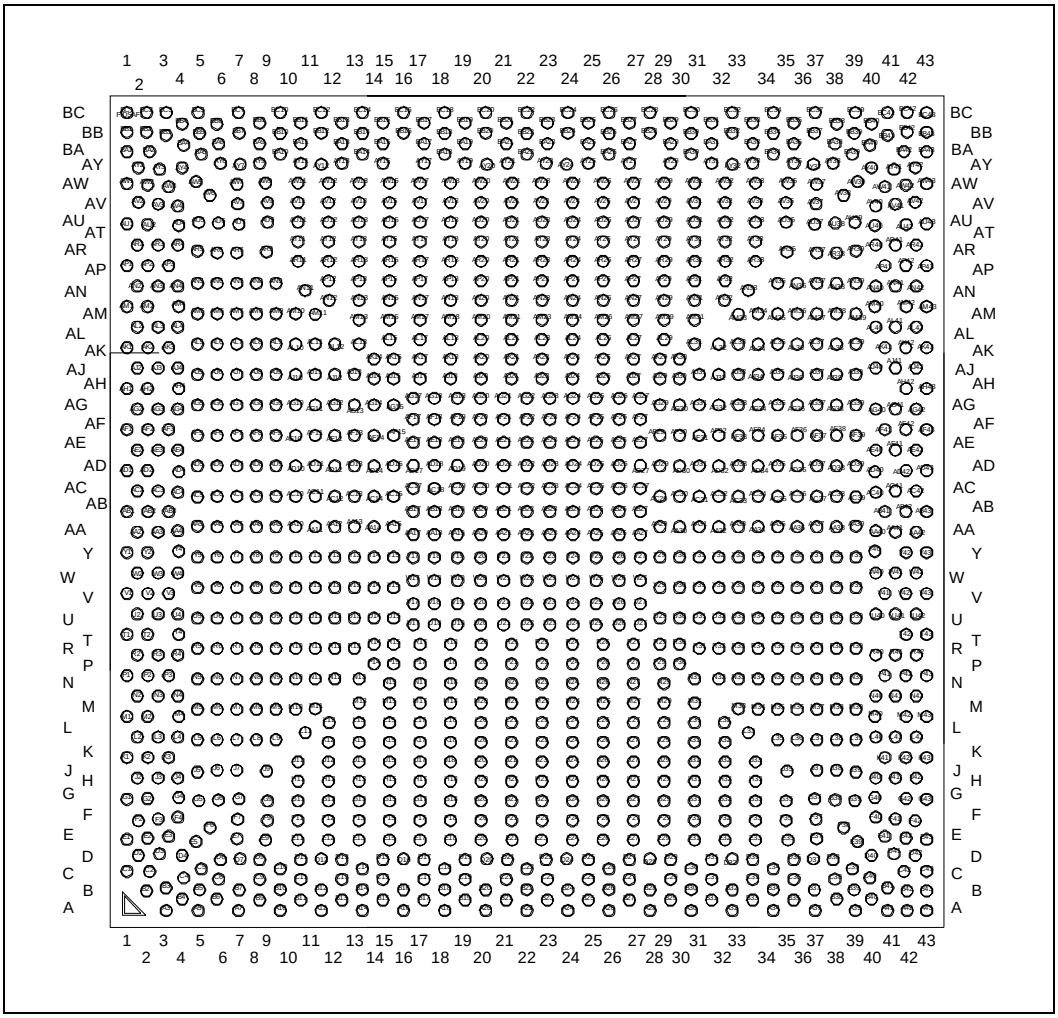


Figure 12-5. (G)MCH Non-Grid Ball Array



13 Testability

In the (G)MCH, testability for Automated Test Equipment (ATE) board level testing has been implemented as an XOR chain. An XOR-tree is a chain of XOR gates each with one input pin connected to it which allows for pad to ball to trace connection testing.

The XOR testing methodology is to boot the part using straps to enter XOR mode (A description of the boot process follows). Once in XOR mode, all of the pins of an XOR chain are driven to logic 1. This action will force the output of that XOR chain to either a 1 if the number of the pins making up the chain is even, and a 0 if the number of the pins making up the chain is odd.

Once a valid output is detected on the XOR chain output, a walking 0 pattern is moved from one end of the chain to the other. Every time the walking 0 is applied to a pin on the chain, the output will toggle. If the output does not toggle, there is a disconnect somewhere between die, package, and board and the system can be considered a failure.

13.1 XOR Test Mode Initialization

Figure 13-1. XOR Test Mode Initialization Cycles

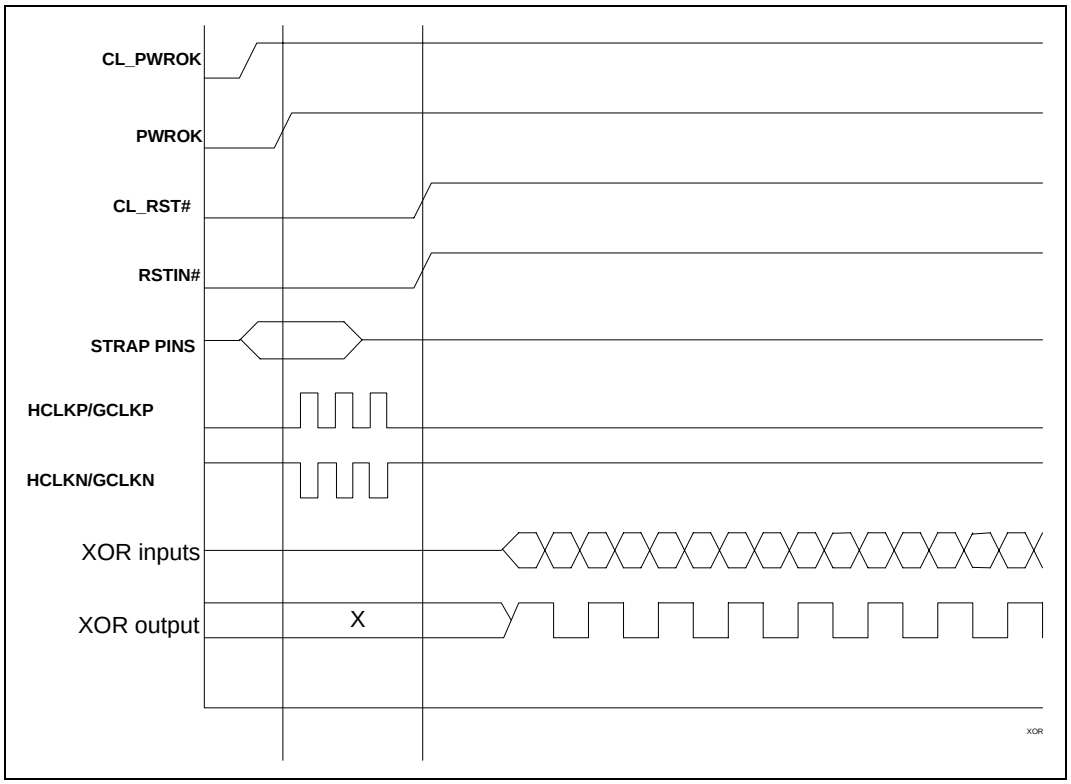


Figure 13-1 shows the wave forms to be able to boot the part into XOR mode. The straps that need to be controlled during this boot process are BSEL[2:0], SDVO_CTRLDATA, EXP_EM, EXP_SLR, and XORTEST.

On Q965, Q963, G965, P965 Express chipset platforms, all strap values must be driven before PWROK asserts. BSEL0 must be a 1. BSEL[2:1] need to be defined values, but logic value in any order will do. XORTEST must be driven to 0.

If SDVO is present in the design, SDVO_CTRLDATA must be pulled to logic 1. Depending on if Static Lane Reversal is used and if the SDVO/PCI Express Coexistence is selected, EXP_SLR and EXP_EN must be pulled in a valid manner.

Because of the different functionalities of the SDVO/PCI Express interface, not all of the pins will be used in all implementations. Due to the need to minimize test points and unnecessary routing, the XOR Chain 14 is dynamic depending on the values of SDVO_CTRLDATA, EXP_SLR, and EXP_EN. See Table 13-1 for what parts of XOR Chain 14 become valid XOR inputs depending on the use of SDVO_CTRLDATA, EXP_SLR, and EXP_EN.

Table 13-1. XOR Chain 14 functionality

SDVO_CTRLDATA	EXP_EN	EXP_SLR	XOR Chain 14
0	1	0	EXP_RXP[15:0] EXP_RXN[15:0] EXP_TXP[15:0] EXP_TXN[15:0]
0	1	1	EXP_RXP[15:0] EXP_RXN[15:0] EXP_TXP[15:0] EXP_TXN[15:0]
1	0	0	EXP_RXP[15:8] EXP_RXN[15:8] EXP_TXP[15:8] EXP_TXN[15:8]
1	0	1	EXP_RXP[7:0] EXP_RXN[7:0] EXP_TXP[7:0] EXP_TXN[7:0]
1	1	0	EXP_RXP[15:0] EXP_RXN[15:0] EXP_TXP[15:0] EXP_TXN[15:0]
1	1	1	EXP_RXP[15:0] EXP_RXN[15:0] EXP_TXP[15:0] EXP_TXN[15:0]

13.2 XOR Chain Definition

The (G)MCH chipset has 15 XOR chains. The XOR chain outputs are driven out on the following output pins. During full width testing, XOR chain outputs will be visible on both pins.

Table 13-2. XOR Chain Outputs

XOR Chain	Output Pins	Coordinate Location
xor_out0	ALLZTEST	K20
xor_out1	XORTEST	F20
xor_out2	ICH_SYNC#	J13
xor_out3	RSV	F17
xor_out4	RSV	AA9
xor_out5	RSV	AA10
xor_out6	BSEL1	J20
xor_out7	BSEL2	J18
xor_out8	RSV	AA11
xor_out9	RSV	Y12
xor_out10	EXP_SLR	E18
xor_out11	EXP_EN	J17
xor_out12	MTYPE	G18
xor_out13	RSV	K17
xor_out14	BSEL0	G20

13.3 XOR Chains

Table 13-3 through Table 13-17 show the XOR chains. Section 0 has a pin exclusion list.

Table 13-3. XOR Chain 0

Pin Count	Ball #	Signal Name
1	C35	HD49
2	D42	HD52
3	B35	HD61
4	B33	HD58
5	D37	HD57
6	A32	HD62
7	C33	HD48
8	D32	HD63
9	B40	HD55
10	D35	HD54
11	C38	HD56
12	C34	HD60
13	B41	HD51
14	E41	HD50
15	D33	HD59
16	C40	HD53
17	B34	HD31
18	C42	HD16
19	E39	HD21
20	E35	HD28
21	D41	HD17
22	C39	HD23
23	F33	HD27
24	E37	HD22
25	G33	HD25
26	F38	HD18
27	B39	HD24
28	G37	HD19
29	K32	HD29
30	H32	HD30
31	E42	HD20
32	A37	HD26
33	L27	HD42

Table 13-3. XOR Chain 0

Pin Count	Ball #	Signal Name
34	F31	HD39
35	F29	HD41
36	J26	HD46
37	E31	HD35
38	H26	HD44
39	K27	HD43
40	J31	HD32
41	F32	HD33
42	L26	HD45
43	J29	HD40
44	K31	HD36
45	M31	HD34
46	K29	HD38
47	G31	HD37
48	M26	HD47
49	J41	HD11
50	F42	HD15
51	G40	HD13
52	L42	HD10
53	F41	HD14
54	N42	HD7
55	K41	HD12
56	N41	HD6
57	J39	HD9
58	M39	HD5
59	N40	HD3
60	L41	HD8
61	P41	HD1
62	R40	HD0
63	R41	HD2
64	R42	HD4

Table 13-4. XOR Chain 1

Pin Count	Ball #	Signal Name
1	G43	HREQ4#
2	F40	HREQ0#
3	J42	HA3#
4	L36	HA7#
5	L37	HA6#
6	L35	HREQ1#
7	N32	HA9#
8	N35	HA15#
9	M36	HA13#
10	J40	HA5#
11	M34	HADSTB0#
12	M38	HA11#
13	N37	HA12#
14	G43	HREQ3#
15	K42	HA8#
16	N38	HA16#
17	L39	HA4#
18	L38	HREQ2#
19	N34	HA10#
20	R34	HA14#
21	R39	HA21#
22	N39	HA18#
23	V38	HA31#
24	Y36	HA32#
25	R42	HA20#
26	V35	HA28#
27	R38	HA23#
28	U33	HA25#
29	R37	HA19#
30	R35	HA26#
31	U34	HADSTB1#
32	Y38	HA33#
33	V42	HA30#
34	U36	HA24#
35	V36	HA22#
36	U37	HA17#
37	AA37	HA35#
38	Y39	HA34#
39	V33	HA27#
40	Y34	HA29#

Table 13-5. XOR Chain 2

Pin Count	Ball #	Signal Name
1	H33	HDSTBN1#
2	G35	HDSTBP1#
3	AA41	HRS1#
4	U42	HHIT#
5	Y40	HTRDY#
6	Y43	HHITM#
7	H27	HDSTBN2#
8	G27	HDSTBP2#
9	M43	HDSTBN0#
10	L40	HDSTBP0#
11	W42	HBNR#
12	G39	HBPRI#
13	V41	HLOCK#
14	C31	HCPURST#

Table 13-6. XOR Chain 3

Pin Count	Ball #	Signal Name
1	D38	HDSTBN3#
2	B38	HDSTBP3#
3	E33	HDINV3#
4	J33	HDINV1#
5	T43	HDEFER#
6	U41	HRS0#
7	W41	HDRDY#
8	U40	HDBSY#
9	U39	HRS2#
10	G29	HDINV2#
11	M40	HDINV0#
12	W40	HADS#
13	F40	HBREQ0#

Table 13-7. XOR Chain 4

Pin Count	Ball #	Signal Name
1	BA38	SODT_A1
2	BA35	SCS_A1#
3	AY37	SODT_A0
4	AW35	SCS_A0#
5	BA31	SMA_A0
6	AY33	SMA_A10
7	AY25	SMA_A4
8	BB25	SMA_A1
9	BA26	SMA_A2
10	BA25	SMA_A3
11	AV33	SCLK_A2
12	AW33	SCLK_A2#
13	AU31	SCLK_A0
14	AR31	SCLK_A0#
15	AN27	SCLK_A1#
16	AP27	SCLK_A1
17	BA23	SMA_A5
18	BA22	SMA_A9
19	BB23	SMA_A8
20	AY24	SMA_A6
21	BC20	SCKE_A0
22	AY23	SMA_A7
23	AY20	SCKE_A1
24	AU18	SDQS_A3#
25	AN18	SDM_A3
26	BA9	SDQS_A2#
27	AY9	SDM_A2
28	BA4	SDQS_A1#
29	BA2	SDM_A1
30	AR3	SDQS_A0#
31	AR2	SDM_A0

Table 13-8. XOR Chain 5

Pin Count	Ball #	Signal Name
1	AC41	SDQS_A7#
2	AC40	SDM_A7
3	AG41	SDQS_A6#
4	AG40	SDM_A6
5	AL40	SDQS_A5#
6	AM43	SDM_A5
7	AR40	SDQS_A4#
8	AU43	SDM_A4
9	AY38	SMA_A13
10	AY35	SCAS_A#
11	BB33	SRAS_A#
12	BA33	SBS_A0
13	BB34	SWE_A#
14	AW32	SBS_A1
15	BB22	SMA_A11
16	BA21	SMA_A14
17	BB21	SBS_A2
18	AW21	SMA_A12
19	AD12	CL_DATA
20	AD13	CL_CLK

Table 13-9. XOR Chain 6

Pin Count	Ball #	Signal Name
1	AC42	SDQS_A7
2	AD43	SDQ_A57
3	AB42	SDQ_A63
4	AE41	SDQ_A61
5	AE42	SDQ_A60
6	AD40	SDQ_A56
7	AC39	SDQ_A62
8	AB41	SDQ_A58
9	AA40	SDQ_A59
10	AG42	SDQS_A6
11	AF41	SDQ_A54
12	AE40	SDQ_A51
13	AJ42	SDQ_A52
14	AJ41	SDQ_A53
15	AF39	SDQ_A50
16	AJ40	SDQ_A48
17	AF42	SDQ_A55
18	AH43	SDQ_A49
19	AL41	SDQS_A5
20	AN40	SDQ_A44
21	AK41	SDQ_A43
22	AM39	SDQ_A41
23	AL39	SDQ_A47
24	AN41	SDQ_A40
25	AL42	SDQ_A46
26	AN42	SDQ_A45
27	AK42	SDQ_A42
28	AR41	SDQS_A4
29	AV42	SDQ_A32
30	AP42	SDQ_A34
31	AR42	SDQ_A38
32	AV41	SDQ_A37
33	AU40	SDQ_A33
34	AN39	SDQ_A35
35	AP41	SDQ_A39
36	AV40	SDQ_A36
37	AT20	SDQS_A3

Table 13-9. XOR Chain 6

Pin Count	Ball #	Signal Name
38	AV20	SDQ_A31
39	AU21	SDQ_A26
40	AT18	SDQ_A24
41	AR18	SDQ_A25
42	AT21	SDQ_A27
43	AN17	SDQ_A29
44	AP20	SDQ_A30
45	AP17	SDQ_A28
46	BB9	SDQS_A2
47	AY11	SDQ_A19
48	BA10	SDQ_A22
49	BC7	SDQ_A17
50	BB10	SDQ_A23
51	AW11	SDQ_A18
52	BA6	SDQ_A21
53	BB6	SDQ_A20
54	AY7	SDQ_A16
55	BB3	SDQS_A1
56	BA5	SDQ_A14
57	AW2	SDQ_A12
58	BB5	SDQ_A10
59	BB4	SDQ_A15
60	AY6	SDQ_A11
61	AY3	SDQ_A9
62	AY2	SDQ_A8
63	AW3	SDQ_A13
64	AU4	SDQS_A0
65	AV4	SDQ_A7
66	AP2	SDQ_A5
67	AP3	SDQ_A4
68	AR4	SDQ_A1
69	AR5	SDQ_A0
70	AU1	SDQ_A6
71	AV2	SDQ_A3
72	AV3	SDQ_A2

Table 13-10. XOR Chain 7

Pin Count	Ball #	Signal Name
1	BA39	SODT_A3
2	BB38	SCS_A3#
3	BB35	SODT_A2
4	BA34	SCS_A2#
5	AP29	SCLK_A3
6	AP31	SCLK_A3#
7	AU33	SCLK_A5#
8	AT33	SCLK_A5
9	AM26	SCLK_A4
10	AM27	SCLK_A4#
11	AY21	SCKE_A2
12	BA19	SCKE_A3

Table 13-11. XOR Chain 8

Pin Count	Ball #	Signal Name
1	BB30	SCS_B1#
2	BA30	SODT_B1
3	BA29	SODT_B0
4	BB27	SCS_B0#
5	AV32	SCLK_B2
6	AT32	SCLK_B2#
7	AV31	SCLK_B0
8	AW31	SCLK_B0#
9	AU27	SCLK_B1
10	AT27	SCLK_B1#
11	AW18	SMA_B10
12	BB17	SMA_B0
13	AU26	SDQS_B3#
14	AP23	SDM_B3
15	BC16	SMA_B3
16	BA15	SMA_B5
17	AY17	SMA_B1
18	BA17	SMA_B2
19	AW15	SMA_B4
20	BB14	SMA_B9

Table 13-11. XOR Chain 8

Pin Count	Ball #	Signal Name
21	AY15	SMA_B8
22	BB15	SMA_B6
23	BA14	SMA_B7
24	AW12	SCKE_B1
25	AY12	SCKE_B0
26	AR15	SDQS_B2#
27	AW13	SDM_B2
28	AP12	SDQS_B1#
29	AW9	SDM_B1
30	AU5	SDQS_B0#
31	AR7	SDM_B0

Table 13-12. XOR Chain 9

Pin Count	Ball #	Signal Name
1	AC37	SDQS_B7#
2	AD38	SDM_B7
3	AG36	SDQS_B6#
4	AG39	SDM_B6
5	AL34	SDQS_B5#
6	AM37	SDM_B5
7	AU39	SDQS_B4#
8	AU37	SDM_B4
9	AY29	SMA_B13
10	AW29	SCAS_B#
11	BA27	SWE_B#
12	AW26	SRAS_B#
13	BA18	SBS_B1
14	AY19	SBS_B0
15	BB13	SMA_B11
16	BC12	SBS_B2
17	BA13	SMA_B12
18	AY13	SMA_B14

Table 13-13. XOR Chain 10

Pin Count	Ball #	Signal Name
1	AC36	SDQS_B7
2	AF38	SDQ_B61
3	AD36	SDQ_B56
4	AA36	SDQ_B59
5	AA33	SDQ_B63
6	AD34	SDQ_B60
7	AC34	SDQ_B62
8	AC33	SDQ_B57
9	AA34	SDQ_B58
10	AG35	SDQS_B6
11	AJ37	SDQ_B52
12	AJ38	SDQ_B49
13	AG38	SDQ_B48
14	AF34	SDQ_B55
15	AF33	SDQ_B51
16	AG33	SDQ_B54
17	AF35	SDQ_B50
18	AJ35	SDQ_B53
19	AL35	SDQS_B5
20	AL38	SDQ_B43
21	AL32	SDQ_B47
22	AR39	SDQ_B44
23	AJ34	SDQ_B42
24	AM38	SDQ_B41
25	AM35	SDQ_B40
26	AL37	SDQ_B46
27	AM34	SDQ_B45
28	AW39	SDQS_B4
29	AN37	SDQ_B35
30	AR37	SDQ_B39
31	AW37	SDQ_B32
32	AN36	SDQ_B34
33	AV38	SDQ_B33
34	AR35	SDQ_B37
35	AN35	SDQ_B38
36	AU35	SDQ_B36
37	AT24	SDQS_B3

Table 13-13. XOR Chain 10

Pin Count	Ball #	Signal Name
38	AP26	SDQ_B27
39	AW23	SDQ_B29
40	AR24	SDQ_B30
41	AV24	SDQ_B24
42	AT23	SDQ_B25
43	AT26	SDQ_B26
44	AN26	SDQ_B31
45	AU23	SDQ_B28
46	AP15	SDQS_B2
47	AU17	SDQ_B18
48	AW17	SDQ_B23
49	AV15	SDQ_B22
50	AT17	SDQ_B19
51	AU15	SDQ_B16
52	AM13	SDQ_B21
53	AV13	SDQ_B17
54	AU13	SDQ_B20
55	AR12	SDQS_B1
56	AP13	SDQ_B10
57	AU12	SDQ_B15
58	AV12	SDQ_B14
59	AR13	SDQ_B11
60	AU11	SDQ_B9
61	AT11	SDQ_B8
62	AU9	SDQ_B13
63	AR11	SDQ_B12
64	AV6	SDQS_B0
65	AN6	SDQ_B5
66	AN8	SDQ_B1
67	AU7	SDQ_B7
68	AN9	SDQ_B6
69	AN7	SDQ_B0
70	AW5	SDQ_B2
71	AW7	SDQ_B3
72	AN5	SDQ_B4

Table 13-14. XOR Chain 11

Pin Count	Ball #	Signal Name
1	AY31	SCS_B3#
2	BB31	SODT_B3
3	AY27	SCS_B2#
4	BB29	SODT_B2
5	AV29	SCLK_B4
6	AP32	SCLK_B5#
7	AN33	SCLK_B5
8	AW27	SCLK_B4#
9	AR29	SCLK_B3#
10	ZU29	SCLK_B3
11	BA11	SCKE_B3
12	BB11	SCKE_B2

Table 13-15. XOR Chain 12

Pin Count	Ball #	Signal Name
1	G17	SDVO_CTRLDATA
2	E17	SDVO_CTRLCLK
3	L13	DDC_DATA
4	M13	DDC_CLK

Table 13-16. XOR Chain 13

Pin Count	Ball #	Signal Name
1	AA2	DMI_TXN3
2	Y2	DMI_TXP3
3	AA4	DMI_RXN3
4	AB3	DMI_RXP3
5	AC9	DMI_TXN2
6	AC8	DMI_TXP2
7	AA6	DMI_RXN2
8	AA7	DMI_RXP2
9	Y4	DMI_TXN1
10	W4	DMI_TXP1
11	Y9	DMI_RXN1
12	Y8	DMI_RXP1
13	V6	DMI_TXN0

Table 13-16. XOR Chain 13

Pin Count	Ball #	Signal Name
14	V7	DMI_TXP0
15	V1	DMI_RXN0
16	W2	DMI_RXP0

Table 13-17. XOR Chain 14

Pin Count	Ball #	Signal Name
1	U4	EXP_TXN15
2	V3	EXP_TXP15
3	R7	EXP_RXN15
4	R6	EXP_RXP15
5	T2	EXP_TXN14
6	U2	EXP_TXP14
7	R4	EXP_RXN14
8	T4	EXP_RXP14
9	P1	EXP_TXN13
10	R2	EXP_TXP13
11	R10	EXP_RXN13
12	R9	EXP_RXP13
13	N4	EXP_TXN12
14	P3	EXP_TXP12
15	M6	EXP_RXN12
16	M5	EXP_RXP12
17	M2	EXP_TXN11
18	N2	EXP_TXP11
19	L4	EXP_RXN11
20	M4	EXP_RXP11
21	K1	EXP_TXN10
22	L2	EXP_TXP10
23	M9	EXP_RXN10
24	M8	EXP_RXP10
25	K3	EXP_TXN9
26	J4	EXP_TXP9
27	L8	EXP_RXN9
28	L9	EXP_RXP9
29	G4	EXP_TXN8
30	F4	EXP_TXP8
31	G5	EXP_RXN8
32	G6	EXP_RXP8
33	E2	EXP_TXN7

Table 13-17. XOR Chain 14

Pin Count	Ball #	Signal Name
34	F2	EXP_TXP7
35	D2	EXP_RXN7
36	C2	EXP_RXP7
37	B4	EXP_TXN6
38	B3	EXP_TXP6
39	F6	EXP_RXN6
40	E5	EXP_RXP6
41	B6	EXP_TXN5
42	B5	EXP_TXP5
43	E7	EXP_RXN5
44	F7	EXP_RXP5
45	D6	EXP_TXN4
46	D7	EXP_TXP4
47	H11	EXP_RXN4
48	J11	EXP_RXP4
49	B7	EXP_TXN3
50	B9	EXP_TXP3

Table 13-17. XOR Chain 14

Pin Count	Ball #	Signal Name
51	H12	EXP_RXN3
52	J12	EXP_RXP3
53	D9	EXP_TXN2
54	C10	EXP_TXP2
55	E12	EXP_RXN2
56	F12	EXP_RXP2
57	A10	EXP_TXN1
58	B11	EXP_TXP1
59	J15	EXP_RXN1
60	K15	EXP_RXP1
61	D12	EXP_TXN0
62	D11	EXP_TXP0
63	G15	EXP_RXN0
64	F15	EXP_RXP0

13.4 PADs Excluded from XOR Mode(s)

A large number of pads do not support XOR testing. The majority of the pads that fall into this category are analog related pins (see Table 13-18).

Table 13-18. XOR Pad Exclusion List

PCI Express*	FSB	SM	Miscellaneous
GCLKN	HCLKN	SRCOMP[3 :0]	RED
GCLKP	HCLKP	SVREF	RED#
EXP_COMPO	HRCOMP	SMRCOMPVOL	GREEN
EXP_COMPI	HSCOMP	SMRCOMPVOH	GREEN#
	HSCOMP#		BLUE
	HSWING		BLUE#
	HDVREF		DREFCLKN
	HACCVREF		DREFCLKP
			REFSET
			HSYNC
			VSYNC
			DREFCLKN
			DREFCLKP
			TEST[2 :0]
			CL_DATA
			CL_CLK
			CL_VREF

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