80960CF-40, -33, -25
32-Bit High-Performance Superscalar Embedded Microprocessor

Datasheet

Product Features

- Socket and Object Code Compatible with 80960CA
- Two Instructions/Clock Sustained Execution
- Four 71 Mbytes/s DMA Channels with Data Chaining
- Demultiplexed 32-Bit Burst Bus with Pipelining

- 32-Bit Parallel Architecture
  - —Two Instructions/clock Execution
  - —Load/Store Architecture
  - —Sixteen 32-Bit Global Registers
  - —Sixteen 32-Bit Local Registers
  - —Manipulates 64-Bit Bit Fields
  - —11 Addressing Modes
  - —Full Parallel Fault Model
  - —Supervisor Protection Model
- Fast Procedure Call/Return Model
  - —Full Procedure Call in 4 Clocks
- On-Chip Register Cache
  - —Caches Registers on Call/Ret
  - —Minimum of 6 Frames Provided
  - —Up to 15 Programmable Frames
- On-Chip Instruction Cache
  - —4 Kbyte Two-Way Set Associative
  - —128-Bit Path to Instruction Sequencer
  - —Cache-Lock Modes
  - —Cache-Off Mode
- High Bandwidth On-Chip Data RAM
  - —1 Kbyte On-Chip Data RAM
  - —Sustains 128 bits per Clock Access
- Selectable Big or Little Endian Byte Ordering
- Four On-Chip DMA Channels
  - —71 Mbytes/s Fly-by Transfers
  - —40 Mbytes/s Two-Cycle Transfers
  - —Data Chaining
  - —Data Packing/Unpacking
  - —Programmable Priority Method
- 32-Bit Demultiplexed Burst Bus
  - —128-Bit Internal Data Paths to *and* from Registers
  - —Burst Bus for DRAM Interfacing
  - —Address Pipelining Option
  - —Fully Programmable Wait States
  - —Supports 8-, 16- or 32-Bit Bus Widths
  - —Supports Unaligned Accesses
  - —Supervisor Protection Pin
- High-Speed Interrupt Controller
  - —Up to 248 External Interrupts
  - —32 Fully Programmable Priorities
  - —Multi-mode 8-Bit Interrupt Port
  - —Four Internal DMA Interrupts
  - —Separate, Non-maskable Interrupt Pin
  - —Context Switch in 625 ns Typical
- On-Chip Data Cache
  - —1 Kbyte Direct-Mapped, Write Through
  - —128 bits per Clock Access on Cache Hit

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Revision History

Date	Revision	Description
September 2002	002	References to the -16 MHz product have been removed from the datasheet.
June 1996	001	Initial release of the datasheet.



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1.0 Purpose

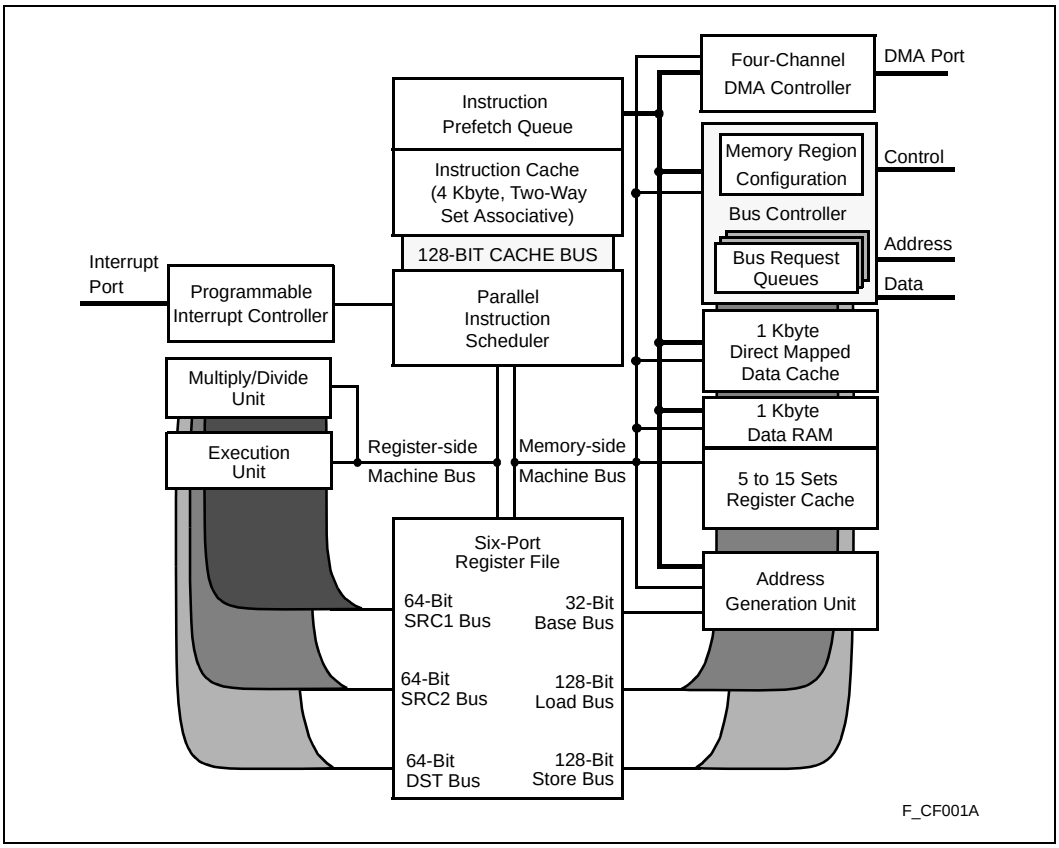
This document provides electrical characteristics of Intel's i960® CF embedded microprocessor. For functional descriptions consult the *i960® CA/CF Microprocessor User's Manual* (order number 270710). To obtain data sheet updates and errata, visit the Intel World Wide Web site at http://www.intel.com or contact your Intel field sales representative.

2.0 80960CF Processor Overview

Intel's 80960CF is the second processor in the series of superscalar i960 microprocessors that also includes the 80960CA and the 80960HA/HD/HT. Upgrading from the 80960CA to the 80960CF is straightforward because the two processors are socket- and object code-compatible.

As shown in Figure 1, the 80960CF's instruction cache is 4 Kbytes; data cache is 1 Kbyte (80960CA instruction cache is 1 Kbyte; it does not have a data cache.) This extra cache on the CF adds a significant performance boost over the CA.

Figure 1. 80960CF Processor-Block Diagram



The 80960CF, object code compatible with the 32-bit 80960 core Architecture, employs Special Function Register extensions to control on-chip peripherals and instruction set extensions to shift 64-bit operands and configure on-chip hardware. Multiple 128-bit internal buses, on-chip instruction caching and a sophisticated instruction scheduler allow the processor to sustain execution of two instructions per clock with peak execution of three instructions per clock.

A 32-bit demultiplexed and pipelined burst bus provides a 132 Mbyte/s bandwidth to a system's high-speed external memory subsystem. Also, the 80960CF's on-chip caching of instructions, procedure context and critical program data substantially decouples system performance from the wait states associated with accesses to the system's slower, cost sensitive, main memory subsystem.

The 80960CF bus controller integrates full wait state and bus width control for highest system performance with minimal system design complexity. Unaligned access and Big Endian byte order support reduces the cost of porting existing applications to the 80960CF.

The processor also integrates four complete data-chaining DMA channels and a high-speed interrupt controller on-chip. DMA channels perform single-cycle or two-cycle transfers, data packing and unpacking and data chaining. Block transfers — in addition to source or destination synchronized transfers — are supported.

The interrupt controller provides full programmability of 248 interrupt sources into 32 priority levels with a typical interrupt task switch (latency) time of 625 ns.

2.1 The 80960C-Series Core

The C-Series core is a very high performance microarchitectural implementation of the 80960 Core Architecture. This core may sustain execution of two instructions per clock (80 MIPS at 40 MHz). To achieve this level of performance, Intel has incorporated state-of-the-art silicon technology and innovative microarchitectural constructs into the C-Series core implementation. Factors that contribute to the core's performance include:

- Parallel instruction decoding allows issuance of up to three instructions per clock.
- Single-clock execution of most instructions
- Parallel instruction decode allows sustained, simultaneous execution of two single-clock instructions every clock cycle.
- Efficient instruction pipeline minimizes pipeline break losses.
- Register and resource scoreboarding allow simultaneous multi-clock instruction execution.
- Branch look-ahead and prediction allows many branches to execute with no pipeline break.
- Local Register Cache integrated on-chip caches Call/Return context.
- Two-way set associative, 4 Kbyte integrated instruction cache
- 1 Kbyte integrated Data RAM sustains a four-word (128-bit) access every clock cycle.
- Direct mapped, 1 Kbyte data cache, write through, write allocate

2.2 Pipelined, Burst Bus

A 32-bit high performance bus controller interfaces the 80960CF to external memory and peripherals. The Bus Control Unit features a maximum transfer rate of 160 Mbytes per second (at 40 MHz). Internally programmable wait states and 16 separately configurable memory regions allow the processor to interface with a variety of memory subsystems with a minimum of system complexity and a maximum of performance. The Bus Control Unit's main features include:

- Demultiplexed, burst bus to exploit most efficient DRAM access modes
- Address pipelining to reduce memory cost while maintaining performance
- 32-, 16- and 8-bit modes for I/O interfacing ease
- Full internal wait state generation to reduce system cost
- Little and Big Endian support to ease application development
- Unaligned access support for code portability
- Three-deep request queue to decouple the bus from the core

2.3 Instruction Set Summary

Table 1 summarizes the 80960CF instruction set by logical groupings. For a complete description of the instruction set, see the *i960® CA/CF Microprocessor User's Manual* (order number 270710).

2.4 Flexible DMA Controller

A four-channel DMA controller provides high speed DMA control for data transfers involving peripherals and memory. The DMA provides advanced features such as data chaining, byte assembly and disassembly and a high performance fly-by mode capable of transfer speeds of up to 71 Mbytes per second at 40 MHz. The DMA controller features a performance and flexibility which is only possible by integrating the DMA controller and the 80960CF core.

2.5 Priority Interrupt Controller

A programmable-priority interrupt controller manages up to 248 external sources through the 8-bit external interrupt port. The Interrupt Unit also handles the four internal sources from the DMA controller and a single non-maskable interrupt input. The 8-bit interrupt port may also be configured to provide individual interrupt sources that are level or edge triggered.

80960CF interrupts are prioritized and signaled within 225 ns of the request. When the interrupt is of higher priority than the processor priority, the context switch to the interrupt routine typically completes in another 400 ns. The interrupt unit provides the mechanism for the low latency and high throughput interrupt service which is essential for embedded applications.

Table 1 presents the 80960CF Instruction Set.

Table 1. 80960CF Instruction Set

Data Movement	Arithmetic	Logical	Bit / Bit Field / Byte
Load Store Move Load Address	Add Subtract Multiply Divide Remainder Modulo Shift *Extended Shift Extended Multiply Extended Divide Add with Carry Subtract with Carry Rotate	And Not And And Not Or Exclusive Or Not Or Or Not Nor Exclusive Nor Not Nand	Set Bit Clear Bit Not Bit Alter Bit Scan For Bit Span Over Bit Extract Modify Scan Byte for Equal
Comparison	**Branch**	**Call/Return**	**Fault**
Compare Conditional Compare Compare and Increment Compare and Decrement Test Condition Code Check Bit	Unconditional Branch Conditional Branch Compare and Branch	Call Call Extended Call System Return Branch and Link	Conditional Fault Synchronize Faults
Debug	**Processor Mgmt**	**Atomic**	
Modify Trace Controls Mark Force Mark	Flush Local Registers Modify Arithmetic Controls Modify Process Controls *System Control *DMA Control	Atomic Add Atomic Modify	

NOTE: Instructions marked by (*) are 80960Cx extensions to the 80960 instruction set.

3.0 Package Information

3.1 Package Introduction

This section describes the pins, pinouts and thermal characteristics for the 80960CF in the 168-pin Ceramic Pin Grid Array (PGA) package; the 80960CF-33 and -25 devices are also available in the 196-pin Plastic Quad Flat Package (PQFP). For complete package specifications and information, see the *Intel Packaging Databook*, available in individual chapters, at http://www.intel.com.

3.2 Pin Descriptions

This section defines the 80960CF pins. Table 2 presents the legend for interpreting the pin descriptions in Tables 3 through 5. Table 3 presents the external bus signals. Table 4 presents processor control signals. Table 5 presents the DMA and Interrupt Unit control signals.

Note: All pins float while the processor is in the ONCE mode.

Table 2. Symbol Legend

Symbol	Description
I	Input only pin
O	Output only pin
I/O	Pin may be either an input or output
–	Pins “must be” connected as described
S(...)	Synchronous. Inputs must meet setup and hold times relative to PCLK2:1 for proper operation. Outputs are synchronous to PCLK2:1. S(E) Edge sensitive input S(L) Level sensitive input
A(...)	Asynchronous. Inputs may be asynchronous to PCLK2:1. A(E)Edge sensitive input A(L)Level sensitive input
H(...)	While the bus is in the Hold Acknowledge or Bus Backoff state, the pin: H(1) is driven to V_{CC} H(0)is driven to V_{SS} H(Z) floats H(Q)continues to be a valid input
R(...)	While the processor’s $\overline{\text{RESET}}$ pin is low, the pin: R(1) is driven to V_{CC} R(0)is driven to V_{SS} R(Z) floats R(Q)continues to be a valid output

Table 3. 80960CF Pin Description—External Bus Signals (Sheet 1 of 2)

Name	Type	Description
A31:2	**O** S H(Z) R(Z)	**ADDRESS BUS** carries the physical address' upper 30 bits. A31 is the most significant bit; A2 is least significant. During a bus access, A31:2 identify all external addresses to word (4-byte) boundaries. Byte enable signals indicate the selected byte in each word. During burst accesses, A3:2 increment to indicate successive data cycles.
D31:0	**I/O** S(L) H(Z) R(Z)	**DATA BUS** carries 32-, 16- or 8-bit data quantities depending on bus width configuration. The least significant bit is carried on D0 and the most significant on D31. When the bus is configured for 8-bit data, the lower 8 data lines, D7:0 are used. For 16-bit data bus widths, D15:0 are used. For 32-bit bus widths the full data bus is used.
$\overline{\text{BE3:0}}$	**O** S H(Z) R(1)	**BYTE ENABLES** select which of the four bytes addressed by A31:2 are active during an access to a memory region configured for a 32-bit data-bus width. $\overline{\text{BE3}}$ applies to D31:24; $\overline{\text{BE2}}$ applies to D23:16; $\overline{\text{BE1}}$ applies to D15:8 $\overline{\text{BE0}}$ applies to D7:0. 32-bit bus: $\overline{\text{BE3}}$ Byte Enable 3 enable D31:24 $\overline{\text{BE2}}$ Byte Enable 2 enable D23:16 $\overline{\text{BE1}}$ Byte Enable 1 enable D15:8 $\overline{\text{BE0}}$ Byte Enable 0 enable D7:0 For accesses to a memory region configured for a 16-bit data-bus width, the processor uses the $\overline{\text{BE3}}$, $\overline{\text{BE1}}$ and $\overline{\text{BE0}}$ pins as $\overline{\text{BHE}}$, A1 and $\overline{\text{BLE}}$ respectively. 16-bit bus: $\overline{\text{BE3}}$ Byte High Enable ($\overline{\text{BHE}}$) enable D15:8 $\overline{\text{BE2}}$ Not used (driven high or low) $\overline{\text{BE1}}$ Address Bit 1 (A1) $\overline{\text{BE0}}$ Byte Low Enable ($\overline{\text{BLE}}$) enable D7:0 For accesses to a memory region configured for an 8-bit data-bus width, the processor uses the $\overline{\text{BE1}}$ and $\overline{\text{BE0}}$ pins as A1 and A0 respectively. 8-bit bus: $\overline{\text{BE3}}$ Not used (driven high or low) $\overline{\text{BE2}}$ Not used (driven high or low) $\overline{\text{BE1}}$ Address Bit 1 (A1) $\overline{\text{BE0}}$ Address Bit 0 (A0)
W/R	**O** S H(Z) R(0)	**WRITE/READ** is asserted for read requests and deasserted for write requests. The W/R signal changes in the same clock cycle as $\overline{\text{ADS}}$. It remains valid for the entire access in non-pipelined regions. In pipelined regions, W/R is not ensured to be valid in the last cycle of a read access.
$\overline{\text{ADS}}$	**O** S H(Z) R(1)	**ADDRESS STROBE** indicates a valid address and the start of a new bus access. $\overline{\text{ADS}}$ is asserted for the first clock of a bus access.
$\overline{\text{READY}}$	**I** S(L) H(Z) R(Z)	**READY** is an input which signals the termination of a data transfer. $\overline{\text{READY}}$ is used to indicate that read data on the bus is valid or that a write-data transfer has completed. The $\overline{\text{READY}}$ signal works in conjunction with the internally programmed wait-state generator. When $\overline{\text{READY}}$ is enabled in a region, the pin is sampled after the programmed number of wait-states has expired. When the $\overline{\text{READY}}$ pin is deasserted, wait states continue to be inserted until $\overline{\text{READY}}$ becomes asserted. This is true for the N_{RAD}, N_{RDD}, N_{WAD} and N_{WDD} wait states. The N_{XDA} wait states cannot be extended.
$\overline{\text{BTERM}}$	**I** S(L) H(Z) R(Z)	**BURST TERMINATE** is an input which breaks up a burst access and causes another address cycle to occur. The $\overline{\text{BTERM}}$ signal works in conjunction with the internally programmed wait-state generator. When $\overline{\text{READY}}$ and $\overline{\text{BTERM}}$ are enabled in a region, the $\overline{\text{BTERM}}$ pin is sampled after the programmed number of wait states has expired. When $\overline{\text{BTERM}}$ is asserted, a new $\overline{\text{ADS}}$ signal is generated and the access is completed. The $\overline{\text{READY}}$ input is ignored when $\overline{\text{BTERM}}$ is asserted. $\overline{\text{BTERM}}$ must be externally synchronized to satisfy $\overline{\text{BTERM}}$ setup and hold times.
$\overline{\text{WAIT}}$	**O** S H(Z) R(1)	**WAIT** indicates internal wait state generator status. $\overline{\text{WAIT}}$ is asserted when wait states are being caused by the internal wait state generator and not by the $\overline{\text{READY}}$ or $\overline{\text{BTERM}}$ inputs. $\overline{\text{WAIT}}$ may be used to derive a write-data strobe. $\overline{\text{WAIT}}$ may also be thought of as a $\overline{\text{READY}}$ output that the processor provides when it is inserting wait states.

Table 3. 80960CF Pin Description—External Bus Signals (Sheet 2 of 2)

Name	Type	Description
BLAST	**O** S H(Z) R(0)	**BURST LAST** indicates the last transfer in a bus access. BLAST is asserted in the last data transfer of burst and non-burst accesses after the wait state counter reaches zero. BLAST remains asserted until the clock following the last cycle of the last data transfer of a bus access. When the READY or BTERM input is used to extend wait states, the BLAST signal remains asserted until READY or BTERM terminates the access.
DT/R	**O** S H(Z) R(0)	**DATA TRANSMIT/RECEIVE** indicates direction for data transceivers. DT/R is used in conjunction with DEN to provide control for data transceivers attached to the external bus. When DT/R is asserted, the signal indicates that the processor receives data. Conversely, when deasserted, the processor sends data. DT/R changes only while DEN is high.
DEN	**O** S H(Z) R(1)	**DATA ENABLE** indicates data cycles in a bus request. DEN is asserted at the start of the bus request first data cycle and is deasserted at the end of the last data cycle. DEN is used in conjunction with DT/R to provide control for data transceivers attached to the external bus. DEN remains asserted for sequential reads from pipelined memory regions. DEN is deasserted when DT/R changes.
LOCK	**O** S H(Z) R(1)	**BUS LOCK** indicates that an atomic read-modify-write operation is in progress. LOCK may be used to prevent external agents from accessing memory which is currently involved in an atomic operation. LOCK is asserted in the first clock of an atomic operation and deasserted in the clock cycle following the last bus access for the atomic operation. To allow the most flexibility for memory system enforcement of locked accesses, the processor acknowledges a bus hold request when LOCK is asserted. The processor performs DMA transfers while LOCK is active.
HOLD	**I** S(L) H(Z) R(Z)	**HOLD REQUEST** signals that an external agent requests access to the external bus. The processor asserts HOLDA after completing the current bus request. HOLD, HOLDA and BREQ are used together to arbitrate access to the processor's external bus by external bus agents.
BOFF	**I** S(L) H(Z) R(Z)	**BUS BACKOFF**, when asserted, suspends the current access and causes the bus pins to float. When BOFF is deasserted, the ADS signal is asserted on the next clock cycle and the access is resumed.
HOLDA	**O** S H(1) R(Q)	**HOLD ACKNOWLEDGE** indicates to a bus requestor that the processor has relinquished control of the external bus. When HOLDA is asserted, the external address bus, data bus and bus control signals are floated. HOLD, BOFF, HOLDA and BREQ are used together to arbitrate access to the processor's external bus by external bus agents. Since the processor grants HOLD requests and enters the Hold Acknowledge state even while RESET is asserted, the state of the HOLDA pin is independent of the RESET pin.
BREQ	**O** S H(Q) R(0)	**BUS REQUEST** is asserted when the bus controller has a request pending. BREQ may be used by external bus arbitration logic in conjunction with HOLD and HOLDA to determine when to return mastership of the external bus to the processor.
D/C	**O** S H(Z) R(Z)	**DATA OR CODE** is asserted for a data request and deasserted for instruction requests. D/C has the same timing as W/R.
DMA	**O** S H(Z) R(Z)	**DMA ACCESS** indicates whether the bus request was initiated by the DMA controller. DMA is asserted for any DMA request. DMA is deasserted for all other requests.
SUP	**O** S H(Z) R(Z)	**SUPERVISOR ACCESS** indicates whether the bus request is issued while in supervisor mode. SUP is asserted when the request has supervisor privileges and is deasserted otherwise. SUP may be used to isolate supervisor code and data structures from non-supervisor requests.

Table 4. 80960CF Pin Description—Processor Control Signals (Sheet 1 of 2)

Name	Type	Description
RESET	**I** A(L) H(Z) R(Z)	**RESET** causes the chip to reset. When RESET is asserted, all external signals return to the reset state. When RESET is deasserted, initialization begins. When the 2-x clock mode is selected, RESET must remain asserted for 32 CLKIN cycles before being deasserted to ensure correct processor initialization. When the 1-x clock mode is selected, RESET must remain asserted for 10,000 CLKIN cycles before being deasserted to ensure correct processor initialization. The CLKMODE pin selects 1-x or 2-x input clock division of the CLKIN pin. The Hold Acknowledge bus state functions while the chip is reset. When the bus is in the Hold Acknowledge state when RESET is asserted, the processor internally resets, but maintains the Hold Acknowledge state on external pins until the Hold request is removed. When a Hold request is made while the processor is in the reset state, the processor bus grants HOLDA and enters the Hold Acknowledge state.
FAIL	**O** S H(Q) R(0)	**FAIL** indicates failure of the self-test performed at initialization. When RESET is deasserted and initialization begins, the FAIL pin is asserted. An internal self-test is performed as part of the initialization process. When this self-test passes, the FAIL pin is deasserted; otherwise it remains asserted. The FAIL pin is reasserted while the processor performs an external bus self-confidence test. When this self-test passes, the processor deasserts the FAIL pin and branches to the user's initialization routine; otherwise the FAIL pin remains asserted. Internal self-test and the use of the FAIL pin may be disabled with the STEST pin.
STEST	**I** S(L) H(Z) R(Z)	**SELF TEST** enables or disables the internal self-test feature at initialization. STEST is read on the rising edge of RESET. When asserted, internal self-test and external bus confidence tests are performed during processor initialization. When deasserted, only the bus confidence tests are performed during initialization.
ONCE	**I** A(L) H(Z) R(Z)	**ON CIRCUIT EMULATION**, when asserted, causes all outputs to be floated. ONCE is continuously sampled while RESET is low and is latched on the rising edge of RESET. To place the processor in the ONCE state: (1) Assert RESET and ONCE (order does not matter) (2) Wait for at least 16 CLKIN periods in 2-x mode—or 10,000 CLKIN periods in 1-x mode—after V_{CC} and CLKIN are within operating specifications (3) Deassert RESET (4) Wait at least 32 CLKIN periods (The processor may now be latched in the ONCE state while RESET is high.) To exit the ONCE state, bring V_{CC} and CLKIN to operating conditions, then assert RESET and bring ONCE high prior to deasserting RESET. CLKIN must operate within the specified operating conditions until Step 4 completes. CLKIN may then be changed to DC to achieve the lowest possible ONCE mode leakage current. ONCE may be used by emulator products or board testers to effectively make an installed processor transparent in the board.
CLKIN	**I** A(E) H(Z) R(Z)	**CLOCK INPUT** is an input for the external clock needed to run the processor. The external clock is internally divided as prescribed by the CLKMODE pin to produce PCLK2:1.
CLKMODE	**I** A(L) H(Z) R(Z)	**CLOCK MODE** selects the division factor applied to the external clock input (CLKIN). When CLKMODE is high, CLKIN is divided by one to create PCLK2:1 and the processor's internal clock. When CLKMODE is low, CLKIN is divided by two to create PCLK2:1 and the processor's internal clock. CLKMODE should be tied high or low in a system as the clock mode is not latched by the processor. When left unconnected, the processor internally pulls the CLKMODE pin low, enabling the 2-x clock mode.

Table 4. 80960CF Pin Description—Processor Control Signals (Sheet 2 of 2)

Name	Type	Description
PCLK2:1	**O** S H(Q) R(Q)	**PROCESSOR OUTPUT CLOCKS** provide a timing reference for all inputs and outputs. All input and output timings are specified in relation to PCLK2 and PCLK1. PCLK2 and PCLK1 are identical signals. Two output pins are provided to allow flexibility in the system's allocation of capacitive loading on the clock. PCLK2:1 may also be connected at the processor to form a single clock signal.
V_{SS}	–	**GROUND** connections must be connected externally to a V_{SS} board plane.
V_{CC}	–	**POWER** connections must be connected externally to a V_{CC} board plane.
V_{CCPLL}	–	**V_{CCPLL}** is a separate V_{CC} supply pin for the phase lock loop used in 1-x clock mode. Connecting a simple lowpass filter to V_{CCPLL} may help reduce clock jitter (T_{CP}) in noisy environments. Otherwise, V_{CCPLL} should be connected to V_{CC}.
NC	–	**NO CONNECT** pins must not be connected in a system.

Table 5. 80960CF Pin Description—DMA and Interrupt Unit Control Signals

Name	Type	Description
$\overline{\text{DREQ3:0}}$	**I** A(L) H(Z) R(Z)	**DMA REQUEST** is used to request a DMA transfer. Each of the four signals requests a transfer on a single channel. DREQ0 requests channel 0, DREQ1 requests channel 1, etc. When two or more channels are requested simultaneously, the channel with the highest priority is serviced first. Channel priority mode is programmable.
$\overline{\text{DACK3:0}}$	**O** S H(1) R(1)	**DMA ACKNOWLEDGE** indicates that a DMA transfer is being executed. Each of the four signals acknowledges a transfer for a single channel. DACK0 acknowledges channel 0, DACK1 acknowledges channel 1, etc. DACK3:0 are asserted when the requesting device of a DMA is accessed.
$\overline{\text{EOP}}$/$\overline{\text{TC3:0}}$	**I/O** A(L) H(Z/Q) R(Z)	**END OF PROCESS/TERMINAL COUNT** may be programmed as either an input ($\overline{\text{EOP3:0}}$) or output ($\overline{\text{TC3:0}}$), but not both. Each pin is individually programmable. When programmed as an input, $\overline{\text{EOP}}$x causes termination of a current DMA transfer for the channel that corresponds to the $\overline{\text{EOP}}$x pin. $\overline{\text{EOP0}}$ corresponds to channel 0, $\overline{\text{EOP1}}$ corresponds to channel 1, etc. When a channel is configured for source *and* destination chaining, the EOP pin for that channel causes termination of only the current buffer transferred and causes the next buffer to be transferred. $\overline{\text{EOP3:0}}$ are asynchronous inputs. When programmed as an output, the channel's $\overline{\text{TC}}$x pin indicates that the channel byte count has reached 0 and a DMA has terminated. $\overline{\text{TC}}$x is driven with the same timing as $\overline{\text{DACK}}$x during the last DMA transfer for a buffer. When the last bus request is executed as multiple bus accesses, $\overline{\text{TC}}$x stays asserted for the entire bus request.
$\overline{\text{XINT7:0}}$	**I** A(E/L) H(Z) R(Z)	**EXTERNAL INTERRUPT PINS** cause interrupts to be requested. These pins may be configured in three modes: **Dedicated Mode:** Each pin is a dedicated external interrupt source. Dedicated inputs may be individually programmed to be level (low) or edge (falling) activated. **Expanded Mode:** The eight pins act together as an 8-bit vectored interrupt source. The interrupt pins in this mode are level activated. Since the interrupt pins are active low, the vector number requested is the 1's complement of the positive logic value place on the port. This eliminates glue logic to interface to combinational priority encoders which output negative logic. **Mixed Mode:** $\overline{\text{XINT7:5}}$ are dedicated sources and $\overline{\text{XINT4:0}}$ act as the five most significant bits of an expanded mode vector. The least significant bits are set to 010 internally.
$\overline{\text{NMI}}$	**I** A(E) H(Z) R(Z)	**NON-MASKABLE INTERRUPT** causes a non-maskable interrupt event to occur. $\overline{\text{NMI}}$ is the highest priority interrupt recognized. $\overline{\text{NMI}}$ is an edge (falling) activated source.

3.3 80960CF Mechanical Data

3.3.1 80960CF PGA Pinout

Figure 2 shows the complete 80960CF PGA pinout as viewed from the top side of the component (i.e., pins facing down). Figure 3 shows the complete 80960CF PGA pinout as viewed from the pin-side of the package (i.e., pins facing up).

Table 6 presents the 80960CF pin names and package location in signal order. Table 7 presents the pin names and package location in pin order. See Section 4.0, “Electrical Specifications” on page 26 for specifications and recommended connections.

Figure 2. 80960CF PGA Pinout—View from Top (Pins Facing Down)

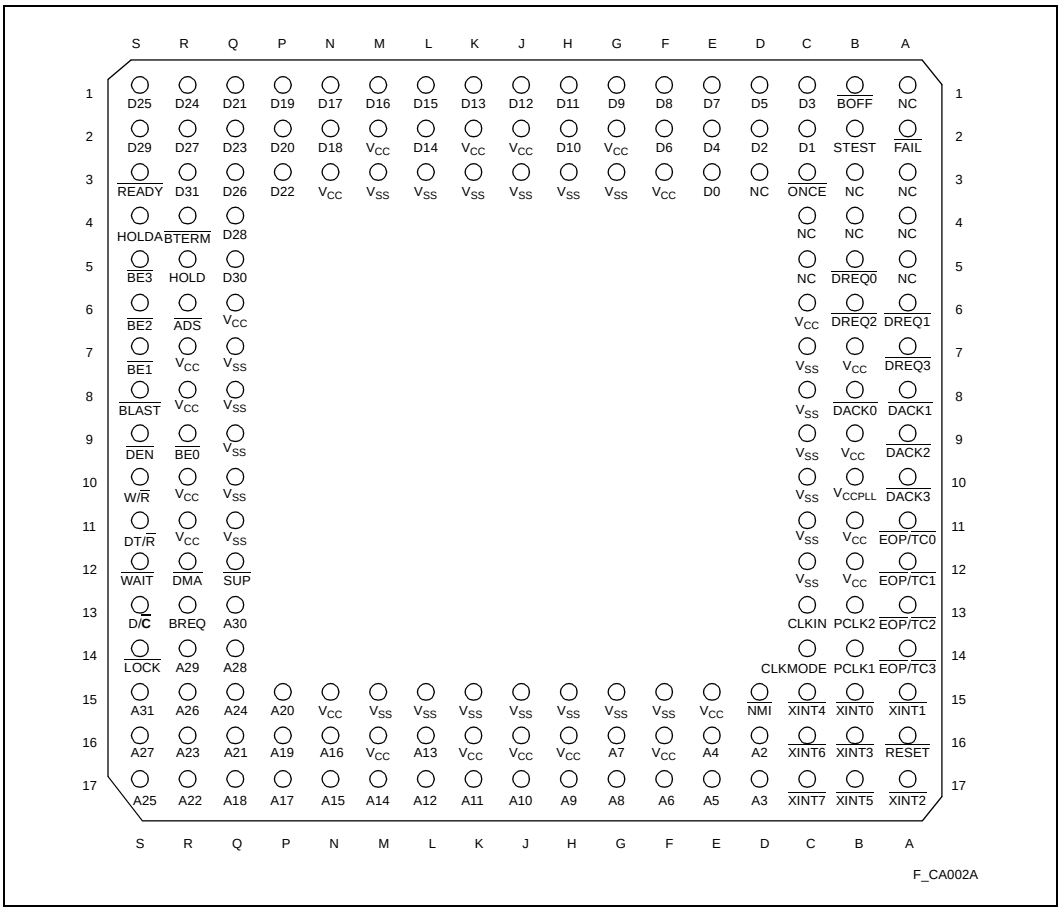


Figure 3. 80960CF PGA Pinout—View from Bottom (Pins Facing Up)

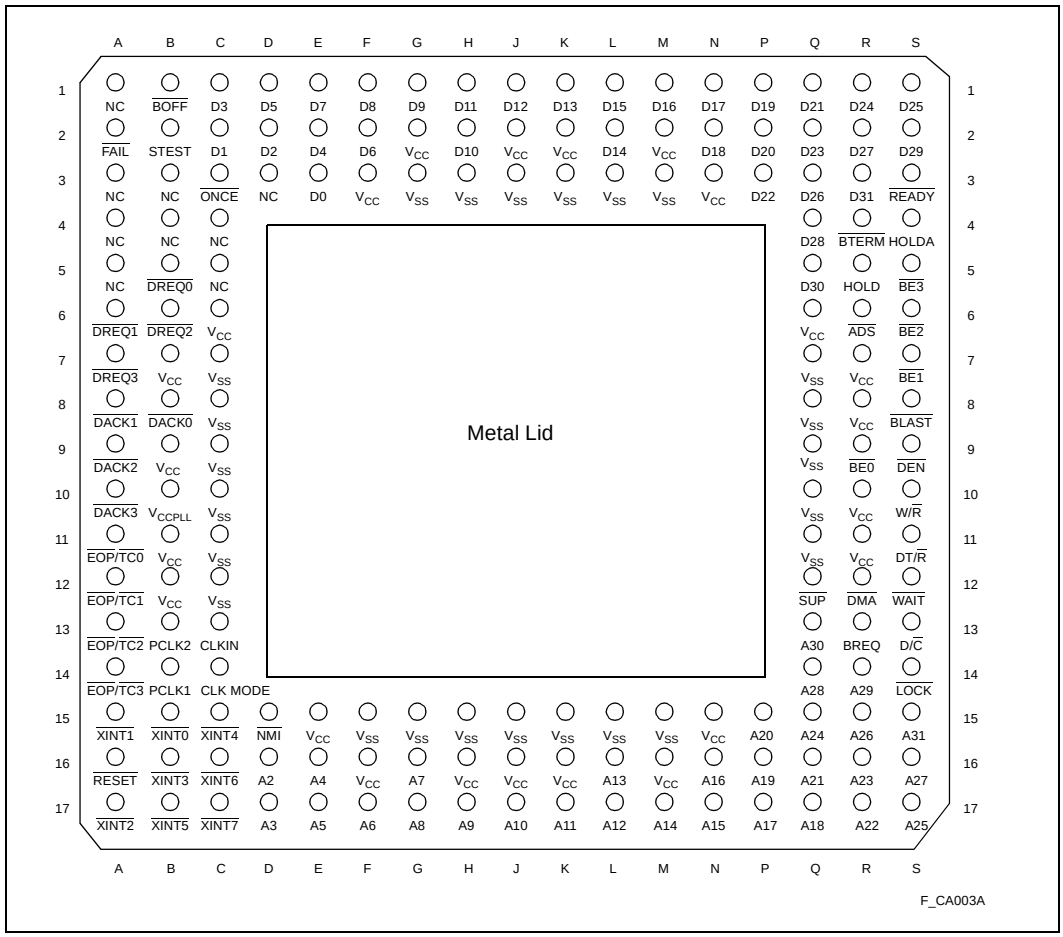


Table 6. 80960CF PGA Pinout—In Signal Order

Address Bus		Data Bus		Bus Control		Processor Control		I/O	
Signal	**Pin**	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**	**Pin**
A31	S15	**D31**	R3	**$\overline{BE3}$**	S5	**$\overline{RESET}$**	A16	**$\overline{DREQ3}$**	A7
A30	Q13	**D30**	Q5	**$\overline{BE2}$**	S6			**$\overline{DREQ2}$**	B6
A29	R14	**D29**	S2	**$\overline{BE1}$**	S7	**$\overline{FAIL}$**	A2	**$\overline{DREQ1}$**	A6
A28	Q14	**D28**	Q4	**$\overline{BE0}$**	R9			**$\overline{DREQ0}$**	B5
A27	S16	**D27**	R2			**STEST**	B2		
A26	R15	**D26**	Q3	**W/$\overline{R}$**	S10			**$\overline{DACK3}$**	A10
A25	S17	**D25**	S1			**$\overline{ONCE}$**	C3	**$\overline{DACK2}$**	A9
A24	Q15	**D24**	R1	**$\overline{ADS}$**	R6			**$\overline{DACK1}$**	A8
A23	R16	**D23**	Q2			**CLKIN**	C13	**$\overline{DACK0}$**	B8
A22	R17	**D22**	P3	**$\overline{READY}$**	S3	**CLKMODE**	C14		
A21	Q16	**D21**	Q1	**$\overline{BTERM}$**	R4	**PLCK1**	B14	**$\overline{EOP}$/$\overline{TC3}$**	A14
A20	P15	**D20**	P2			**PLCK2**	B13	**$\overline{EOP}$/$\overline{TC2}$**	A13
A19	P16	**D19**	P1	**$\overline{WAIT}$**	S12			**$\overline{EOP}$/$\overline{TC1}$**	A12
A18	Q17	**D18**	N2	**$\overline{BLAST}$**	S8	**V_{SS}**		**$\overline{EOP}$/$\overline{TC0}$**	A11
A17	P17	**D17**	N1			Location			
A16	N16	**D16**	M1	**DT/$\overline{R}$**	S11	C7, C8, C9, C10, C11, C12, F15, G3, G15, H3, H15, J3, J15, K3, K15, L3, L15, M3, M15, Q7, Q8, Q9, Q10, Q11		**$\overline{XINT7}$**	C17
A15	N17	**D15**	L1	**$\overline{DEN}$**	S9			**$\overline{XINT6}$**	C16
A14	M17	**D14**	L2					**$\overline{XINT5}$**	B17
A13	L16	**D13**	K1	**LOCK**	S14			**$\overline{XINT4}$**	C15
A12	L17	**D12**	J1					**$\overline{XINT3}$**	B16
A11	K17	**D11**	H1			**V_{CC}**		**$\overline{XINT2}$**	A17
A10	J17	**D10**	H2	**HOLD**	R5	Location		**$\overline{XINT1}$**	A15
A9	H17	**D9**	G1	**HOLDA**	S4	B7, B9, B11, B12, C6, E15, F3, F16, G2, H16, J2, J16, K2, K16, M2, M16, N3, N15, Q6, R7, R8, R10, R11		**$\overline{XINT0}$**	B15
A8	G17	**D8**	F1	**BREQ**	R13				
A7	G16	**D7**	E1					**$\overline{NMI}$**	D15
A6	F17	**D6**	F2	**D/$\overline{C}$**	S13				
A5	E17	**D5**	D1	**$\overline{DMA}$**	R12				
A4	E16	**D4**	E2	**$\overline{SUP}$**	Q12	**V_{CCPLL}**	B10		
A3	D17	**D3**	C1			No Connect			
A2	D16	**D2**	D2	**$\overline{BOFF}$**	B1	Location			
		D1	C2			A1, A3, A4, A5, B3, B4, C4, C5, D3			
		D0	E3						

Table 7. 80960CF PGA Pinout—In Pin Order

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	NC	C1	D3	F17	A6	M15	V_{SS}	R3	D31
A2	FAIL	C2	D1	G1	D9	M16	V_{CC}	R4	BTERM
A3	NC	C3	ONCE	G2	V_{CC}	M17	A14	R5	HOLD
A4	NC	C4	NC	G3	V_{SS}	N1	D17	R6	ADS
A5	NC	C5	NC	G15	V_{SS}	N2	D18	R7	V_{CC}
A6	DREQ1	C6	V_{CC}	G16	A7	N3	V_{CC}	R8	V_{CC}
A7	DREQ3	C7	V_{SS}	G17	A8	N15	V_{CC}	R9	BE0
A8	DACK1	C8	V_{SS}	H1	D11	N16	A16	R10	V_{CC}
A9	DACK2	C9	V_{SS}	H2	D10	N17	A15	R11	V_{CC}
A10	DACK3	C10	V_{SS}	H3	V_{SS}	P1	D19	R12	DMA
A11	EOP/TC0	C11	V_{SS}	H15	V_{SS}	P2	D20	R13	BREQ
A12	EOP/TC1	C12	V_{SS}	H16	V_{CC}	P3	D22	R14	A29
A13	EOP/TC2	C13	CLKIN	H17	A9	P15	A20	R15	A26
A14	EOP/TC3	C14	CLKMODE	J1	D12	P16	A19	R16	A23
A15	XINT1	C15	XINT4	J2	V_{CC}	P17	A17	R17	A22
A16	RESET	C16	XINT6	J3	V_{SS}	Q1	D21	S1	D25
A17	XINT2	C17	XINT7	J15	V_{SS}	Q2	D23	S2	D29
B1	BOFF	D1	D5	J16	V_{CC}	Q3	D26	S3	READY
B2	STEST	D2	D2	J17	A10	Q4	D28	S4	HOLDA
B3	NC	D3	NC	K1	D13	Q5	D30	S5	BE3
B4	NC	D15	NMI	K2	V_{CC}	Q6	V_{CC}	S6	BE2
B5	DREQ0	D16	A2	K3	V_{SS}	Q7	V_{SS}	S7	BE1
B6	DREQ2	D17	A3	K15	V_{SS}	Q8	V_{SS}	S8	BLAST
B7	V_{CC}	E1	D7	K16	V_{CC}	Q9	V_{SS}	S9	DEN
B8	DACK0	E2	D4	K17	A11	Q10	V_{SS}	S10	W/R
B9	V_{CC}	E3	D0	L1	D15	Q11	V_{SS}	S11	DT/R
B10	V_{CCPLL}	E15	V_{CC}	L2	D14	Q12	SUP	S12	WAIT
B11	V_{CC}	E16	A4	L3	V_{SS}	Q13	A30	S13	D/C
B12	V_{CC}	E17	A5	L15	V_{SS}	Q14	A28	S14	LOCK
B13	PCLK2	F1	D8	L16	A13	Q15	A24	S15	A31
B14	PCLK1	F2	D6	L17	A12	Q16	A21	S16	A27
B15	XINT0	F3	V_{CC}	M1	D16	Q17	A18	S17	A25
B16	XINT3	F15	V_{SS}	M2	V_{CC}	R1	D24		
B17	XINT5	F16	V_{CC}	M3	V_{SS}	R2	D27		

3.3.2 80960CF PQFP Pinout (80960CF-33 and -25 Only)

Table 8 and Table 9 present the 80960CF pin names with package location. Figure 4 shows the 80960CF PQFP pinout as viewed from the top side. See Section 4.0, "Electrical Specifications" on page 26 for specifications and recommended connections.

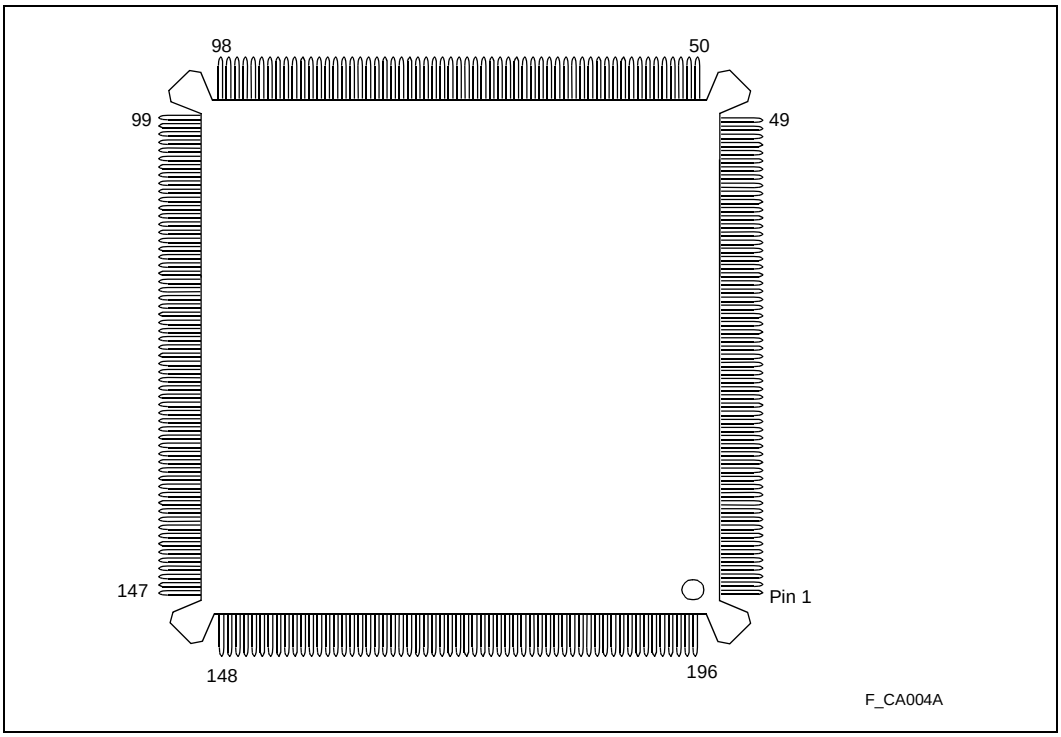
Table 8. 80960CF PQFP Pinout—In Signal Order (80960CF-33 and -25 Only)

Address Bus		Data Bus		Bus Control		Processor Control		I/O	
Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
A31	153	D31	186	$\overline{BE3}$	176	$\overline{RESET}$	91	$\overline{DREQ3}$	60
A30	152	D30	187	$\overline{BE2}$	175	$\overline{FAIL}$	45	$\overline{DREQ2}$	59
A29	151	D29	188	$\overline{BE1}$	172	STEST	46	$\overline{DREQ1}$	58
A28	145	D28	189	$\overline{BE0}$	170	$\overline{ONCE}$	43	$\overline{DREQ0}$	57
A27	144	D27	191			CLKIN	87		
A26	143	D26	192	W/$\overline{R}$	164	CLKMODE	85	$\overline{DACK3}$	65
A25	142	D25	194			PCLK2	74	$\overline{DACK2}$	64
A24	141	D24	195	$\overline{ADS}$	178	PCLK1	78	$\overline{DACK1}$	63
A23	139	D23	3			V_{SS}		$\overline{DACK0}$	62
A22	138	D22	4	$\overline{READY}$	182	Location			
A21	137	D21	5	$\overline{BTERM}$	184	2, 7, 16, 24, 30, 38, 39, 49, 56, 70, 75, 77, 81, 83, 88, 89, 92, 98, 105, 109, 110, 121, 125, 131, 135, 147, 150, 161, 165, 173, 174, 185, 196		$\overline{EOP/TC3}$	69
A20	136	D20	6					$\overline{EOP/TC2}$	68
A19	134	D19	8	$\overline{WAIT}$	162			$\overline{EOP/TC1}$	67
A18	133	D18	9	$\overline{BLAST}$	169			$\overline{EOP/TC0}$	66
A17	132	D17	10						
A16	130	D16	11	DT/$\overline{R}$	163			$\overline{XINT7}$	107
A15	129	D15	13	$\overline{DEN}$	167	V_{CC}		$\overline{XINT6}$	106
A14	128	D14	14			Location		$\overline{XINT5}$	102
A13	124	D13	15	$\overline{LOCK}$	156	1, 12, 20, 28, 32, 37, 44, 50, 61, 71, 79, 82, 96, 99, 103, 115, 127, 140, 148, 154, 168, 171, 180, 190		$\overline{XINT4}$	101
A12	123	D12	17					$\overline{XINT3}$	100
A11	122	D11	18	HOLD	181			$\overline{XINT2}$	95
A10	120	D10	19	HOLDA	179			$\overline{XINT1}$	94
A9	119	D9	21	BREQ	155			$\overline{XINT0}$	93
A8	118	D8	22			V_{CCPLL}	72		
A7	117	D7	23	D/$\overline{C}$	159	No Connect		$\overline{NMI}$	108
A6	116	D6	25	$\overline{DMA}$	160	Location			
A5	114	D5	26	$\overline{SUP}$	158	29, 31, 41, 42, 47, 48, 51, 52, 53, 54, 55, 73, 76, 80, 84, 86, 90, 97, 104, 126, 146, 149, 157, 166, 177, 183, 193			
A4	113	D4	27						
A3	112	D3	33	$\overline{BOFF}$	40				
A2	111	D2	34						
		D1	35						
		D0	36						

Table 9. 80960CF PQFP Pinout—In Pin Order (80960CF-33 and -25 Only)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	V_{CC}	34	D2	67	$\overline{EOP}/\overline{TC1}$	100	$\overline{XINT3}$	133	A18	166	NC
2	V_{SS}	35	D1	68	$\overline{EOP}/\overline{TC2}$	101	$\overline{XINT4}$	134	A19	167	$\overline{DEN}$
3	D23	36	D0	69	$\overline{EOP}/\overline{TC3}$	102	$\overline{XINT5}$	135	V_{SS}	168	V_{CC}
4	D22	37	V_{CC}	70	V_{SS}	103	V_{CC}	136	A20	169	$\overline{BLAST}$
5	D21	38	V_{SS}	71	V_{CC}	104	NC	137	A21	170	$\overline{BE0}$
6	D20	39	V_{SS}	72	V_{CCPLL}	105	V_{SS}	138	A22	171	V_{CC}
7	V_{SS}	40	$\overline{BOFF}$	73	NC	106	$\overline{XINT6}$	139	A23	172	$\overline{BE1}$
8	D19	41	NC	74	PCLK2	107	$\overline{XINT7}$	140	V_{CC}	173	V_{SS}
9	D18	42	NC	75	V_{SS}	108	$\overline{NMI}$	141	A24	174	V_{SS}
10	D17	43	$\overline{ONCE}$	76	NC	109	V_{SS}	142	A25	175	$\overline{BE2}$
11	D16	44	V_{CC}	77	V_{SS}	110	V_{SS}	143	A26	176	$\overline{BE3}$
12	V_{CC}	45	$\overline{FAIL}$	78	PCLK1	111	A2	144	A27	177	NC
13	D15	46	STEST	79	V_{CC}	112	A3	145	A28	178	$\overline{ADS}$
14	D14	47	NC	80	NC	113	A4	146	NC	179	HOLDA
15	D13	48	NC	81	V_{SS}	114	A5	147	V_{SS}	180	V_{CC}
16	V_{SS}	49	V_{SS}	82	V_{CC}	115	V_{CC}	148	V_{CC}	181	HOLD
17	D12	50	V_{CC}	83	V_{SS}	116	A6	149	NC	182	$\overline{READY}$
18	D11	51	NC	84	NC	117	A7	150	V_{SS}	183	NC
19	D10	52	NC	85	CLKMODE	118	A8	151	A29	184	$\overline{BTERM}$
20	V_{CC}	53	NC	86	NC	119	A9	152	A30	185	V_{SS}
21	D9	54	NC	87	CLKIN	120	A10	153	A31	186	D31
22	D8	55	NC	88	V_{SS}	121	V_{SS}	154	V_{CC}	187	D30
23	D7	56	V_{SS}	89	V_{SS}	122	A11	155	BREQ	188	D29
24	V_{SS}	57	$\overline{DREQ0}$	90	NC	123	A12	156	$\overline{LOCK}$	189	D28
25	D6	58	$\overline{DREQ1}$	91	$\overline{RESET}$	124	A13	157	NC	190	V_{CC}
26	D5	59	$\overline{DREQ2}$	92	V_{SS}	125	V_{SS}	158	$\overline{SUP}$	191	D27
27	D4	60	$\overline{DREQ3}$	93	$\overline{XINT0}$	126	NC	159	$\overline{D/C}$	192	D26
28	V_{CC}	61	V_{CC}	94	$\overline{XINT1}$	127	V_{CC}	160	$\overline{DMA}$	193	NC
29	NC	62	$\overline{DACK0}$	95	$\overline{XINT2}$	128	A14	161	V_{SS}	194	D25
30	V_{SS}	63	$\overline{DACK1}$	96	V_{CC}	129	A15	162	$\overline{WAIT}$	195	D24
31	NC	64	$\overline{DACK2}$	97	NC	130	A16	163	$\overline{DT/R}$	196	V_{SS}
32	V_{CC}	65	$\overline{DACK3}$	98	V_{SS}	131	V_{SS}	164	$\overline{W/R}$		
33	D3	66	$\overline{EOP}/\overline{TC0}$	99	V_{CC}	132	A17	165	V_{SS}		

Figure 4. 80960CF PQFP Pinout—Top View (80960CF-33 and -25 Only)



3.4 Package Thermal Specifications

The 80960CF is specified for operation when case temperature (T_C) is within the range of 0 °C–100 °C for 33 and 25 MHz, and 0 °C–85 °C for 40 MHz. T_C may be measured in any environment to determine whether the 80960CF is within specified operating range. Case temperature should be measured at the center of the top surface, opposite the pins. Refer to Figure 5 for more information.

Ambient temperature (T_A) is calculated from thermal resistance from case to ambient (θ_{CA}) using Equation 1:

Equation 1. Calculation of Ambient Temperature (T_A)

$$T_A = T_C - (P \cdot \theta_{CA})$$

Table 10 shows the maximum T_A allowable (without exceeding T_C) at various airflows and operating frequencies (f_{PCLK}).

Note that T_A is greatly improved by attaching fins or a heatsink to the package. Maximum power consumption (P) is calculated by using the typical I_{CC} as tabulated in Section 4.4, “D.C. Specifications” on page 27 and V_{CC} of 5 V.

Figure 5. Measuring 80960CF PGA and PQFP Case Temperature

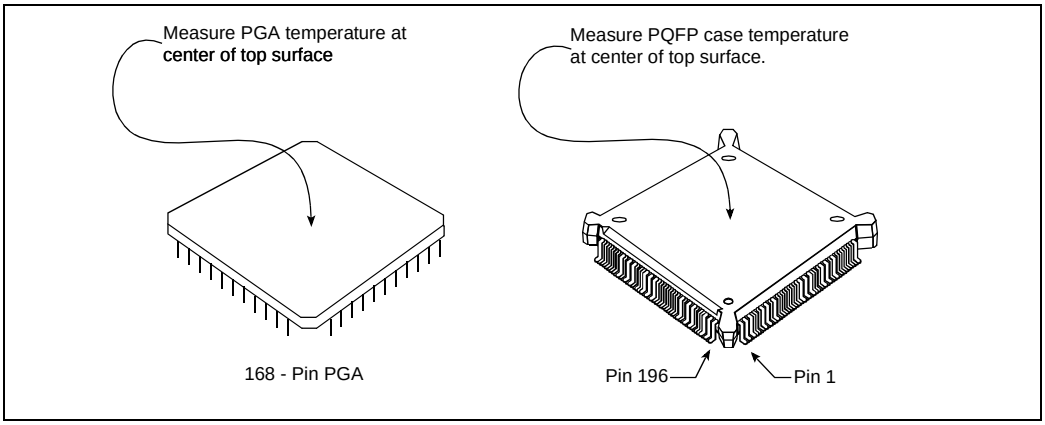


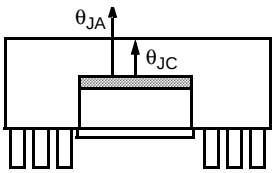
Table 10. Maximum T_A at Various Airflows in ^{O}C (PGA Package Only)

		Airflow-ft/min (m/sec)					
	f_{PCLK} (MHz)	0 (0)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)	1000 (5.07)
T_A with Heatsink (†)	40	20	40	58	60	66	68
	33	38	57	74	76	81	84
	25	50	65	79	81	85	87
	16	63	74	84	86	89	90
T_A without Heatsink (†)	40	0	15	30	40	50	52
	33	18	33	47	57	66	67
	25	34	46	57	65	72	74
	16	51	60	68	74	80	81

† 0.285” high unidirectional heatsink (Al alloy 6061, 50 mil fin width, 150 mil center-to-center fin spacing).

Table 11. 80960CF PGA Package Thermal Characteristics

Thermal Resistance — °C/Watt						
Parameter	Airflow — ft./min (m/sec)					
	0 (0)	200 (1.01)	400 (2.03)	600 (3.07)	800 (4.06)	1000 (5.07)
θ Junction-to-Case (Case measured as shown in Figure 5.)	1.5	1.5	1.5	1.5	1.5	1.5
θ Case-to-Ambient (No Heatsink)	17	14	11	9	7.1	6.6
θ Case-to-Ambient (With Heatsink) (See Note 3.)	13	9	5.5	5	3.9	3.4

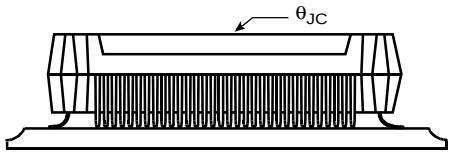


NOTES:
1. This table applies to 80960CF PGA plugged into socket or soldered directly to board.
2. $\theta_{JA} = \theta_{JC} + \theta_{CA}$
3. 0.285" high unidirectional heatsink (Al alloy 6061, 50 mil fin width, 150 mil center-to-center fin spacing).

Table 12. 80960CF PQFP Package Thermal Characteristics

Thermal Resistance — °C/Watt							
Parameter	Airflow — ft./min (m/sec)						
	0 (0)	50 (0.25)	100 (0.50)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)
θ Junction-to-Case (Case Measured as shown in Figure 5.)	5	5	5	5	5	5	5
θ Case-to-Ambient (No Heatsink)	19	18	17	15	12	10	9

NOTES:
1. This table applies to 80960CF PQFP soldered directly to board.
2. $\theta_{JA} = \theta_{JC} + \theta_{CA}$



3.5 Stepping Register Information

Upon reset, register g0 contains die stepping information (see Figure 6). The most significant byte contains ASCII 0; the upper middle byte contains an ASCII C; the lower middle byte contains an ASCII F. The least significant byte contains the stepping number in ASCII, and g0 retains this information until it is overwritten by the user program. Table 13 contains a cross reference of the number in the least significant byte of register g0 to the die stepping number.

Figure 6. Register g0

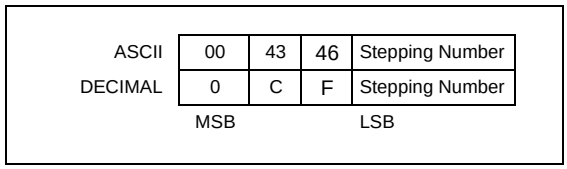


Table 13. Die Stepping Cross Reference

g0 Least Significant Byte	Die Stepping
01	A
02	B
03	C
04	D
05	E

3.6 Sources for Accessories

The following is a list of suggested sources for 80960CF accessories. This is neither an endorsement nor a warranty of the performance of any of the listed products and/or companies.

Sockets

1. 3M Textool Test and Interconnection Products
   6801 River Place Blvd. Mail Stop 130-3N-29
   Austin, TX 78726-9000
   (800) 328-0411
2. Augat, Inc. Interconnection Products Group
   452 John Dietsch Blvd.
   Attleboro Falls, MA 02763
   (508) 699-7646
3. Concept Mfg., Inc. (Decoupling Sockets)
   400 Walnut St. Suite 609
   Redwood City, CA 94063
   (415) 365-1162 FAX: (415)265-1164

Heatsinks/Fins

1. Thermalloy, Inc.
   2021 West Valley View Lane
   Dallas, TX 75234
   (214) 243-4321
   FAX: (214) 241-4656
2. Wakefield Engineering
   60 Audubon Road
   Wakefield, MA 01880
   (617) 245-5900

4.0 Electrical Specifications

4.1 Absolute Maximum Ratings

Table 14 presents the absolute maximum ratings for the 80960CF.

Table 14. Absolute Maximum Ratings

Parameter	Maximum Rating
Storage Temperature	–65 °C to +150 °C
Case Temperature Under Bias	–65 °C to +110 °C
Supply Voltage wrt. V_{SS}	–0.5 V to + 6.5 V
Voltage on Other Pins wrt. V_{SS}	–0.5 V to V_{CC} + 0.5 V

Note: The specifications are subject to change without notice. Verify with your local Intel sales office that you have the latest datasheet before finalizing a design.

Warning: Stressing the device beyond the “Absolute Maximum Ratings” may cause permanent damage. These are stress ratings only. Operation beyond the “Operating Conditions” is not recommended and extended exposure beyond the “Operating Conditions” may affect device reliability.

4.2 Operating Conditions

Table 15 presents the operating conditions for the 80960CF.

Table 15. Operating Conditions

Symbol	Parameter	Min	Max	Units	Notes
V_{CC}	Supply Voltage 80960CF-40 80960CF-33 80960CF-25	 4.75 4.50 4.50	 5.25 5.50 5.50	V	
f_{CLK2x}	Input Clock Frequency (2-x Mode) 80960CF-40 80960CF-33 80960CF-25	 0 0 0	 80 66 50	MHz	
f_{CLK1x}	Input Clock Frequency (1-x Mode) 80960CF-40 80960CF-33 80960CF-25	 8 8 8	 40 33 25	MHz	(†)
T_C	Case Temp Under Bias PGA Pkg. (80960CF-40) PGA Pkg. (80960CF-33, -25 Only) 196-Pin PQFP (80960CF-33, -25 Only)	 0 0 0	 85 100 100	°C	

† When in the 1-x input clock mode, CLKIN is an input to an internal phase-locked loop and must maintain a minimum frequency of 8 MHz for proper processor operation. However, in the 1-x mode, CLKIN may still be stopped when the processor is in a reset condition. When CLKIN is stopped, the specified $\overline{\text{RESET}}$ low time must be provided once CLKIN restarts and has stabilized.

4.3 Recommended Connections

Power and ground connections must be made to multiple V_{CC} and V_{SS} (GND) pins. Every 80960CF-based circuit board should include power (V_{CC}) and ground (V_{SS}) planes for power distribution. Every V_{CC} pin must be connected to the power plane, and every V_{SS} pin must be connected to the ground plane. Pins identified as 'NC' **must not** be connected in the system.

Liberal decoupling capacitance should be placed near the 80960CF. The processor may cause transient power surges when its numerous output buffers transition, particularly when connected to large capacitive loads.

Low inductance capacitors and interconnects are recommended for best high frequency electrical performance. Inductance may be reduced by shortening the board traces between the processor and decoupling capacitors as much as possible. Capacitors specifically designed for PGA packages may offer the lowest possible inductance.

For reliable operation, always connect unused inputs to an appropriate signal level. In particular, any unused interrupt ($\overline{XINT}$, $\overline{NMI}$), DMA ($\overline{DREQ}$), or $\overline{BTERM}$ input should be connected to V_{CC} through a pull-up resistor. Pull-up resistors should be in the in the range of 20 KW for each pin tied high. When $\overline{READY}$ or HOLD are not used, the unused input should be connected to ground. **N.C. pins must always remain unconnected.** For additional information refer to the *i960® CA/CF Microprocessor User's Manual* (order number 270710).

4.4 D.C. Specifications

Table 16 presents the D.C. specifications of the 80960CF.

Table 16. D.C. Specifications

Symbol	Parameter (1)	Min	Max	Units	Notes
V_{IL}	Input Low Voltage for all pins except $\overline{RESET}$	– 0.3	+0.8	V	
V_{IH}	Input High Voltage for all pins except $\overline{RESET}$	2.0	V_{CC} + 0.3	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 5 mA
V_{OH}	Output High Voltage I_{OH} = –1 mA I_{OH} = – 200 µA	2.4 V_{CC} – 0.5		V V	
V_{ILR}	Input Low Voltage for $\overline{RESET}$	– 0.3	1.5	V	
V_{IHR}	Input High Voltage for $\overline{RESET}$	3.5	V_{CC} + 0.3	V	
I_{LI1}	Input Leakage Current for each pin *except*: $\overline{BTERM}$, $\overline{ONCE}$, $\overline{DREQ3:0}$, $\overline{STEST}$, $\overline{EOP3:0}$/TC3:0, NMI, XINT7:0, $\overline{BOFF}$, READY, HOLD, CLKMODE		±15	µA	$0 \le V_{IN} \le V_{CC}$ (2)
I_{LI2}	Input Leakage Current for: $\overline{BTERM}$, $\overline{ONCE}$, $\overline{DREQ3:0}$, $\overline{STEST}$, $\overline{EOP3:0}$/TC3:0, NMI, XINT7:0, $\overline{BOFF}$	0	– 300	µA	V_{IN} = 0.45 V (3)
I_{LI3}	Input Leakage Current for: READY, HOLD, CLKMODE	0	500	µA	V_{IN} = 2.4 V (4, 8)
I_{LO}	Output Leakage Current		±15	µA	$0.45 \le V_{OUT} \le V_{CC}$
I_{CC}	Supply Current (80960CF-40, 33): I_{CC} Max I_{CC} Typ		 1150 1000	 mA mA	 (5) (6)
I_{CC}	Supply Current (80960CF-25): I_{CC} Max I_{CC} Typ		 950 775	 mA mA	 (5) (6)
I_{CC}	Supply Current (80960CF-16): I_{CC} Max I_{CC} Typ		 750 575	 mA	 (5) (6)
I_{ONCE}	ONCE-mode Supply Current 80960CF-40 80960CF-33, -25, -16		 225 150	 mA	
C_{IN}	Input Capacitance for: CLKIN, $\overline{RESET}$, $\overline{ONCE}$, $\overline{READY}$, $\overline{HOLD}$, $\overline{DREQ3:0}$, $\overline{BOFF}$, $\overline{XINT7:0}$, NMI, $\overline{BTERM}$, CLKMODE	0	12	pF	F_C = 1 MHz
C_{OUT}	Output Capacitance of each output pin		12	pF	F_C = 1 MHz (7)
$C_{I/O}$	I/O Pin Capacitance		12	pF	F_C = 1 MHz

NOTES:
1. 80960CF-33 and -25 under the conditions described in Section 4.2, “Operating Conditions” on page 26.
2. No pullup or pulldown.
3. These pins have internal pullup resistors.
4. These pins have internal pulldown resistors.
5. Measured at worst case frequency, V_{CC} and temperature, with device operating and outputs loaded to the test conditions described in Section 4.5.1, “A.C. Test Conditions” on page 35**.**
6. I_{CC} Typical is not tested.
7. Output Capacitance is the capacitive load of a floating output.
8. CLKMODE pin has a pulldown resistor only when $\overline{ONCE}$ pin is deasserted.

4.5 A.C. Specifications

Table 17. 80960CF AC Characteristics (40 MHz) (Sheet 1 of 2)

Symbol	Parameter (1)		Min	Max	Units	Notes
Input Clock (2, 10)						
T_F	CLKIN Frequency		0	80	MHz	
T_C	CLKIN Period	In 1-x Mode (f_{CLK1x}) In 2-x Mode (f_{CLK2x})	25 12.5	125 ∞	ns ns	(12)
T_{CS}	CLKIN Period Stability	In 1-x Mode (f_{CLK1x})		±0.1%	Δ	(13)
T_{CH}	CLKIN High Time	In 1-x Mode (f_{CLK1x}) In 2-x Mode (f_{CLK2x})	5 5	62.5 ∞	ns ns	(12)
T_{CL}	CLKIN Low Time	In 1-x Mode (f_{CLK1x}) In 2-x Mode (f_{CLK2x})	5 5	62.5 ∞	ns ns	(12)
T_{CR}	CLKIN Rise Time		0	6	ns	
T_{CF}	CLKIN Fall Time		0	6	ns	
Output Clocks (2, 9)						
T_{CP}	CLKIN to PCLK2:1 Delay	In 1-x Mode (f_{CLK1x}) In 2-x Mode (f_{CLK2x})	– 2 2	2 25	ns ns	(4, 13) (4)
T	PCLK2:1 Period	In 1-x Mode (f_{CLK1x}) In 2-x Mode (f_{CLK2x})	T_C $2T_C$		ns ns	(13) (4)
T_{PH}	PCLK2:1 High Time		(T/2) – 2	T/2	ns	(13)
T_{PL}	PCLK2:1 Low Time		(T/2) – 2	T/2	ns	(13)
T_{PR}	PCLK2:1 Rise Time		1	4	ns	(4)
T_{PF}	PCLK2:1 Fall Time		1	4	ns	(4)
Synchronous Outputs (9)						
T_{OH} T_{OV}	Output Valid Delay, Output Hold					(7, 11)
	T_{OH1}, T_{OV1}	A31:2	3	14	ns	
	T_{OH2}, T_{OV2}	BE3:0	3	16	ns	
	T_{OH3}, T_{OV3}	ADS	6	16	ns	
	T_{OH4}, T_{OV4}	W/R	3	16	ns	
	T_{OH5}, T_{OV5}	D/C, SUP, DMA	4	16	ns	
	T_{OH6}, T_{OV6}	BLAST, WAIT	5	16	ns	
	T_{OH7}, T_{OV7}	DEN	3	16	ns	
	T_{OH8}, T_{OV8}	HOLDA, BREQ	4	16	ns	
	T_{OH9}, T_{OV9}	LOCK	4	16	ns	
	T_{OH10}, T_{OV10}	DACK3:0	4	16	ns	
	T_{OH11}, T_{OV11}	D31:0	3	16	ns	
	T_{OH12}, T_{OV12}	DT/R	T/2 + 3	T/2 + 14	ns	
	T_{OH13}, T_{OV13}	FAIL	2	14	ns	
	T_{OH14}, T_{OV14}	EOP3:0/TC3:0	3	16	ns	(7, 11)
T_{OF}	Output Float for all outputs		3	22	ns	(7)
Synchronous Inputs (2, 10, 11)						
T_{IS}	Input Setup					
	T_{IS1}	D31:0	3		ns	
	T_{IS2}	BOFF	15		ns	
	T_{IS3}	BTERM/READY	7		ns	
	T_{IS4}	HOLD	5		ns	

Table 17. 80960CF AC Characteristics (40 MHz) (Sheet 2 of 2)

Symbol	Parameter (1)	Min	Max	Units	Notes
T_{IH}	Input Hold T_{IH1} D31:0 T_{IH2} BOFF T_{IH3} BTERM/READY T_{IH4} HOLD	 5 5 2 3		 ns ns ns ns	
Relative Output Timings (2, 3, 4, 9)					
T_{AVSH1}	A31:2 Valid to ADS Rising	T – 4	T + 4	ns	
T_{AVSH2}	BE3:0, W/R, SUP, D/C, DMA, DACK3:0 Valid to ADS Rising	T – 6	T + 6	ns	
T_{AVEL1}	A31:2 Valid to DEN Falling	T – 4	T + 4	ns	
T_{AVEL2}	BE3:0, W/R, SUP, INST,DMA, DACK3:0 Valid to DEN Falling	T – 6	T + 6	ns	
T_{NLQV}	WAIT Falling to Output Data Valid	± 6		ns	
T_{DVNH}	Output Data Valid to WAIT Rising	N*T – 6	N*T + 6	ns	(5)
T_{NLNH}	WAIT Falling to WAIT Rising	N*T ± 4		ns	(5)
T_{NHQX}	Output Data Hold after WAIT Rising	(N+1)*T–8	(N+1)*T+6	ns	(6)
T_{EHTV}	DT/R Hold after DEN High	T/2 – 7		ns	(7)
T_{TVEL}	DT/R Valid to DEN Falling	T/2 – 4		ns	
Relative Input Timings (2, 3, 4)					
T_{IS5}	RESET Input Setup (2-x Clock Mode)	6		ns	(14)
T_{IH5}	RESET Input Hold (2-x Clock Mode)	5		ns	(14)
T_{IS6}	DREQ3:0 Input Setup	12		ns	(8)
T_{IH6}	DREQ3:0 Input Hold	7		ns	(8)
T_{IS7}	XINT7:0, NMI Input Setup	7		ns	(16)
T_{IH7}	XINT7:0, NMI Input Hold	3		ns	(16)
T_{IS8}	RESET Input Setup (1-x Clock Mode)	3		ns	(15)
T_{IH8}	RESET Input Hold (1-x Clock Mode)	T/4 + 1		ns	(15)

NOTES:
1. 80960CF-40 only, per the conditions in Section 4.2, Operating Conditions and Section 4.5.1, A.C. Test Conditions.
2. See Table 19 for all notes related to AC specifications.

Table 18. 80960CF AC Characteristics (33 MHz) (Sheet 1 of 2)

Symbol	Parameter (1)		Min	Max	Units	Notes
Input Clock (2, 10)						
T_F	CLKIN Frequency		0	66.66	MHz	
T_C	CLKIN Period	In 1-x Mode (f_{CLK1x}) In 2-x Mode (f_{CLK2x})	30 15	125 ∞	ns ns	(12)
T_{CS}	CLKIN Period Stability	In 1-x Mode (f_{CLK1x})		±0.1%	Δ	(13)
T_{CH}	CLKIN High Time	In 1-x Mode (f_{CLK1x}) In 2-x Mode (f_{CLK2x})	5 5	62.5 ∞	ns ns	(12)
T_{CL}	CLKIN Low Time	In 1-x Mode (f_{CLK1x}) In 2-x Mode (f_{CLK2x})	5 5	62.5 ∞	ns ns	(12)
T_{CR}	CLKIN Rise Time		0	6	ns	
T_{CF}	CLKIN Fall Time		0	6	ns	
Output Clocks (2, 9)						
T_{CP}	CLKIN to PCLK2:1 Delay	In 1-x Mode (f_{CLK1x}) In 2-x Mode (f_{CLK2x})	– 2 2	2 25	ns ns	(4,13) (4)
T	PCLK2:1 Period	In 1-x Mode (f_{CLK1x}) In 2-x Mode (f_{CLK2x})	TC 2TC		ns ns	(13) (4)
T_{PH}	PCLK2:1 High Time		(T/2) – 2	T/2	ns	(13)
T_{PL}	PCLK2:1 Low Time		(T/2) – 2	T/2	ns	(13)
T_{PR}	PCLK2:1 Rise Time		1	4	ns	(4)
T_{PF}	PCLK2:1 Fall Time		1	4	ns	(4)
Synchronous Outputs (9)						
T_{OH} T_{OV}	Output Valid Delay, Output Hold T_{OH1}, T_{OV1} T_{OH2}, T_{OV2} T_{OH3}, T_{OV3} T_{OH4}, T_{OV4} T_{OH5}, T_{OV5} T_{OH6}, T_{OV6} T_{OH7}, T_{OV7} T_{OH8}, T_{OV8} T_{OH9}, T_{OV9} T_{OH10}, T_{OV10} T_{OH11}, T_{OV11} T_{OH12}, T_{OV12} T_{OH13}, T_{OV13} T_{OH14}, T_{OV14}	 A31:2 BE3:0 ADS W/R D/C, SUP, DMA BLAST, WAIT DEN HOLDA, BREQ LOCK DACK3:0 D31:0 DT/R FAIL EOP3:0/TC3:0	 3 3 6 3 4 5 3 4 4 4 3 T/2 + 3 2 3	 14 16 18 18 16 16 16 16 16 18 16 T/2 + 14 14 18	 ns ns ns ns ns ns ns ns ns ns ns ns ns ns ns	(7, 11) (7, 11)
T_{OF}	Output Float for all outputs		3	22	ns	(7)
Synchronous Inputs (2, 10, 11)						
T_{IS}	Input Setup TIS1 TIS2 TIS3 TIS4	 D31:0 BOFF BTERM/READY HOLD	 3 17 7 7		 ns ns ns ns	
T_{IH}	Input Hold TIH1 TIH2 TIH3 TIH4	 D31:0 BOFF BTERM/READY HOLD	 5 5 2 3		 ns ns ns ns	

Table 18. 80960CF AC Characteristics (33 MHz) (Sheet 2 of 2)

Symbol	Parameter (1)	Min	Max	Units	Notes
Relative Output Timings (2, 3, 4, 9)					
T_{AVSH1}	A31:2 Valid to $\overline{ADS}$ Rising	T – 4	T + 4	ns	
T_{AVSH2}	$\overline{BE3:0}$, W/$\overline{R}$, $\overline{SUP}$, D/$\overline{C}$, $\overline{DMA}$, $\overline{DACK3:0}$ Valid to $\overline{ADS}$ Rising	T – 6	T + 6	ns	
T_{AVEL1}	A31:2 Valid to $\overline{DEN}$ Falling	T – 4	T + 4	ns	
T_{AVEL2}	$\overline{BE3:0}$, W/$\overline{R}$, $\overline{SUP}$, $\overline{INST}$,$\overline{DMA}$, $\overline{DACK3:0}$ Valid to $\overline{DEN}$ Falling	T – 6	T + 6	ns	
T_{NLQV}	$\overline{WAIT}$ Falling to Output Data Valid	± 6		ns	
T_{DVNH}	Output Data Valid to $\overline{WAIT}$ Rising	N*T – 6	N*T + 6	ns	(5)
T_{NLNH}	$\overline{WAIT}$ Falling to $\overline{WAIT}$ Rising	N*T ± 4		ns	(5)
T_{NHQX}	Output Data Hold after $\overline{WAIT}$ Rising	(N+1)*T–8	(N+1)*T+6	ns	(6)
T_{EHTV}	DT/$\overline{R}$ Hold after $\overline{DEN}$ High	T/2 – 7	∞	ns	(7)
T_{TVEL}	DT/$\overline{R}$ Valid to $\overline{DEN}$ Falling	T/2 – 4		ns	
Relative Input Timings (2, 3, 4)					
T_{IS5}	$\overline{RESET}$ Input Setup (2-x Clock Mode)	6		ns	(14)
T_{IH5}	$\overline{RESET}$ Input Hold (2-x Clock Mode)	5		ns	(14)
T_{IS6}	$\overline{DREQ3:0}$ Input Setup	12		ns	(8)
T_{IH6}	$\overline{DREQ3:0}$ Input Hold	7		ns	(8)
T_{IS7}	$\overline{XINT7:0}$, NMI Input Setup	7		ns	(16)
T_{IH7}	$\overline{XINT7:0}$, NMI Input Hold	3		ns	(16)
T_{IS8}	$\overline{RESET}$ Input Setup (1-x Clock Mode)	3		ns	(15)
T_{IH8}	$\overline{RESET}$ Input Hold (1-x Clock Mode)	T/4 + 1		ns	(15)

NOTES:
1. 80960CF-33 only, per the conditions in Section 4.2, Operating Conditions and Section 4.5.1, A.C. Test Conditions.
2. See Table 19 for all notes related to AC specifications.

Table 19. 80960CF AC Characteristics (25 MHz) (Sheet 1 of 3)

Symbol	Parameter (1)		Min	Max	Unit	Notes
	Input Clock (2, 10)					
T_F	CLKIN Frequency		0	50	MHz	
T_C	CLKIN Period	In 1-x Mode (f_{CLK1x}) In 2-x Mode (f_{CLK2x})	40 20	125 ∞	ns ns	(12)
T_{CS}	CLKIN Period Stability	In 1-x Mode (f_{CLK1x})		±0.1%	Δ	(13)
T_{CH}	CLKIN High Time	In 1-x Mode (f_{CLK1x}) In 2-x Mode (f_{CLK2x})	8 8	62.5 ∞	ns ns	(12)
T_{CL}	CLKIN Low Time	In 1-x Mode (f_{CLK1x}) In 2-x Mode (f_{CLK2x})	8 8	62.5 ∞	ns ns	(12)
T_{CR}	CLKIN Rise Time		0	6	ns	
T_{CF}	CLKIN Fall Time		0	6	ns	
	Output Clocks (2, 9)					
T_{CP}	CLKIN to PCLK2:1 Delay	In 1-x Mode (f_{CLK1x}) In 2-x Mode (f_{CLK2x})	– 2 2	2 25	ns ns	(4, 13) (4)
T	PCLK2:1 Period	In 1-x Mode (f_{CLK1x}) In 2-x Mode (f_{CLK2x})	T_C $2T_C$		ns ns	(13) (4)
T_{PH}	PCLK2:1 High Time		(T/2) – 3	T/2	ns	(13)
T_{PL}	PCLK2:1 Low Time		(T/2) – 3	T/2	ns	(13)
T_{PR}	PCLK2:1 Rise Time		1	4	ns	(4)
T_{PF}	PCLK2:1 Fall Time		1	4	ns	(4)
	Synchronous Outputs (9)					
T_{OH} T_{OV}	Output Valid Delay, Output Hold					(7, 11)
	T_{OH1}, T_{OV1}	A31:2	3	16	ns	
	T_{OH2}, T_{OV2}	BE3:0	3	18	ns	
	T_{OH3}, T_{OV3}	ADS	6	20	ns	
	T_{OH4}, T_{OV4}	W/R	3	20	ns	
	T_{OH5}, T_{OV5}	D/C, SUP, DMA	4	18	ns	
	T_{OH6}, T_{OV6}	BLAST, WAIT	5	18	ns	
	T_{OH7}, T_{OV7}	DEN	3	18	ns	
	T_{OH8}, T_{OV8}	HOLDA, BREQ	4	18	ns	
	T_{OH9}, T_{OV9}	LOCK	4	18	ns	
	T_{OH10}, T_{OV10}	DACK3:0	4	20	ns	
	T_{OH11}, T_{OV11}	D31:0	3	18	ns	
	T_{OH12}, T_{OV12}	DT/R	T/2 + 3	T/2 + 16	ns	
	T_{OH13}, T_{OV13}	FAIL	2	16	ns	
	T_{OH14}, T_{OV14}	EOP3:0/TC3:0	3	20	ns	(7, 11)
T_{OF}	Output Float for all outputs		3	22	ns	(7)
	Synchronous Inputs (2, 10, 11)					
T_{IS}	Input Setup					
	T_{IS1}	D31:0	5		ns	
	T_{IS2}	BOFF	19		ns	
	T_{IS3}	BTERM/READY	9		ns	
	T_{IS4}	HOLD	9		ns	
T_{IH}	Input Hold					
	T_{IH1}	D31:0	5		ns	
	T_{IH2}	BOFF	19		ns	
	T_{IH3}	BTERM/READY	9		ns	
	T_{IH4}	HOLD	9		ns	

Table 19. 80960CF AC Characteristics (25 MHz) (Sheet 2 of 3)

Symbol	Parameter (1)	Min	Max	Unit	Notes
Relative Output Timings (2, 3, 4, 9)					
T_{AVSH1}	A31:2 Valid to $\overline{ADS}$ Rising	T – 4	T + 4	ns	
T_{AVSH2}	$\overline{BE3:0}$, W/$\overline{R}$, $\overline{SUP}$, D/$\overline{C}$, $\overline{DMA}$, DACK3:0 Valid to $\overline{ADS}$ Rising	T – 6	T + 6	ns	
T_{AVEL1}	A31:2 Valid to $\overline{DEN}$ Falling	T – 4	T + 4	ns	
T_{AVEL2}	$\overline{BE3:0}$, W/$\overline{R}$, $\overline{SUP}$, $\overline{INST}$, $\overline{DMA}$, DACK3:0 Valid to $\overline{DEN}$ Falling	T – 6	T + 6	ns	
T_{NLQV}	$\overline{WAIT}$ Falling to Output Data Valid	± 6		ns	
T_{DVNH}	Output Data Valid to $\overline{WAIT}$ Rising	N*T – F	N*T + 6	ns	(5)
T_{NLNH}	$\overline{WAIT}$ Falling to $\overline{WAIT}$ Rising	N*T ± 4		ns	(5)
T_{NHQX}	Output Data Hold after $\overline{WAIT}$ Rising	(N+1)*T–8	(N+1)*T+6	ns	(6)
T_{EHTV}	DT/$\overline{R}$ Hold after $\overline{DEN}$ High	T/2 – 7	∞	ns	(7)
T_{TVEL}	DT/$\overline{R}$ Valid to $\overline{DEN}$ Falling	T/2 – 4		ns	
Relative Input Timings (2, 3, 4)					
T_{IS5}	$\overline{RESET}$ Input Setup (2-x Clock Mode)	8		ns	(14)
T_{IH5}	$\overline{RESET}$ Input Hold (2-x Clock Mode)	7		ns	(14)
T_{IS6}	$\overline{DREQ3:0}$ Input Setup	14		ns	(8)
T_{IH6}	$\overline{DREQ3:0}$ Input Hold	9		ns	(8)
T_{IS7}	$\overline{XINT7:0}$, $\overline{NMI}$ Input Setup	9		ns	(16)
T_{IH7}	$\overline{XINT7:0}$, $\overline{NMI}$ Input Hold	5		ns	(16)
T_{IS8}	$\overline{RESET}$ Input Setup (1-x Clock Mode)	3		ns	(15)
T_{IH8}	$\overline{RESET}$ Input Hold (1-x Clock Mode)	T/4 + 1		ns	(15)

Table 19. 80960CF AC Characteristics (25 MHz) (Sheet 3 of 3)

Symbol	Parameter (1)	Min	Max	Unit	Notes

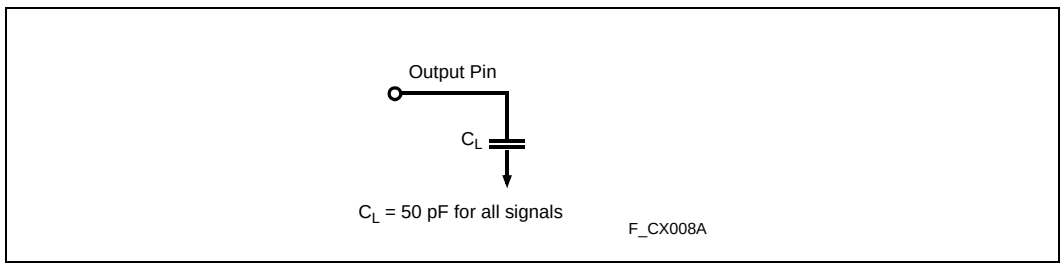
NOTES:
1. 80960CF-25 only, per the conditions in Section 4.2, Operating Conditions and Section 4.5.1, A.C. Test Conditions.
2. See Section 4.5.2, A.C. Timing Waveforms for waveforms and definitions.
3. See Figure 16 for capacitive derating information for output delays and hold times.
4. See Figure 17 for capacitive derating information for rise and fall times.
5. Where N is the number of NRAD, NRDD, NWAD or NWDD wait states that are programmed in the Bus Controller Region Table. WAIT never goes active when there are no wait states in an access.
6. N = Number of wait states inserted with READY.
7. Output Data and/or DT/R may be driven indefinitely following a cycle when there is no subsequent bus activity.
8. Since asynchronous inputs are synchronized internally by the 80960CF, they have no required setup or hold times to be recognized and for proper operation. However, to ensure recognition of the input at a particular edge of PCLK2:1, the setup times shown must be met. Asynchronous inputs must be active for at least two consecutive PCLK2:1 rising edges to be seen by the processor.
9. These specifications are ensured by the processor.
10. These specifications must be met by the system for proper operation of the processor.
11. This timing is dependent upon the loading of PCLK2:1. Use the derating curves of Section 4.5.3, Derating Curves to adjust the timing for PCLK2:1 loading.
12. In the 1-x input clock mode, the maximum input clock period is limited to 125 ns while the processor is operating. When the processor is in reset, the input clock may stop even in 1-x mode.
13. When in the 1-x input clock mode, these specifications assume a stable input clock with a period variation of less than ± 0.1% between adjacent cycles.
14. In 2-x clock mode, RESET is an asynchronous input which has no required setup and hold time for proper operation. However, to ensure the device exits reset synchronized to a particular clock edge, the RESET pin must meet setup and hold times to the falling edge of the CLKIN. (See Figure 23.)
15. In 1-x clock mode, RESET is an asynchronous input which has no required setup and hold time for proper operation. However, to ensure the device exits reset synchronized to a particular clock edge, the RESET pin must meet setup and hold times to the rising edge of the CLKIN. (See Figure 24.)
16. The interrupt pins are synchronized internally by the 80960CF. They have no required setup or hold times for proper operation. These pins are sampled by the interrupt controller every other clock and must be active for at least three consecutive PCLK2:1 rising edges when asserting them asynchronously. To ensure recognition at a particular clock edge, the setup and hold times shown must be met for two consecutive PCLK2:1 rising edges.

4.5.1 A.C. Test Conditions

The AC Specifications in Section 4.5, “A.C. Specifications” on page 29 are tested with the 50 pF load shown in Figure 7. Figure 16 shows how timings vary with load capacitance.

Specifications are measured at the 1.5 V crossing point, unless otherwise indicated. Input waveforms are assumed to have a rise and fall time of $\leq$ 2 ns from 0.8 V to 2.0 V. See Section 4.5.2, “A.C. Timing Waveforms” on page 36 for AC specification definitions, test points and illustrations.

Figure 7. A.C. Test Load



4.5.2 A.C. Timing Waveforms

Figure 8. Input and Output Clocks Waveform

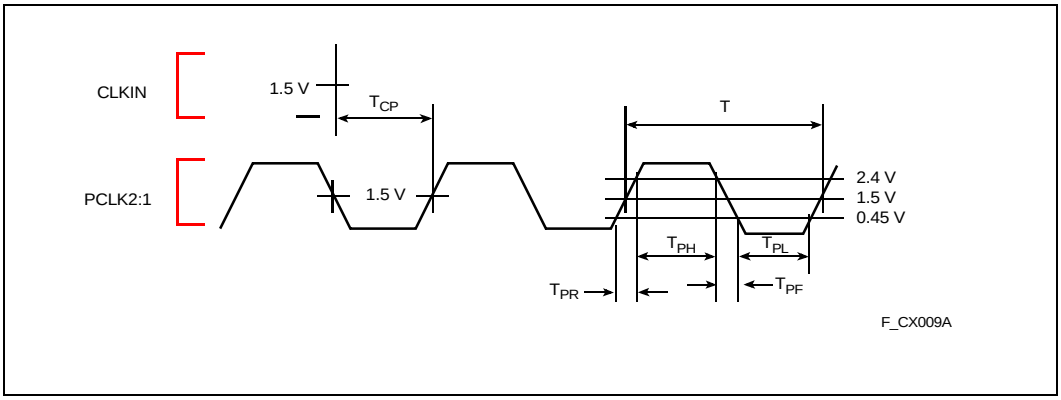


Figure 9. CLKIN Waveform

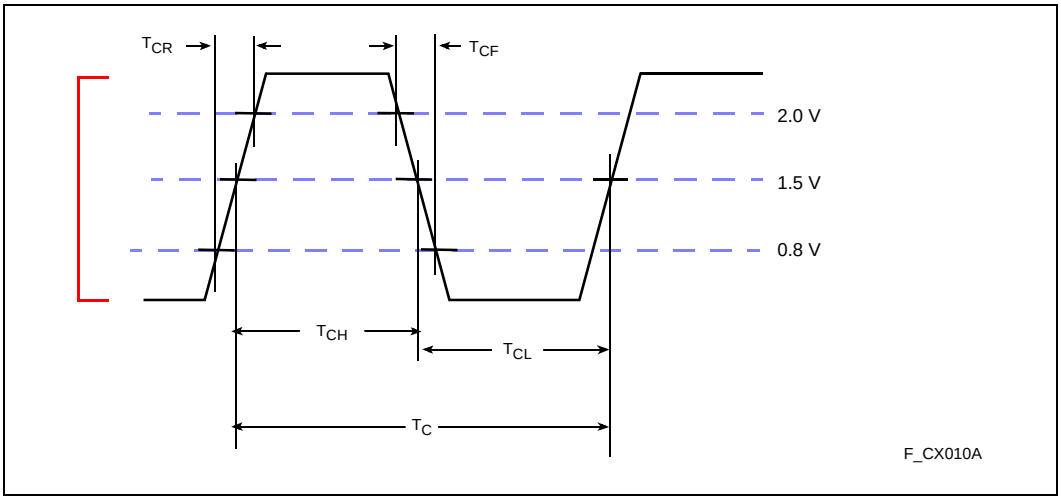
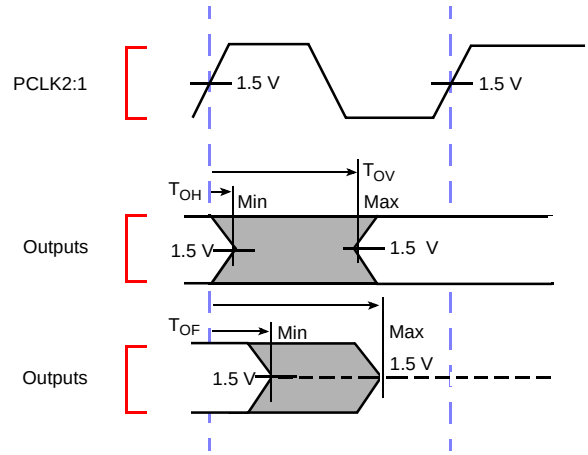
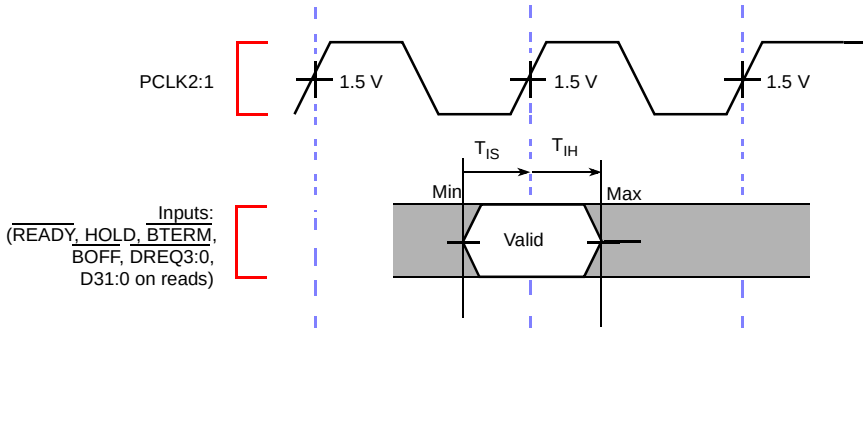


Figure 10. Output Delay and Float Waveform



NOTES:
1. T_{OV} T_{OH} - OUTPUT DELAY - Maximum output delay is referred to as Output Valid Delay (T_{OV}); minimum output delay is referred to as Output Hold (T_{OH}).
2. T_{OF} - OUTPUT FLOAT DELAY - Output float condition occurs when the maximum output current becomes less that I_{LO} in magnitude.

Figure 11. Input Setup and Hold Waveform



NOTE: T_{IS} T_{IH} - INPUT SETUP AND HOLD - The input setup and hold requirements specify the sampling window during which synchronous inputs must be stable for correct processor operation.

Figure 12. NMI, XINT7:0 Input Setup and Hold Waveform

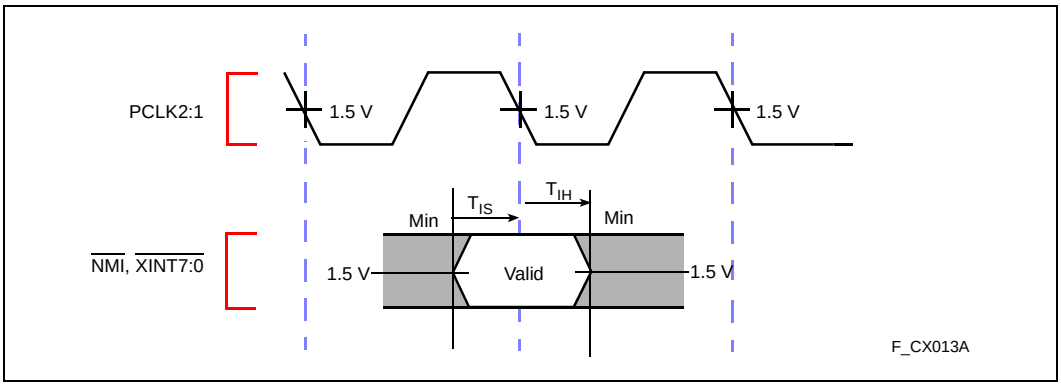
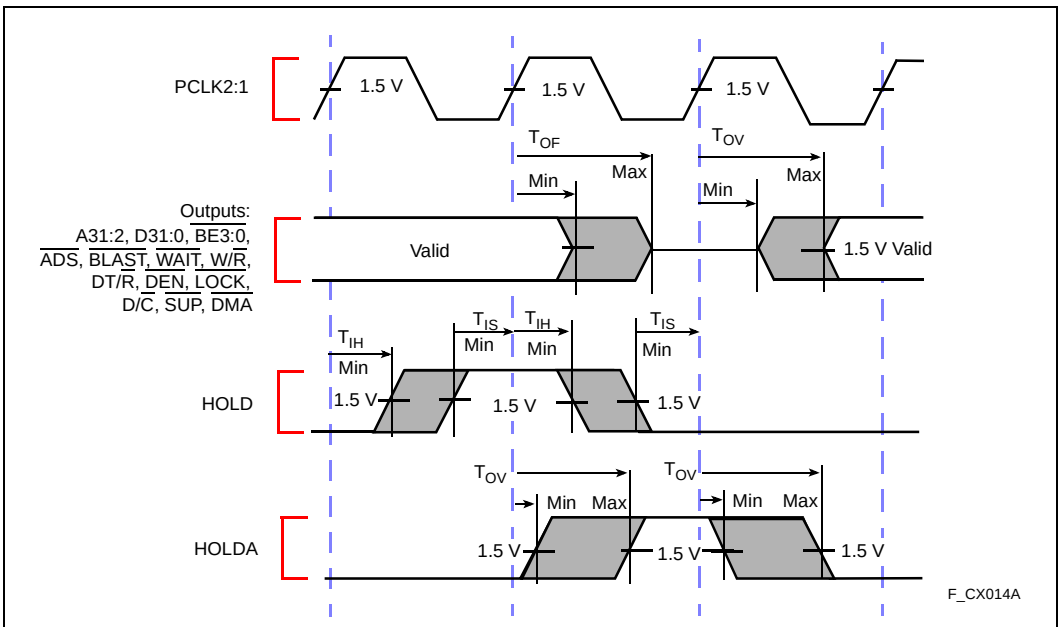


Figure 13. Hold Acknowledge Timings



NOTES:

1. T_{OV} T_{OH} - OUTPUT DELAY - Maximum output delay is referred to as Output Valid Delay (T_{OV}); minimum output delay is referred to as Output Hold (T_{OH}).
2. T_{OF} - OUTPUT FLOAT DELAY - Output float condition occurs when the maximum output current becomes less that I_{LO} in magnitude.
3. T_{IS} T_{IH} - INPUT SETUP AND HOLD - The input setup and hold requirements specify the sampling window during which synchronous inputs must be stable for correct processor operation.

Figure 14. Bus Backoff (BOFF) Timings

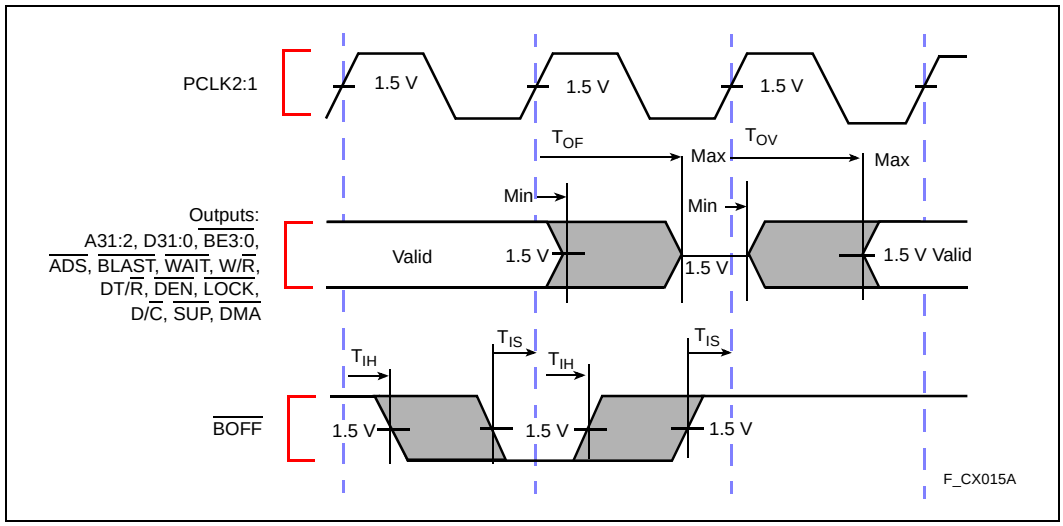
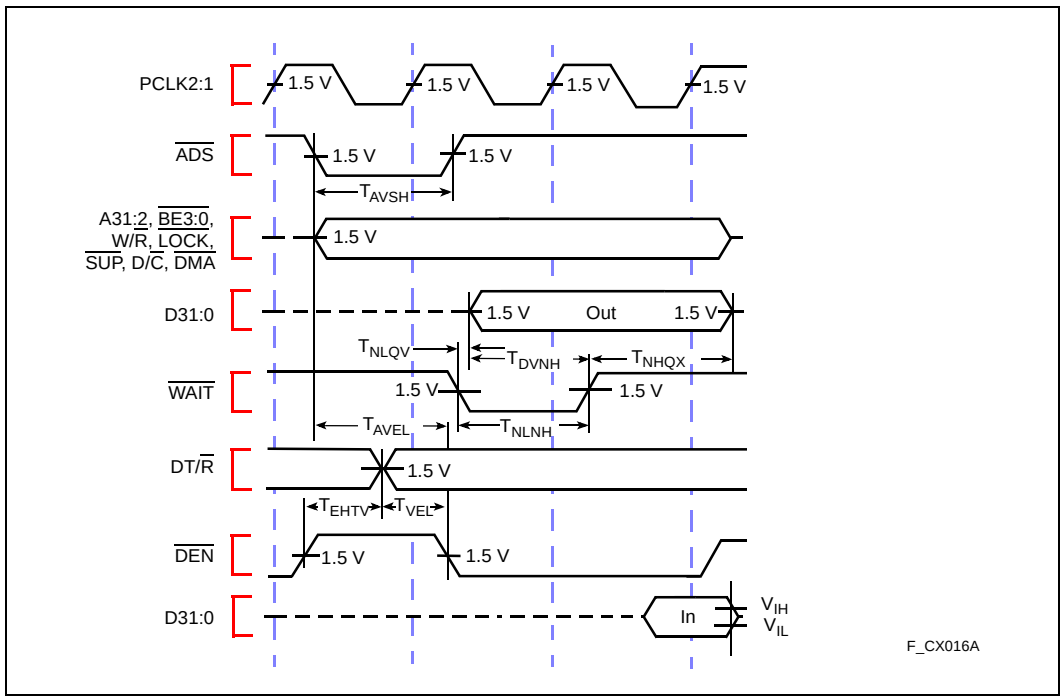


Figure 15. Relative Timings Waveforms



4.5.3 Derating Curves

Figure 16. Output Delay or Hold vs. Load Capacitance

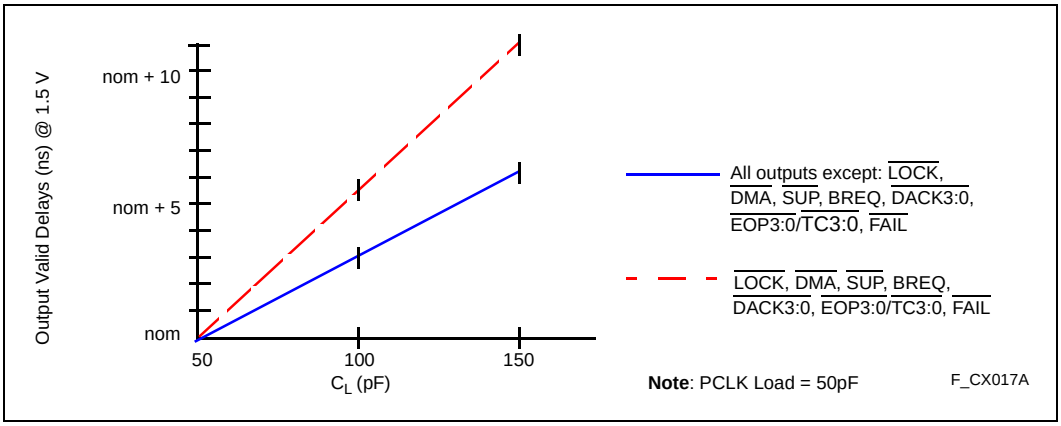


Figure 17. Rise and Fall Time Derating at Highest Operating Temperature and Minimum V_{CC}

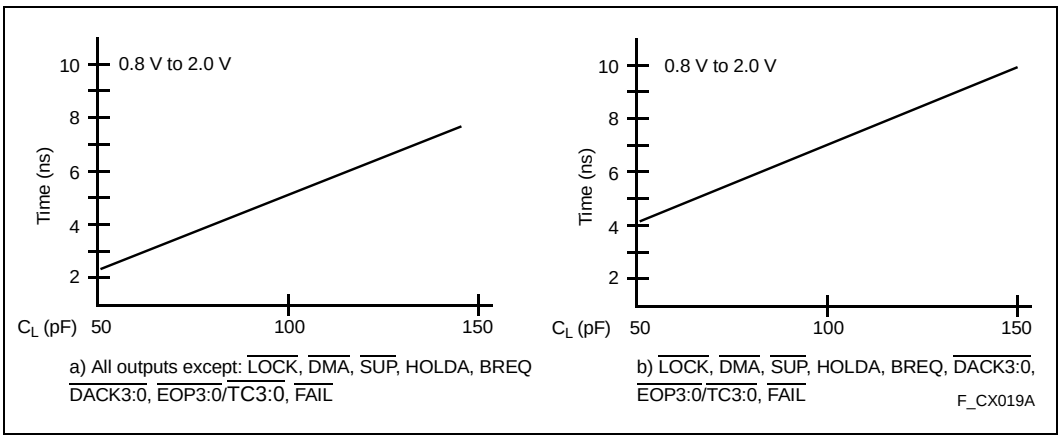


Figure 18. I_{CC} vs. Frequency and Temperature—80960CF-33 and -25

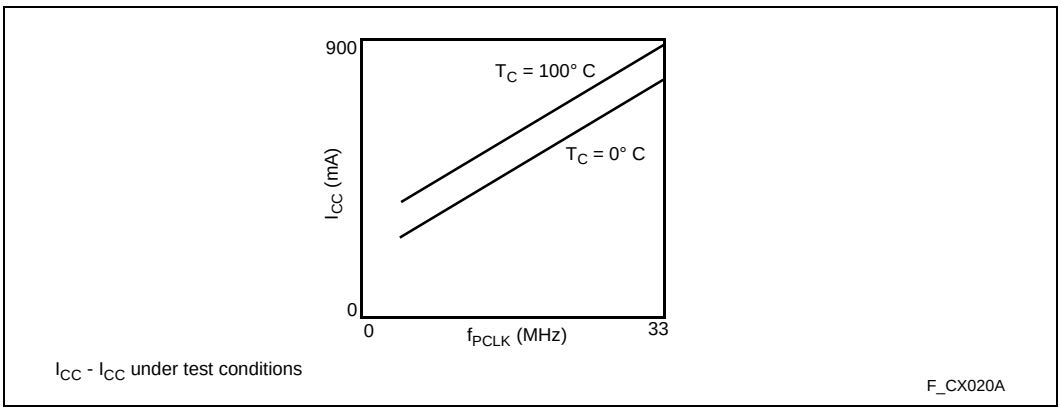
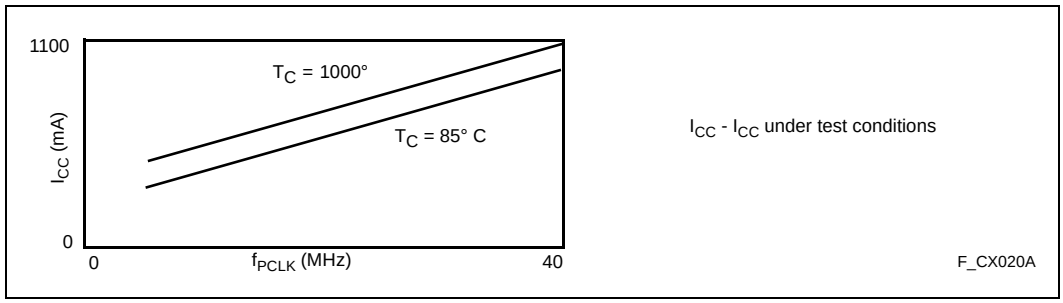


Figure 19. I_{CC} vs. Frequency and Temperature—80960CF-40



5.0 Reset, Backoff and Hold Acknowledge

Table 20 lists the condition of each processor output pin while $\overline{\text{RESET}}$ is asserted (low). Table 21 lists the condition of each processor output pin while HOLDA is asserted (high).

In Table 21, with regard to bus output pin state only, the Hold Acknowledge state takes precedence over the reset state. Although asserting the $\overline{\text{RESET}}$ pin internally resets the processor, the processor's bus output pins do not enter the reset state when Hold Acknowledge has been granted to a previous HOLD request (HOLDA is active). Furthermore, the processor grants new HOLD requests and enters the Hold Acknowledge state even while in reset.

For example, when HOLD is asserted while HOLDA is inactive and the processor is in the reset state, the processor's bus pins enter the Hold Acknowledge state and HOLDA is granted. The processor is not able to perform memory accesses until the HOLD request is removed, even when the $\overline{\text{RESET}}$ pin is brought high. This operation is provided to simplify boot-up synchronization among multiple processors sharing the same bus.

Table 20. Reset Conditions

Pins	State During Reset (HOLDA inactive)
A31:2	Floating
D31:0	Floating
$\overline{BE3:0}$	Driven high (Inactive)
W/$\overline{R}$	Driven low (Read)
$\overline{ADS}$	Driven high (Inactive)
$\overline{WAIT}$	Driven high (Inactive)
$\overline{BLAST}$	Driven low (Active)
DT/$\overline{R}$	Driven low (Receive)
$\overline{DEN}$	Driven high (Inactive)
$\overline{LOCK}$	Driven high (Inactive)
BREQ	Driven low (Inactive)
D/$\overline{C}$	Floating
$\overline{DMA}$	Floating
$\overline{SUP}$	Floating
$\overline{FAIL}$	Driven low (Active)
$\overline{DACK3:0}$	Driven high (Inactive)
$\overline{EOP3:0}$/$\overline{TC3:0}$	Floating (Set to input mode)

Table 21. Hold Acknowledge and Backoff Conditions

Pins	State During HOLDA
A31:2	Floating
D31:0	Floating
$\overline{BE3:0}$	Floating
W/$\overline{R}$	Floating
$\overline{ADS}$	Floating
$\overline{WAIT}$	Floating
$\overline{BLAST}$	Floating
DT/$\overline{R}$	Floating
$\overline{DEN}$	Floating
$\overline{LOCK}$	Floating
BREQ	Driven (High or low)
$\overline{D/C}$	Floating
$\overline{DMA}$	Floating
$\overline{SUP}$	Floating
$\overline{FAIL}$	Driven high (Inactive)
$\overline{DACK3:0}$	Driven high (Inactive)
$\overline{EOP3:0}$/$\overline{TC3:0}$	Driven (When output)

6.0 Bus Waveforms

Figure 20. Cold Reset Waveform

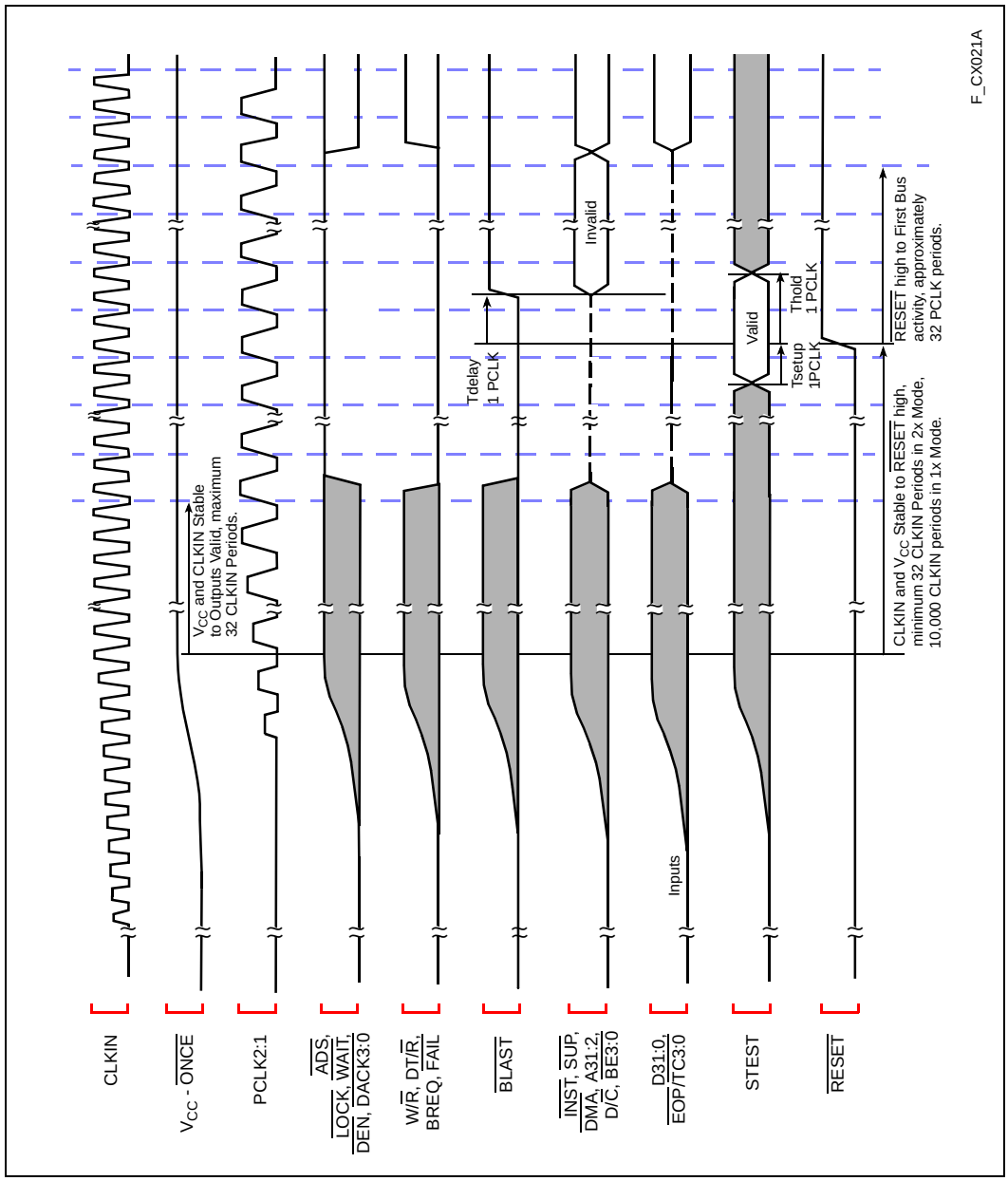


Figure 21. Warm Reset Waveform

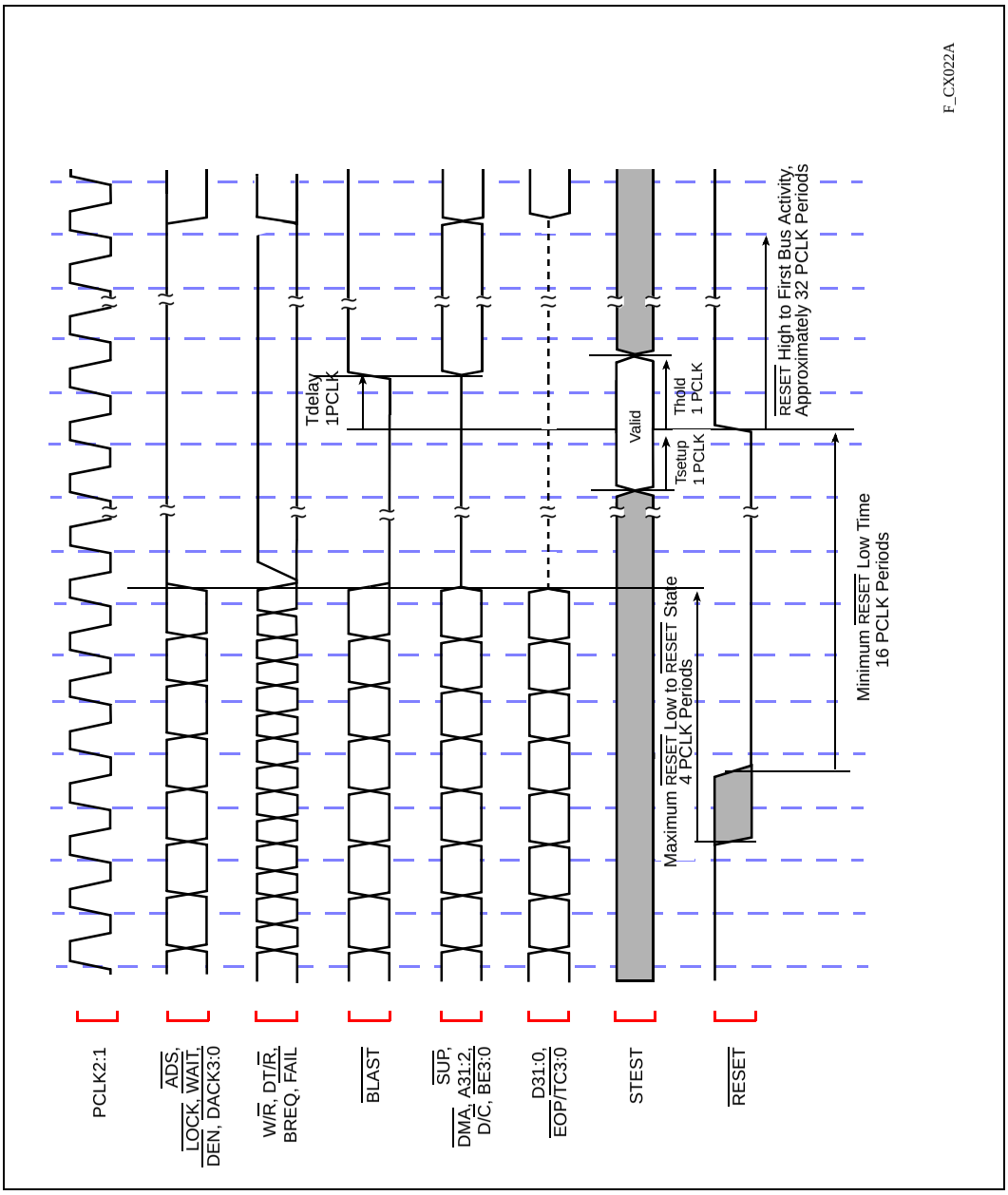


Figure 22. Entering the ONCE State

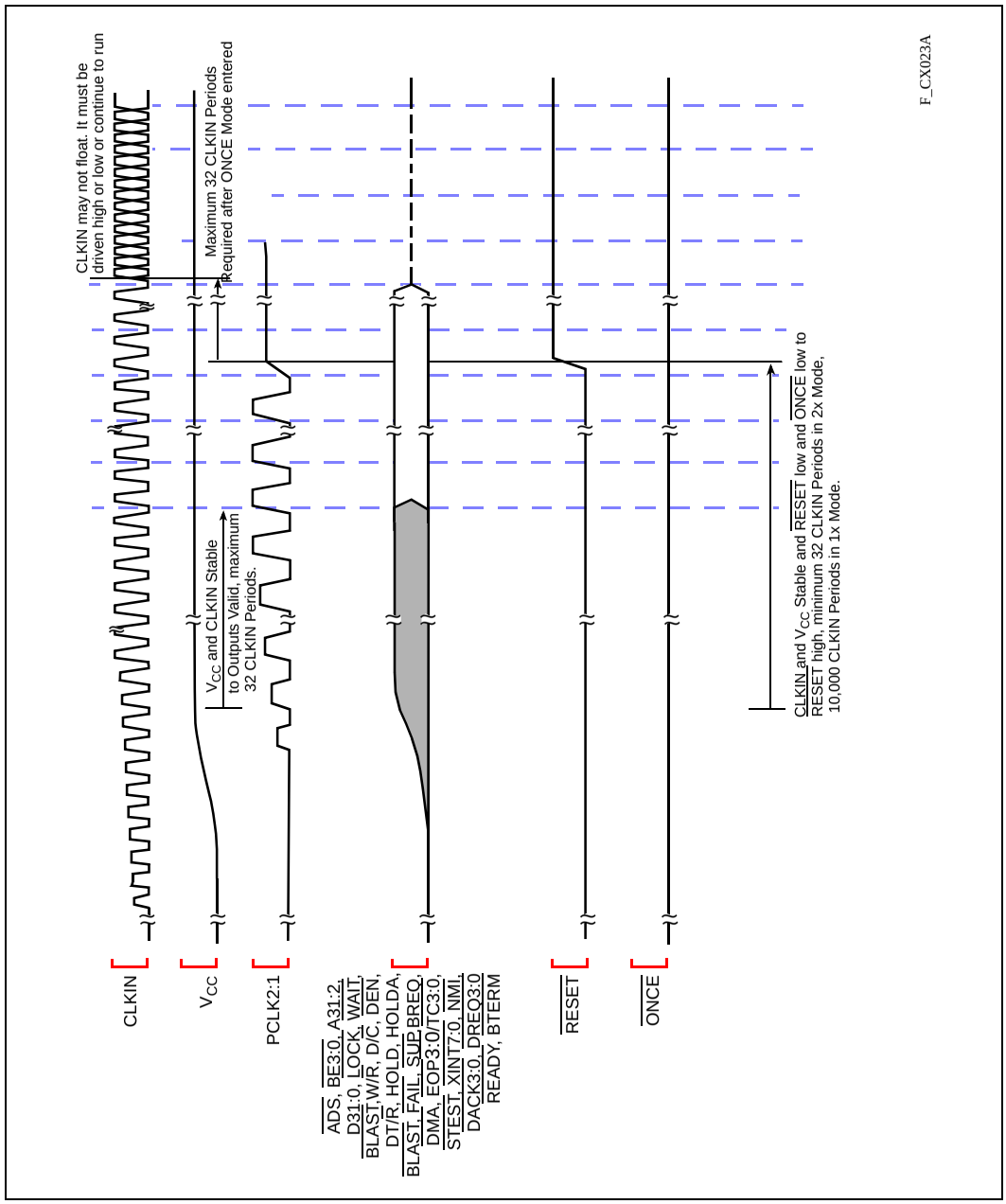
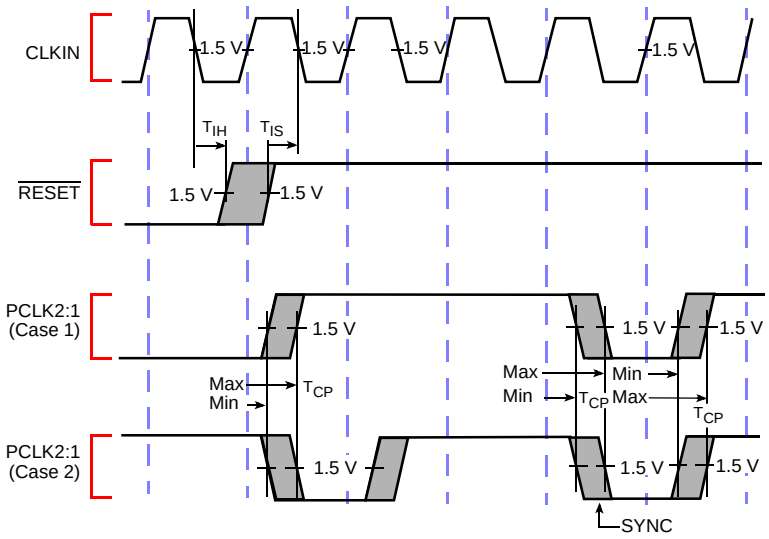


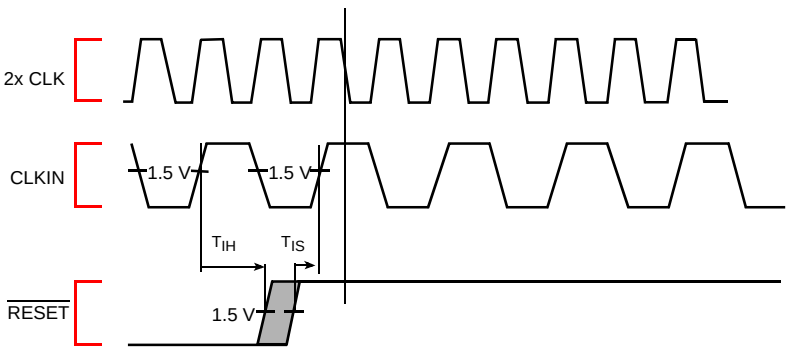
Figure 23. Clock Synchronization in the 2-x Clock Mode



Note: Case 1 and Case 2 show two possible polarities of PCLK2:1

F_CX024A

Figure 24. Clock Synchronization in the 1-x Clock Mode



Note: In 1x clock mode, the $\overline{\text{RESET}}$ pin is actually sampled on the falling edge of 2xCLK. 2xCLK is an internal signal generated by the PLL and is not available on an external pin. Therefore, $\overline{\text{RESET}}$ is specified relative to the rising edge of CLKIN. The $\overline{\text{RESET}}$ pin is sampled when PCLK is high.

F_CX025A

Figure 25. Non-Burst, Non-Pipelined Requests Without Wait States

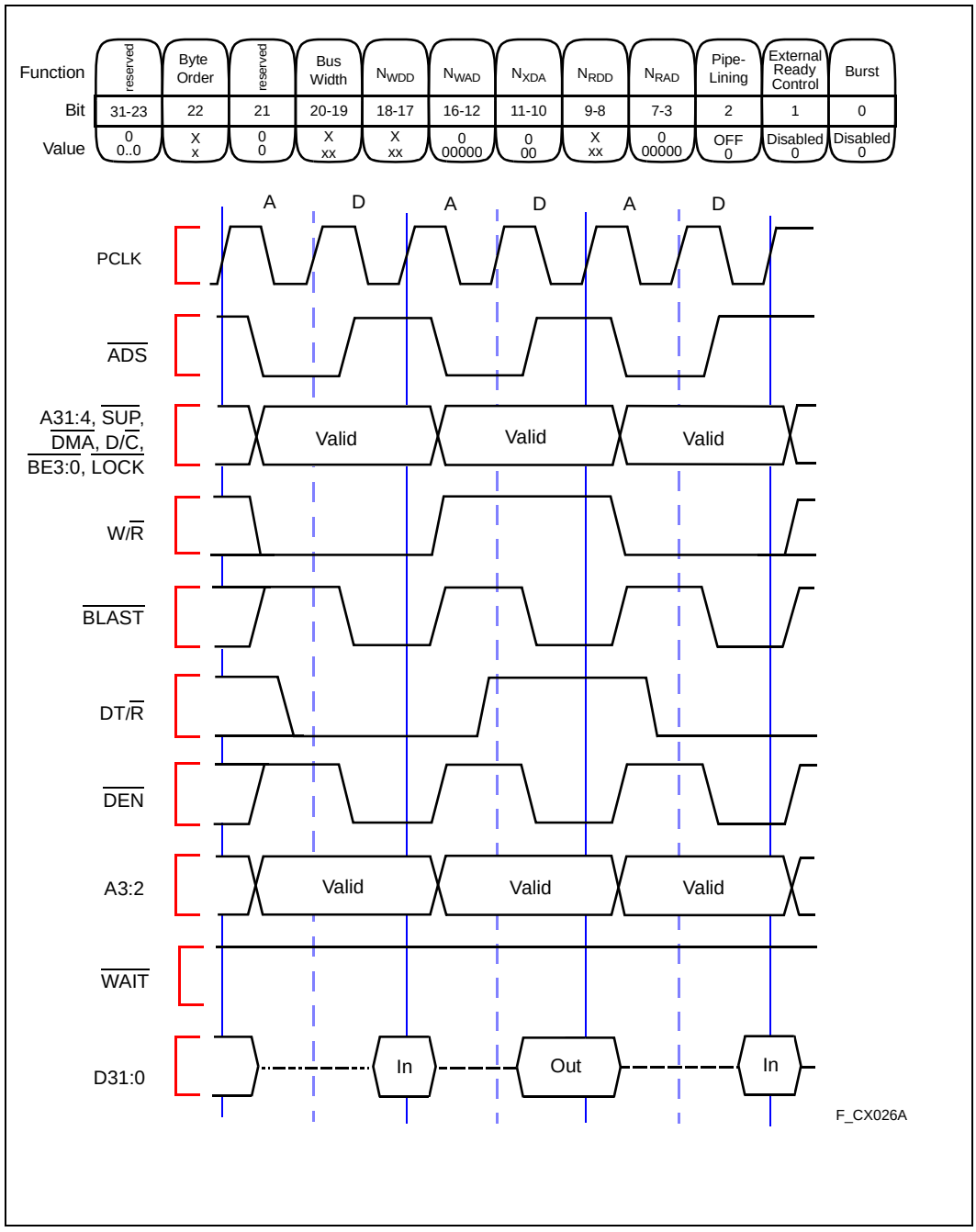


Figure 26. Non-Burst, Non-Pipelined Read Request With Wait States

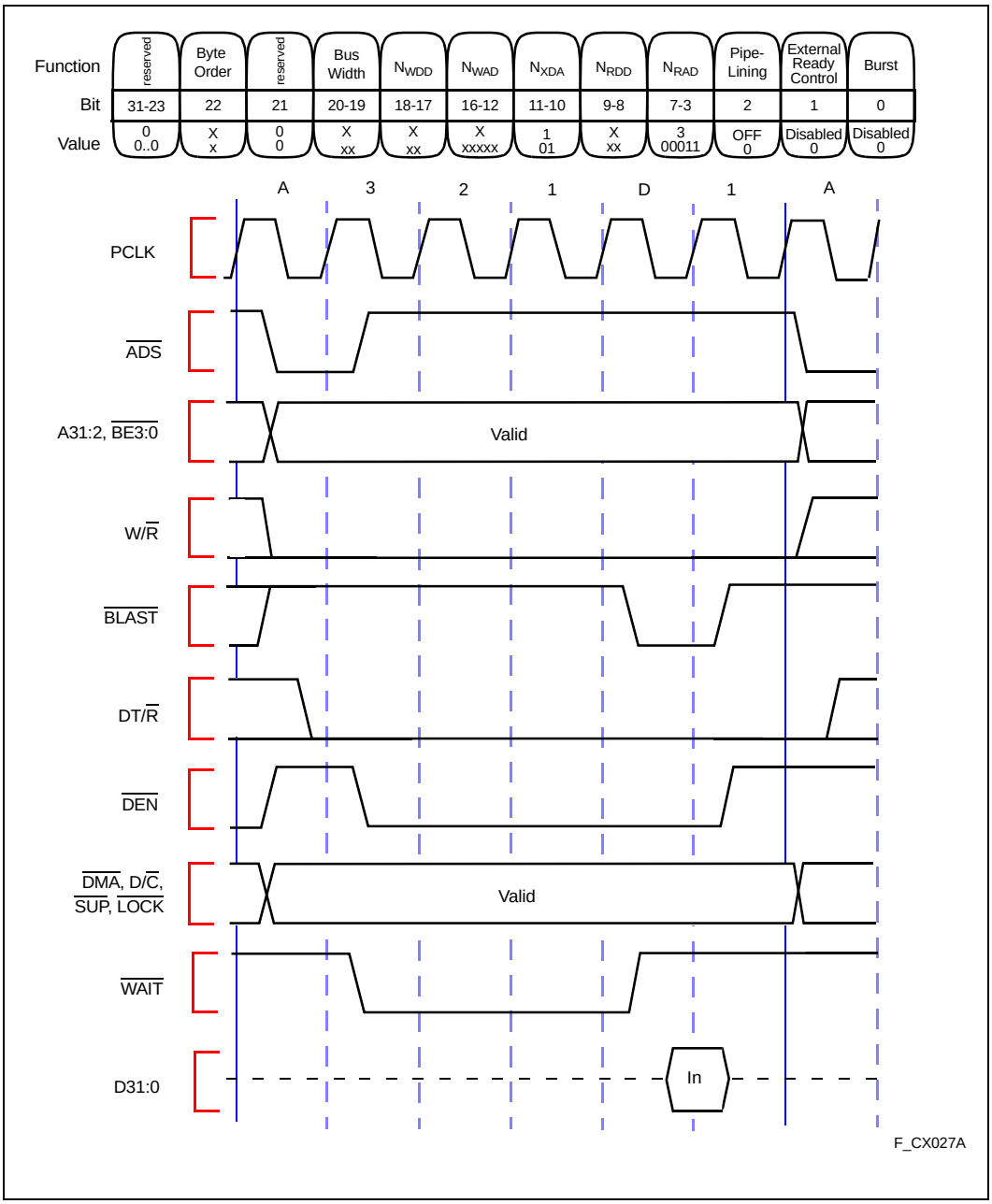


Figure 27. Non-Burst, Non-Pipelined Write Request With Wait States

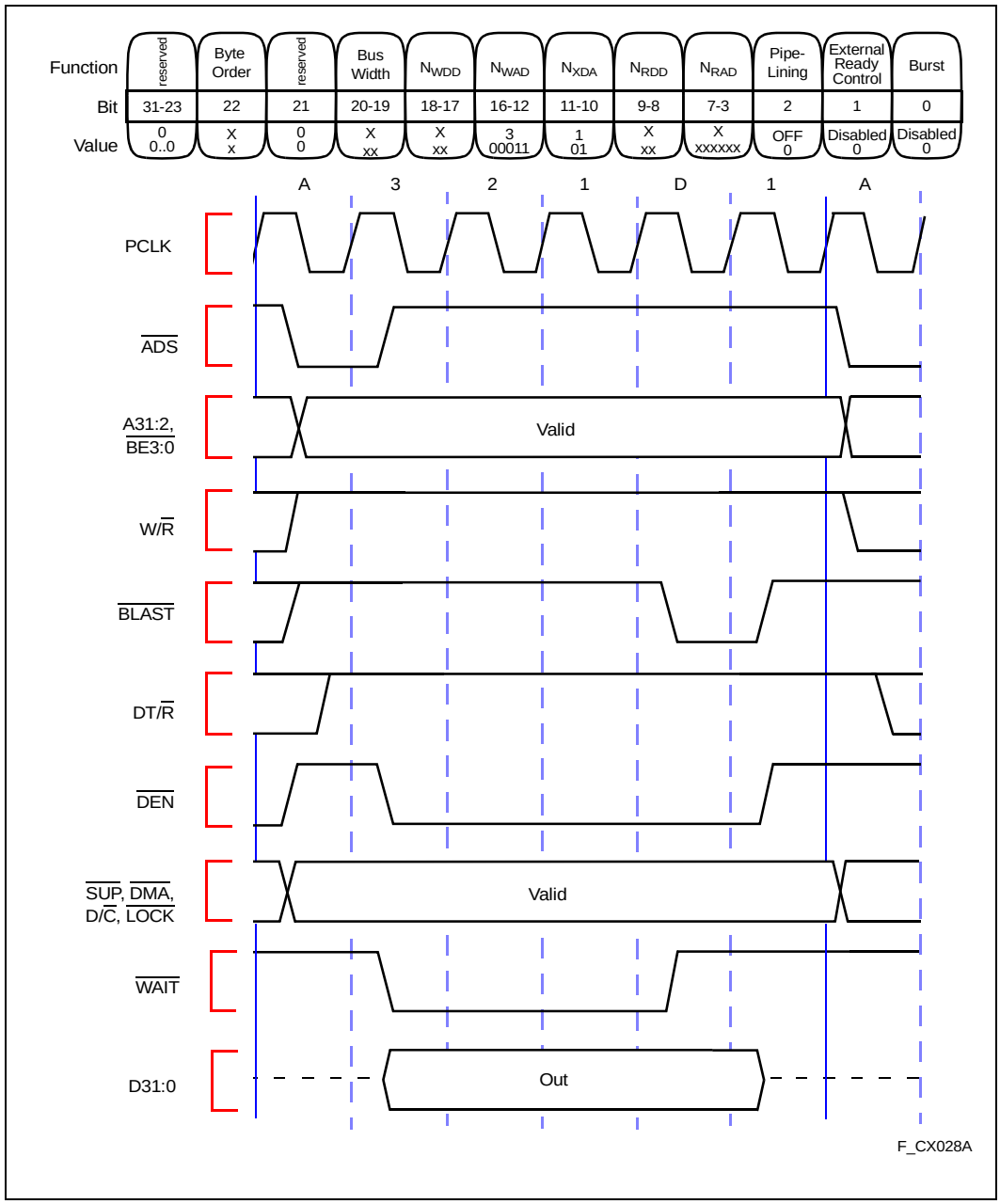


Figure 28. Burst, Non-Pipelined Read Request Without Wait States, 32-Bit Bus

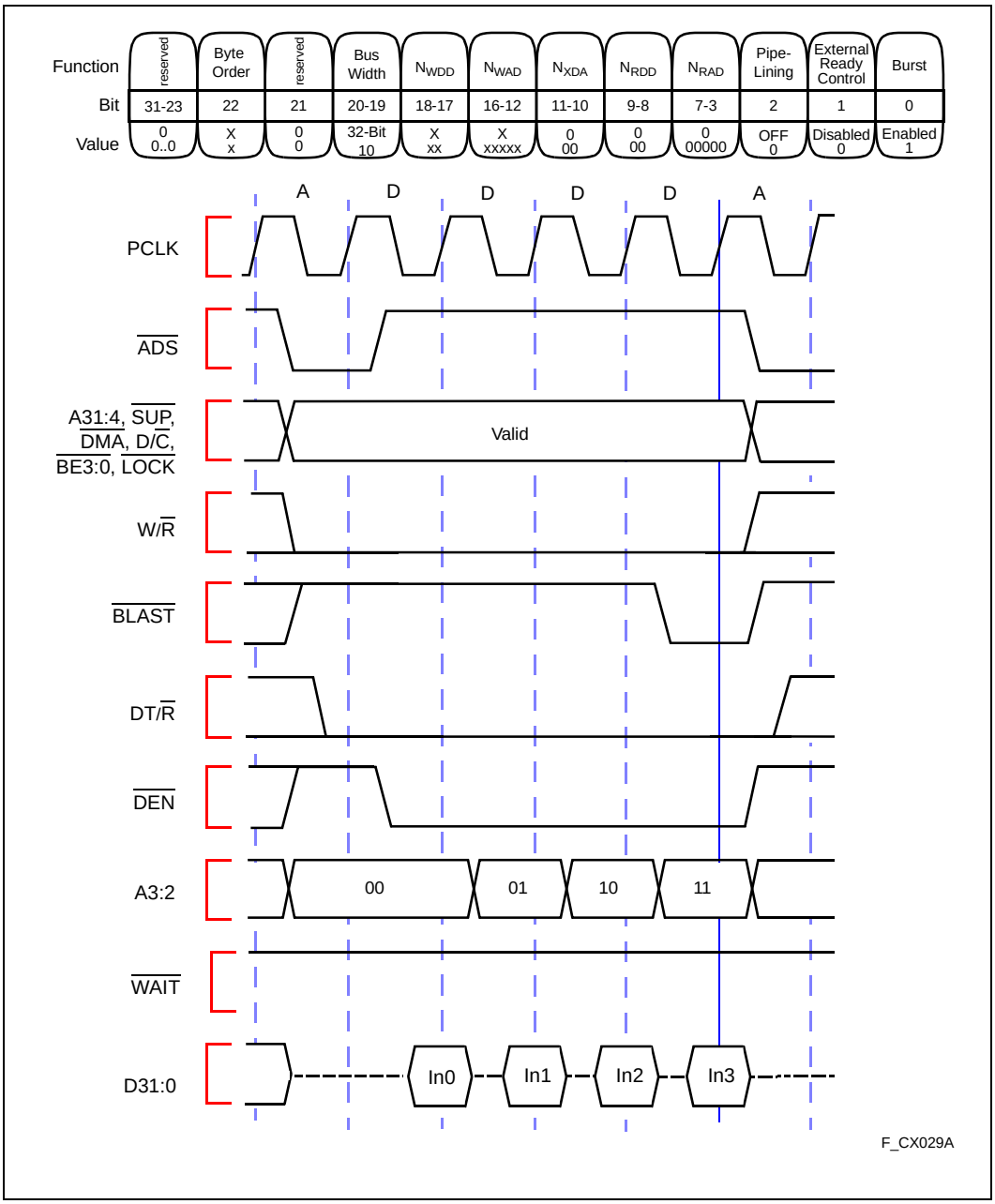


Figure 29. Burst, Non-Pipelined Read Request With Wait States, 32-Bit Bus

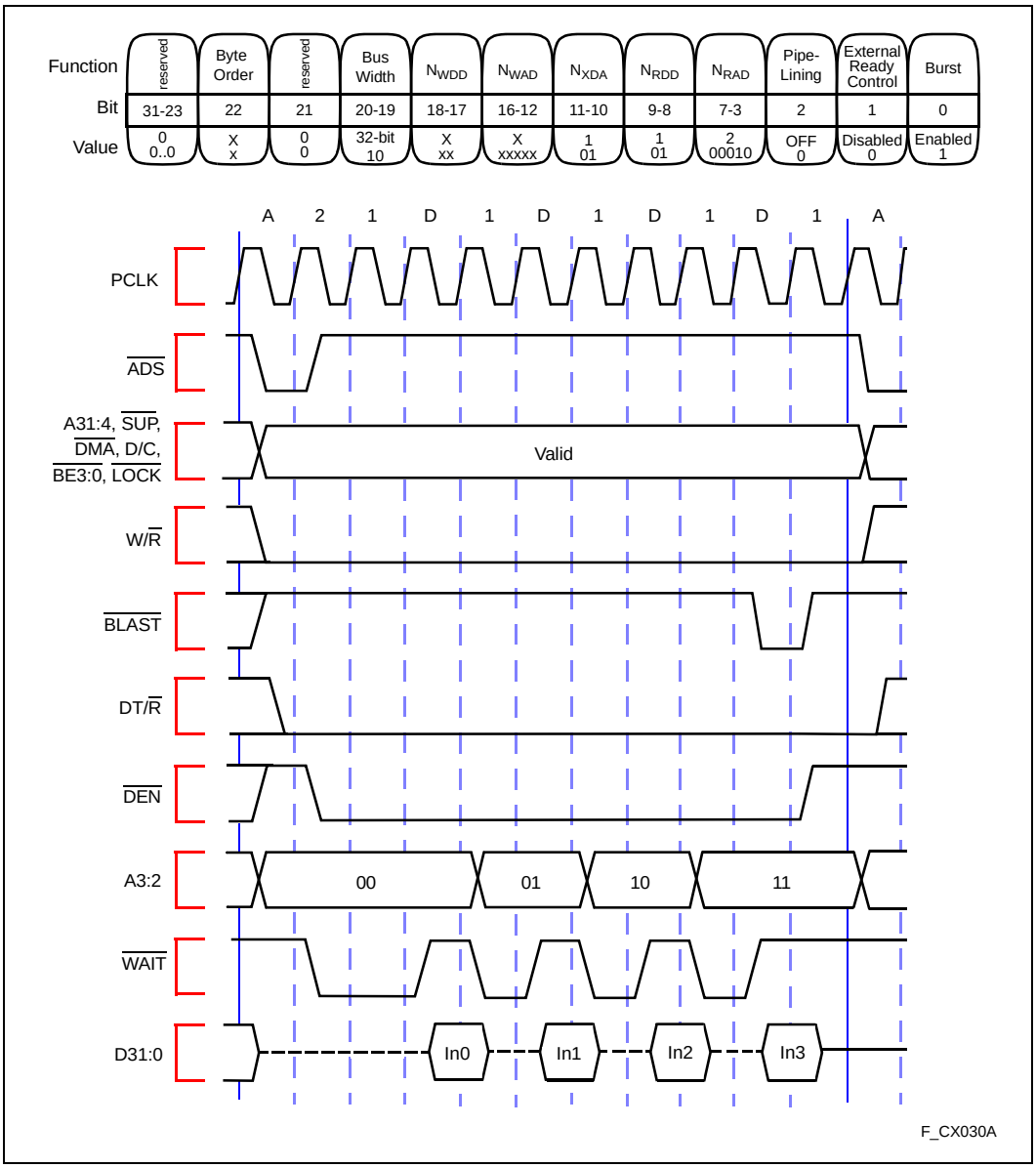


Figure 30. Burst, Non-Pipelined Write Request Without Wait States, 32-Bit Bus

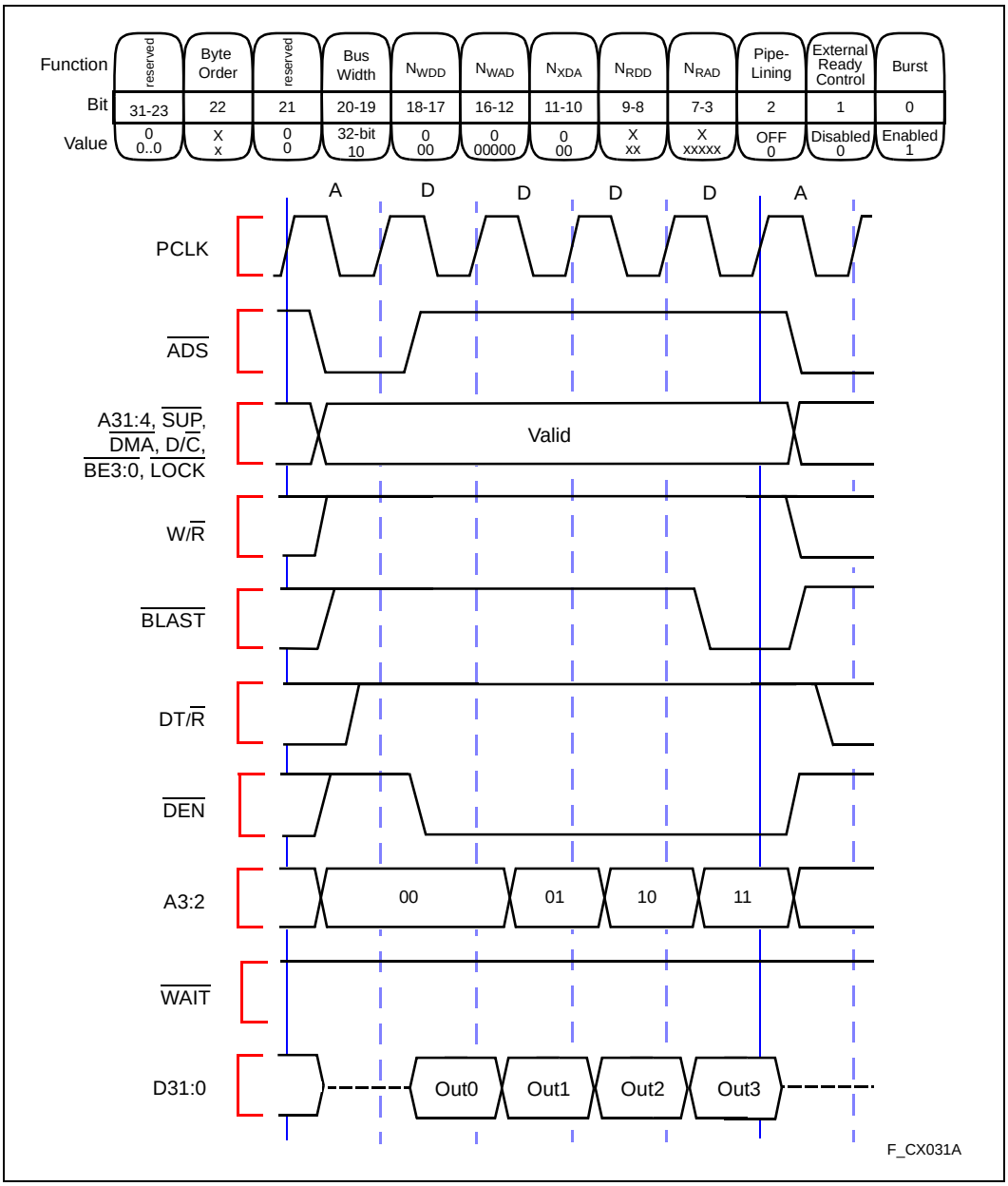


Figure 31. Burst, Non-Pipelined Write Request With Wait States, 32-Bit Bus

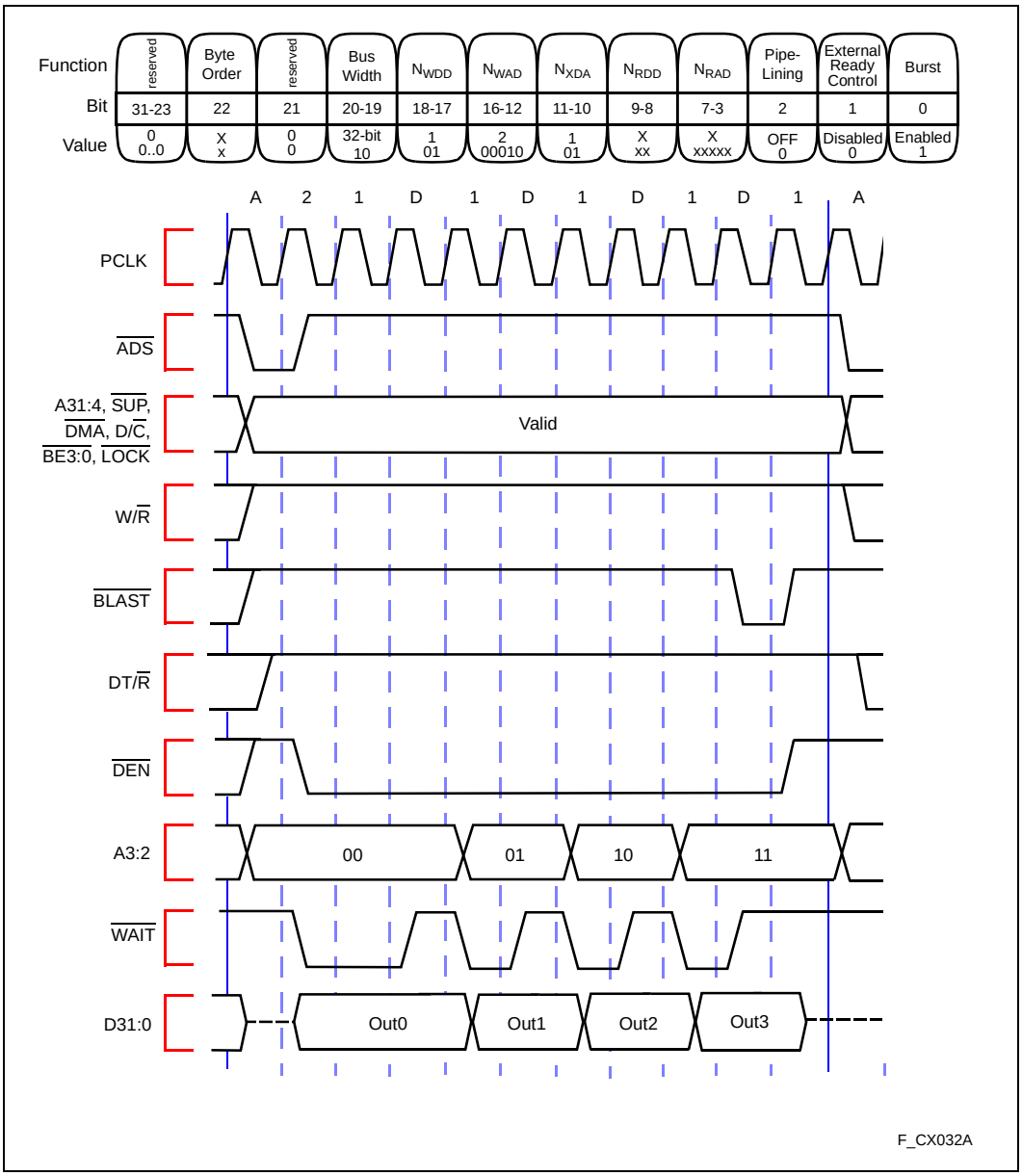


Figure 32. Burst, Non-Pipelined Read Request With Wait States, 16-Bit Bus

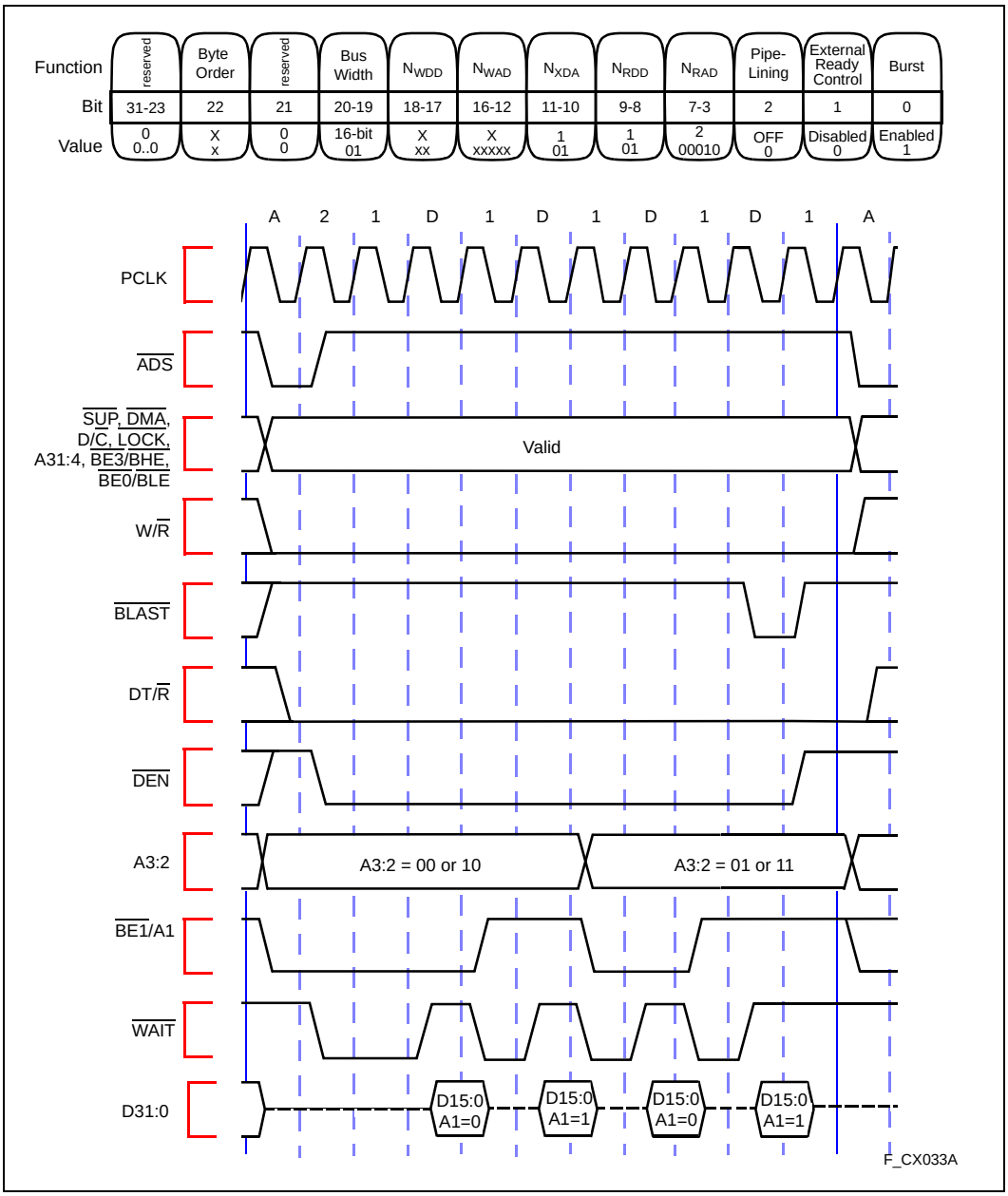


Figure 33. Burst, Non-Pipelined Read Request With Wait States, 8-Bit Bus

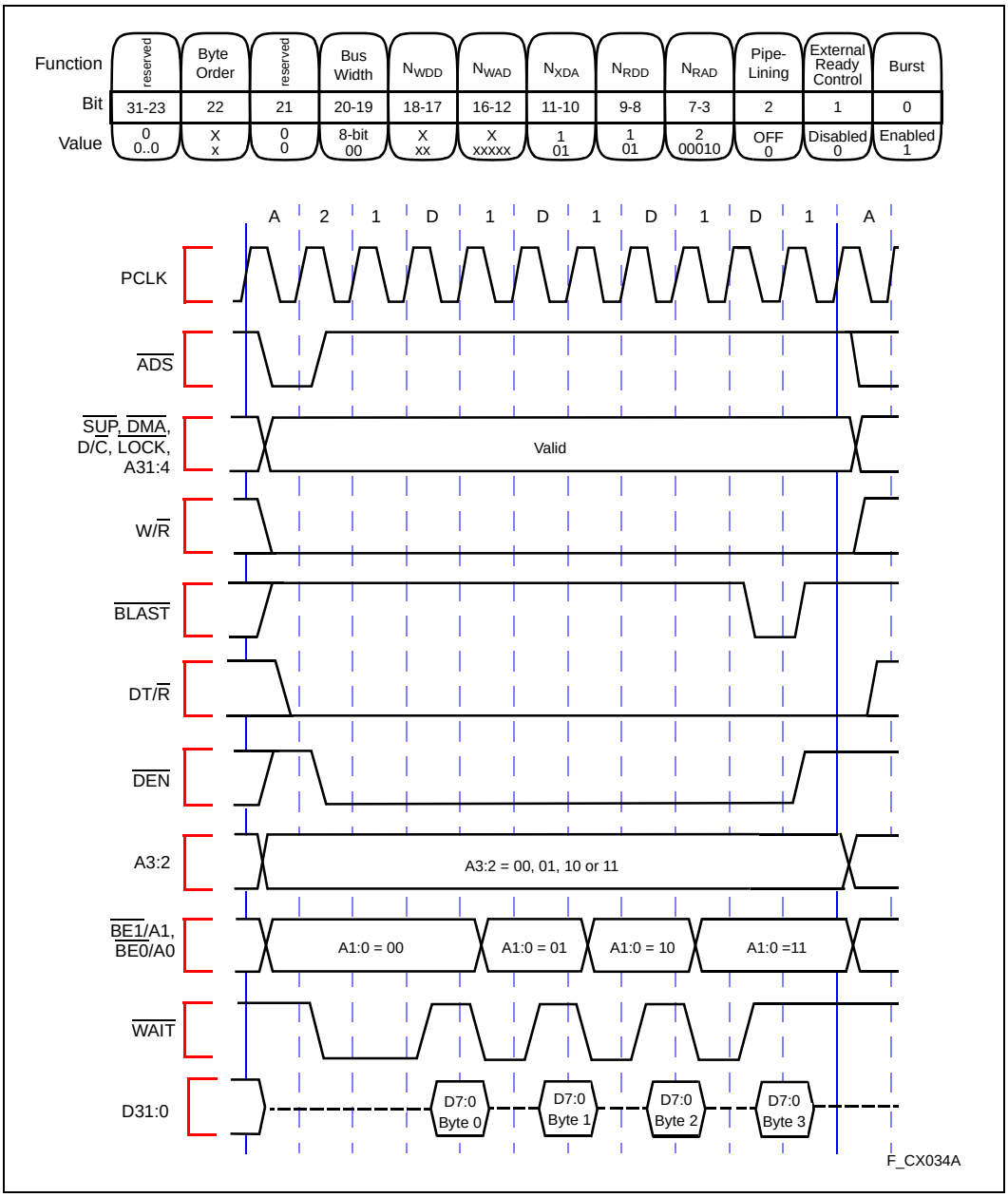


Figure 34. Non-Burst, Pipelined Read Request Without Wait States, 32-Bit Bus

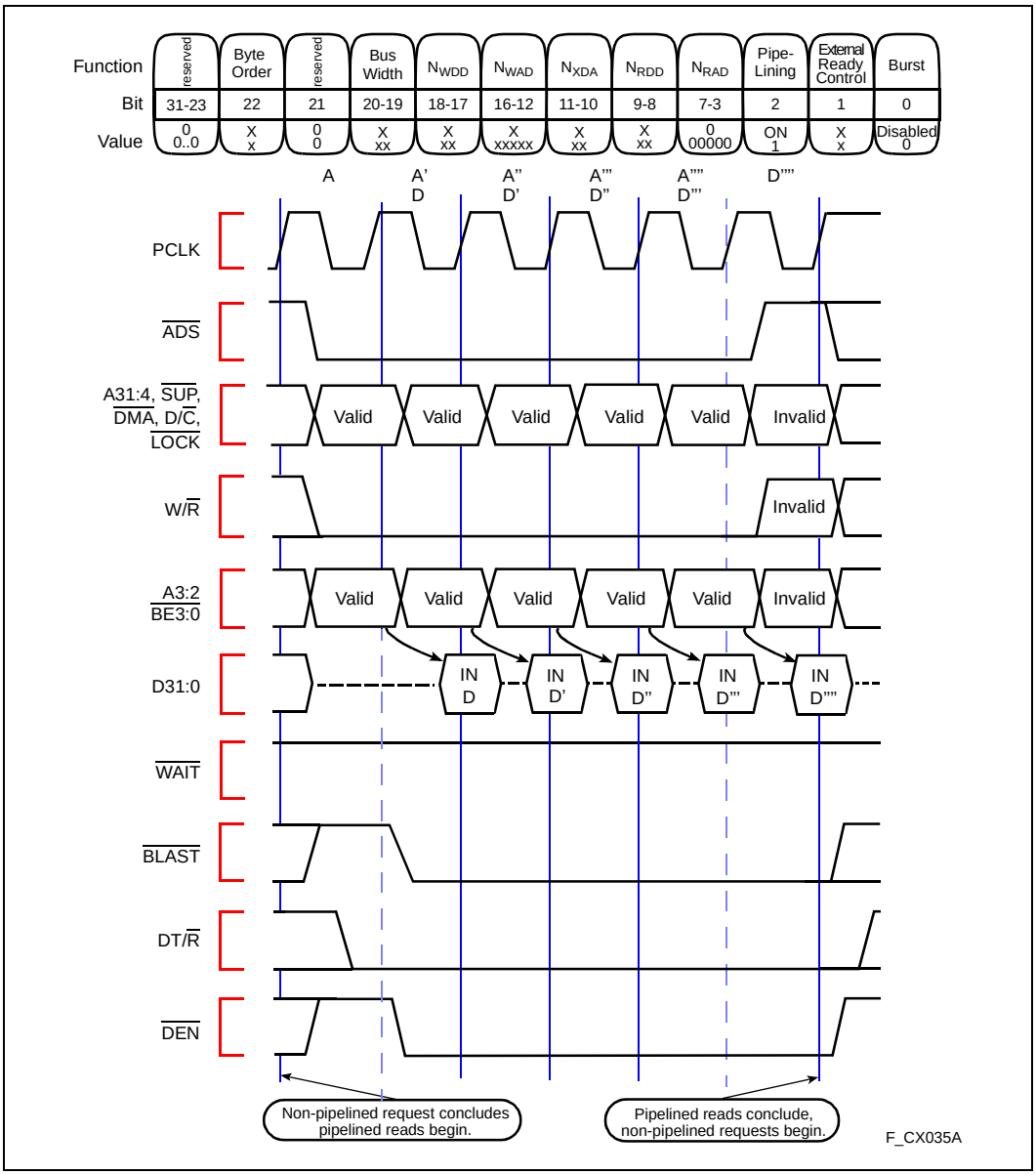


Figure 35. Non-Burst, Pipelined Read Request With Wait States, 32-Bit Bus

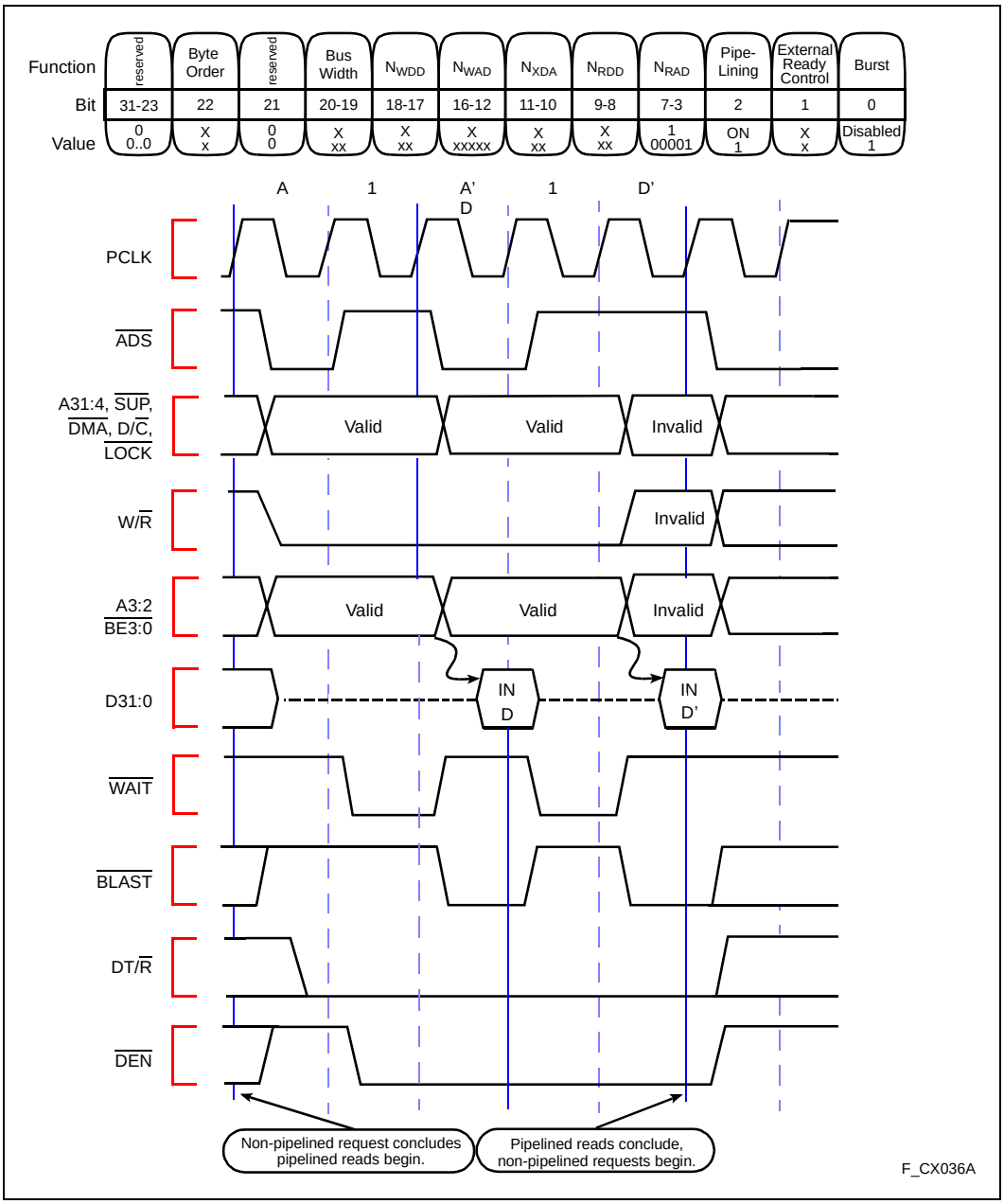


Figure 36. Burst, Pipelined Read Request Without Wait States, 32-Bit Bus

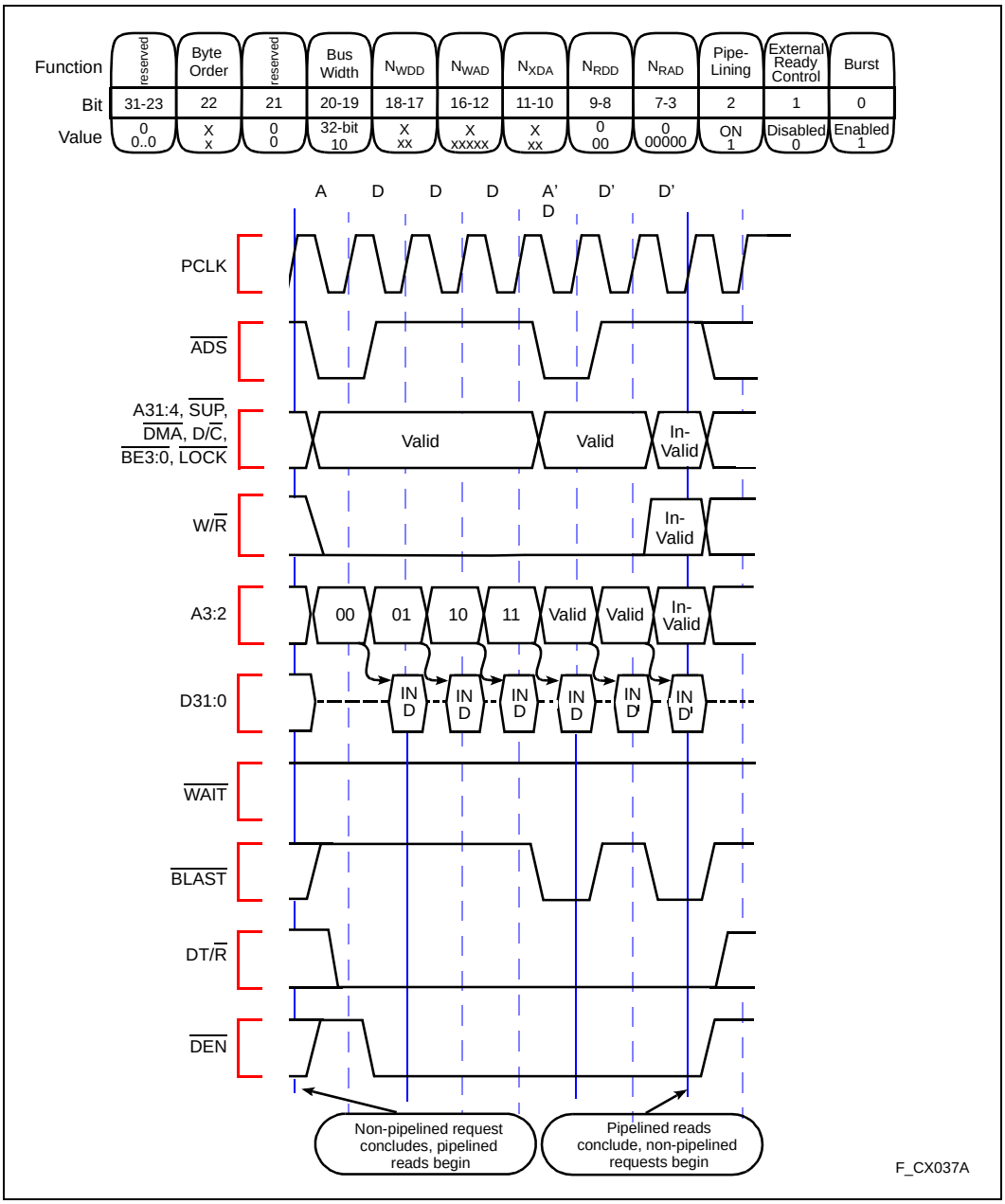


Figure 37. Burst, Pipelined Read Request With Wait States, 32-Bit Bus

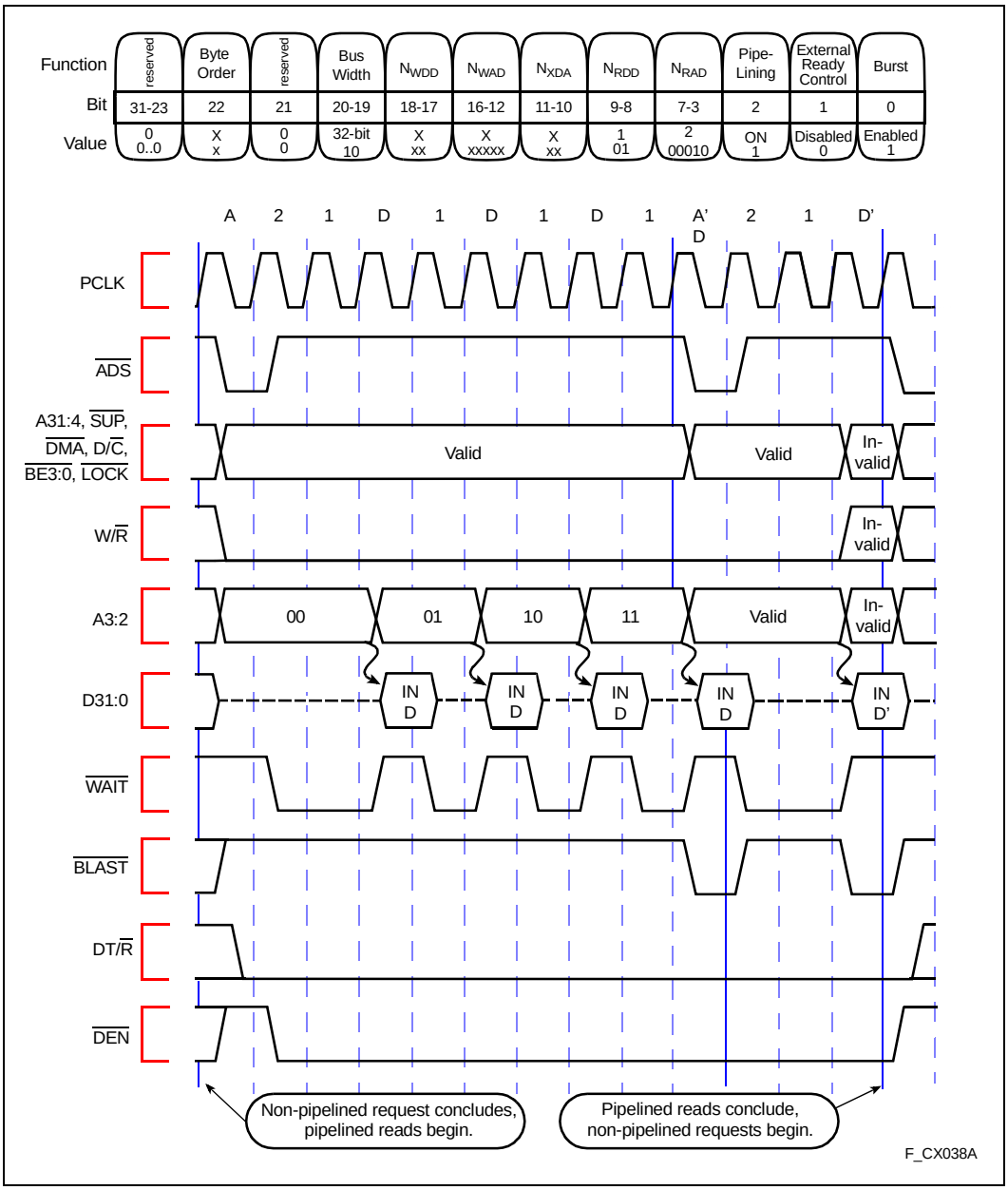


Figure 38. Burst, Pipelined Read Request With Wait States, 16-Bit Bus

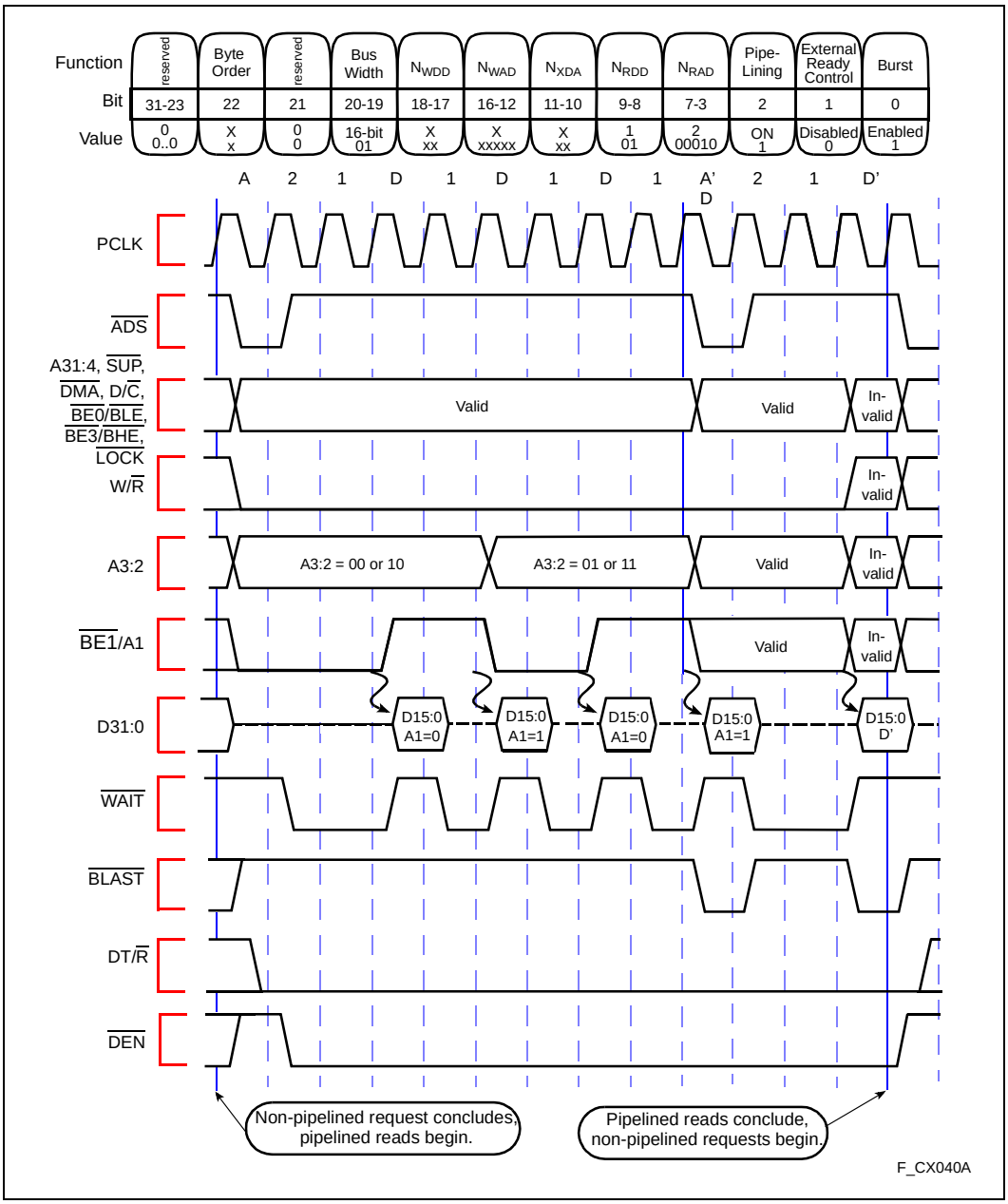


Figure 39. Burst, Pipelined Read Request With Wait States, 8-Bit Bus

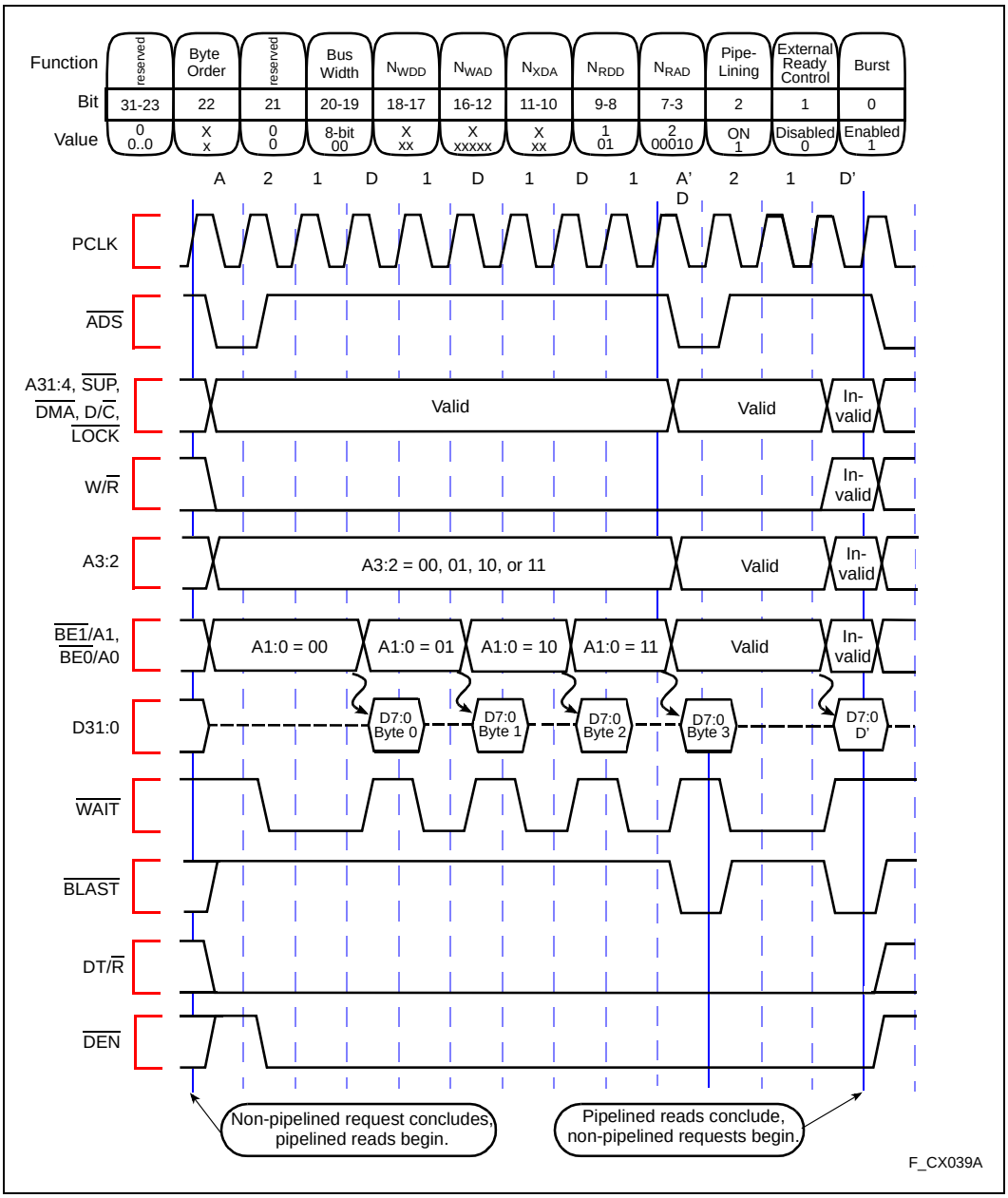


Figure 40. Using External $\overline{\text{READY}}$

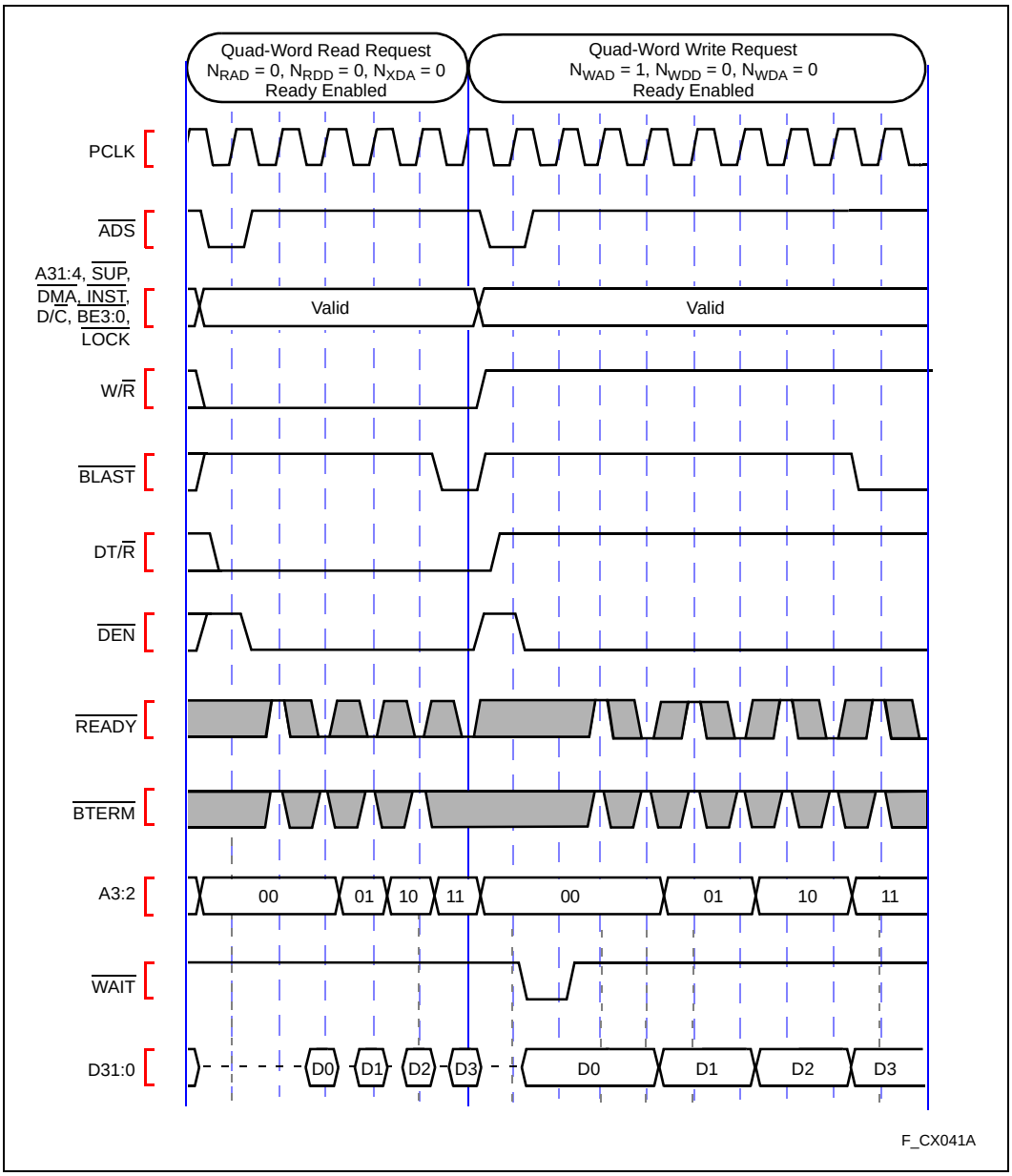
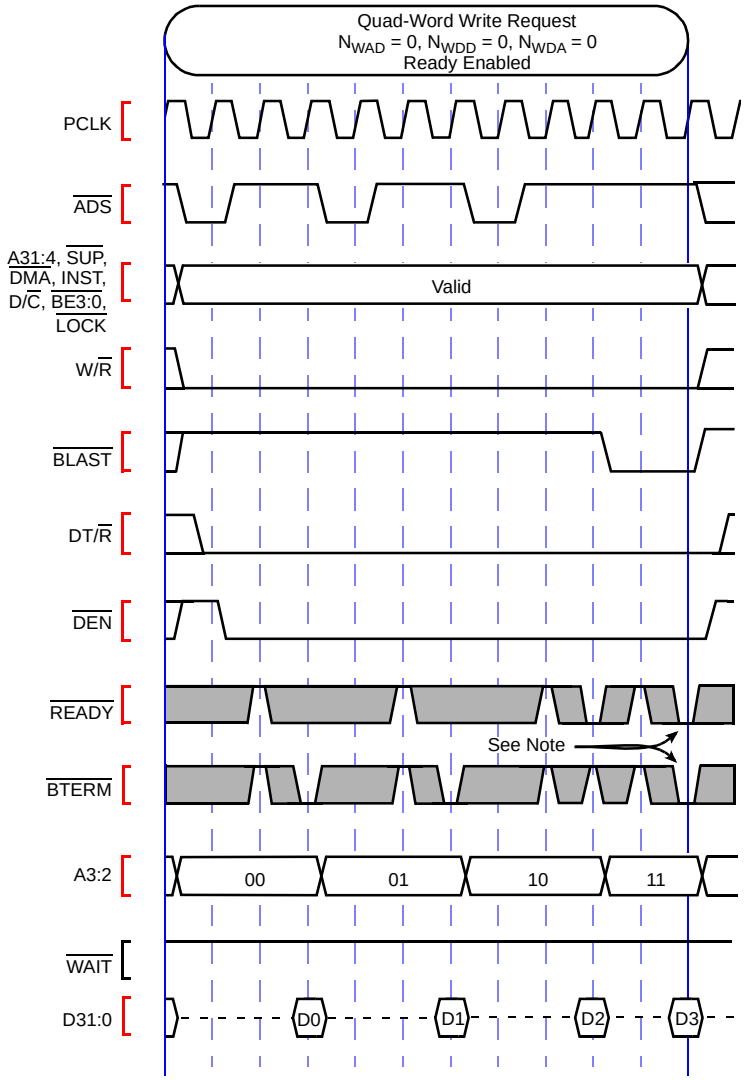


Figure 41. Terminating a Burst with BTERM



Note: READY adds memory access time to data transfers, whether or not the bus access is a burst access. BTERM interrupts a bus access, whether or not the bus access has more data transfers pending. Either the READY signal or the BTERM signal may terminate a bus access when the signal is asserted during the last (or only) data transfer of the bus access.

F_CX042A

Figure 42. $\overline{\text{BOFF}}$ Functional Timing

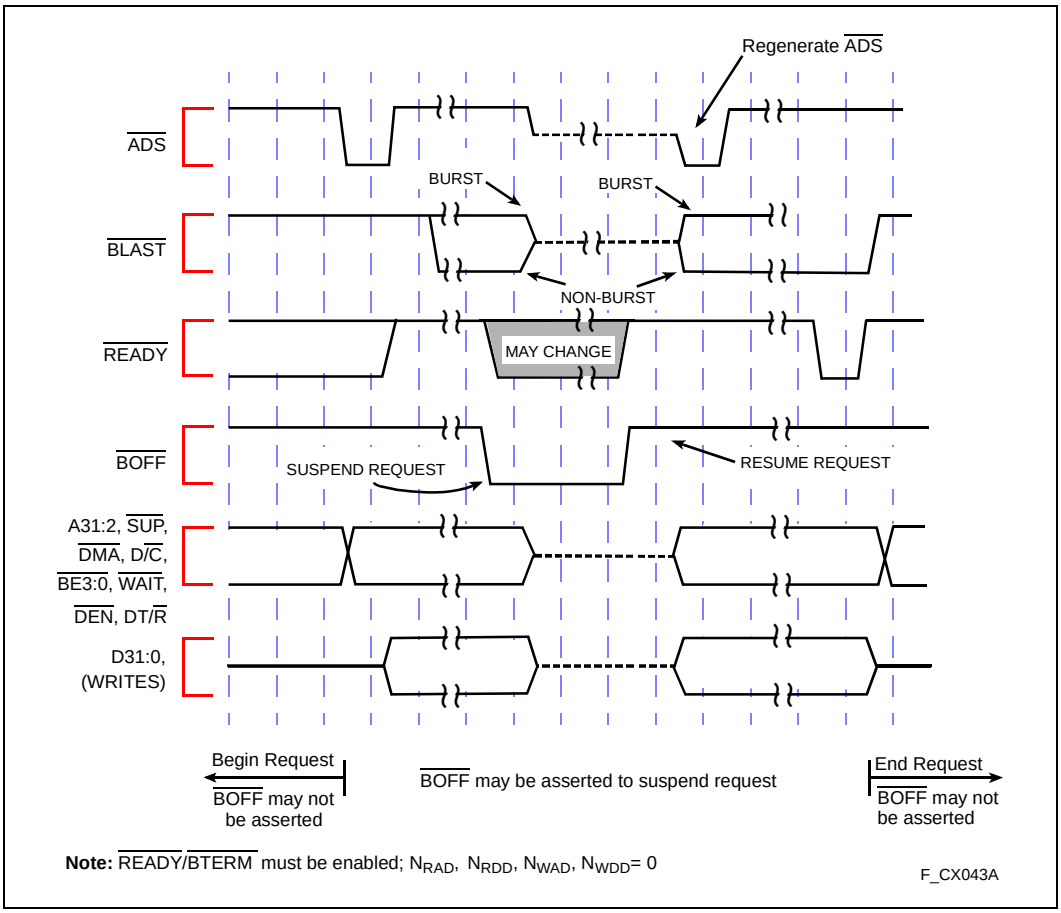


Figure 43. HOLD Functional Timing

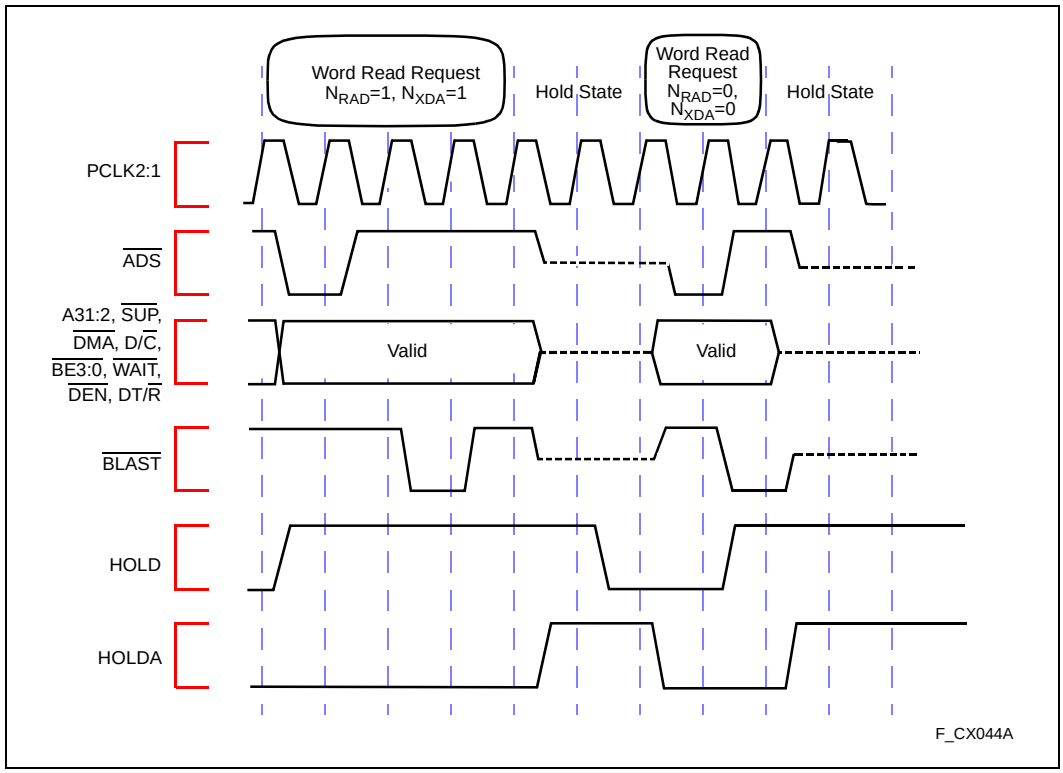
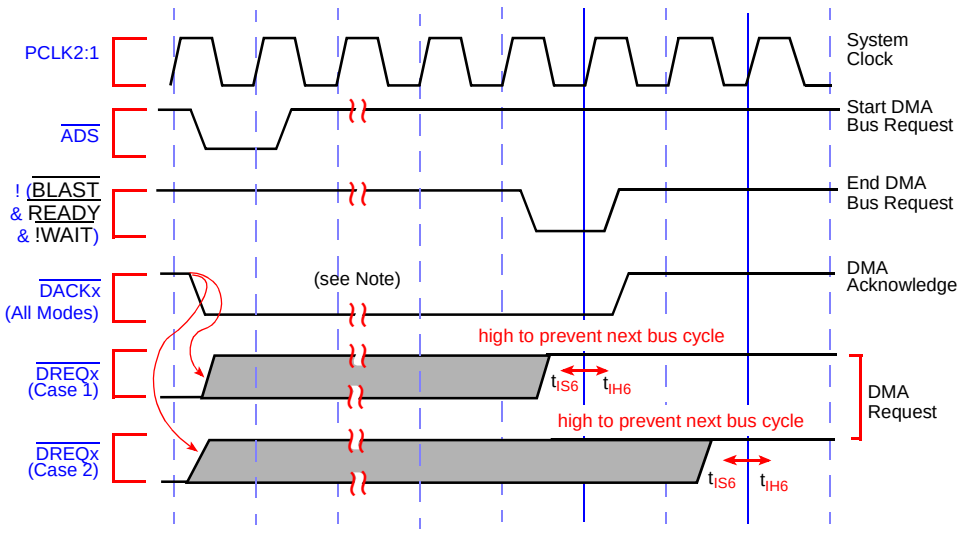


Figure 44. DREQ and DACK Functional Timing

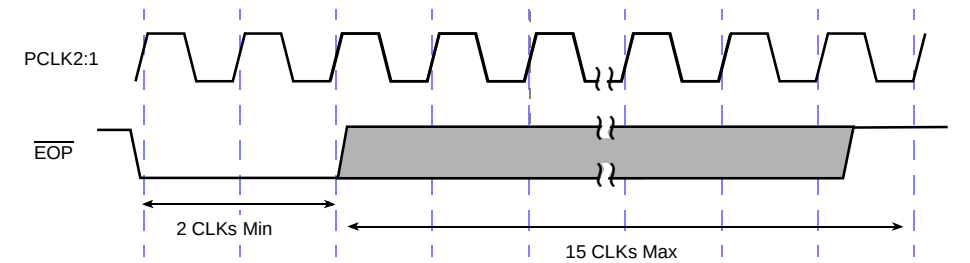


Note:

1. Case 1: DREQ must deassert before DACK deasserts. This applies to all Fly-By modes: source synchronized packing modes and destination synchronized unpacking modes.
2. Case 2: DREQ must be deasserted by the second clock (rising edge) after DACK is driven high. This applies to all other DMA transfers.
3. DACKx is asserted for the duration of a DMA bus request. The request may consist of multiple bus accesses (defined by ADS and BLAST).

F_CX018A

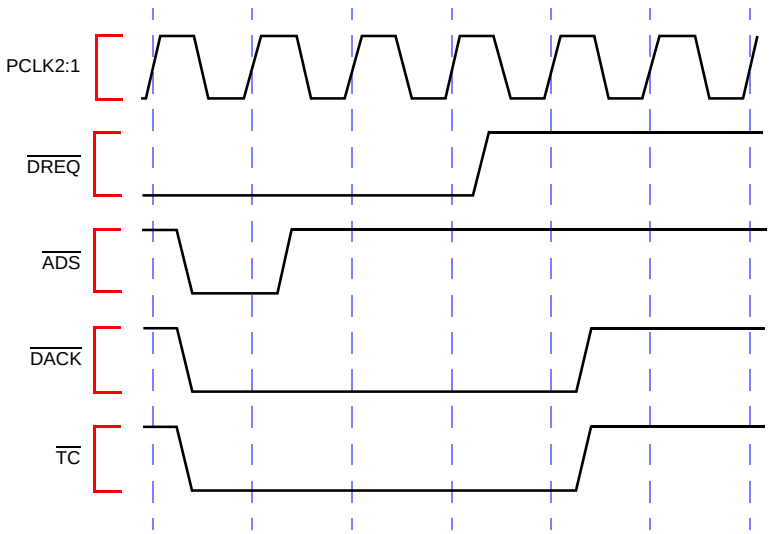
Figure 45. EOP Functional Timing



Note: EOP has the same AC Timing Requirements as DREQ to prevent unwanted DMA requests. EOP is NOT edge triggered. EOP must be held for a minimum of 2 clock cycles then deasserted within 15 clock cycles.

F_CX045A

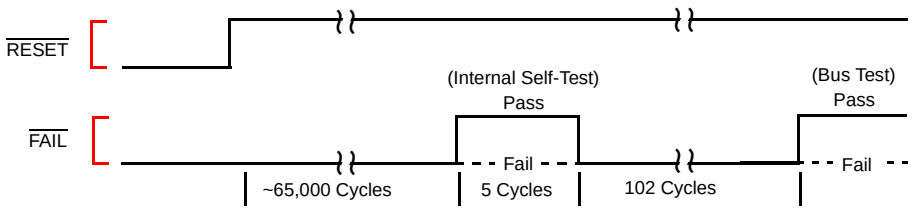
Figure 46. Terminal Count Functional Timing



Note: Terminal Count becomes active during the last bus request of a buffer transfer. When the last LOAD/STORE bus request is executed as multiple bus accesses, the TC may be active for the entire bus request. Refer to the *i960® Cx Microprocessor User's Manual* for further information.

F_CX046A

Figure 47. FAIL Functional Timing



F_CX047A

Figure 48. A Summary of Aligned and Unaligned Transfers for Little Endian Regions

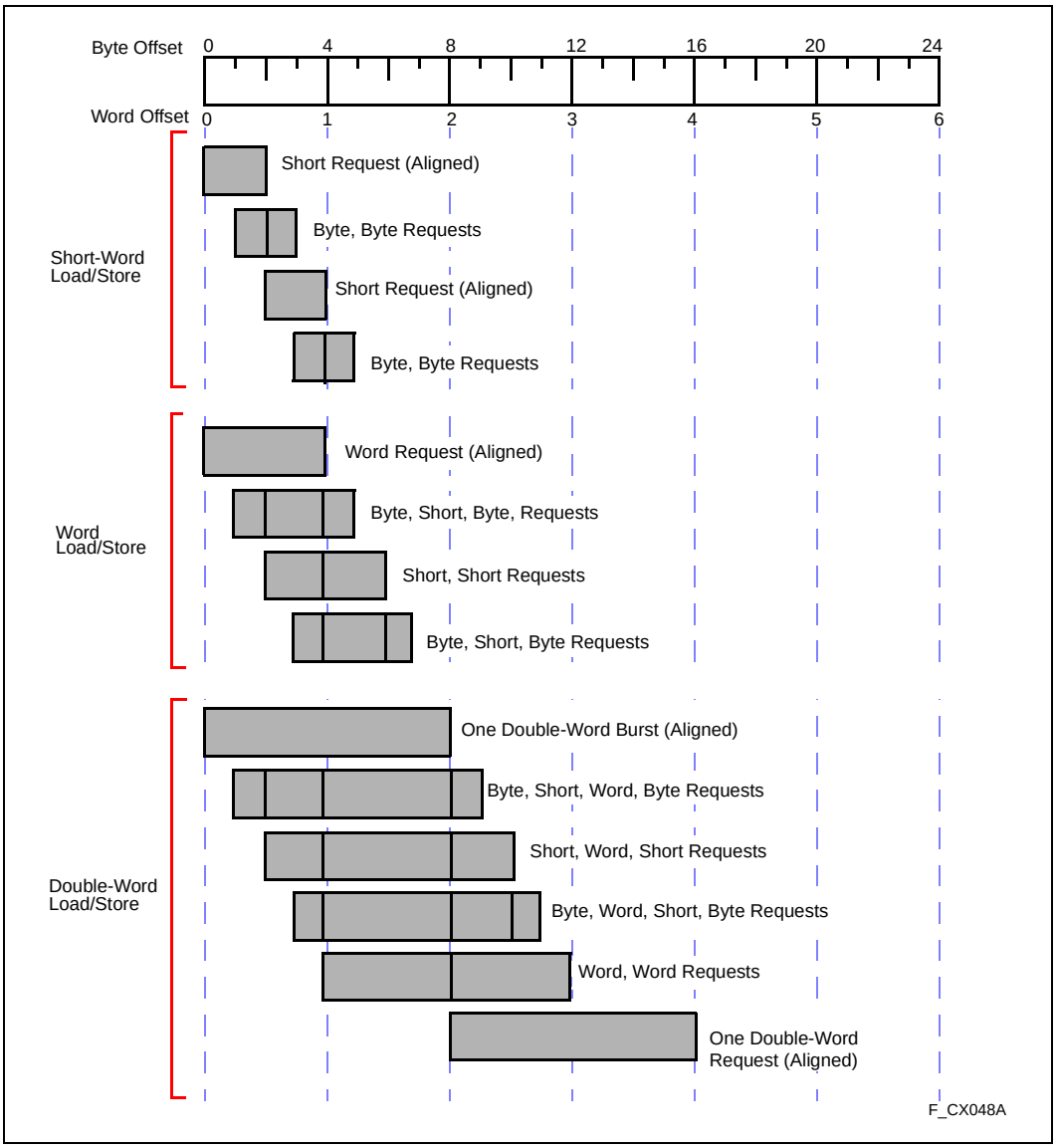


Figure 49. A Summary of Aligned and Unaligned Transfers for Little Endian Regions

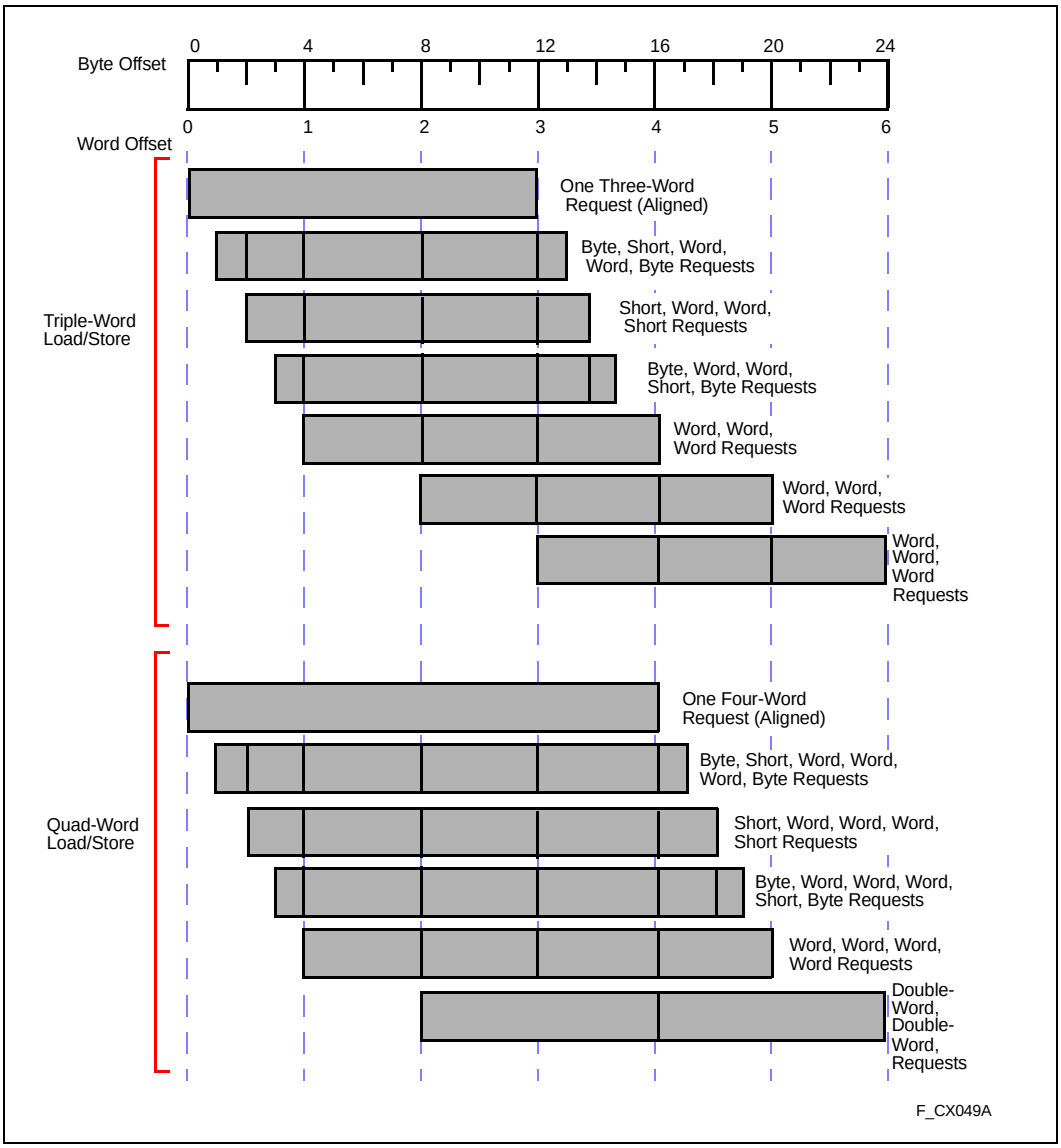
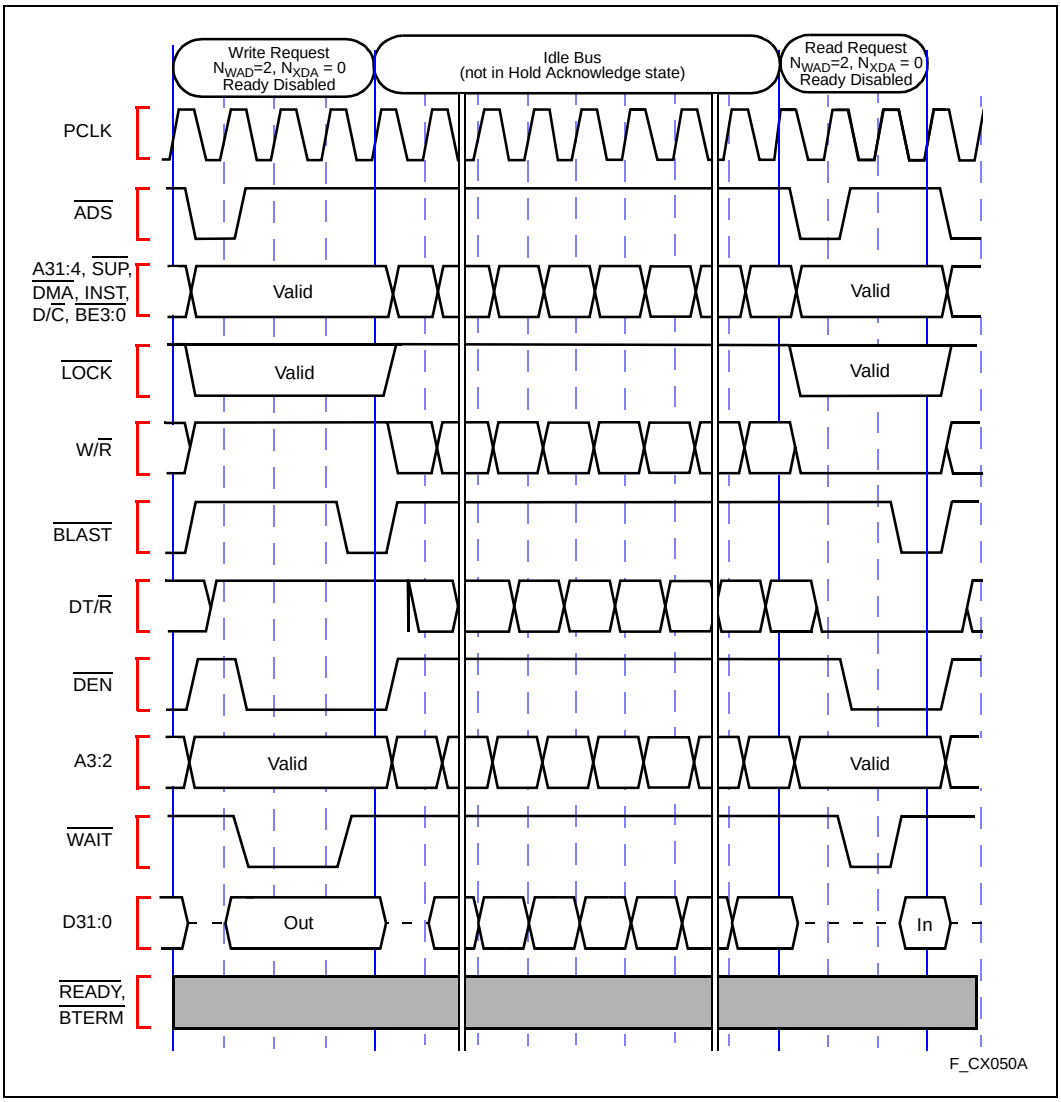


Figure 50. Idle Bus Operation



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