Atmel ATA6628/ATA6630 Development Board V1.1

1. Introduction

The development board for the Atmel® ATA6628/ATA6630 is designed to give users a quick start using these ICs and prototyping and testing new LIN designs.

The Atmel ATA6628 and Atmel ATA6630 are system basis chips (SBCs) with a fully integrated LIN transceiver in compliance with the LIN specification 2.0, 2.1 and SAEJ2602-2. The SBCs each have a window watchdog with adjustable trigger time and a 3.3V/85mA respectively 5V/85mA low drop voltage regulator. The output current of the regulator can be boosted by using an external NPN transistor. In addition, the Atmel ATA6628/ATA6630 has an integrated voltage divider that makes it possible to measure the battery voltage precisely.

The ATA6628 and the ATA6630 are nearly identical, the only difference between these circuits is the regulator's output voltage.

The combination of the features included in the Atmel ATA6628/ATA6630 makes it possible to develop simple though powerful and cheap slave and master nodes for LIN bus systems.

The ICs are designed to handle low-speed data communication in vehicles such as that found in convenience electronics. Improved slope control at the LIN driver ensures secure data communication of up to 20kBaud.

Sleep mode and silent mode guarantee very low current consumption even in the case of a floating bus or a short circuit between the bus line and GND.

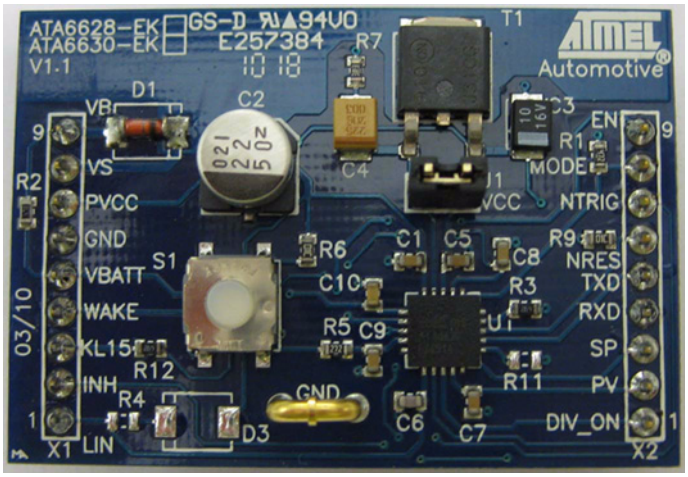
This document has been created as a quick start guide on using the Atmel ATA6628/ATA6630 development board. For more detailed information about the use of these devices, please refer to the corresponding datasheet.

Atmel ATA6628/ Atmel ATA6630 Development Board V1.1

Application Note

9202B–AUTO–03/11

Figure 1-1. ATA6628/ATA6630 Development Board V1.1



1.1 Development Board Features

The development board for the Atmel® ATA6628/ATA6630 has the following features:

- **All Components for Putting the Atmel ATA6628/ATA6630 in Operation Included**
- **Placeholders for some Optional Components for Extended Functions Included**
- **Easy Accessibility of All Pins**
- **Easily Adaptable Watchdog Times by Replacing a Resistor**
- **Possibility to Boost Up the Output Current of the Voltage Regulator Using the Onboard NPN Transistor T1 by Removing the Jumper J1**
- **Option between Master or Slave Operation (Mounting D3 and R4)**

1.2 Quick Start

The development board for the Atmel ATA6628/ATA6630 is shipped with all necessary components and a default jumper setting to immediately start the development of a LIN slave node.

Connecting an external 12V DC power supply between the terminals VB and GND, puts the circuit in fail-safe mode and a voltage of 5V (3.3V) DC supplied by the internal voltage regulator can be measured between VCC and GND.

In addition, the following voltage states can be measured at the pins WD_OSC, INH, RXD and LIN as given in Table 1-1 and Table 1-2.

Table 1-1. Atmel® ATA6630

	PVCC	WD_OSC	INH	RXD	LIN	Transceiver
Fail-safe mode	5V	1.23V	On	Low	recessive	Off
Normal mode	5V	1.23V	On	LIN depending	TXD depending	On

Table 1-2. Atmel ATA6628

	PVCC	WD_OSC	INH	RXD	LIN	Transceiver
Fail-safe mode	3.3V	1.23V	On	Low	recessive	Off
Normal mode	3.3V	1.23V	On	LIN depending	TXD depending	On

Because the window watchdog of the Atmel ATA6628/ATA6630 is already active in fail-safe mode, a periodic reset signal is generated at the NRES pin as long as no trigger signal can be received at the watchdog trigger input NTRIG. Normally the connected microcontroller is monitored with the watchdog, so it has to generate the required trigger signal described in Section 2.3 “The Window Watchdog (NTRIG and NRES)” on page 7 and in more detail in the datasheet of the Atmel ATA6628/ATA6630. For the quick start it is sufficient to generate a square-wave signal with $V_{PP} = V_{CC}$ and f = 50Hz at the NTRIG pin (this is only recommended for testing purposes). In order to check that the watchdog is triggered in the expected way, the NRES reset pin can be monitored until a continuous high level is available.

Please note that the communication is still inactive during fail-safe mode.

In order to communicate via the LIN bus interface you have to switch to normal mode by applying the VCC voltage (5V or 3.3V respectively) to the EN pin.

2. Hardware Description

The following sections contain a brief description of normal operating conditions. Please refer to the respective datasheet for more information about any of the features mentioned.

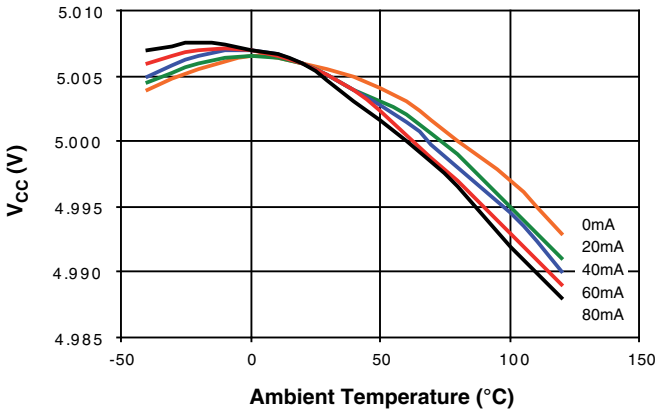
2.1 Power Supply (VB and GND)

In order to get the development board running, an external 5.7V - 27V DC power supply is required between the terminals VB and GND. The input circuit is protected against inverse polarity with the D1 protection diode, resulting in a difference between the VB and VS level of approximately 0.7V.

2.2 Voltage Regulator (PVCC and VCC)

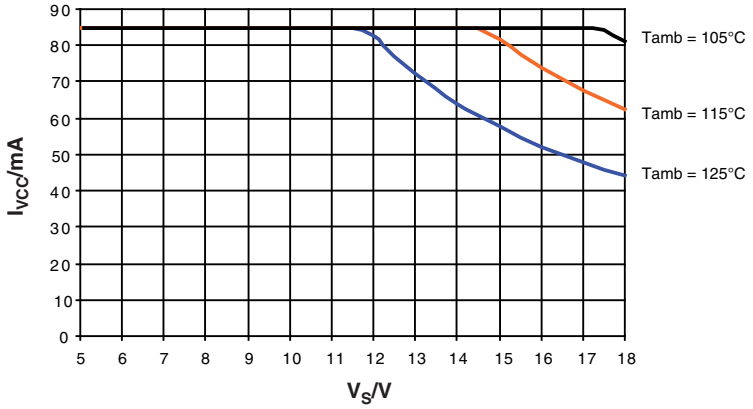
The internal 5V or 3.3V low drop voltage regulator is capable of driving loads up to 50mA over a wide range of supply voltage and ambient temperature with an accuracy of ±2%, so the SBC is able to supply a microcontroller, sensors and/or other ICs. In regular operation the PVCC and VCC pins have to be connected directly on the development board. This is done by setting the J1 jumper; the PVCC pin is led off the board. In the application these two adjacent pins are directly connected by soldering. All characteristics and descriptions in this chapter are valid for a direct connection between PVCC and VCC and have been measured with the Atmel® ATA6630. The curves for the ATA6628 are generally the same but the absolute value is 3.3V instead of 5V. The PVCC voltage versus the ambient temperature at different load currents is shown in Figure 2.1.

Figure 2-1. PVCC versus Temperature at Different Load Currents (ATA6630)



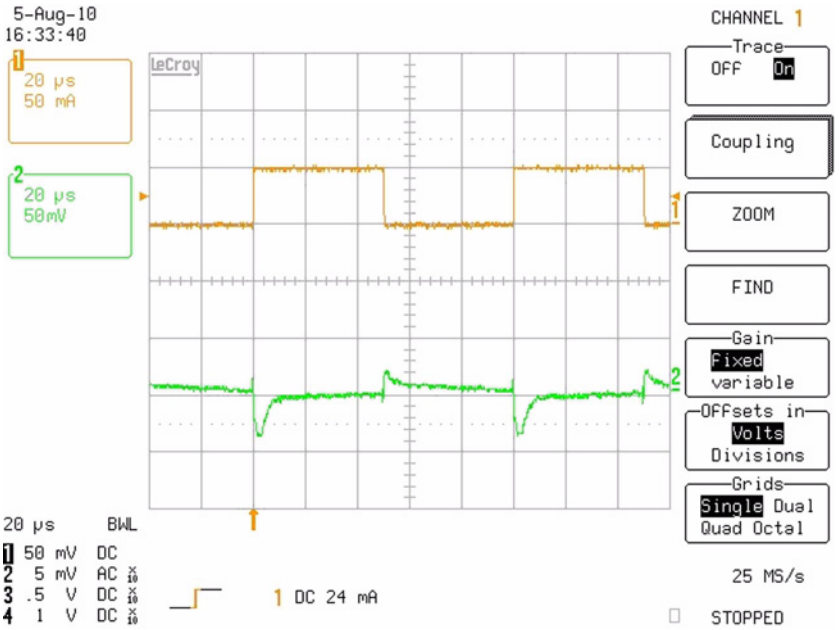
The voltage regulator is able to drive load currents higher than 50mA, but the limiting factor is the resulting power dissipation. The current limitation is specified with at least 85mA, meaning the circuit can deliver at least this current but due to the power dissipation not at a high supply voltage and/or high ambient temperature. It is possible to achieve an excellent thermal behavior with the heat slug soldered to the PCB. The resulting SOA curve is depicted in Figure 2-2 on page 5.

Figure 2-2. SOA: I_PVCC versus V_S at Different Ambient Temperatures



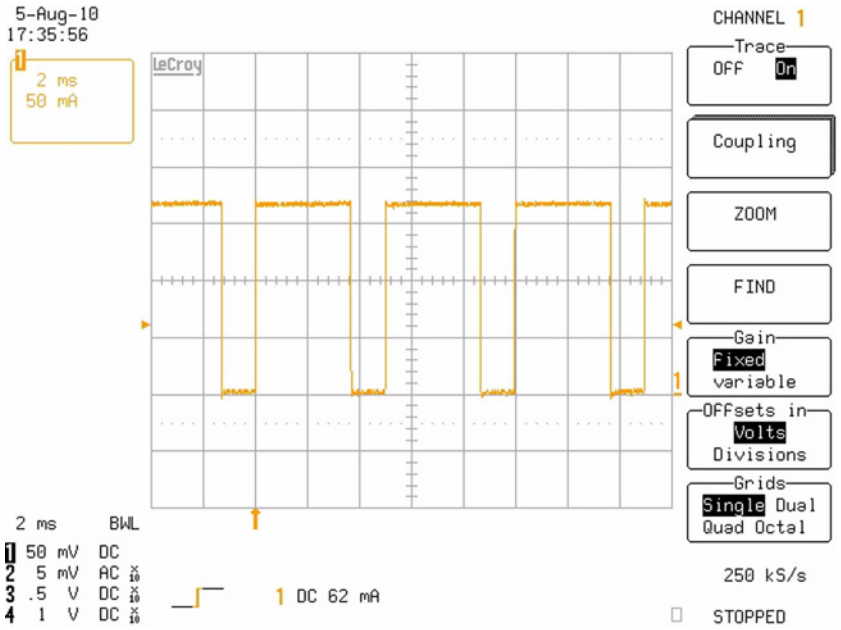
The voltage regulator is protected against overloads by means of current limitation and overtemperature shutdown. In addition, the output voltage is monitored and causes a reset signal at the NRES pin if it drops below the undervoltage threshold. The voltage regulator requires an external capacitor for compensation and for smoothing disturbances from the microcontroller and the other devices supplied by the PVCC voltage. Atmel® recommends using an electrolytic capacitor with C ≥ 1.8µF and a ceramic capacitor with C = 100nF. The values of these capacitors can be varied by the customer, depending on the application. But the ESR value of the electrolytic capacitor should be 0.2Ω < ESR < 5Ω in order to guarantee stable behavior under all conditions (load, supply voltage, temperature). A Tantalum capacitor with 10µF and a ceramic capacitor with 100nF are mounted on the development board at the regulator's output. The following diagram shows what the load-transient response looks like with this external circuitry.

Figure 2-3. Load-transient Response, Ch1: I_{OUT}, Ch2: PVCC



At a short circuit between PVCC and GND, the output of the regulator limits the output current. Because of undervoltage, NRES switches to low and sends a reset to the microcontroller. The IC switches into fail-safe mode. Due to the power dissipation the chip temperature increases and, if it exceeds the PVCC overtemperature threshold, the output switches off. The chip cools down and after the temperature hysteresis the output switches on again. Because of fail-safe mode, the PVCC voltage switches on again even if EN is low. The resulting characteristic of the output current at a short circuit depends on the supply voltage, the ambient temperature, and the thermal connection of the IC to the PCB. The short-circuit current of the voltage regulator at room temperature and a battery voltage of 18V is depicted in Figure 2-4.

Figure 2-4. Voltage Regulator: Current Limitation at a Short-circuit between PVCC and GND



To boost the maximum load current, an external NPN transistor may be used with its base connected to the VCC pin and its emitter connected to the PVCC pin. In this case the regulated output voltage of 5V or 3.3V is available at the PVCC pin. For this reason the PVCC pin and not the VCC pin is led off the board and is always mentioned when a connection has to be made to the 5V or 3.3V regulator. The procedure of boosting the voltage regulator is described in Section 3. “Boosting Up the Voltage Regulator” on page 12.

Note: If an external NPN transistor is used for boosting the output current, there is no short-circuit protection at PVCC.

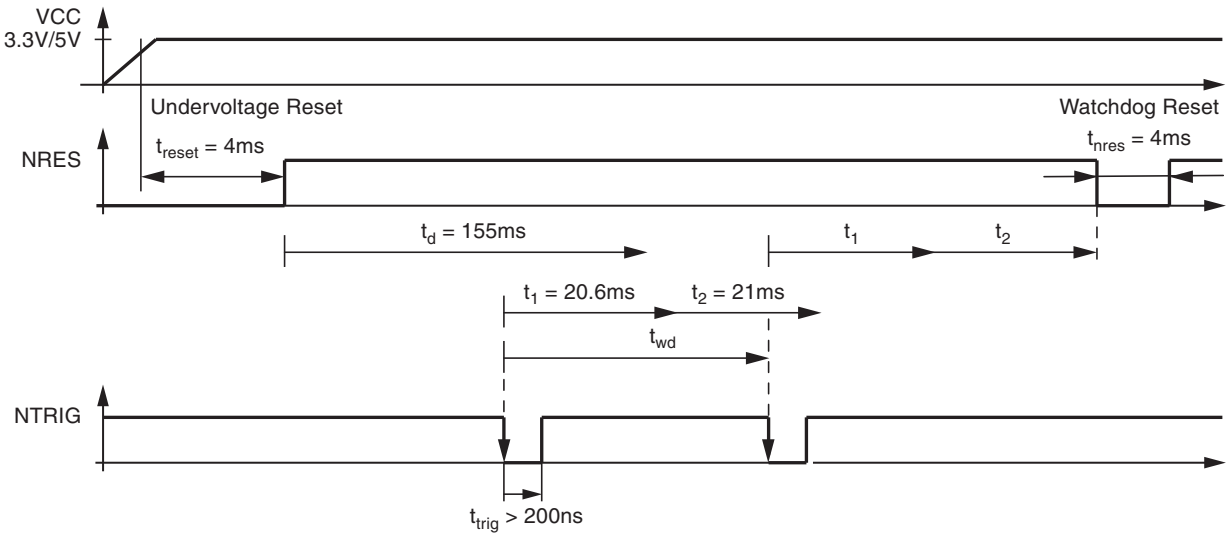
2.3 The Window Watchdog (NTRIG and NRES)

The watchdog anticipates a trigger signal from the microcontroller at the NTRIG input (negative edge) within a defined time window. If no correct trigger signal is received, a reset signal is generated at the NRES output. During Silent or Sleep Mode the watchdog is switched off to reduce current consumption. The NTRIG input includes a pull-down resistor.

A minimum time for the first watchdog pulse is required after the undervoltage reset at the NRES pin disappears and is defined as lead time t_d.

The timing basis of the watchdog is provided by the internal oscillator, whose time period t_{OSC} is adjustable via the external resistor R3 at the pin WD_OSC. The voltage at this pin is 1.23V. There is the resistor R3 with a value of 51kΩ mounted on the development board resulting in the timing sequence in Figure 2-5.

Figure 2-5. Timing Sequence with R3 = 51kΩ



If you want to change the watchdog times mentioned above, it is only necessary to change the value of the external resistor R3 (refer to the datasheet).

If the watchdog is not used in the application it can be disabled by connecting the mode pin with PVCC. This switches off the voltage at the pin WD_OSC and you can either tie this pin to GND or leave it open.

2.4 LIN Interface (LIN, TXD and RXD)

2.4.1 Bus Pin (LIN)

A low side driver with internal current limitation, thermal shutdown, and an internal pull-up resistor in compliance with LIN spec 2.x is implemented. LIN receiver thresholds comply with the LIN protocol specification. The fall time from recessive to dominant bus state and the rise time from dominant to recessive bus state are slope-controlled. The allowed voltage range is between –27V and +40V. The reverse current from the LIN bus to V_S is < 2µA even in case of battery disconnection.

During a short circuit at the pin LIN to Vbattery, the output limits the output current. Due to the power dissipation the chip temperature exceeds the overtemperature threshold and the LIN output is switched off. The chip cools down and after the temperature hysteresis the output switches on again. RXD stays on high because LIN is high. During LIN overtemperature switch-off, the VCC voltage regulator works independently.

On the board the LIN pin is equipped with a 220pF capacitor to GND. In addition, the two extra components diode D2 (LL4148) in series with resistor R3 (1 kΩ) needed for using the development board for a LIN master application have designated placeholders for convenient mounting.

2.4.2 Input/ Output Pin (TXD)

In normal mode the TXD pin is the microcontroller interface for controlling the LIN output state. TXD must be pulled to ground in order to have the LIN bus low. If TXD is high or not connected (internal pull-up resistor), the LIN output transistor is turned off with the bus in recessive state pulled up by the internal resistor. If TXD is low, the LIN output transistor is turned on and the bus is in dominant state.

An internal timer prevents the bus line from being driven permanently in dominant state. If the TXD input is forced to low for longer than t_{dom} > 27ms, the LIN bus driver is switched to recessive state. To reactivate the LIN Bus driver, switch TXD to high for longer than 10µs.

The actual level at the TXD pin is relevant even when switching to sleep mode.

During fail-safe mode, this pin is used as an output and signals the fail-safe source. It is current limited to I < 8mA.

2.4.3 Output Pin (RXD)

This pin reports the state of the LIN bus to the microcontroller. LIN high (recessive state) is reported by a high level at RXD, LIN low (dominant state) is reported by a low level at RXD. The output has an internal pull up resistor with typ. 5kΩ to PVCC.

The output is short-circuit protected. RXD is switched off in unpowered mode.

During fail-safe mode it signals the fail-safe source together with the TXD pin.

2.5 Voltage Monitoring (VBATT, PV, DIV_ON)

With the integrated switchable voltage divider it is possible to very accurately measure the battery voltage. The upper terminal of the divider is connected via a switch to the VBATT pin, the tap is connected to the PV pin, and the lower terminal is internally connected to GND. The control of the switch is done by the independent low voltage input DIV_ON. A high level (PVCC) switches the voltage divider on and a low level switches it off. There is an integrated pull-down resistor at the DIV_ON input. With this switch it is possible to reduce the current consumption, because the voltage divider can be only active during measurement of battery voltage.

The VBATT pin can be connected directly with the battery voltage via a low-ohmic resistor. The divider ratio is for both versions 1:6, the total resistance is about 100kΩ The input current at VBATT consists of the current through the voltage divider and a constant current of about 20µA, which is needed for the control of the internal switch at VBATT.

2.6 Enable Input (EN)

This pin controls the operating mode of the device. If EN = 1 the circuit is in normal mode, with transmission paths from TXD to LIN and from LIN to RXD both active and the voltage regulator also switched on.

IF EN is switched to low while TXD is still high, the device is forced to silent mode. No data transmission is then possible, the LIN pin is pulled to VS by a weak current source, the current consumption is reduced to IVS typ. 40µA, but the voltage regulator has its full functionality.

If EN is switched to low while TXD is low, the device is forced into sleep mode, the LIN pin is pulled to VS by a weak current source, and the voltage regulator is switched off. During sleep mode the device is still supplied from the battery voltage, the supply current is typically 10µA. The pin EN provides a pull-down resistor in order to force the transceiver into sleep or silent mode if the pin is not connected.

In order to avoid any influence to the LIN pin while switching into sleep mode, it is possible to switch the EN to low up to 3.2µs earlier than the TXD. Therefore, the best and easiest way to switch the Atmel® ATA6628/ATA6630 into sleep mode is with two simultaneous falling edges at TXD and EN.

2.7 SP_ Mode Input Pin

The SP_Mode pin is a low-voltage input. A high level during normal mode activates the high speed mode of the LIN transceiver. In this mode the slope control is switched off so the rising edge as well as the falling edge of the LIN signal are shorter. In high speed mode the achieved baud rate is higher than 100Kbaud. With this feature for example the flash memory of the connected microcontroller can be programmed via the LIN bus in an acceptable time.

During high speed mode the EMC characteristics of the circuit are different from the values in normal LIN communication.

Reverting to LIN 2.x transceiver mode with slope control is possible if you switch the SP_MODE pin to low.

2.8 Mode and TM inputs (MODE and TM)

The TM input is only used for Atmel® internal testing purposes and therefore always connected directly to GND.

The mode input is pulled down by the 4.7kΩ resistor R1 on the board thus the watchdog is active in fail-safe and normal mode.

Especially during the early development phase it can be helpful to have the option of deactivating the watchdog in order to debug the application program without disturbing RESETS caused by the watchdog. The watchdog can therefore be switched off by connecting the MODE pin to PVCC externally.

If the watchdog is not used in an application, the mode pin can be connected directly to PVCC.

2.9 Wake Input (WAKE)

The WAKE input is a high-voltage input used to wake up the device from sleep mode or silent mode. It is usually connected to an external transistor or a switch to generate a local wake-up. A pull-up current source with typically 10µA is implemented as well as a debounce timer with a typical debounce time of 70µs.

On the development board there is the push button S1 to generate a local wake-up by pulling the WAKE pin to GND. The resistor R5 = 2.7kΩ is needed to limit the input current in case of voltage transients and in case of GND shifts.

Even if the WAKE pin is pulled to GND, it is possible to switch the IC into sleep or silent mode. Connect the WAKE pin directly to VS if you do not need it.

2.10 Reset Output (NRES)

The Reset pin is an open drain output that switches to low during PVCC undervoltage or a watchdog failure.

After ramping up the battery voltage or after a wake-up from sleep mode the voltage regulator is switched on and the PVCC voltage exceeds the undervoltage threshold. The implemented undervoltage delay keeps the NRES output at the low level for typ. 4ms after PVCC reaches its nominal value. Then the NRES switches to high and the watchdog waits for the trigger sequence from the microcontroller.

The NRES pin also switches to low if the watchdog is not triggered correctly (see Section 2.3 “The Window Watchdog (NTRIG and NRES)” on page 7).

An external resistor connected to PVCC is necessary for pulling up the NRES output. This resistor R9 has a value of 10kΩ on the development board.

If a reset occurs (NRES is low), the circuit switches to fail-safe mode.

2.11 KL_15 Input (KL_15)

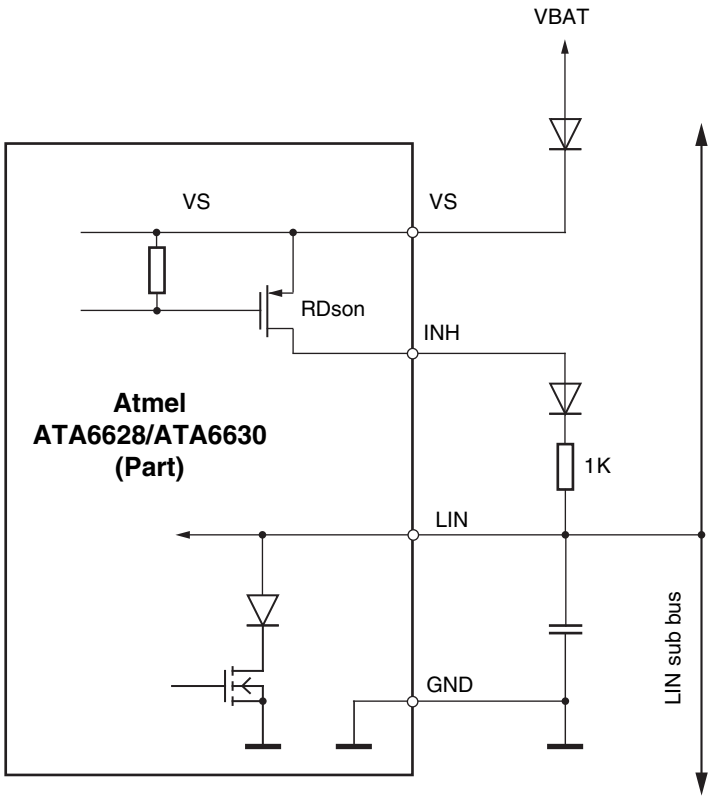
This pin is a high voltage input used to wake-up the device from sleep or silent mode. It is an edge sensitive pin (low to high transition). It is usually connected to the ignition in order to generate a local wake up in the application, if the ignition is switched on. Although KL_15 pin is at high voltage (Vbat), it is possible to switch the IC into sleep or silent mode. Connect the KL_15 pin directly to GND if you do not need it. A debounce timer with a typical debounce time of 160µs is implemented.

To protect this pin against voltage transients a series resistor R12 = 47kΩ and a ceramic capacitor C8 with 100nF are recommended. With this RC combination the wake-up time t_{W_KL15} and therefore the sensitivity against transients on the ignition KL15 can be increased. The wake-up time can be increased further by higher values for C8.

2.12 Inhibit output (INH)

This pin is a high-side switch to V_S and it is normally used to switch on an external load during normal mode or fail-safe mode. This load could for example be a voltage regulator that supplies a separate module or a voltage divider for measuring the supply voltage. In sleep mode or silent mode the INH output is switched off. For master node applications it is possible to switch off the external master pull-up resistor (R4) by the INH pin.

Figure 2-6. Switching the LIN Master Pull-up Resistor Using the INH Output



With this measure the current consumption is reduced to a minimum in case of a short circuit between LIN and GND because the Atmel® ATA6628/ATA6630 can be switched into sleep mode, meaning the INH output is off.

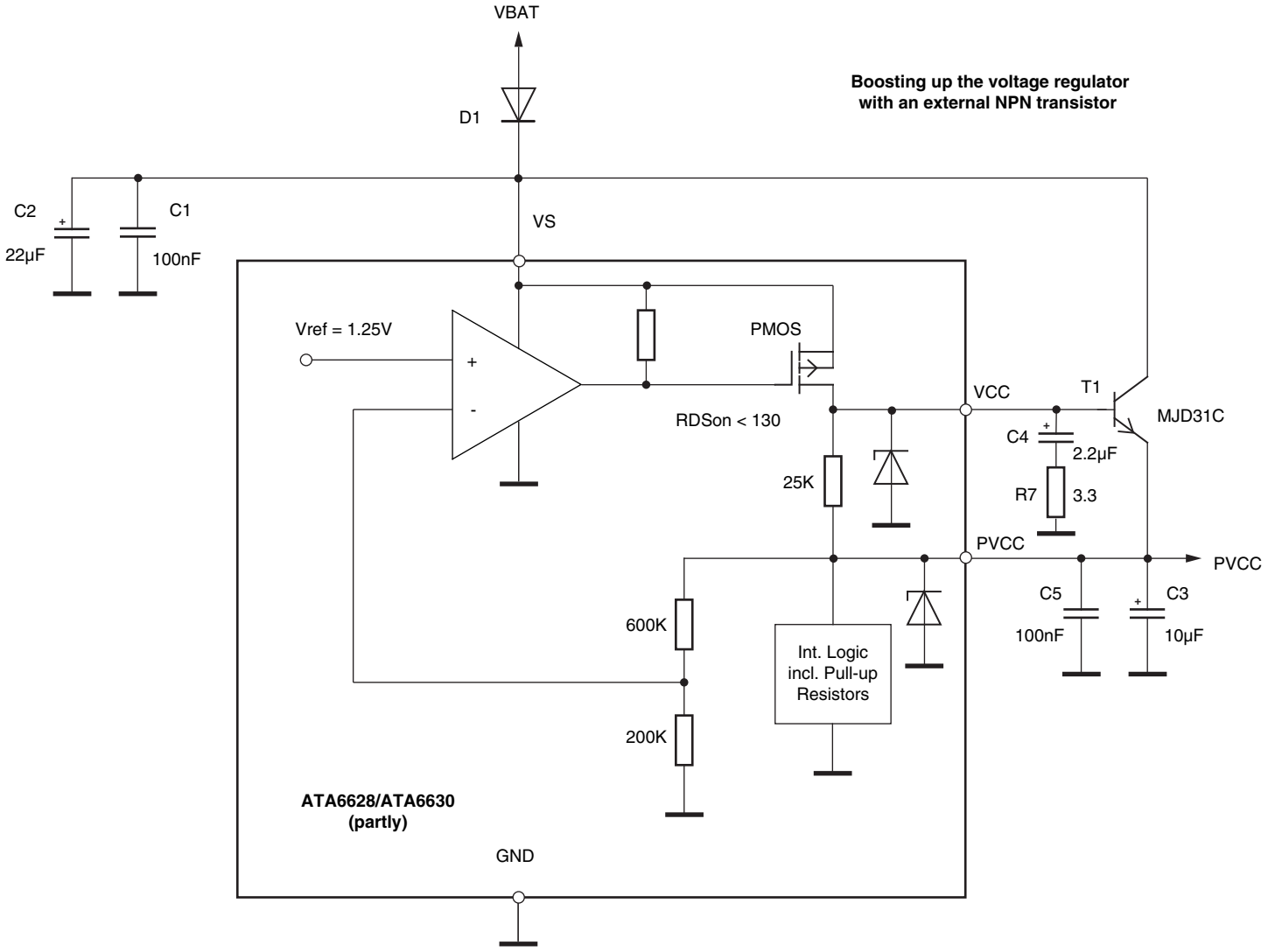
3. Boosting Up the Voltage Regulator

For some applications there is a need for a higher current than the internal voltage regulator can deliver. As the main power dissipation of the IC is created from the output transistor of the voltage regulator, the output current of the voltage regulator has a significant influence on the safe operating area shown in Figure 2-1 on page 4.

If the Atmel® ATA6628/ATA6630 needs to be operated above the curves depicted in Figure 2-2 on page 5, it is possible to boost the maximum output current by using an external NPN transistor. It is also possible to use this external transistor for increasing the maximum ambient temperature even at a low PVCC output current. With this external transistor the power dissipation of the IC becomes very low because the voltage regulator only has to drive the base current of the transistor T1. This leads to an increased maximum ambient temperature at which the Atmel ATA6628/ATA6630 can operate.

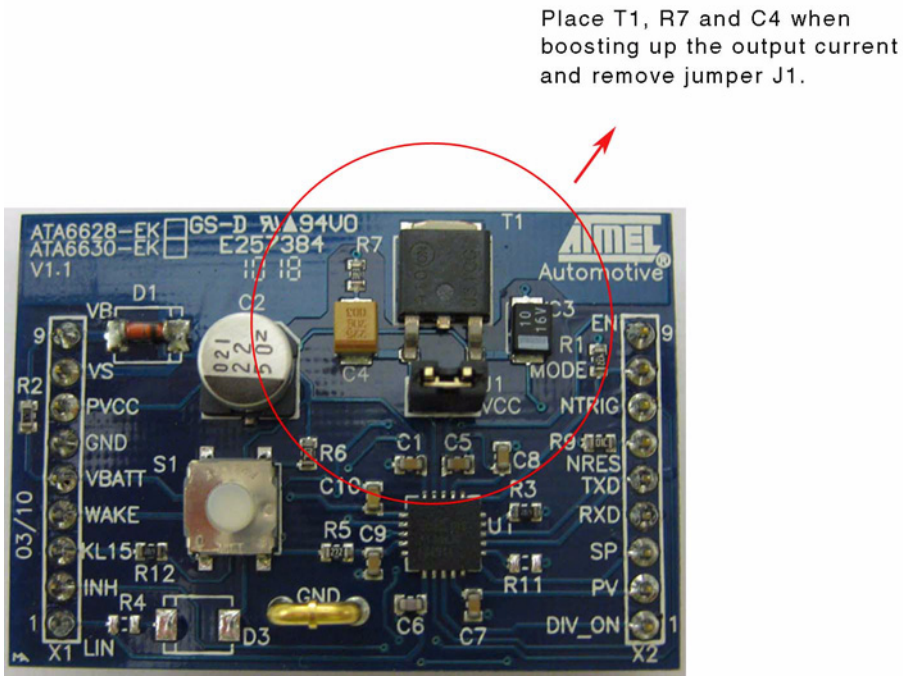
Please note that the output voltage is no longer short circuit protected when boosting the output current with an external NPN transistor.

Figure 3-1. Voltage Regulator: Boosting Procedure with an External NPN



For this case on the development board the NPN transistor T1 (MJD31C) is already mounted in a D-PAK package. The base of the transistor T1 is connected to VCC and the emitter is connected to PVCC. In addition to the transistor itself there are two more components that need to be placed on the development board: the resistor R7 (3.3Ω) and the electrolytic capacitor C4 (2.2µF) connected to the base of T1. These two parts are needed for stability reasons. The jumper J1 has to be removed in order to activate the transistor T1.

Figure 3-2. Boosting up the Voltage Regulator



The limiting parameter for the output current is the maximum power dissipation of the external NPN transistor. In the version at this stage the thermal resistance of the MJD31C soldered on the minimum pad size is 80K/W, this means the possible maximum output current at V_S = 12V is approximately 230mA at room temperature. It is not recommended to exceed this limit because the transistor could be damaged as a result of overtemperature. If a higher output current is required, additional cooling of the external transistor has to be ensured (see Figure 3-3, Figure 3-4 and Figure 3-5 on page 14).

The diagrams on this page show the maximum output current Imax of the voltage regulator as a function of the supply voltage V_S at different levels of cooling respectively thermal resistances R_{thJA} of the external NPN- transistor T1.

Figure 3-3. Imax versus V_S at R_{thJA} = 80K/W

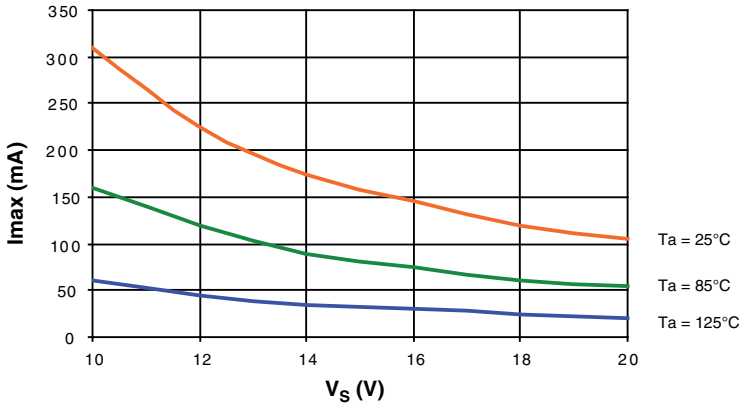


Figure 3-4. Imax versus V_S at R_{thJA} = 50K/W

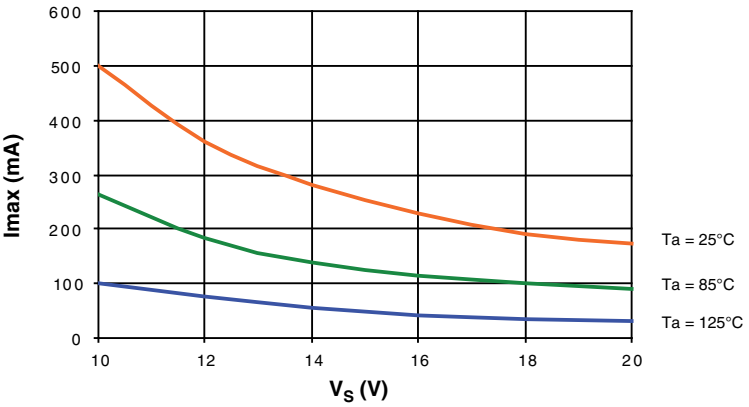
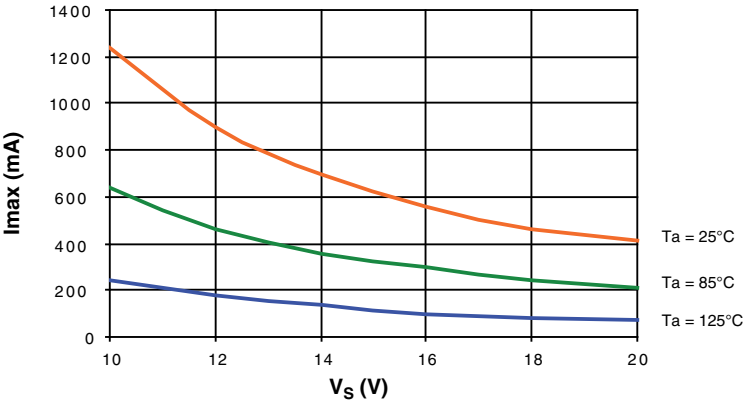


Figure 3-5. Imax versus V_S at R_{thJA} = 20K/W



In the following diagrams some typical operating characteristics measured with the Atmel® ATA6630-EK development board are shown. The supply voltage VS is approximately a diode forward voltage lower than the battery voltage VB (reverse battery protection). Please note that if an external NPN transistor is used for boosting this voltage, the PVCC voltage has no short circuit protection.

Figure 3-6. Output Voltage PV_{CC} versus Temperature at Different Load Currents

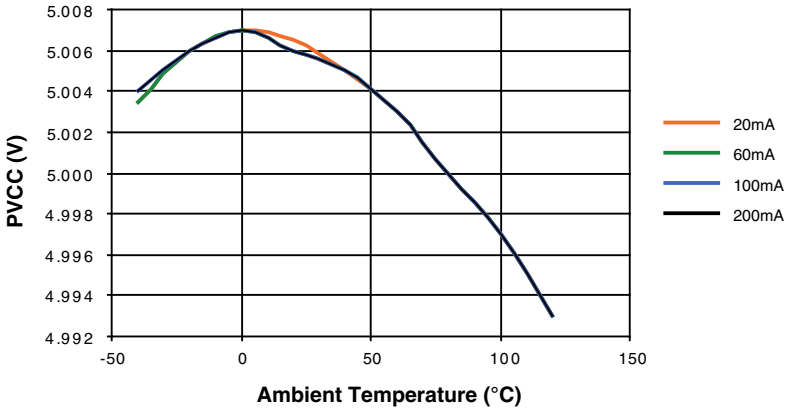
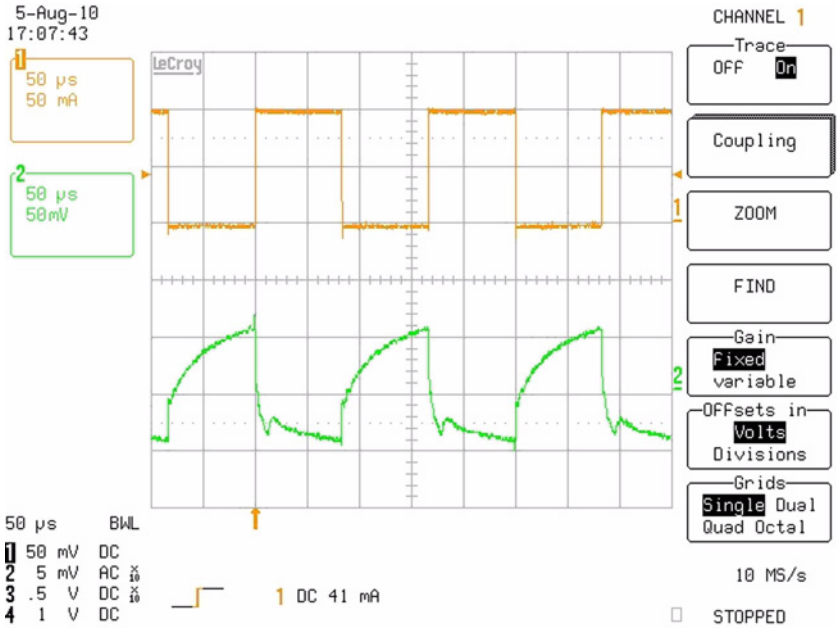
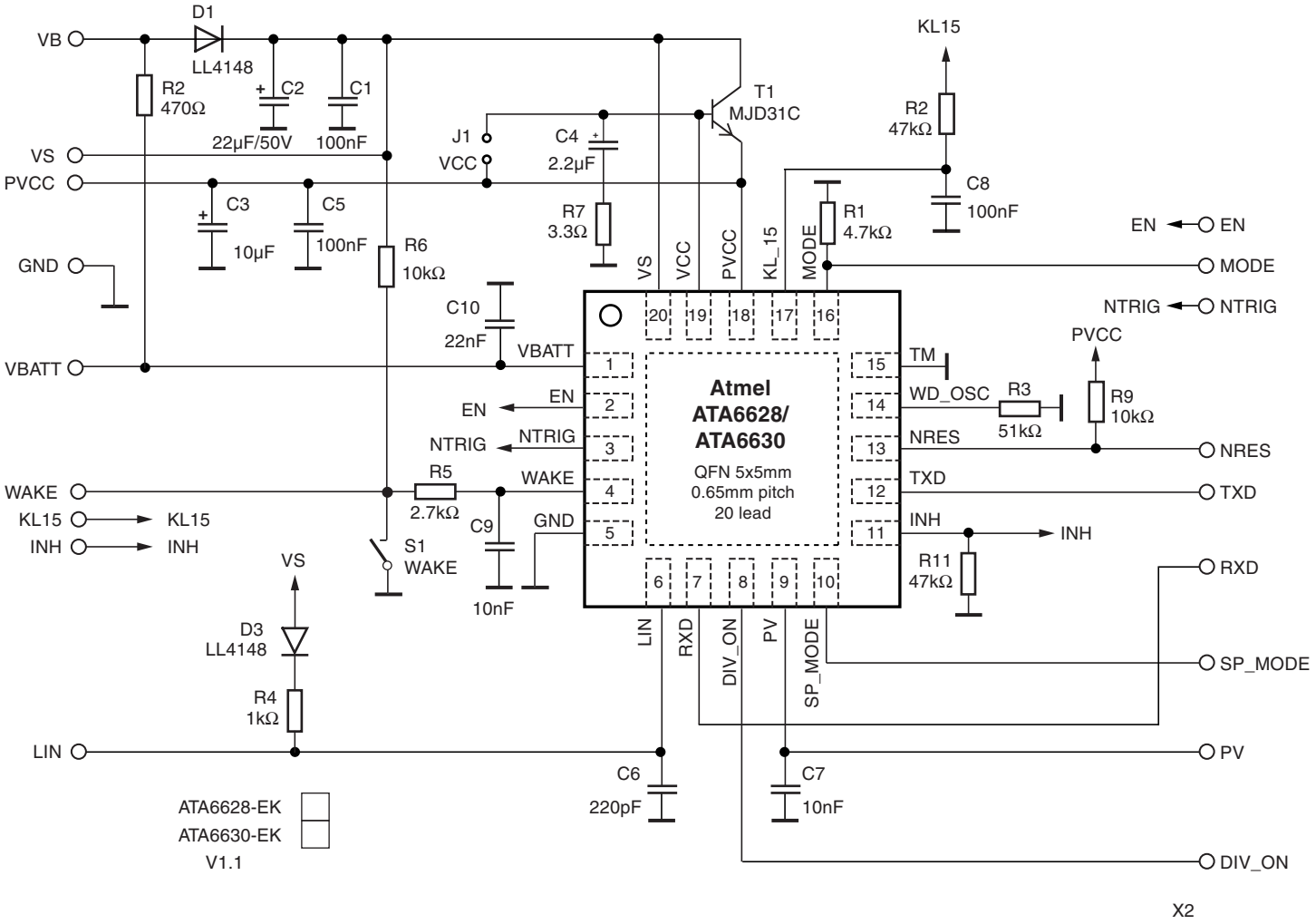


Figure 3-7. Load Transient Response Ch1: I_{OUT}, Ch2: PVCC



4. Schematic and Layout of the Development Board for the Atmel ATA6628/ATA6630

Figure 4-1. Schematic of the Development board for the Atmel® ATA6628/ATA6630



Notes:
1. D3 and R4 are only necessary for a master node and not mounted
2. C9 is no longer needed and therefore not mounted
3. R11 is not mounted

Figure 4-2. Atmel® ATA6628/ATA6630 Board Component Placement; Top Side, Top View

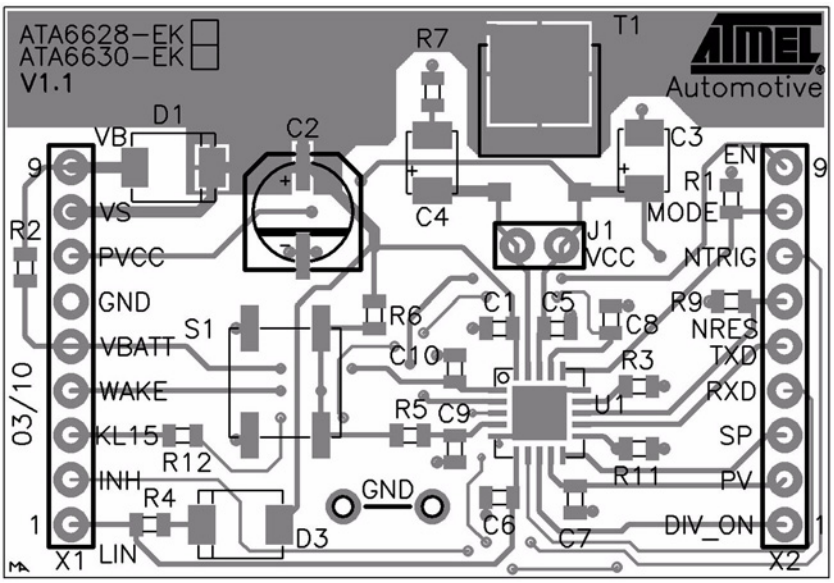


Figure 4-3. Atmel ATA6628/ATA6630 Development Board; Top Side, Top View

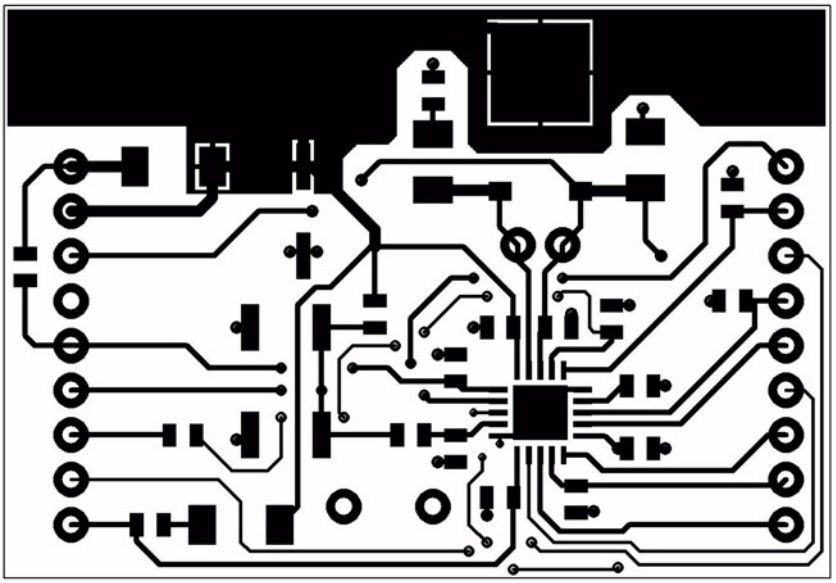
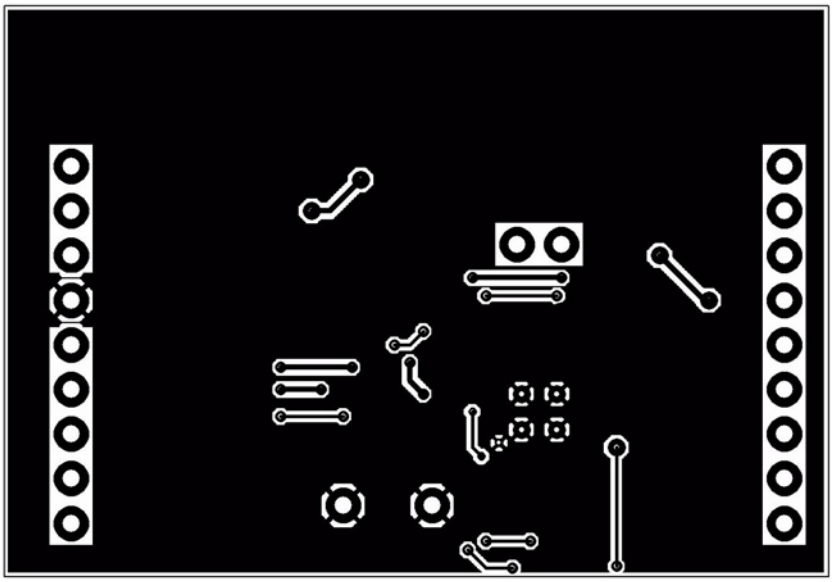


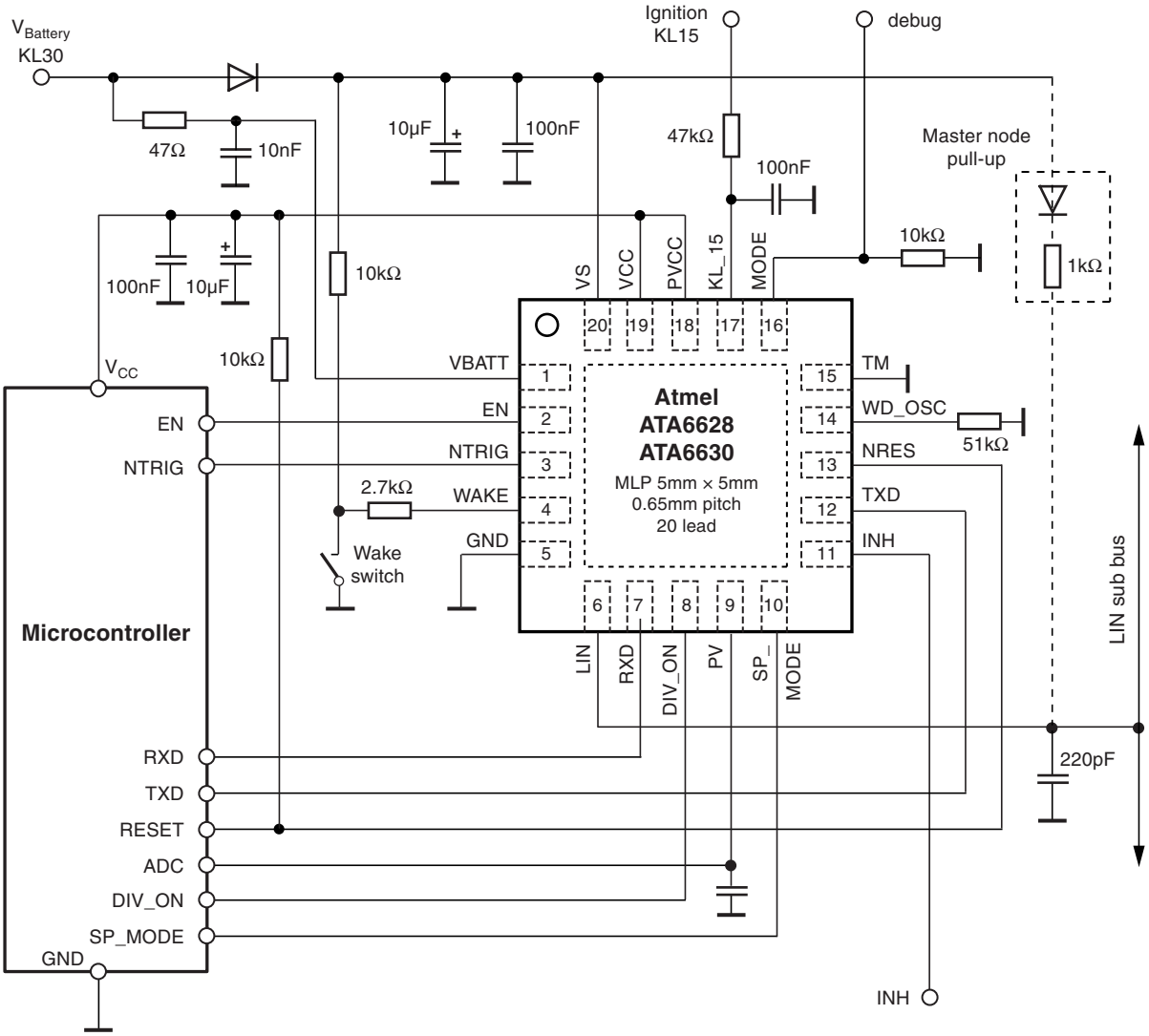
Figure 4-4. Atmel® ATA6628/ATA6630 Development Board; Bottom Side, Top View (as if PCB was Transparent)



5. Application Examples

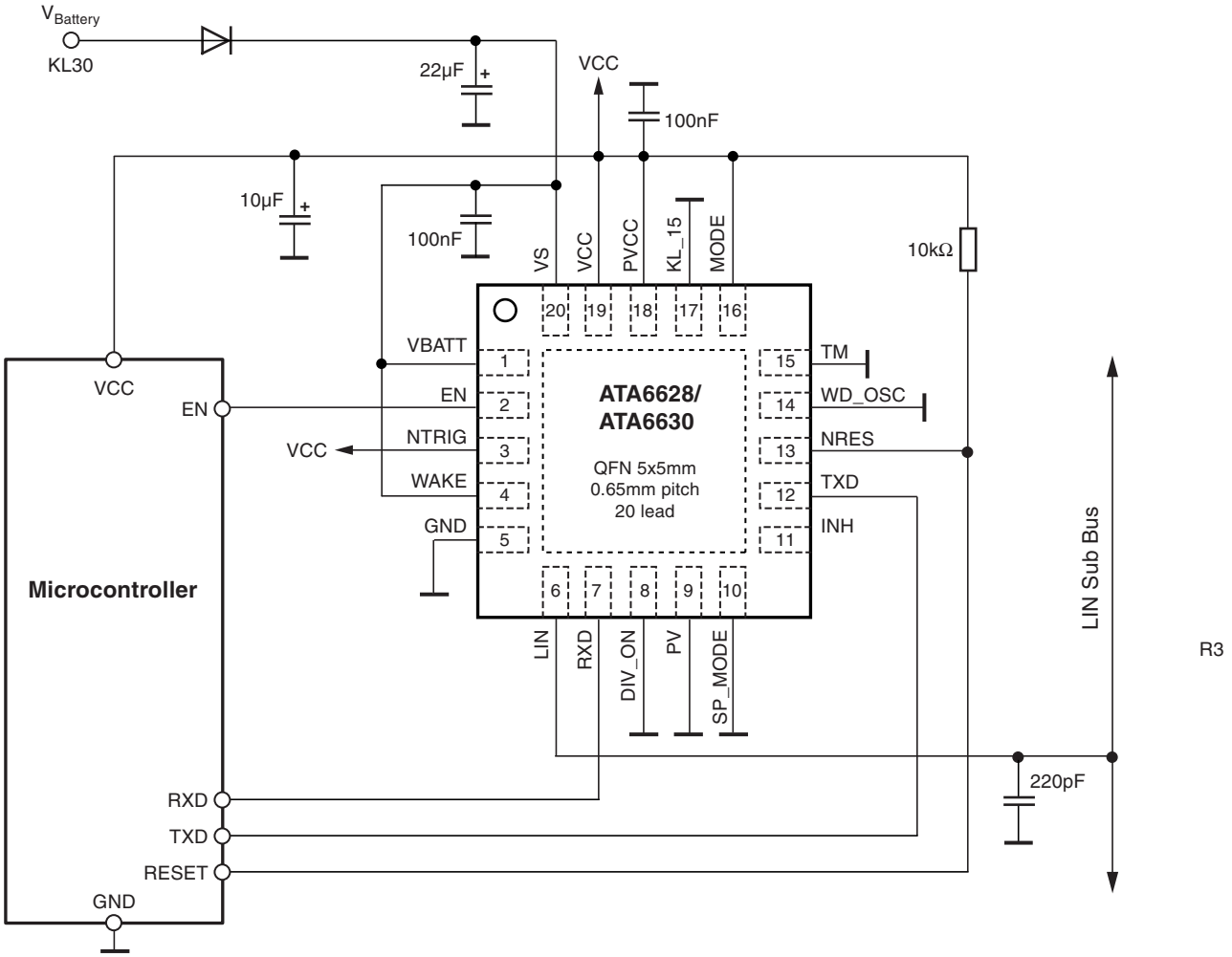
Just to show how easy it is to develop a LIN-based application with the development board for the Atmel® ATA6628/ATA6630 there are some application circuits depicted on the following pages.

Figure 5-1. Typical Application Circuit



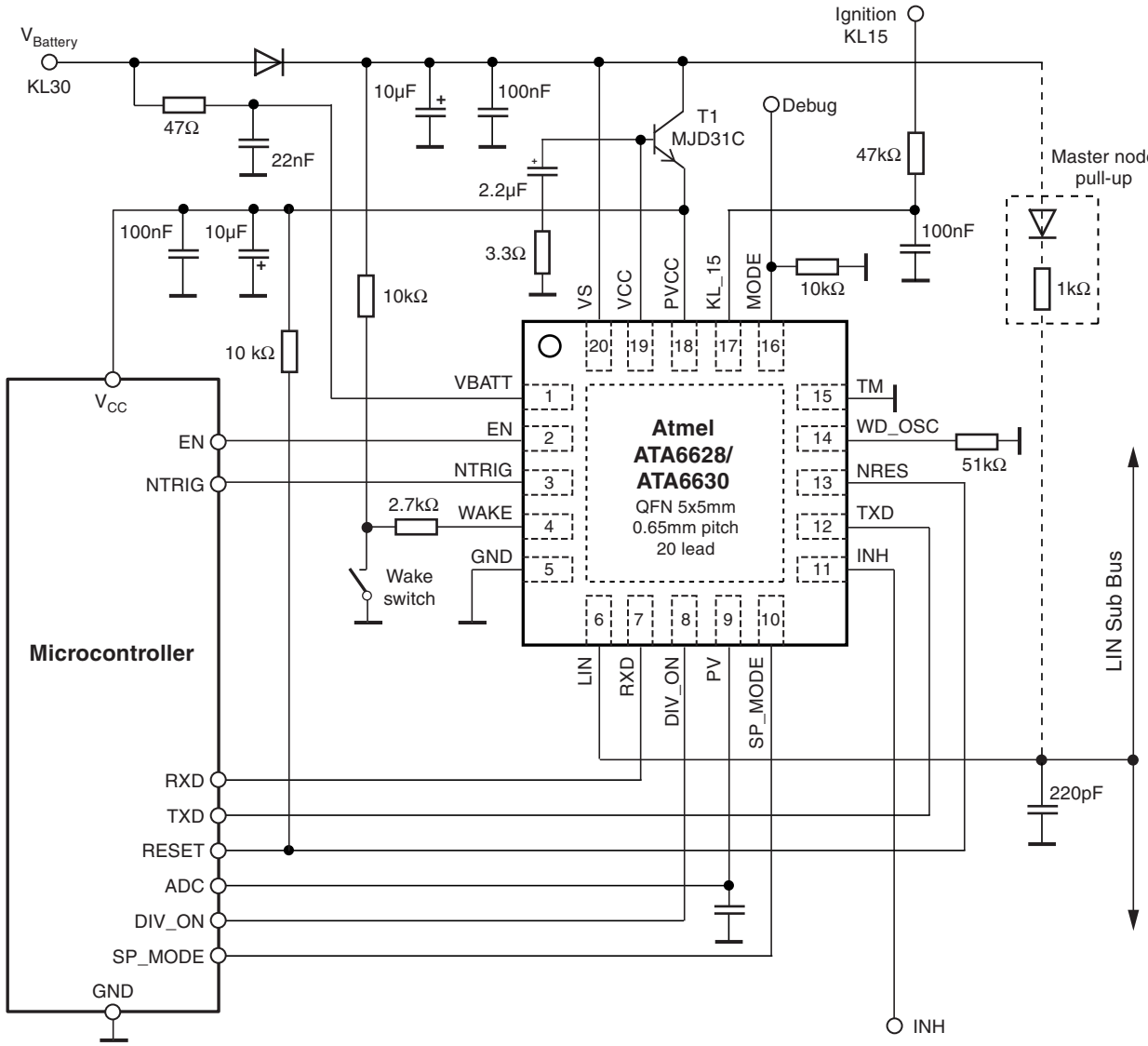
Note: All features active

Figure 5-2. LIN Slave with Minimum External Devices



Notes:
1. No local wake-up
2. No watchdog
3. No battery voltage monitoring

Figure 5-3. Application Circuit with NPN Transistor for Boosting the Voltage Regulator



Notes: 1. All features active
No Short circuit protection of the voltage regulator output (PVCC)

Note: Application examples have not been examined for series use or reliability, and no worst case scenarios have been developed. Customers who adapt any of these proposals must carry out their own tests and make sure that no negative consequences arise from the proposals.

6. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
9202B-AUTO-03/11	• Section 1 “Introduction” on page 1 changed • Figure 2-2 “SOA: I_PVCC versus V_S...” on page 5 changed

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