

7.0V to 9.5V

0.001% (Typ)

0.002% (Typ)

2.3Vrms(Typ)

-100dB(Typ)

-40°C to +85°C

38mA (Typ)

Sound Processor with Built-in 3-band Equalizer **BD37544FS**

General Description

BD37544FS is a sound processor with built-in 3-band equalizer for car audio. The functions are stereo input selector (which can switch single and GND isolation), input-gain control, main volume, super bass, 5ch fader volume, LPF/HPF for subwoofer, and mixing input. Moreover, "Advanced switch circuit", which is an original ROHM technology, can reduce various switching noise (ex. No-signal, low frequency like 20Hz & large signal inputs). Also, "Advanced switch" makes control of microcomputer easier, and can construct a high quality car audio system.

Features

- Reduced switching noise of input gain control, mute, main volume, fader volume, bass, middle, treble, super bass, mixing by using advanced switch circuit.
- Built-in differential input selector that can make various combination of single-ended / differential input.
- Built-in ground isolation amplifier inputs, which is ideal for external stereo input.
- Built-in input gain controller reduces switching noise for volume of a portable audio input.
- Decreased number of external components due to built-in 3-band equalizer filter, LPF for subwoofer, and HPF. It is possible to control Q, Gv, fo of 3-band equalizer and fc of LPF/HPF through I²C BUS control.
- It is possible to adjust the gain of the bass, middle, and treble up to ±20dB with 1 dB step gain adjustment.
- It is equipped with output terminals for Subwoofer. Moreover, the stereo signal output of the front and rear can also be chosen by the I²C BUS control.
- Built-in mixing input and mixing attenuator.
- Energy-saving design resulting in low-current consumption is achieved by utilizing the Bi-CMOS process. It has the advantage in quality over scaling down the power heat control of the internal regulators.
- Input terminals and output terminals are organized and separately laid out to keep the signal flow in one direction which results in simpler and smaller PCB lavout.
- It is possible to control the I²C BUS by 3.3V / 5V.

Applications

It is optimal for car audio systems. It can also be used for audio equipment of mini Compo, micro Compo, TV, etc.

Key Specifications

- Power Supply Voltage Range:
- Circuit Current (No Signal):
- Total Harmonic Distortion: THD+N1 THD+N2 Maximum Input Voltage:
- Cross-talk Between Selectors:
- Volume Control Range:
- +15 dB to -79dB Output Noise Voltage: V_{NO1} 3.8µVrms(Typ) V_{NO2} 4.8µVrms(Typ) 1.8µVrms(Typ)
- **Residual Output Noise Voltage:**
- **Operating Temperature Range:**

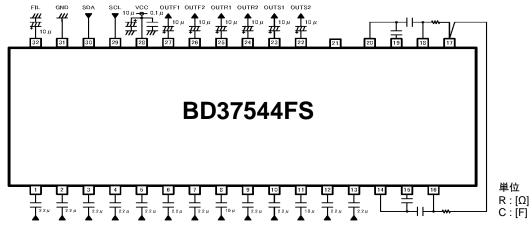
Package

W(Typ) x D(Typ) x H(Max)

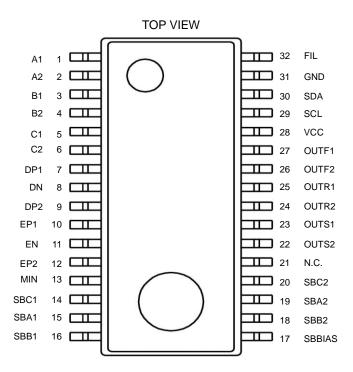


OProduct structure : Silicon monolithic integrated circuit OThis product has no designed protection against radioactive rays

Typical Application Circuit



Pin Configuration



Pin Descriptions

Pin No.	Pin Name	Description	Pin No.	Pin Name	Description
1	A1	A input terminal of 1ch	17	SBBIAS	SuperBass bias terminal
2	A2	A input terminal of 2ch	18	SBB2	SuperBass setting terminal of 2ch
3	B1	B input terminal of 1ch	19	SBA2	SuperBass setting terminal of 2ch
4	B2	B input terminal of 2ch	20	SBC2	SuperBass setting terminal of 2ch
5	C1	C input terminal of 1ch	21	N.C.	No connection
6	C2	C input terminal of 2ch	22	OUTS2	Subwoofer output terminal of 2ch
7	DP1	D positive input terminal of 1ch	23	OUTS1	Subwoofer output terminal of 1ch
8	DN	D negative input terminal	24	OUTR2	Rear output terminal of 2ch
9	DP2	D positive input terminal of 2ch	25	OUTR1	Rear output terminal of 1ch
10	EP1	E positive input terminal of 1ch	26	OUTF2	Front output terminal of 2ch
11	EN	E negative input terminal	27	OUTF1	Front output terminal of 1ch
12	EP2	E positive input terminal of 2ch	28	VCC	Power supply terminal
13	MIN	Mixing input terminal	29	SCL	I ² C Communication clock terminal
14	SBC1	SuperBass setting terminal of 1ch	30	SDA	I ² C Communication data terminal
15	SBA1	SuperBass setting terminal of 1ch	31	GND	GND terminal
16	SBB1	SuperBass setting terminal of 1ch	32	FIL	VCC/2 terminal

Block Diagram

32 31 30 29 28	27 26	25 24	23 22	21	20	19 18	17
V 777 VCC/2 GND I2C BUS LOGIC							VCC/2
■ Fader Gain:+15dB to -79dB/1dB step				የ			
★no pop noise ■LPF fc=55/85/120/160Hz							
HPF fc=55/85/120/160Hz ■ATT Gain: +7dB to -79dB/1dB step	Fader	Fader★	Fader	ATT★			
★no pop noise Super Bass ★no pop noise 3 Band P-EQ (Tone control) Gain: +20dB to -20dB/1dB step							
★no pop noise •Bass: f0=60/80/100/120Hz Q=0.5/1.0/1.5/2.0 •Meddle:f0=500/1k/1.5k/2.5kHz							
Q=0.75/1/.25/1.5 •Treble : f0=7.5k/10k/12.5k/15kHz Q=0.75/1.25		★Super Bass					
■Volume Gain: +15dB to -79dB/1dB step		★3 Band P-EG (Tone control)	Į				
★no pop noise ■Input Gain Gain: +20dB to -0dB/1dB step		★Volume/Mute					
★no pop noise		★Input Gain					
Input selector	(3 single-end a	nd 2 stereo ISO))				
	Buffe ISO	rdGND amp ISO amp	BufferdGND ISO amp	ufferdGND ISO amp			
							<u> </u>
1 2 3 4 5	6 7	89	10 11	12 13	14	15	16

Absolute Maximum Ratings (Ta=25°C)

Parameter Symbol		Rating	Unit
Power Supply Voltage	Vcc	10.0	V
Input Voltage	V _{IN}	V _{cc} +0.3 to GND-0.3	V
Power Dissipation	Pd	0.95 (Note 1)	W
Storage Temperature	Tstg	-55 to +150	°C

(Note 1) When mounted on the standard board (70 x 70 x 1.6 mm³), derate by 7.6mW/°C for Ta above 25°C.

 Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions

Parameter	Symbol	Min	Тур	Max	Unit
Power Supply Voltage	Vcc	7.0	-	9.5	V
Temperature	Topr	-40	-	+85	°C

Electrical Characteristics

(Unless specified, Ta=25°C, V_{CC}=8.5V, f=1kHz, V_{IN}=1Vrms, Rg=600Ω, R_L=10kΩ, A1 input, Input gain 0dB, Mute OFF, Volume 0dB, Tone control 0dB, Loudness 0dB, LPF OFF, HPF OFF, Mixing OFF, Fader 0dB)

BLOCK	Parameter	Symbol	•	Limit	G	Unit	Conditions	
BLC	Parameter	Symbol	Min	Тур	Max	Unit	Conduons	
	Circuit Current (No Signal)	la	-	38	48	mA	No signal	
	Voltage Gain	Gv	-1.5	0	+1.5	dB	G _V =20log(V _{OUT} /V _{IN})	
	Channel Balance	СВ	-1.5	0	+1.5	dB	$CB = G_{V1}-G_{V2}$	
	Total Harmonic Distortion 1 (FRONT,REAR)	THD+N1	-	0.001	0.05	%	V _{OUT} =1Vrms BW=400Hz-30KHz	
	Total Harmonic Distortion 2 (SUBWOOFER)	THD+N2	-	0.002	0.05	%	V _{OUT} =1Vrms BW=400Hz-30KHz	
GENERAL	Output Noise Voltage 1 (FRONT,REAR) *	V _{NO1}	-	3.8	15	μVrms	Rg = 0Ω BW = IHF-A	
GENI	Output Noise Voltage 2 (SUBWOOFER) *	V_{NO2}	-	4.8	15	µVrms	Rg = 0Ω BW = IHF-A	
	Residual Output Noise Voltage*	V _{NOR}	-	1.8	10	μVrms	Fader = -∞dB Rg = 0Ω BW = IHF-A	
	Cross-talk Between Channels *	СТС	-	-100	-90	dB	$\begin{array}{l} Rg = 0\Omega \\ CTC = 20log(V_{OUT}/V_{IN}) \\ BW = IHF-A \end{array}$	
	Ripple Rejection	RR	-	-70	-40	dB	f=1kHz V _{RR} =100mVrms RR=20log(V _{CC} IN/V _{OUT})	
	Input Impedance(A, B,C)	R _{IN_s}	70	100	130	kΩ		
~	Input Impedance(D, E)	RIN_D	175	250	325	kΩ		
SELECTOR	Maximum Input Voltage	V _{IM}	2.1	2.3	-	Vrms	V _{IM} at THD+N(V _{OUT})=1% BW=400Hz-30KHz	
UT SEL	Cross-talk Between Selectors *	СТЅ	-	-100	-90	dB	$\label{eq:response} \begin{array}{l} Rg = 0\Omega \\ CTS = 20 log(V_OUT/V_IN) \\ BW = IHF-A \end{array}$	
INPUT	Common Mode Rejection Ratio*	CMRR	50	65	-	dB	XP1 and XN input XP2 and XN input CMRR=20log(V _{IN} /V _{OUT}) BW = IHF-A,[*XD,E]	

Electrical Characteristics - continued

				Limit					
BLOCK	Parameter	Symbol	Min	Тур	Max	Unit	Conditions		
GAIN	Minimum Input Gain	Gin_min	-2	0	+2	dB	Input gain 0dB V _{IN} =100mVrms G _{IN} =20log(V _{OUT} /V _{IN})		
INPUT G	Maximum Input Gain	Gin_max	18	20	22	dB	Input gain 20dB V _{IN} =100mVrms G _{IN} =20log(V _{OUT} /V _{IN})		
	Gain Set Error	Gin_err	-2	0	+2	dB	GAIN=+20dB to +1dB		
MUTE	Mute Attenuation *	Gmute	-	-105	-85	dB	Mute ON G _{MUTE} =20log(V _{OUT} /V _{IN}) BW = IHF-A		
	Maximum Gain	G _{V_MAX}	13	15	17	dB	Volume = $15dB$ V _{IN} =100mVrms G _V =20log(V _{OUT} /V _{IN})		
VOLUME	Maximum Attenuation *	Gv_min	-	-100	-85	dB	$ Volume = -∞dB \\ G_V=20log(V V_{OUT}/V_{IN}) \\ BW = IHF-A $		
02	Attenuation Set Error 1	Gv_err1	-2	0	+2	dB	GAIN & ATT=+15dB to -15dB		
	Attenuation Set Error 2	G_{V_ERR2}	-3	0	+3	dB	ATT=-16dB to -47dB		
	Attenuation Set Error 3	Gv_err3	-4	0	+4	dB	ATT=-48dB to -79dB		
	Maximum Boost Gain	GB_BST	18	20	22	dB	Gain=+20dB f=100Hz V _{IN} =100mVrms G _B =20log (V _{OUT} /V _{IN}) Gain=-20dB f=100Hz V _{IN} =2Vrms G _B =20log (V _{OUT} /V _{IN})		
BASS	Maximum Cut Gain	Gb_cut	-22	-20	-18	dB			
	Gain Set Error	Gb_err	-2	0	+2	dB	Gain=-20dB to +20dB f=100Hz		
щ	Maximum Boost Gain	G _{M_BST}	18	20	22	dB	Gain=+20dB f=1kHz V _{IN} =100mVrms G _M =20log (V _{OUT} /V _{IN})		
MIDDLE	Maximum Cut Gain	G м_сит	-22	-20	-18	dB	Gain=-20dB f=1kHz V _{IN} =2Vrms G _M =20log (V _{OUT} /V _{IN})		
	Gain Set Error	Gm_err	-2	0	+2	dB	Gain=-20dB to +20dB f=1kHz		
ш	Maximum Boost Gain	G _{T_BST}	18	20	22	dB	Gain=+20dB f=10kHz V _{IN} =100mVrms Gτ=20log (V _{OUT} /V _{IN})		
TREBLE	Maximum Cut Gain	Gt_cut	-22	-20	-18	dB	Gain=-20dB f=10kHz V _{IN} =2Vrms GT=20log (V _{OUT} /V _{IN})		
	Gain Set Error	Gt_err	-2	0	+2	dB	Gain=-20dB to +20dB f=10kHz		
	Input Impedance	RIN_M	19	27	35	kΩ			
ð	Maximum Input Voltage	VIM_M	2.0	2.2	-	Vrms	V _{IM} at THD+N(V _{OUT})=1% BW=400Hz-30KHz		
MIXING	Maximum Attenuation *	GMX_MIN	-	-100	-85	dB	MIX=OFF Gмx=20log(V _{OUT} /VіN) BW=INF-A		
	Maximum Gain	Gмх_мах	5	7	9	dB	ATT=+7dB G _{MX} =20log(V _{OUT} /V _{IN})		

Electrical Characteristics - continued

BLOCK	Parameter	Symbol	Limit			Unit	Conditions
BLC	Parameter	Symbol	Min	Тур	Max	Unit	Conditions
	Maximum Boost Gain	G _{F_BST}	13	15	17	dB	Fader=15dB V _{IN} =100mVrms G _F =20log(V _{OUT} /V _{IN})
SUBWOOFER	Maximum Attenuation *	GF_MIN	-	-100	-90	dB	$\label{eq:GF} \begin{array}{l} Fader = -\infty dB \\ G_F = 20 log(V_OUT/V_IN) \\ BW = IHF-A \end{array}$
BWG	Gain Set Error	Gf_err	-2	0	+2	dB	GAIN=+1dB to +15dB
/ SU	Attenuation Set Error 1	GF_err1	-2	0	+2	dB	ATT=-1dB to -15dB
FADER	Attenuation Set Error 2	Gf_err2	-3	0	+3	dB	ATT=-16dB to -47dB
FAD	Attenuation Set Error 3	G _{F_ERR3}	-4	0	+4	dB	ATT=-48dB to -79dB
	Output Impedance	Rout	-	-	50	Ω	V _{IN} =100mVrms
	Maximum Output Voltage	V _{ом}	2	2.2	-	Vrms	THD+N=1% BW=400Hz-30KHz

VP-9690A(Average value detection, effective value display) filter by Matsushita Communication is used for * measurement. Phase between input / output is same.

Typical Performance Curves

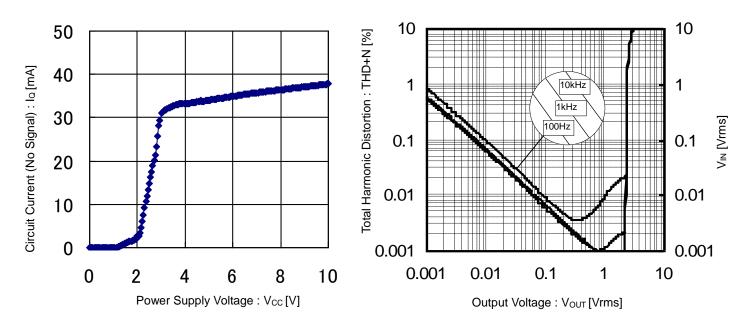


Figure 1. Circuit Current (No Signal) vs Power Supply Voltage

Figure 2. Total Harmonic Distortion vs Output Voltage

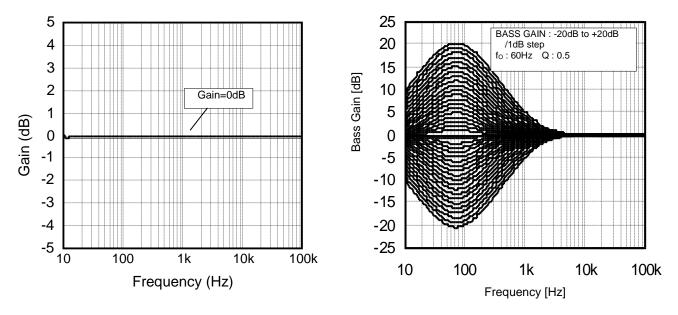


Figure 3. Gain vs Frequency

Figure 4. Bass Gain vs Frequency

Typical Performance Curves – continued

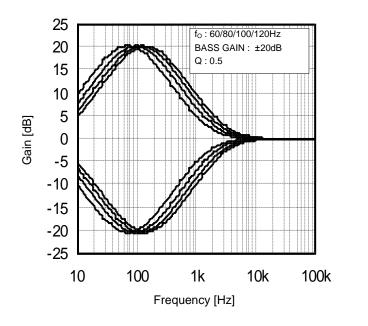
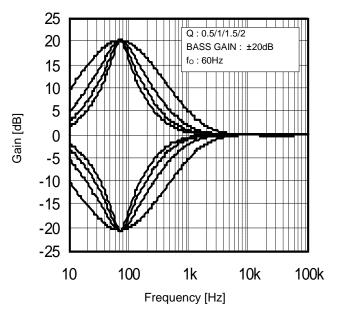
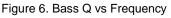


Figure 5. Bass fo vs Frequency





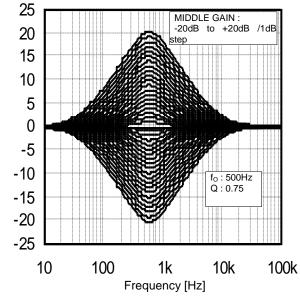


Figure 7. Middle Gain vs Frequency

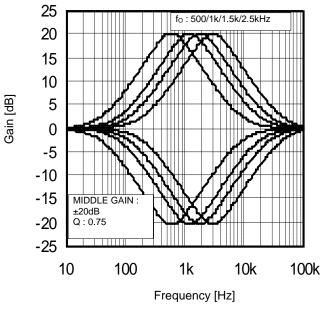
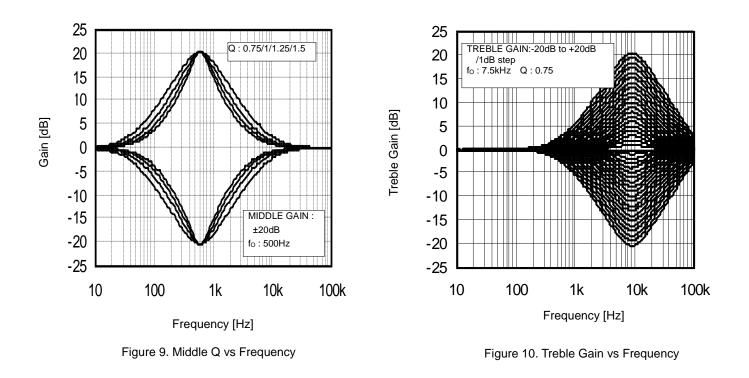


Figure 8. Middle fo vs Frequency

Middle Gain [dB]

Typical Performance Curves – continued



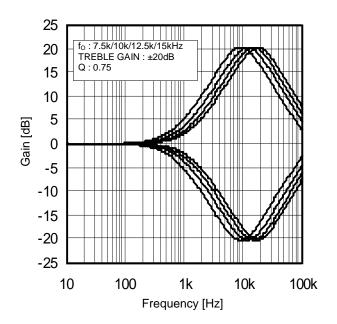


Figure 11. Treble fo vs Frequency

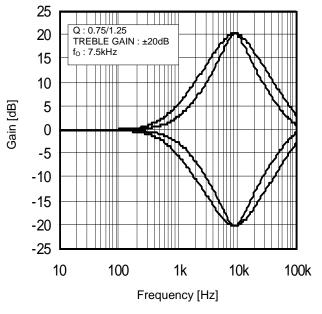


Figure 12. Treble Q vs Frequency

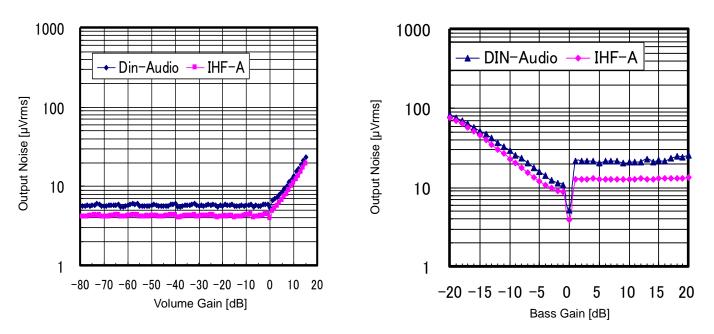
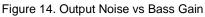


Figure 13. Output Noise vs Volume Gain

Figure 15. Output Noise vs Middle Gain



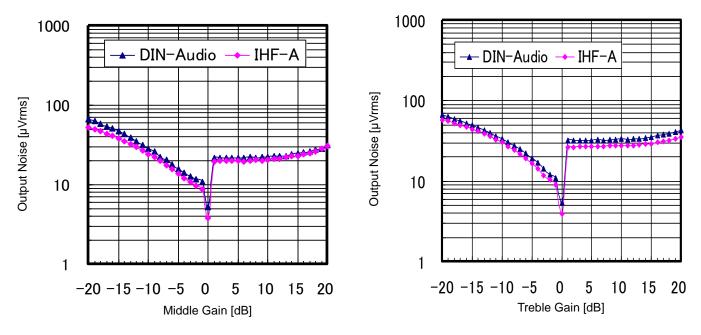


Figure 16. Output Noise vs Treble Gain

Typical Performance Curves – continued

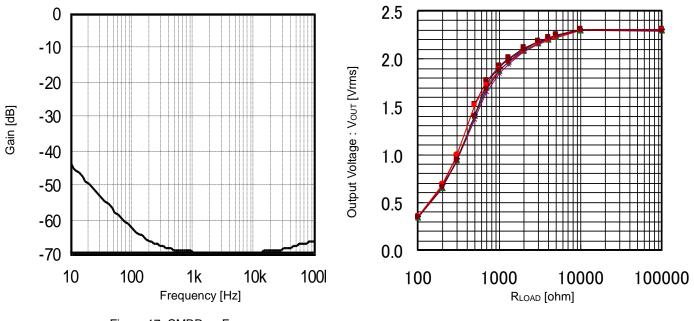
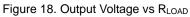


Figure 17. CMRR vs Frequency



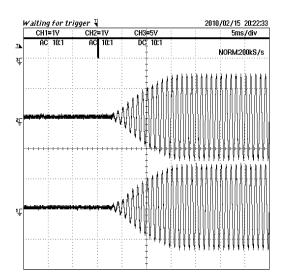


Figure 19. Advanced Switch 1

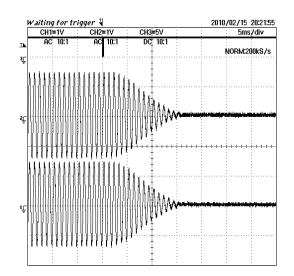


Figure 20. Advanced Switch 2

Timing Chart CONTROL SIGNAL SPECIFICATION

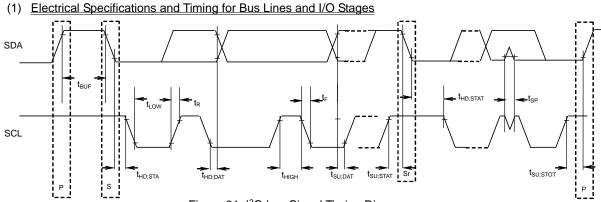


Figure 21. I²C-bus Signal Timing Diagram

Table 1	Characteristics of the	SDA and SCL bus lines for	r I ² C-bus devices (Ta=25°C, V _C	c=8.5V)
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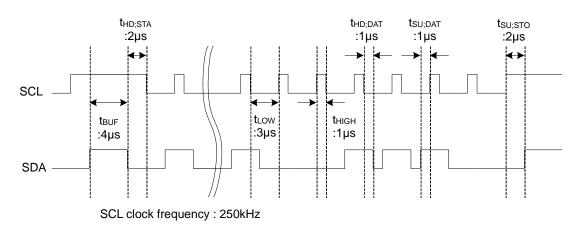
	Parameter	Symbol	Fast-mode	Unit	
	Falalletel	Symbol	Min	Max	Unit
1	SCL clock frequency	fscL	0	400	kHz
2	Bus free time between a STOP and START condition	t BUF	1.3	-	μS
3	Hold time (repeated) START condition. After this period, the first clock	t _{HD:STA}	0.0		
3	pulse is generated		0.6	-	μS
4	LOW period of the SCL clock	tLOW	1.3	-	μS
5	HIGH period of the SCL clock	tнigн	0.6	-	μS
6	Set-up time for a repeated START condition	t _{SU;STA}	0.6	-	μS
7	Data hold time:	thd;dat	0.06 (Note)	-	μS
8	Data set-up time	tsu;dat	120	-	ns
9	Set-up time for STOP condition	t _{su;sтo}	0.6	-	μS

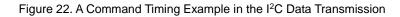
All values refer to VIH Min and VIL Max Levels (see Table 2).

(Note) A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the VIH Min of the SCL signal) in order to bridge the undefined region of the falling edge of SCL. For 7(tHD;DAT), 8(tsu;DAT), make the setup in which the margin is full.

Table 2 Characteristics of the SDA and SCL I/O stages for I²C-bus devices

	Parameter	Symbol	Fast-mode	Unit	
	Falamelei	Symbol	Min	Max	Unit
10	LOW level input voltage:	VIL	-0.3	+1	V
11	HIGH level input voltage:	Vін	2.3	5	V
12	Pulse width of spikes which must be suppressed by the input filter.	t _{SP}	0	50	ns
13	LOW level output voltage: at 3mA sink current	Vol1	0	0.4	V
14	Input current each I/O pin with an input voltage between 0.4V and 4.5V.	h	-10	+10	μA





(2) <u>I²C BUS FORMAT</u>

	MSB LSB	MSB	LSB	MSB	LSB			
S	Slave Address	A Select	Address A	Data	А	Р		
1bit	8bit		8bit 1bit	8bit	1bit	1bit		
	S	= Start condition	n (Recognition of	start bit)				
	Slave Address = Recognition of slave address. The first 7 bits correspond to the slave address.							
		The least sign	ificant bit is "L" w	hich corresponds	to write mode	э.		
	А	= ACKNOWLED	OGE bit (Recognit	ion of acknowled	gement)			
	Select Address = Select address corresponding to volume, bass or treble.							
	Data = Data on every volume and tone.							
	Р	= Stop condition	(Recognition of	stop bit)				

(3) <u>I²C BUS Interface Protocol</u>

(a)	Basic Format									
S	Slave Addre	ess	Α	Select A	ddress	Α	Da	ta	Α	Ρ
	MSB	LSB		MSB	LSB	Ν	/ISB	LSE	3	

(b) Automatic Increment (Select Address increases (+1) according to the number of data.)

	S	Slave A	Address	А	Select A	ddress	А	Data	a1	А	Data2	А		DataN	А	Ρ
	1	MSB	LSE	3	MSB	LSE	3 1	MSB	LSE	3	MSB	LS	В	MSB	LS	В
((Exar	nple)														

Data1 shall be set as data of address specified by Select Address.
 Data2 shall be set as data of address specified by Select Address +1.

③ DataN shall be set as data of address specified by Select Address +N-1.

(c) Configuration Unavailable for Transmission (In this case, only Select Address1 is set.)

 S
 Slave Address
 A
 Select Address1
 A
 Data
 A
 Select Address1
 Select Address1
 A
 Select Address1
 A
 Select Address1
 Select Address1

S	SI	ave Address	Α	Select Ad	dress1	А	Data	a	А	Select	Addres	ss 2	А	Dat	ta	А	Ρ
Ν	/ISB	LS	βB	MSB	LSB		MSB	LS	В	MSB		LSB	N	ISB	LS	В	
		(Note) If any	data	a is transmit	ted as Se	elec	ct Addı	ress	; 2 r	next to da	ata, it is	s reco	gni	zed			
		as d	ata,	not as Sele	ct Addres	ss 2	2.										

(4) Slave Address

Ν	MSB							LSB	
	A6	A5	A4	A3	A2	A1	A0	R/W	
	1	0	0	0	0	0	0	0	80H

(5) Select Address & Data

Itomo	Select Address	MSB			Da	ata			LSB		
Items	(hex)	D7	D6	D5	D4	D3	D2	D1	D0		
Initial setup 1	01	Advanced switch ON/OFF	0	Input Gai Tone/Fader	witch time of n/Volume /Super Bass ting	0	1		switch time Aute		
Initial setup 2	02	LPF Phase	0		er Output lect	0	Su	ibwoofer LP	F f _C		
Initial setup 3	03	Front HPF Pass	Rear HPF Pass	Fro	nt / Rear HP	PF f _C	0 1 0				
Input Selector	05	Full-diff Type	0	0			Input selecto	or			
Input gain	06	Mute ON/OFF	0	0		Input Gain					
Volume gain	20		-	١	/olume Gain	/ Attenuatio	n				
Fader 1ch Front	28		Fader Gain / Attenuation								
Fader 2ch Front	29	Fader Gain / Attenuation									
Fader 1ch Rear	2A				Fader Gain	/ Attenuatio	า				
Fader 2ch Rear	2B				Fader Gain	/ Attenuatio	า				
Fader Subwoofer	2C				Fader Gain	/ Attenuatio	า				
Mixing	30				Mixing Gain	/ Attenuatio	n				
Bass setup	41	0	0	Bas	s fo	0	0	Bas	ss Q		
Middle setup	44	0	0	Mido	lle fo	0	0	Mide	dle Q		
Treble setup	47	0	0	Treb	le fo	0	0	0	Treble Q		
Bass gain	51	Bass Boost/ Cut	0	0			Bass Gain				
Middle gain	54	Middle Boost/ Cut	0	0 0 Middle Gain							
Treble gain	57	Treble Boost/ Cut	0	0			Treble Gain	l			
Super Bass Gain	75	0	0	0		Si	uper Bass G	ain			
System Reset	FE	1	0	0	0	0	0	0	1		

Advanced switch

Note

- 1. The Advanced Switch works in the latch part while changing from one function to another.
- 2. Upon continuous data transfer, the Select Address rolls over because of the automatic increment function, as shown below.

$$\rightarrow 01 \rightarrow 02 \rightarrow 03 \rightarrow 05 \rightarrow 06 \rightarrow 20 \rightarrow 28 \rightarrow 29 \rightarrow 2A \rightarrow 2B \rightarrow 2C$$

$$\rightarrow 30 \rightarrow 41 \rightarrow 44 \rightarrow 47 \rightarrow 51 \rightarrow 54 \rightarrow 57 \rightarrow 75$$

- 3. Advanced switch is not used for the function of input selector and subwoofer output select, etc. Therefore, please apply mute on the side when changing these settings.
- 4. When using mute function of this IC at the time of changing input selector, please switch mute ON/OFF for waiting advanced-mute time.

|--|

Time	MSB	Advanced switch time of Mute							
TIIIIC	D7	D6	D5	D4	D3	D2	D1	D0	
0.6msec	Advonced		Advanced	switch time			0	0	
1.0msec	Advanced Switch	0	of Input ga	ain/Volume	0	1	0	1	
1.4msec	ON/OFF	0		ler/Super	0	1	1	0	
3.2msec	UN/OFF		Bass/	Mixing			1	1	

Time	MSB	Super Bass/Mixing											
	D7	D6	D5	D4	D3	D2	D1	D0					
4.7 msec	Advonced		0	0									
7.1 msec	Advanced Switch	0	0	1	0	1	Advanced switch						
11.2 msec	ON/OFF	0	1	0	U	I	Time	of Mute					
14.4 msec			1	1									

Mode	MSB		Advan	ced s	witch (ON/OF	F	LSB
Mode	D7	D6	D5	D4	D3	D2	D1	D0
OFF	0	0	of Input ga	switch time ain/Volume	0	1		ed switch
ON	1	Ū		ler/Super Mixing	0	-	Time o	of Mute

Select address 02(hex)

fa	MSB		Su	bwoot	fer LP	F fc		LSB			
fc	D7	D6	D5	D4	D3	D2	D1	D0			
OFF						0	0	0			
55Hz						0	0	1			
85Hz	LPF	0	Subwoof	er Output	0	0	1	0			
120Hz	Phase	0	Se	lect	0	0	1	1			
160Hz						1	0	0			
Prohibition						(Other setting	g			

Mode	MSB	:	Subwo	oofer (Dutput	Selec	ct	LSB
Mode	D7	D6	D5	D4	D3	D2	D1	D0
LPF			0	0				•
Front	LPF	0	0	1		Subwoofer LPF f_{C}		
Rear	Phase	0	1	0	0			
Prohibition			1	1				

Phase	MSB				LSB			
Flidse	D7	D6	D5	D4	D3	D2	D1	D0
0°	0	0	Subwoof	er output	0	S.,	bwoofer LPI	= fo
180°	1	0	sel	lect	0	Su		

Select address 03(hex)

Mode	MSB		Fro	nt/Rea	ar HPI	F fc	LSB	
Mode	D7	D6	D5	D4	D3	D2	D1	D0
55Hz			0	0	0			
85Hz	Front	Rear	0	0	1			
120Hz	HPF	HPF	1	1	0	0	1	0
160Hz	Pass	Pass	0	1	0			
Prohibition			(Other setting	9			

Mode	MSB	MSB Rear HPF							
iviode	D7	D6	D5	D4	D3	D2	D1	D0	
pass	Front	0	F ₁		- 4	0		0	
NOT pass	HPF Pass	1	Fro	ont/Rear HPI	F TC	0	1	0	

Mode	MSB			Front		LSB		
Mode	D7	D6	D5	D4	D3	D2	D1	D0
pass	0	Rear	Г		- 4	0 1	4	0
NOT pass	1	HPF Pass	Front/Rear HPF fc 0 1					U

Select address 05(hex)

Mode			MSB		In	put S	electo	or		LSB								
wode	OUTF1	OUTF2	D7	D6	D5	D4	D3	D2	D1	D0								
Α	A1	A2				0	0	0	0	0								
В	B1	B2				0	0	0	0	1								
С	C1	C2				0	0	0	1	0								
D single	DP1	DP2	Full- diff bias			0	0	0	1	1								
E single	EP1	EP2		0		0	0	1	0	0								
A diff	A1	B1			0	0	1	1	1	1								
C diff	B2	C2	type select			1	0	0	0	0								
D diff	DP1	DP2	361601			0	0	1	1	0								
E diff	EP1	EP2												0	0	1	1	1
Inp	out SHOR	RΤ.				0	1	0	0	1								
P	Prohibitior	1					C	ther setting	g									

Input SHORT : The input impedance of each input terminal is lowered from $100k\Omega(Typ)$ to $6 k\Omega(Typ)$. (For quick charge of coupling capacitor)

BD37544FS

201000	address 05(hex)	MSB	F		f Bias	Туре	Selec	t	LSB
	Mode	D7	D6	D5	D4	D3	D2	D1	D0
	Negative Input	0	0	0			nput Selecto	or	
	Bias	1	-	-		-		-	
	Negative input typ	be		1ch 1ch signal inp	out	▶ ‡+	EP1	1ch	
	For Ground –isola	ation type.				И+	EN1	Different	ial
							EN2		
					-	<u>↓</u> <u> </u> +	-12	2ch	
				2ch 2ch signal inp	-	,, ▶[]+	EP2 13	Different	ial
	Bias type						EP1		
	For differential am	nplifier type				▶+	-10	1ch	
				1ch 1ch signal input	\sim	. 141	EN1	Differen	tial
						►	EN2		
				2ch	V	► И	EP2	2ch Differen	tial
				2ch signal input		▶∄⁺	13	-	

Select address 06 (hex)

Gain	MSB		-	Inpu	it Gair	<u>ו</u>		LSB	
Gain	D7	D6	D5	D4	D3	D2	D1	D0	
0dB				0	0	0	0	0	
1dB				0	0	0	0	1	
2dB				0	0	0	1	0	
3dB				0	0	0	1	1	
4dB				0	0	1	0	0	
5dB				0	0	1	0	1	
6dB				0	0	1	1	0	
7dB				0	0	1	1	1	
8dB				0	1	0	0	0	
9dB			0		0	1	0	0	1
10dB				0	1	0	1	0	
11dB	Mute	0		0	1	0	1	1	
12dB	ON/OFF			0	1	1	0	0	
13dB				0	1	1	0	1	
14dB				0	1	1	1	0	
15dB				0	1	1	1	1	
16dB				1	0	0	0	0	
17dB				1	0	0	0	1	
18dB				1	0	0	1	0	
19dB				1	0	0	1	1	
20dB				1	0	1	0	0	
				1	1	0	1	1	
Prohibition								:	
				. 1	. 1	1	. 1	. 1	

: Initial condition

Г

Select address 06 (hex)

Mode	MSB	3 Mute ON/OFF LS								
Wode	D7	D6	D5	D4	D3	D2	D1	D0		
OFF	0	0	0			Innut Cain				
ON	1	0	0	Input Gain						

Select address 20, 28, 29, 2A, 2B, 2C (hex)

Gain & ATT	MSB	Vo	I, Fad	er Gai	n / Att	enuati	ion	LSB
Gain & ATT	D7	D6	D5	D4	D3	D2	D1	D0
	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	1
Prohibition	:	:	:	:	:	:	:	:
	0	1	1	1	0	0	0	0
15dB	0	1	1	1	0	0	0	1
14dB	0	1	1	1	0	0	1	0
13dB	0	1	1	1	0	0	1	1
:	:	:	:	:	:	:	:	:
-77dB	1	1	0	0	1	1	0	1
-78dB	1	1	0	0	1	1	1	0
-79dB	1	1	0	0	1	1	1	1
	1	1	0	1	0	0	0	0
Prohibition	:	:	:	:	:	:	:	:
	1	1	1	1	1	1	1	0
-∞dB	1	1	1	1	1	1	1	1

Select address 30(hex)

Gain & ATT	MSB	Г	Mixing	Gain	/ Atter	nuation	า	LSB
Gain & ATT	D7	D6	D5	D4	D3	D2	D1	D0
	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	1
Prohibition	:	:	:	:	:	:	:	:
	0	1	1	1	1	0	0	0
7dB	0	1	1	1	1	0	0	1
6dB	0	1	1	1	1	0	1	0
5dB	0	1	1	1	1	0	1	1
:	:	:	:	:	:	:	:	:
-77dB	1	1	0	0	1	1	0	1
-78dB	1	1	0	0	1	1	1	0
-79dB	1	1	0	0	1	1	1	1
	1	1	0	1	0	0	0	0
Prohibition	:	:	:	:	:	:	:	:
·	1	1	1	1	1	1	1	0
MIX OFF	1	1	1	1	1	1	1	1

(Note) See the precaution on P30 together, too.

Select address 41(hex)

Q factor	MSB		В	Bass		Q factor		LSB
QTACION	D7	D6	D5	D4	D3	D2	D1	D0
0.5							0	0
1.0	0	0	Por	o f	0	0	0	1
1.5	0	0	Das	ss f _O			1	0
2.0							1	1

fa	MSB			Bass f _o					
10	D7	D6	D5	D4	D3	D2	D1	D0	
60Hz			0	0					
80Hz		0	0	1	0	0	Bass Q factor		
100Hz	0		1	0	0	0			
120Hz			1	1					

Select address 44(hex)

Q factor	MSB		Mi	Middle		Q factor		LSB
QTACION	D7	D6	D5	D4	D3	D2	D1	D0
0.75							0	0
1.0	0	0	Middle fo		0	0	0	1
1.25	U						1	0
1.5							1	1

fo	MSB			Midd	LSB			
10	D7	D6	D5	D4	D3	D2	D1	D0
500Hz			0	0	0	0	Middle Q factor	
1kHz	0	0	0	1				
1.5kHz			1	0		0		
2.5kHz			1	1				

Select address 47 (hex)

Q factor	MSB		Т	ctor		LSB		
QTACION	D7	D6	D5	D4	D3	D2	D1	D0
0.75	0	0	Troh	lo fe	0	0	0	0
1.25	0	0	Trec	ole fo	0	0	0	1

fo	MSB			Treble fo					
TO	D7	D6	D5	D4	D3	D2	D1	D0	
7.5kHz			0	0					
10kHz		0	0	1	0	0	0	Treble	
12.5kHz	0	0	1	0	0	0	0	Q factor	
15kHz			1	1					

Cain	MSB		Bass/I	Middle	e/Trebl	e Gaiı	n	LSE
Gain	D7	D6	D5	D4	D3	D2	D1	D0
0dB				0	0	0	0	0
1dB				0	0	0	0	1
2dB				0	0	0	1	0
3dB				0	0	0	1	1
4dB				0	0	1	0	0
5dB				0	0	1	0	1
6dB				0	0	1	1	0
7dB				0	0	1	1	1
8dB				0	1	0	0	0
9dB				0	1	0	0	1
10dB	Bass/			0	1	0	1	0
11dB	Middle/			0	1	0	1	1
12dB	Treble	0	0	0	1	1	0	0
13dB	Boost	Ū.	C C	0	1	1	0	1
14dB	/cut			0	1	1	1	0
15dB				0	1	1	1	1
16dB				1	0	0	0	0
17dB				1	0	0	0	1
18dB				1	0	0	1	0
19dB				1	0	0	1	1
20dB				1	0	1	0	0
				1	0	1	0	1
Prohibition				:	:	:	:	:
TOTIDITION				1	1	1	1	0
				1	1	1	1	1

Mode	MSB	SB Bass/Middle/Treble Boost/Cut							
woue	D7	D6	D5	D4	D3	D2	D1	D0	
Boost	0	0	0	Bass/Middle/Treble Gain		a Cain			
Cut	1	0	0		Da55/1		e Gain		

Gain	MSB		Su	iper B	ass G	ain		LSE
Gain	D7	D6	D5	D4	D3	D2	D1	D0
0dB				0	0	0	0	0
1dB				0	0	0	0	1
2dB				0	0	0	1	0
3dB				0	0	0	1	1
4dB				0	0	1	0	0
5dB				0	0	1	0	1
6dB				0	0	1	1	0
7dB				0	0	1	1	1
8dB				0	1	0	0	0
9dB				0	1	0	0	1
10dB				0	1	0	1	0
11dB		-	_	0	1	0	1	1
12dB	0	0	0	0	1	1	0	0
13dB				0	1	1	0	1
14dB				0	1	1	1	0
15dB				0	1	1	1	1
16dB				1	0	0	0	0
17dB				1	0	0	0	1
18dB				1	0	0	1	0
19dB				1	0	0	1	1
20dB				1	0	1	0	0
				1	0	1	0	1
Prohibition				:	:	:	:	:
				1	1	1	1	1

(Note) About Super Bass, the above Gain is for in indication purposes. Actual Gain (=20log (V_{OUT}/V_{IN})) is different. Refer to P31 to P34 for the details.

: Initial condition

(6) About Power ON Reset

Built-in IC initialization is made during power ON of the supply voltage. Please send initial data to all addresses at supply voltage on. And please turn ON mute until this initial data is sent.

Parameter	Symbol		Limit		Unit	Conditions		
Falameter	Symbol	Min	Тур	Max	Unit			
Rise Time of VCC	trise	33	-	-	µsec	V_{CC} rise time from 0V to 5V		
VCC Voltage of Release Power ON Reset	Vpor	-	4.1	-	V			

Application Information

1. Function and Specifications

Function and Specifica	Specifications										
	Stereo input										
	Single-End/Differential										
	(Possible to set the number of single-end/ differential as follows)										
Input selector	Single-End Differential										
	Mode 1 0 4 Mode 2 1 3										
	Mode 3 3 2										
	Mode 4 4 1										
	Mode 5 5 0 Table.1 Combination of input selector										
	+20dB to 0dB (1dB step)										
Input gain	Possible to use "Advanced switch" for prevention of switching noise.										
Mute	Possible to use "Advanced switch" for prevention of switching noise.										
Volume	 +15dB to -79dB (1dB step), -∞dB 										
volume	Possible to use "Advanced switch" for prevention of switching noise.										
	• +20dB to -20dB (1dB step)										
Bass	· Q=0.5, 1, 1.5, 2										
Duss	• f ₀ =60, 80, 100, 120Hz										
	 Possible to use "Advanced switch" for prevention of switching noise. 										
	+20dB to -20dB (1dB step)										
Middle	· Q=0.75, 1, 1.25, 1.5										
	• f ₀ =500, 1k, 1.5k 2.5kHz										
	Possible to use "Advanced switch" for prevention of switching noise.										
	 +20dB to -20dB (1dB step) 										
Treble	• Q=0.75, 1.25										
	• f ₀ =7.5k, 10k, 12.5k, 15kHz										
	Possible to use "Advanced switch" for prevention of switching noise.										
Fader	 +15dB to -79dB(1dB step), -∞dB 										
	Possible to use "Advanced switch" for prevention of switching noise.										
LPF	• fc=55/85/120/160Hz, pass										
	Phase shift (0°/180°)										
HPF	• fc=55/85/120/160Hz, pass										
	Monaural input										
Mixing	 +7dBdB to -79dB (1dB step), -∞dB 										
	Possible to use "Advanced switch" for prevention of switching noise.										
Super Bass	 +20dB to 0dB (1dB step) 										
	Possible to use "Advanced switch" for prevention of switching noise.										

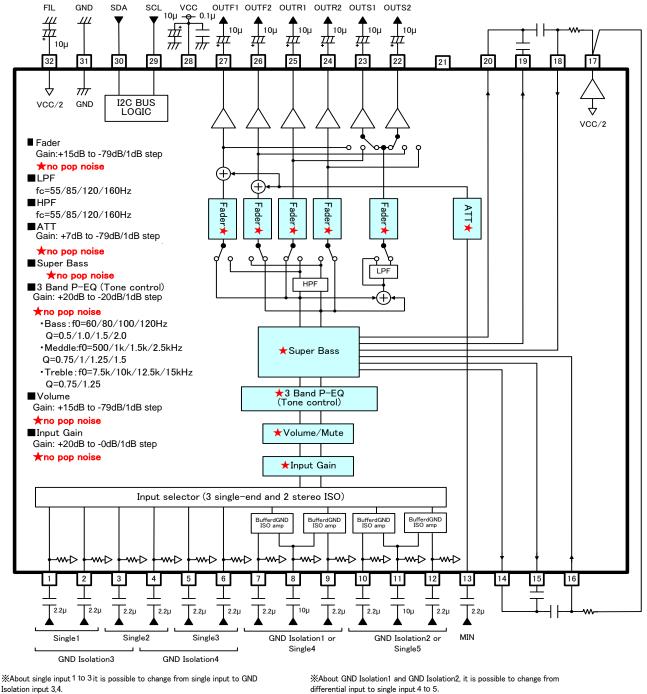
2. Volume / Fader Volume / Mixing ATT Attenuation Data

(dB)	D7	D6	D5	D4	D3	D2	D1	D0	(dB)	D7	D6	D5	D4	D3	D2	D1	D0
+15	0	1	1	1	0	0	0	1	-33	1	0	1	0	0	0	0	1
+14	0	1	1	1	0	0	1	0	-34	1	0	1	0	0	0	1	0
+13	0	1	1	1	0	0	1	1	-35	1	0	1	0	0	0	1	1
+12	0	1	1	1	0	1	0	0	-36	1	0	1	0	0	1	0	0
+11	0	1	1	1	0	1	0	1	-37	1	0	1	0	0	1	0	1
+10	0	1	1	1	0	1	1	0	-38	1	0	1	0	0	1	1	0
+9	0	1	1	1	0	1	1	1	-39	1	0	1	0	0	1	1	1
+8	0	1	1	1	1	0	0	0	-40	1	0	1	0	1	0	0	0
+7	0	1	1	1	1	0	0	1	-41	1	0	1	0	1	0	0	1
+6	0	1	1	1	1	0	1	0	-42	1	0	1	0	1	0	1	0
+5	0	1	1	1	1	0	1	1	-43	1	0	1	0	1	0	1	1
+4	0	1	1	1	1	1	0	0	-44	1	0	1	0	1	1	0	0
+3	0	1	1	1	1	1	0	1	-45	1	0	1	0	1	1	0	1
+2	0	1	1	1	1	1	1	0	-46	1	0	1	0	1	1	1	0
+1	0	1	1	1	1	1	1	1	-47	1	0	1	0	1	1	1	1
0	1	0	0	0	0	0	0	0	-48	1	0	1	1	0	0	0	0
-1	1	0	0	0	0	0	0	1	-49	1	0	1	1	0	0	0	1
-2	1	0	0	0	0	0	1	0	-50	1	0	1	1	0	0	1	0
-3	1	0	0	0	0	0	1	1	-51	1	0	1	1	0	0	1	1
-4	1	0	0	0	0	1	0	0	-52	1	0	1	1	0	1	0	0
-5	1	0	0	0	0	1	0	1	-53	1	0	1	1	0	1	0	1
-6	1	0	0	0	0	1	1	0	-54	1	0	1	1	0	1	1	0
-7	1	0	0	0	0	1	1	1	-55	1	0	1	1	0	1	1	1
-8	1	0	0	0	1	0	0	0	-56	1	0	1	1	1	0	0	0
-9	1	0	0	0	1	0	0	1	-57	1	0	1	1	1	0	0	1
-10	1	0	0	0	1	0	1	0	-58	1	0	1	1	1	0	1	0
-11	1	0	0	0	1	0	1	1	-59	1	0	1	1	1	0	1	1
-12	1	0	0	0	1	1	0	0	-60	1	0	1	1	1	1	0	0
-13	1	0	0	0	1	1	0	1	-61	1	0	1	1	1	1	0	1
-14	1	0	0	0	1	1	1	0	-62	1	0	1	1	1	1	1	0
-15	1	0	0	0	1	1	1	1	-63	1	0	1	1	1	1	1	1
-16	1	0	0	1	0	0	0	0	-64	1	1	0	0	0	0	0	0
-17	1	0	0	1	0	0	0	1	-65	1	1	0	0	0	0	0	1
-18	1	0	0	1	0	0	1	0	-66	1	1	0	0	0	0	1	0
-19	1	0	0	1	0	0	1	1	-67	1	1	0	0	0	0	1	1
-20	1	0	0	1	0	1	0	0	-68	1	1	0	0	0	1	0	0
-21	1	0	0	1	0	1	0	1	-69	1	1	0	0	0	1	0	1
-22	1	0	0	1	0	1	1	0	-70	1	1	0	0	0	1	1	0
-23	1	0	0	1	0	1	1	1	-71	1	1	0	0	0	1	1	1
-24	1	0	0	1	1	0	0	0	-72	1	1	0	0	1	0	0	0
-25	1	0	0	1	1	0	0	1	-73	1	1	0	0	1	0	0	1
-26	1	0	0	1	1	0	1	0	-74	1	1	0	0	1	0	1	0
-27	1	0	0	1	1	0	1	1	-75	1	1	0	0	1	0	1	1
-28	1	0	0	1	1	1	0	0	-76	1	1	0	0	1	1	0	0
-29	1	0	0	1	1	1	0	1	-77	1	1	0	0	1	1	0	1
-30	1	0	0	1	1	1	1	0	-78	1	1	0	0	1	1	1	0
-31	1	0	0	1	1	1	1	1	-79	1	1	0	0	1	1	1	1
-32	1	0	1	0	0	0	0	0	-∞	1	1	1	1	1	1	1	1

Adjustable range of mixing ATT is +7dB to -∞dB.

: Initial condition

3. Application Circuit



3,4.

Figure 23. BD37544FS

Unit R : [Ω] C : [F]

Notes on wiring

①Please connect the decoupling capacitor of the power supply in the shortest possible distance to GND.
 ②GND lines should be one-point connected.
 ③Wiring pattern of Digital should be away from that of Analog unit and cross-talk should not be acceptable.
 ④SCL and SDA lines of I²C BUS should not be parallel if possible.

The lines should be shielded, if they are adjacent to each other.

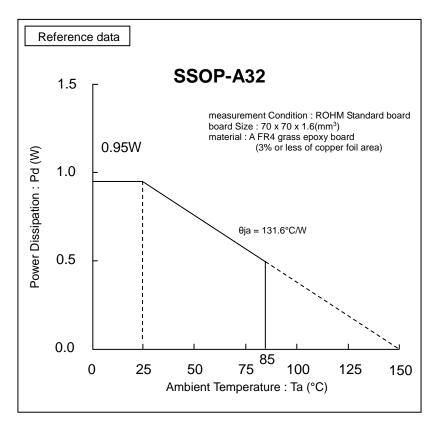
(5) Analog input lines should not be parallel if possible. The lines should be shielded, if they are adjacent.

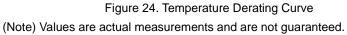
6 Please short Pins 15-16, and Pins 18-19 if the Super Bass is not used.

Power Dissipation

About the thermal design of the IC

Characteristics of an IC have a great deal to do with the temperature at which it is used, and exceeding absolute maximum ratings may degrade and destroy elements. Careful consideration must be given to the heat of the IC from the two standpoints of immediate damage and long-term reliability of operation.





Power dissipation values vary according to the board on which the IC is mounted.

I/O Equivalent Circuits

Terminal No.	Terminal Name	Terminal Voltage	Equivalent Circuit	Terminal Description
1 2 3 4 5 6	A1 A2 B1 B2 C1 C2	4.25		A terminal for signal input. The input impedance is 100kΩ(Typ).
7 8 9 10 11 12	DP1 DN DP2 EP1 EN EP2	4.25		Input terminal available to ingle/Differential mode. The input impedance is 250kΩ(Typ).
16 18	SBB1 SBB2	-		An input terminal for Super Bass
15 17 19 22 23 24 25 26 27	SBA1 SBBIAS SBA2 OUTS2 OUTS1 OUTR2 OUTR1 OUTF2 OUTF1	4.25		A terminal for Super Bass and fader, Subwoofer output.
14 20	SBC1 SBC2	4.25		An output terminal for Super Bass.

Values in the pin explanation and input/output equivalent circuit are reference values only and are not guaranteed.

I/O Equivalent Circuits - continued

Terminal No.	Terminal Name	Terminal Voltage	Equivalent Circuit	Terminal Description
28	VCC	8.5		Power supply terminal.
29	SCL	-		A terminal for clock input of I ² C BUS communication.
30	SDA	-	VCC VCC VCC VCC VCC VCC VCC VCC	A terminal for data input of I ² C BUS communication.
31	GND	0		Ground terminal.
32	FIL	4.25		1/2 VCC terminal. Voltage for reference bias of analog signal system. The simple precharge circuit and simple discharge circuit for an external capacitor are built in.
13	MIN	4.25		A terminal for signal input. The input impedance is 27kΩ(typ).

Values in the pin explanation and input/output equivalent circuit are reference values only and are not guaranteed.

Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Thermal Consideration

Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode. When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

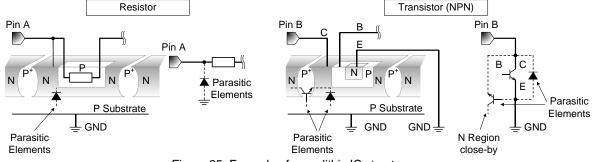
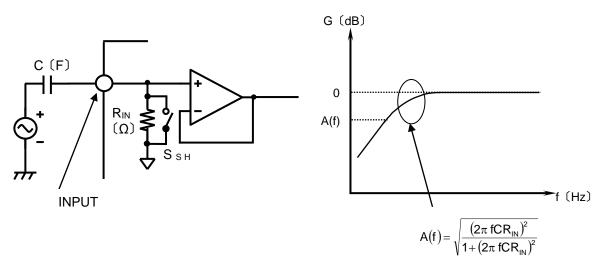


Figure 25. Example of monolithic IC structure

13. About Signal Input

(a) About Input Coupling Capacitor Constant Value

The constant value of input coupling capacitor C(F) is decided with respect to the input impedance $R_{IN}(\Omega)$ at the input signal terminal of the IC. The first HPF characteristic of RC is composed.



(b) About the Input Selector SHORT

SHORT mode is the command which makes switch S_{SH} =ON of input selector part so that the input impedance R_{IN} of all terminals becomes small. Switch S_{SH} is OFF when SHORT command is not selected. The constant time brought about by the small resistance inside and the capacitor outside the LSI becomes small when this command is used. The charge time of the capacitor becomes short. Since SHORT mode turns ON the switch of S_{SH} and makes it low impedance, please use it at no signal condition.

Operational Notes – continued

- 14. About MIX
 - (1) <u>About Specification of Fader -∞ at MIX ON.</u> Mix_signal is added to Main_signal after Fader_Gain(+15dB to -79dB) like the figure. When Fader is set at -∞, the signal after a MIX signal is added is done with MUTE because the -∞ circuit of Fader is in the step after the addition circuit

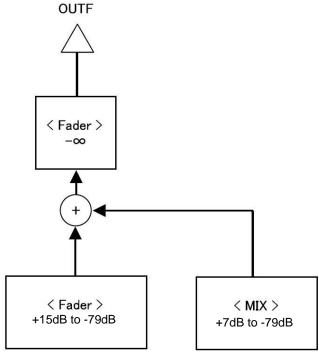
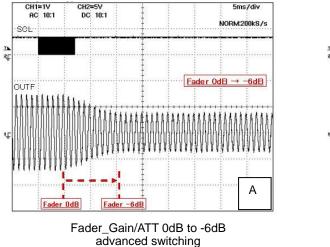
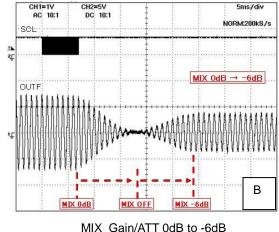


Figure 26. About Front Fader and MIX

(2) <u>About Advanced Switching of MIX_Gain/ATT</u> When advanced switching of MIX_Gain/ATT works, MIX goes a switching movement that it passes through the state of MIX_OFF like in B figure below (from current settingof MIX_Gain/ATT to MIX_OFF to a target setting of MIX_Gain/ATT).





MIX_Gain/ATT 0dB to -6dB advanced switching

Figure 27. Advanced Switching Movement when MIX_Gain/ATT is Changed

Operational Notes – continued

15. About Super Bass Circuit

The (the following Super Bass) which strengthens a low band like the graph below a can be realized by composing an external circuit with the pin 14 to 20 as shown in Figure 28.

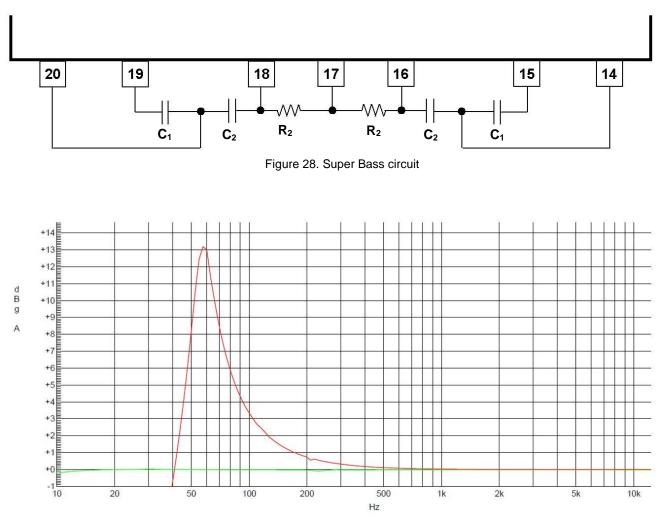
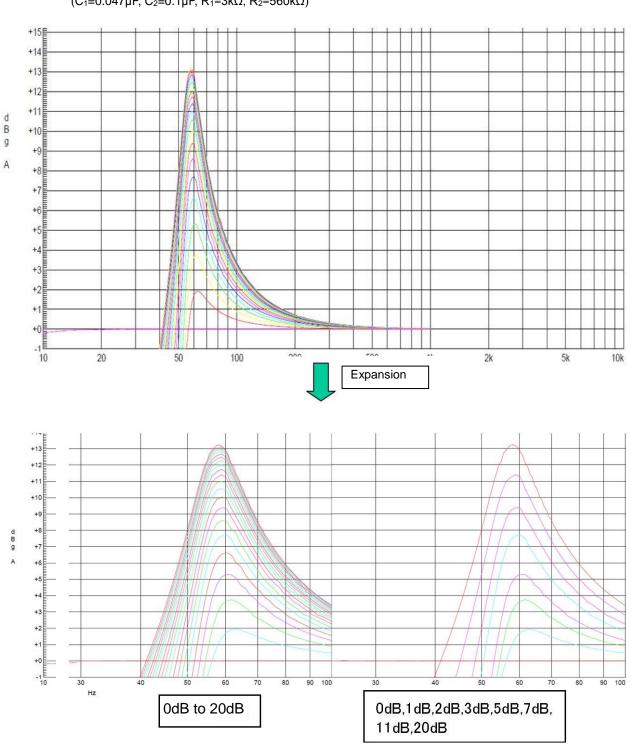


Figure 29. Super Bass Gain vs Frequency

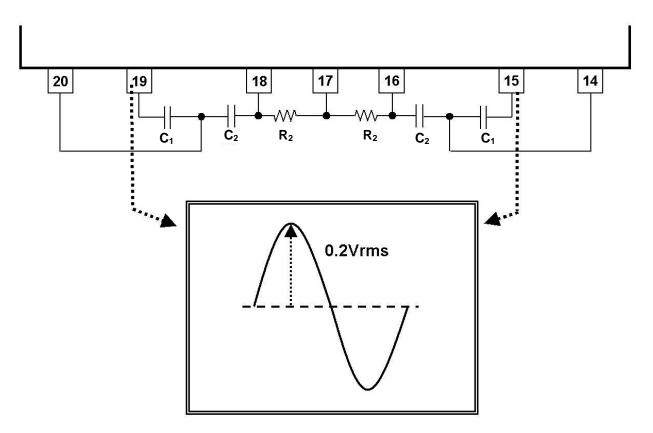


(a) <u>Gain Step Width becomes a Logarithm</u> When a setup of Gain is made 0,1,2,3,5,7,11,20dB, it becomes the following (bottom right) character. $(C_1=0.047\mu$ F, $C_2=0.1\mu$ F, $R_1=3k\Omega$, $R_2=560k\Omega$)

Figure 30. About Gain step of Super Bass

(b) You must take level diagram into consideration so that output may not do a clip

<u>Example (C₁=0.047µF, C₂=0.1µF, R₂=560kohm, V_{CC}=8.5V)</u> To prevent output clipping due to amplification when Super Bass is used, adjust the level diagram with volume until the Tone output level becomes less than 0.2Vrms.



Please adjust so that the maximum level of the Tone output becomes less than 0.2Vrms. (at Vcc=8.5V)

Figure 31. Super Bass Level Diagram

(c) About fo and Gain of Super Bass

fo and Gain of Super Bass deviates due to the deviation of the value of C_1 , C_2 , R_2 (Components with the outside), P_2 (the resistance built in |C|)

 R_1 (the resistance built in IC).

<u>Example</u> : Super Bass Gain – frequency characteristic at Dispersion condition of C_{1} , C_{2} , R_{2} ±5%, R_{1} ±30% (C_{1} =0.047 μ F, C_{2} =0.1 μ F, R_{1} =3kohm, R_{2} =560kohm, Super Bass Gain=20dB)

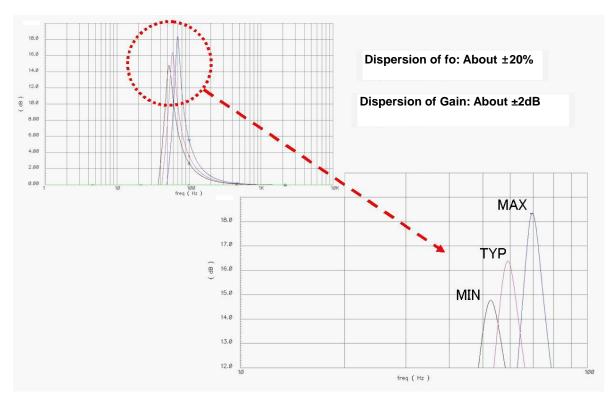
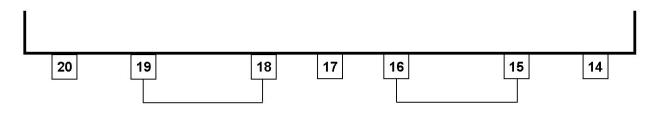


Figure 32. Dispersion of fo and Gain of Super Bass

(d) How to Deal with Pins of Super Bass when not used

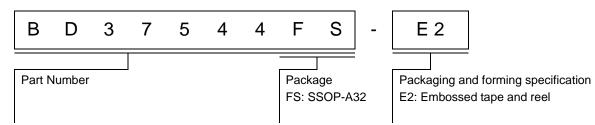
Short Pins 15 to 16, Pins 18 to 19 as shown in Figure 33 when the Super Bass function is not used.



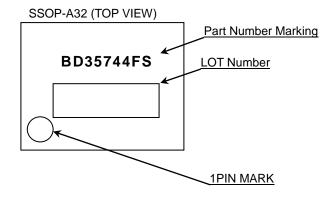
Short Pin 15 to 16, Pin 18 to 19

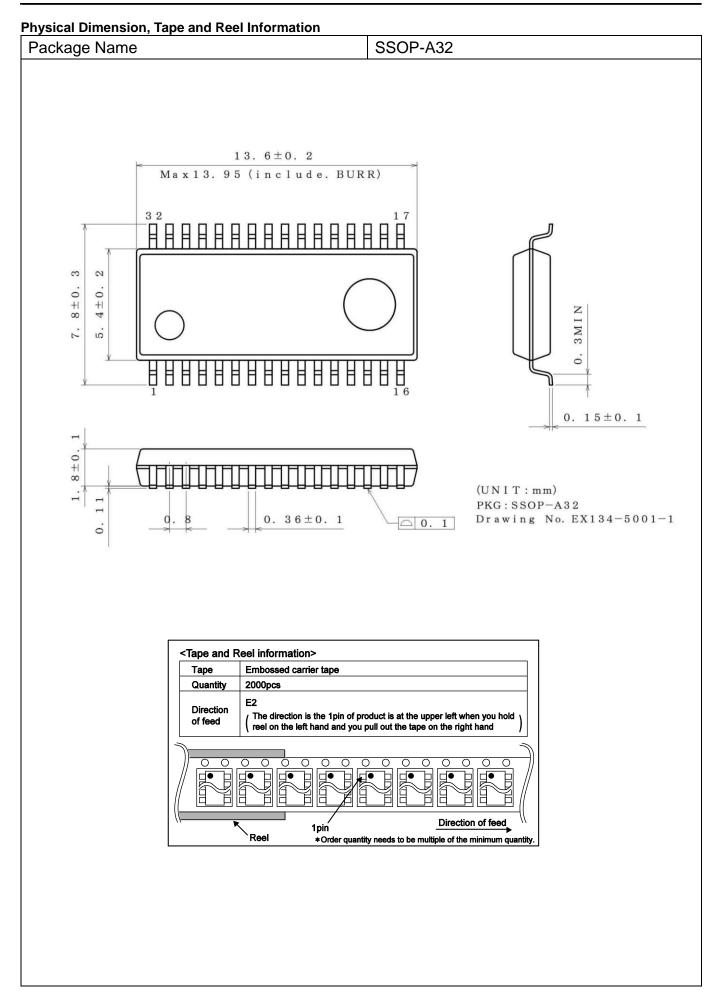
Figure 33. How to Deal with Pins of Super Bass when not used

Ordering Information



Marking Diagram





Revision History

Date	Revision	Changes
16.Dec.2015	001	New Release

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JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASS II b	CLASSI
CLASSⅣ		CLASSⅢ	

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 - [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
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- 4. The Products are not subject to radiation-proof design.
- 5. Please verify and confirm characteristics of the final or mounted products in using the Products.
- 6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
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 - [c] the Products are exposed to direct sunshine or condensation
 - [d] the Products are exposed to high Electrostatic
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