24AA52/24LCS52

2K 2.2V I^2C™ Serial EEPROM with Software Write-Protect

Device Selection Table

Part Number	Vcc Range	Max Clock Frequency	Temp Ranges
24AA52	1.8-5.5	400 kHz(1)	I
24LCS52	2.2-5.5	400 kHz	I

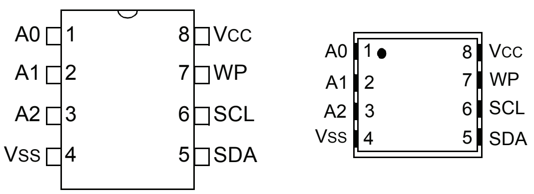
Note 1: 100 kHz for VCC <2.2V

Features:

- Single Supply with Operation Down to 1.8V
- Low-Power CMOS Technology:
  - 1 mA active current, typical
  - 1 μA standby current, typical (I-temp)
- Organized as 1 Block of 256 Bytes (256 x 8)
- Software Write Protection for Lower 128 Bytes
- Hardware Write Protection for Entire Array
- 2-Wire Serial Interface Bus, I^2C™ Compatible
- Schmitt Trigger Inputs for Noise Suppression
- Output Slope Control to Eliminate Ground Bounce
- 100 kHz (24AA52) and 400 kHz (24LCS52) Compatibility
- Self-Timed Write Cycle (including auto-erase)
- Page Write Buffer for up to 16 Bytes
- ESD Protection > 4,000V
- 1,000,000 Erase/Write Cycles
- Data Retention > 200 Years
- 8-Lead PDIP, SOIC, TSSOP, MSOP, DFN and TDFN Packages
- Pb-Free Finishes Available
- Available for Extended Temperature Ranges:
  - Industrial (I): -40°C to +85°C

Package Types

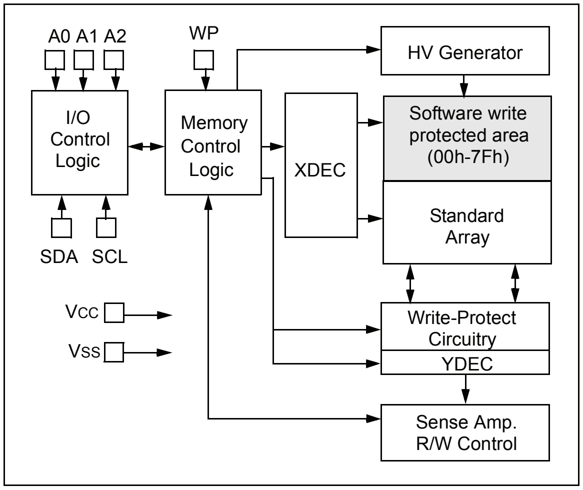
PDIP/SOIC/TSSOP/MSOP/DFN/TDFN



Description:

The Microchip Technology Inc. 24AA52/24LCS52 (24XXX52*) is a 2 Kbit Electrically Erasable PROM capable of operation across a broad voltage range (1.8V to 5.5V). This device has a software write-protect feature for the lower half of the array, as well as an external pin that can be used to write-protect the entire array. The software write-protect feature is enabled by sending the device a special command. Once this feature has been enabled, it cannot be reversed. In addition to the software protect feature, there is a WP pin that can be used to write-protect the entire array, regardless of whether the software write-protect register has been written or not. This allows the system designer to protect none, half, or all of the array, depending on the application. The device is organized as one block of 256 x 8-bit memory with a 2-wire serial interface. Low-voltage design permits operation down to 1.8V, with standby and active currents of only 1 μA and 1 mA, respectively. The 24XXX52 also has a page write capability for up to 16 bytes of data. The 24XXX52 is available in the standard 8-pin PDIP, surface mount SOIC, TSSOP, MSOP, DFN and TDFN packages.

Block Diagram



*24XXX52 is used in this document as a generic part number for the 24AA52/24LCS52 devices.

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings(†)

VCC......6.5V

All inputs and outputs w.r.t. VSS ...... -0.3V to VCC +1.0V

Storage temperature ......-65°C to +150°C

Ambient temperature with power applied......-40°C to +125°C

ESD protection on all pins ......≥ 4 kV

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

TABLE 1-1: DC SPECIFICATIONS

DC CHARACTERISTICS			VCC = +1.8V to +5.5V Industrial (I): TA = -40°C to +85°C				
Param. No.	**Symbol**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
D1	VIH	A0, A1, A2, SCL, SDA and WP pins	—	—	—	—	—
D2	—	High-level input voltage	0.7 VCC	—	—	V	—
D3	VIL	Low-level input voltage	—	—	0.3 VCC	V	0.2 VCC for VCC < 2.5V
D4	VHYS	Hysteresis of Schmitt Trigger inputs	0.05 VCC	—	—	V	**(Note)**
D5	VOL	Low-level output voltage	—	—	0.40	V	IOL = 3.0 mA, VCC = 2.5V
D6	ILI	Input leakage current	—	—	±1	µA	VIN = VSS or VCC
D7	ILO	Output leakage current	—	—	±1	µA	VOUT = VSS or VCC
D8	CIN, COUT	Pin capacitance (all inputs/outputs)	—	—	10	pF	VCC = 5.0V **(Note)** TA = 25°C, FCLK = 1 MHz
D9	ICC write	Operating current	—	1.0	3.0	mA	VCC = 5.5V, SCL = 400 kHz
D10	ICC read		—	0.20	1.0	mA	—
D11	ICCS	Standby current	— —	0.36 —	1.0 —	µA	Industrial SDA = SCL = VCC A0, A1, A2, WP = VSS

Note: This parameter is periodically sampled and not 100% tested.

TABLE 1-2: AC SPECIFICATIONS

AC CHARACTERISTICS			VCC = +1.8V to +5.5V Industrial (I): TA = -40°C to +85°C				
Param. No.	**Symbol**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
1	FCLK	Clock frequency	— —	— —	400 100	kHz	2.2V ≤ VCC ≤ 5.5V 1.8V ≤ VCC < 2.5V (24AA52)
2	THIGH	Clock high time	600 4000	— —	— —	ns	2.2V ≤ VCC ≤ 5.5V 1.8V ≤ VCC < 2.5V (24AA52)
3	TLOW	Clock low time	1300 4700	— —	— —	ns	2.2V ≤ VCC ≤ 5.5V 1.8V ≤ VCC < 2.5V (24AA52)
4	TR	SDA and SCL rise time **(Note 1)**	— —	— —	300 1000	ns	2.2V ≤ VCC ≤ 5.5V 1.8V ≤ VCC < 2.5V (24AA52)
5	TF	SDA and SCL fall time	—	— —	300	ns	**(Note 1)**
6	THD:STA	Start condition hold time	600 4000	— —	— —	ns	2.2V ≤ VCC ≤ 5.5V 1.8V ≤ VCC < 2.5V (24AA52)
7	TSU:STA	Start condition setup time	600 4700	— —	— —	ns	2.2V ≤ VCC ≤ 5.5V 1.8V ≤ VCC < 2.5V (24AA52)
8	THD:DAT	Data input hold time	0	— —	—	ns	**(Note 2)**
9	TSU:DAT	Data input setup time	100 250	— —	— —	ns	2.2V ≤ VCC ≤ 5.5V 1.8V ≤ VCC < 2.5V (24AA52)
10	TSU:STO	Stop condition setup time	600 4000	— —	— —	ns	2.2V ≤ VCC ≤ 5.5V 1.8V ≤ VCC < 2.5V (24AA52)
11	TAA	Output valid from clock **(Note 2)**	— —	— —	900 3500	ns	2.2V ≤ VCC ≤ 5.5V 1.8V ≤ VCC < 2.5V (24AA52)
12	TBUF	Bus free time: Time the bus must be free before a new transmission can start	1300 4700	— —	— —	ns	2.2V ≤ VCC ≤ 5.5V 1.8V ≤ VCC < 2.5V (24AA52)
13	TOF	Output fall time from VIH minimum to VIL maximum	20 + 0.1 CB —	— —	250 250	ns	2.2V ≤ VCC ≤ 5.5V 1.8V ≤ VCC < 2.5V (24AA52)
14	TSP	Input filter spike suppression (SDA and SCL pins)	—	—	50	ns	**(Note 1 and Note 3)**
15	TWC	Write cycle time (byte or page)	—	—	5	ms	—
16	—	Endurance	1M	—	—	cycles	25°C, VCC = 5.0V **(Note 4)**

Note 1: Not 100% tested. CB = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

3: The combined TSP and VHYS specifications are due to new Schmitt Trigger inputs, which provide improved noise spike suppression. This eliminates the need for a TI specification for standard operation.

4: This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model which can be obtained from Microchip's web site at www.microchip.com.

FIGURE 1-1: BUS TIMING DATA

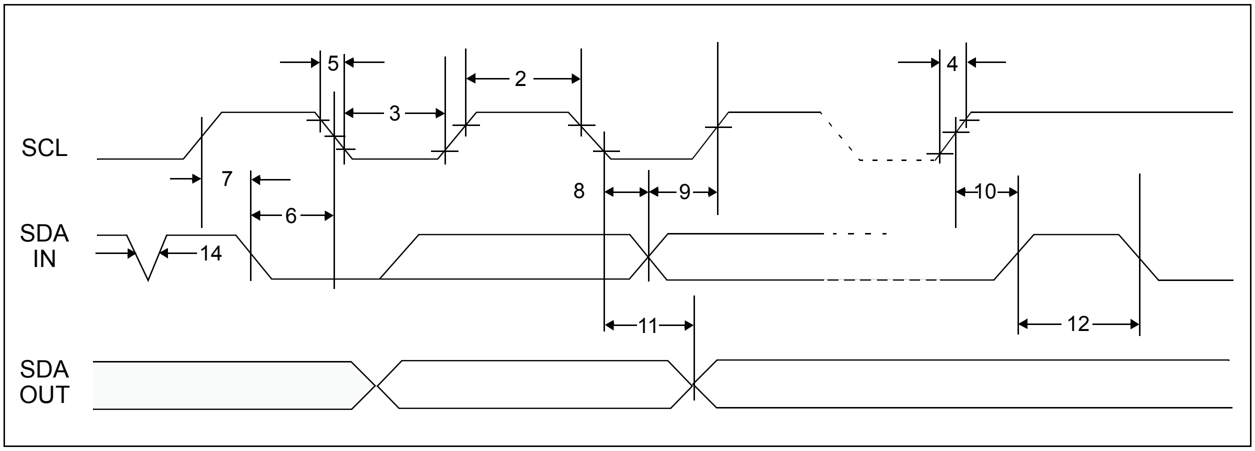
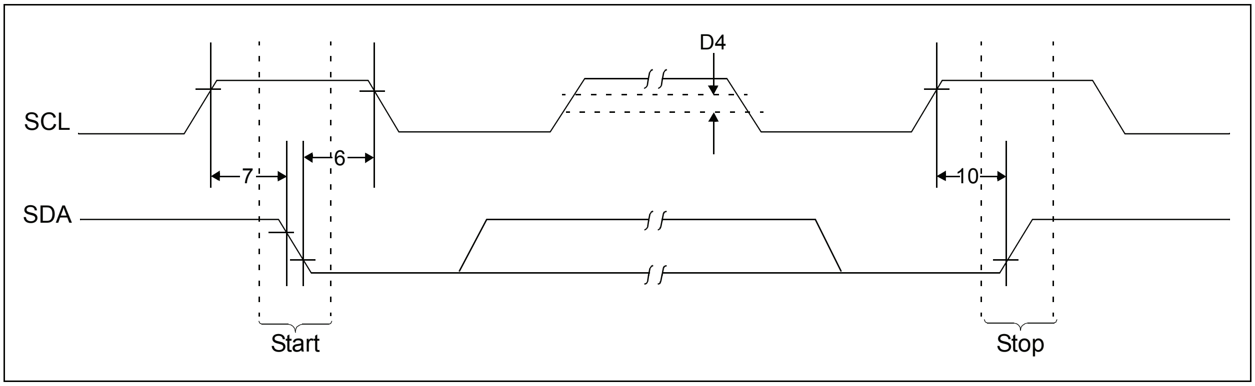


FIGURE 1-2: BUS TIMING START/STOP



2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Symbol	PDIP	SOIC	TSSOP	MSOP	DFN(1)	TDFN(1)	Description
A0	1	1	1	1	1	1	Chip Address Input
A1	2	2	2	2	2	2	Chip Address Input
A2	3	3	3	3	3	3	Chip Address Input
VSS	4	4	4	4	4	4	Ground
SDA	5	5	5	5	5	5	Serial Address/Data I/O
SCL	6	6	6	6	6	6	Serial Clock
WP	7	7	7	7	7	7	Write-Protect Input
VCC	8	8	8	8	8	8	+1.8V to 5.5V Power Supply

Note 1: The exposed pad on the DFN/TDFN packages can be connected to VSS or left floating.

2.1 A0, A1, A2

The levels on these inputs are compared with the corresponding bits in the slave address. The chip is selected if the compare is true.

Up to eight 24XXX52 devices may be connected to the same bus by using different Chip Select bit combinations. These inputs must be connected to either VSS or VCC.

2.2 Serial Address/Data Input/Output (SDA)

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open drain terminal. Therefore, the SDA bus requires a pull-up resistor to VCC (typical 10 kΩ for 100 kHz, 2 kΩ for 400 kHz).

For normal data transfer, SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the Start and Stop conditions.

2.3 Serial Clock (SCL)

This input is used to synchronize the data transfer to and from the device.

2.4 Write-Protect (WP)

This is the hardware write-protect pin. It can be tied to VCC or VSS. If tied to VCC, the hardware write protection is enabled. If the WP pin is tied to VSS, the hardware write protection is disabled.

3.0 FUNCTIONAL DESCRIPTION

The 24XXX52 supports a bidirectional 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as a transmitter, and a device receiving data, as a receiver. The bus has to be controlled by a master device, which generates the Serial Clock (SCL), controls the bus access and generates the Start and Stop conditions, while the 24XXX52 works as slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated.

4.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as a Start or Stop condition.

Accordingly, the following bus conditions have been defined (Figure 4-1).

4.1 Bus Not Busy (A)

Both data and clock lines remain high.

4.2 Start Data Transfer (B)

A high-to-low transition of the SDA line while the clock (SCL) is high determines a Start condition. All commands must be preceded by a Start condition.

4.3 Stop Data Transfer (C)

A low-to-high transition of the SDA line while the clock (SCL) is high determines a Stop condition. All operations must be ended with a Stop condition.

4.4 Data Valid (D)

The state of the data line represents valid data when, after a Start condition, the data line is stable for the duration of the high period of the clock signal.

The data on the line must be changed during the low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a Start condition and terminated with a Stop condition. The number of data bytes transferred between the Start and Stop conditions is determined by the master device and is, theoretically, unlimited; although only the last sixteen will be stored when doing a write operation. When an overwrite does occur, it will replace data in a first-in, first-out (FIFO) fashion.

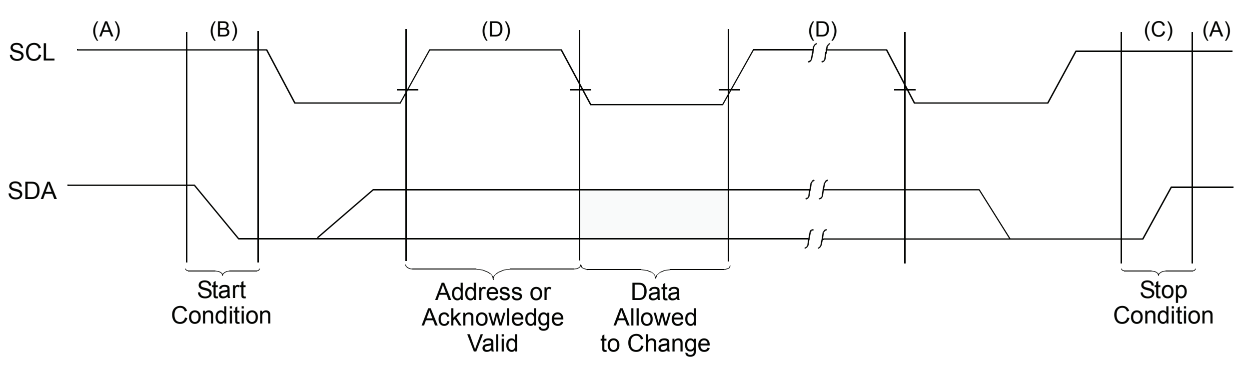
4.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an Acknowledge after the reception of each byte. The master device must generate an extra clock pulse, which is associated with this Acknowledge bit.

Note:	The 24XXX52 does not generate any Acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges has to pull down the SDA line during the Acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end-of-data to the slave by not generating an Acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (24XXX52) will leave the data line high to enable the master to generate the Stop condition.

FIGURE 4-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS



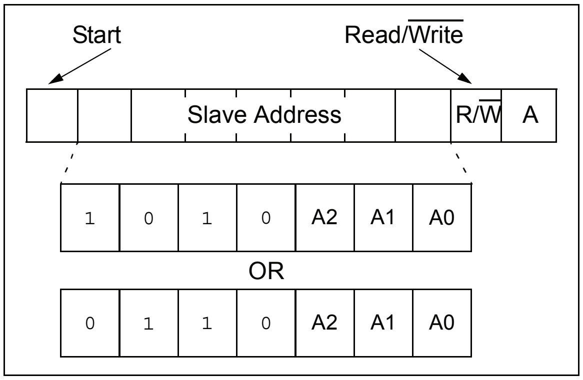
4.6 Device Addressing

A control byte is the first byte received following the Start condition from the master device. The first part of the control byte consists of a 4-bit control code which is set to ‘`1010`’ for normal read and write operations and ‘`0110`’ for writing to the write-protect register. The control byte is followed by three Chip Select bits (A2, A1, A0). The Chip Select bits allow the use of up to eight 24XXX52 devices on the same bus and are used to determine which device is accessed. The Chip Select bits in the control byte must correspond to the logic levels on the corresponding A2, A1 and A0 pins for the device to respond. The device will not acknowledge if you attempt a Read command with the control code set to ‘`0110`’.

The eighth bit of slave address determines if the master device wants to read or write to the 24XXX52 (Figure 4-2). When set to a one, a read operation is selected. When set to a zero, a write operation is selected.

Operation	Control Code	Chip Select	$R/\overline{W}$
Read	`1010`	A2 A1 A0	`1`
Write	`1010`	A2 A1 A0	`0`
Set Write-Protect Register	`0110`	A2 A1 A0	`0`

FIGURE 4-2: CONTROL BYTE ALLOCATION



5.0 WRITE OPERATIONS

5.1 Byte Write

Following the Start signal from the master, the device code (4 bits), the Chip Select bits (3 bits) and the $R/\overline{W}$ bit, which is a logic low, are placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow, once it has generated an Acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the master is the word address and will be written into the Address Pointer of the 24XXX52.

After receiving another Acknowledge signal from the 24XXX52, the master device will transmit the data word to be written into the addressed memory location. The 24XXX52 acknowledges again and the master generates a Stop condition. This initiates the internal write cycle, which means that during this time, the 24XXX52 will not generate Acknowledge signals (Figure 5-1). If an attempt is made to write to the array when the software or hardware write protection has been enabled, the device will acknowledge the command, but no data will be written. The write cycle time must be observed even if the write protection is enabled.

5.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24XXX52 in the same way as in a byte write. Instead of generating a Stop condition, the master transmits up to 15 additional data bytes to the 24XXX52, which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a Stop condition. Upon receipt of each word, the four lower order Address Pointer bits are internally incremented by one. The higher order four bits of the word address remain constant. If the master should transmit more than 16 bytes prior to generating the Stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the Stop condition is received, an internal write cycle will begin (Figure 5-2). If an attempt is made to write to the array when the hardware write protection has been enabled, the device will acknowledge the command, but no data will be written. The write cycle time must be observed even if the write protection is enabled.

Note: Page write operations are limited to writing bytes within a single physical page, regardless of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or ‘page size’) and end at addresses that are integer multiples of [page size – 1]. If a Page Write command attempts to write across a physical page boundary, the result is that the data wraps around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page, as might be expected. It is therefore necessary for the application software to prevent page write operations that would attempt to cross a page boundary.

FIGURE 5-1: BYTE WRITE

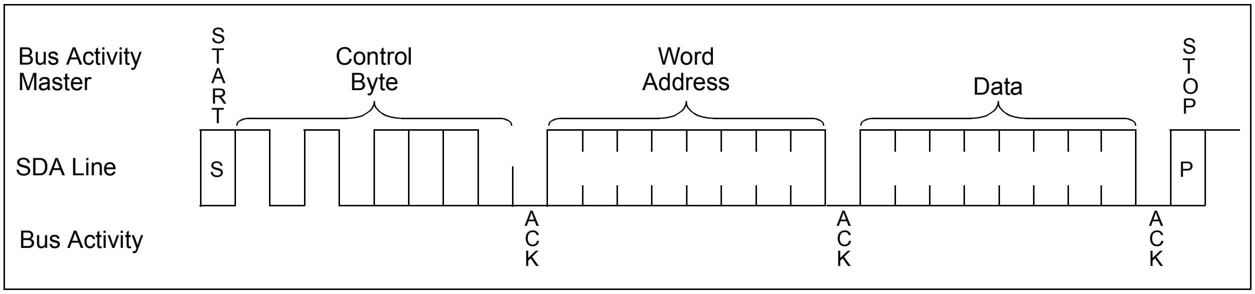
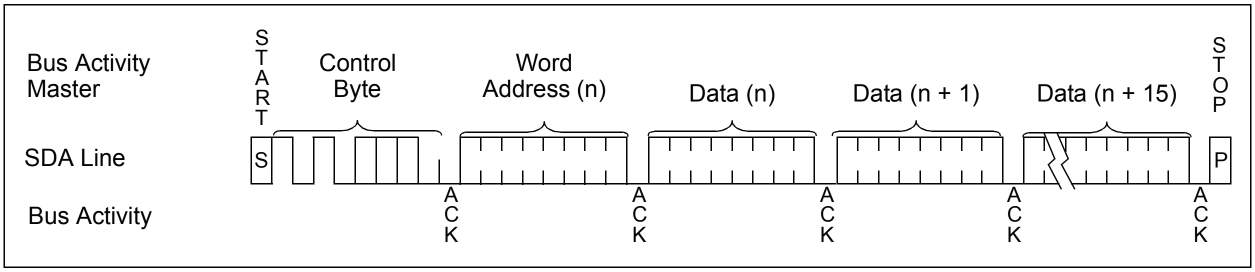


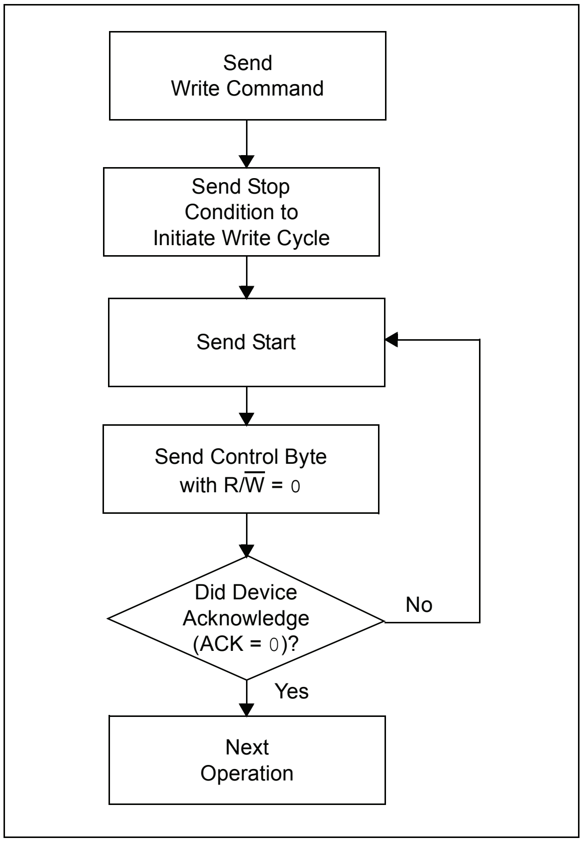
FIGURE 5-2: PAGE WRITE



6.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughput). Once the Stop condition for a Write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a Start condition followed by the control byte for a Write command ($R/\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If the cycle is complete, then the device will return the ACK and the master can then proceed with the next Read or Write command. See Figure 6-1 for flow diagram.

FIGURE 6-1: ACKNOWLEDGE POLLING FLOW



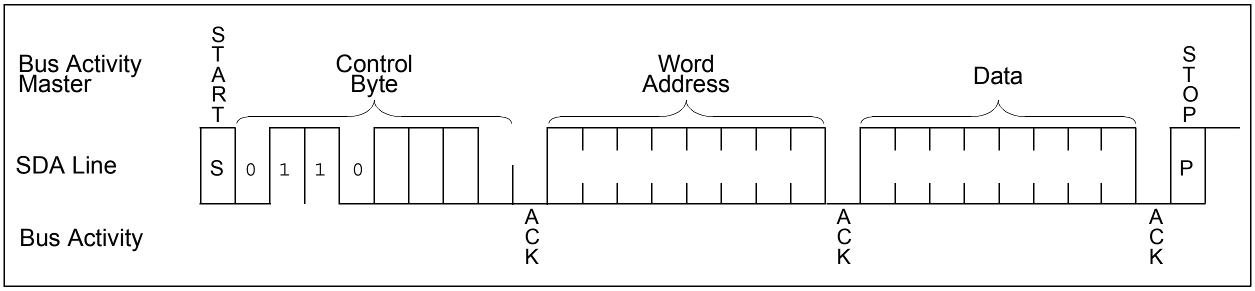
7.0 WRITE PROTECTION

The 24XXX52 has a software write-protect feature that allows the lower half of the array (addresses 00h-7Fh) to be permanently write-protected, as well as a WP pin that can be used to protect the entire array.

7.1 Software Write-Protect

The software write-protect feature is invoked by writing to the write-protect register. This is done by sending a command similar to a normal Write command. As shown in Figure 7-1, the write-protect register is written by sending a Write command with the slave address set to '`0110`' instead of '`1010`' and the address bits and data bits are "don't cares." Once the software write-protect register has been written, the device will not acknowledge the '`0110`' control byte.

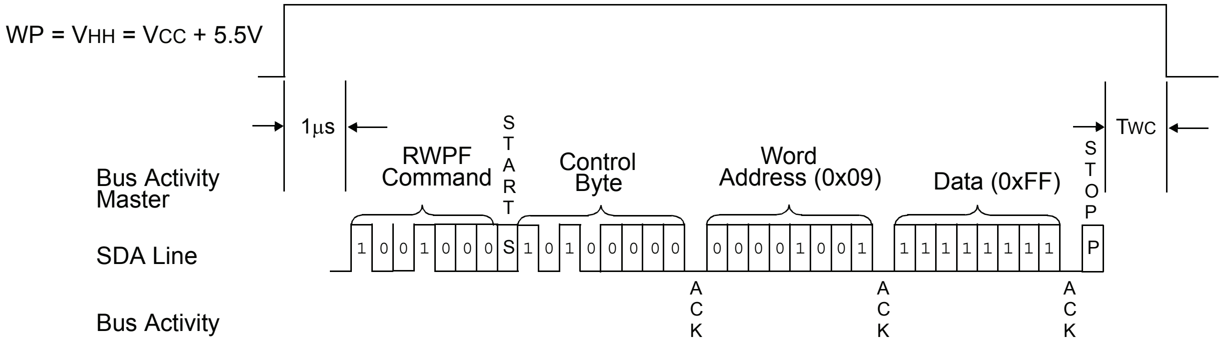
FIGURE 7-1: SETTING WRITE-PROTECT REGISTER



7.2 Resetting the Software Write-Protect Fuse

It is possible to reset the software write-protect feature on the 24XXX52. This is done by sending a command similar to setting the software write-protect command, except the command is sent before the regular control byte and is '`1001`'. The full command will be shown in Figure 7-2. In order for the command to work, a voltage of Vcc + 5.5V must be applied to the WP pin and must be sustained for 1µS before the command is given. The customer should also allow for a 5 ms delay after the Stop bit for TWC.

FIGURE 7-2: RESETTING WRITE-PROTECT FUSE (RWPF)



Note: Clock = 100 kHz, VDD = 1.8V to 5.5V

7.3 Hardware Write-Protect

The WP pin can be tied to VCC or VSS. If tied to VCC, the entire array will be write-protected, regardless of whether the software write-protect register has been written or not. If the WP pin is set to VCC, it will prevent the software write-protect register from being written. If the WP is tied to VSS, write protection is determined by the status of the software write-protect register for addresses 00h-7Fh. Addresses 80h-FFh are solely protected by the WP pin level.

8.0 READ OPERATION

Read operations are initiated in the same way as write operations, with the exception that the R/$\overline{W}$ bit of the slave address is set to '`1`'. There are three basic types of read operations: current address read, random read and sequential read.

8.1 Current Address Read

The 24XXX52 contains an address counter that maintains the address of the last word accessed, internally incremented by '`1`'. Therefore, if the previous access (either a read or write operation) was to address `n`, the next current address read operation would access data from address `n+1`. Upon receipt of the slave address with R/$\overline{W}$ bit set to '`1`', the 24XXX52 issues an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer, but does generate a Stop condition and the 24XXX52 discontinues transmission (Figure 8-1).

8.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, the word address must first be set. This is done by sending the word address to the 24XXX52 as part of a write operation. Once the word address is sent, the master generates a Start condition following the acknowledge. This terminates the write operation, but not before the internal Address Pointer is set. The master then issues the control byte again, but with the R/$\overline{W}$ bit set to a '`1`'. The 24XXX52 then issues an acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer, but does generate a Stop condition and the 24XXX52 discontinues transmission (Figure 8-2).

8.3 Sequential Read

Sequential reads are initiated in the same way as a random read, with the exception that after the 24XXX52 transmits the first data byte, the master issues an acknowledge, as opposed to a Stop condition in a random read. This directs the 24XXX52 to transmit the next sequentially addressed 8-bit word (Figure 8-3).

To provide sequential reads, the 24XXX52 contains an internal Address Pointer, which is incremented by one at the completion of each operation. This Address Pointer allows the entire memory contents to be serially read during one operation.

8.4 Contiguous Addressing Across Multiple Devices

The Chip Select bits (A2, A1, A0) can be used to expand the contiguous address space for up to 16K bits by adding up to eight 24XXX52 devices on the same bus. In this case, software can use A0 of the control byte as address bit A8; A1 as address bit A9, and A2 as address bit A10. It is not possible to sequentially read across device boundaries.

8.5 Noise Protection and Brown-Out

The 24XXX52 employs a VCC threshold detector circuit which disables the internal erase/write logic if the VCC is below 1.5V at nominal conditions.

The SCL and SDA inputs have Schmitt Trigger and filter circuits which suppress noise spikes to assure proper device operation, even on a noisy bus.

FIGURE 8-1: CURRENT ADDRESS READ

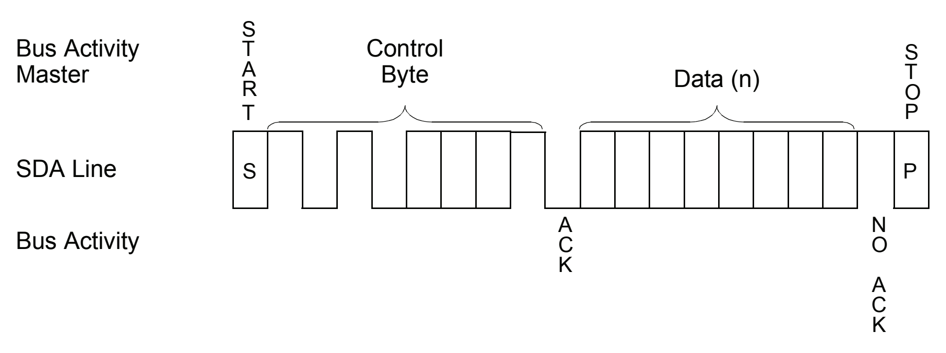


FIGURE 8-2: RANDOM READ

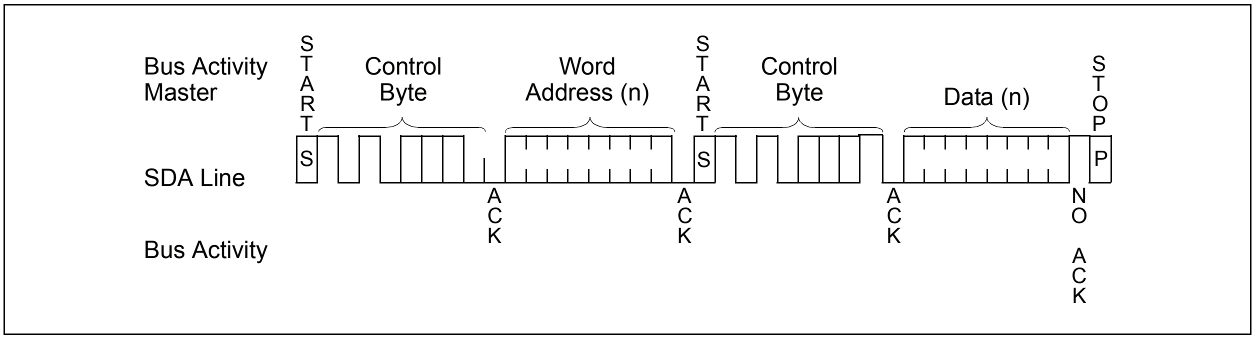
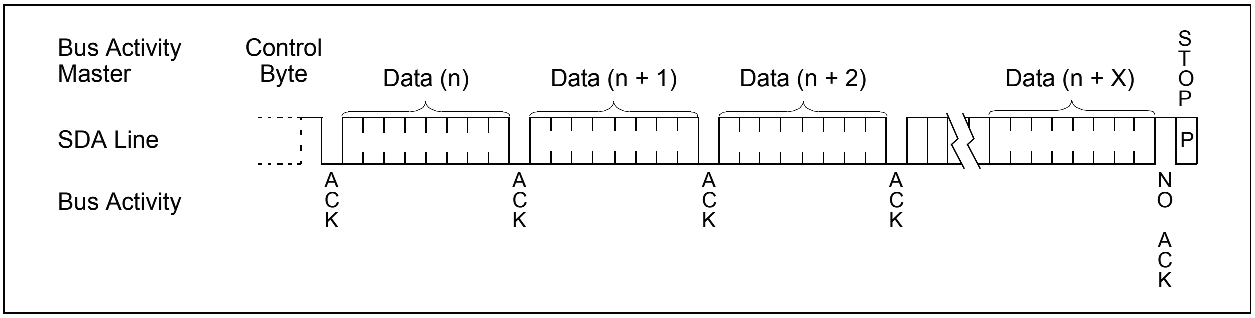


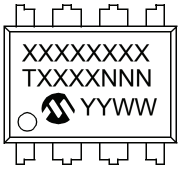
FIGURE 8-3: SEQUENTIAL READ



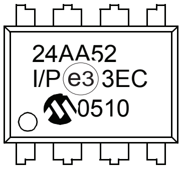
9.0 PACKAGING INFORMATION

9.1 Package Marking Information

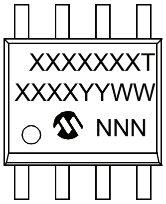
8-Lead PDIP (300 mil)



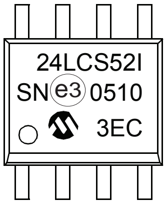
Example:



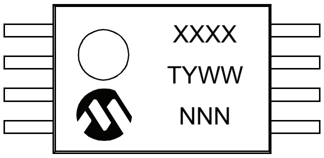
8-Lead SOIC (150 mil)



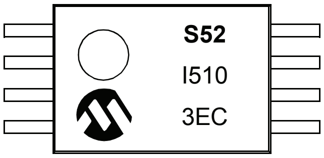
Example:



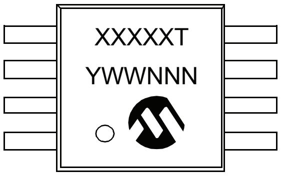
8-Lead TSSOP



Example:



8-Lead MSOP



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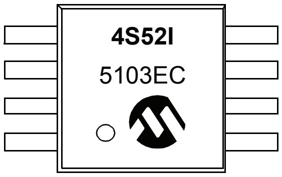
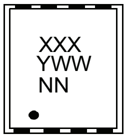


8-Lead 2x3 DFN



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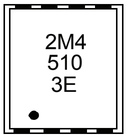
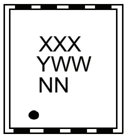
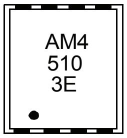


8-Lead 2x3 TDFN



Example:



Part Number	1st Line Marking Codes			
	TSSOP	**MSOP**	**DFN**	**TDFN**
24AA52	A52	4A52I	2M1	AM1
24LCS52	S52	4S52I	2M4	AM4

Legend:	XX...X	Part number or part number code
	T	Temperature (I, E)
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code (2 characters for small packages)
	e3	Pb-free JEDEC designator for Matte Tin (Sn)

Note: For very small packages with no room for the Pb-free JEDEC designator e3 , the marking will only appear on the outer carton or reel label.

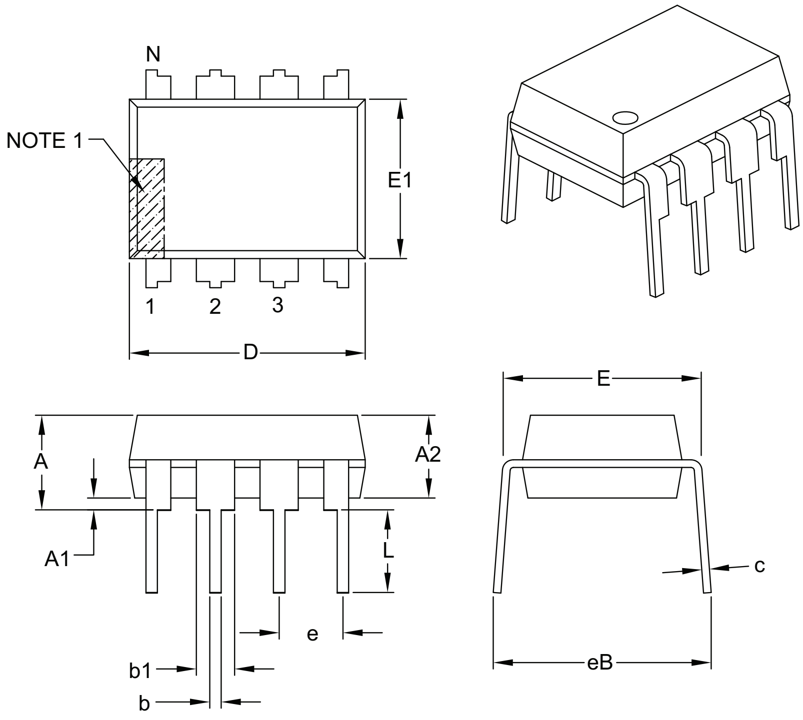
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

Note: Please visit www.microchip.com/Pbfree for the latest information on Pb-free conversion.

*Standard OTP marking consists of Microchip part number, year code, week code, and traceability code.

8-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	.100 BSC		
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

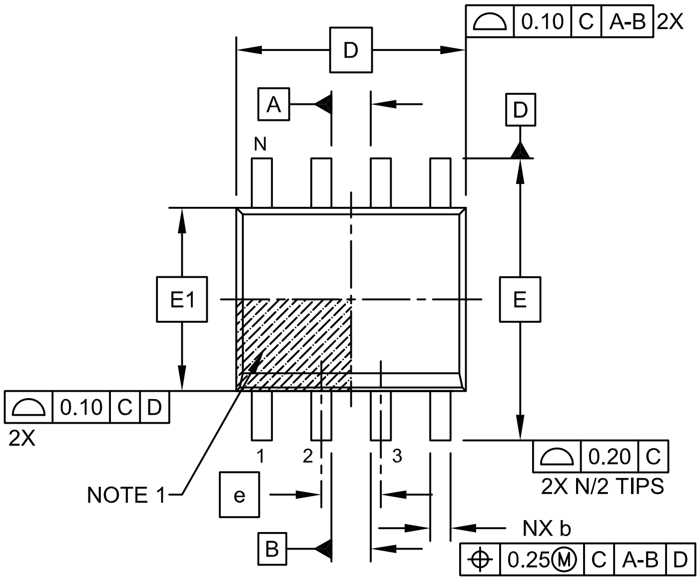
Notes:

1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

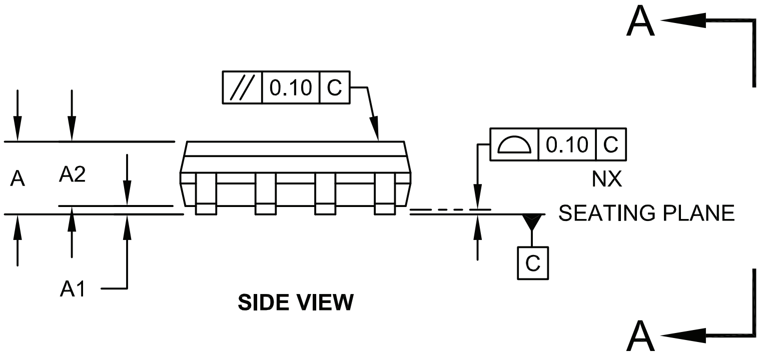
Microchip Technology Drawing C04-018B

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

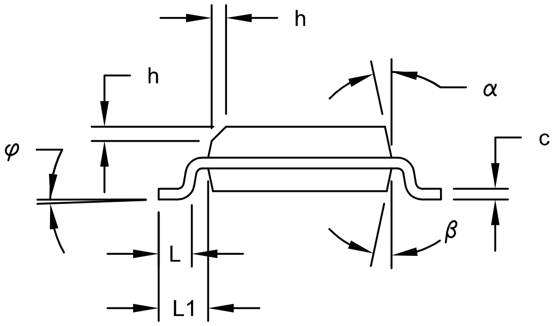
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

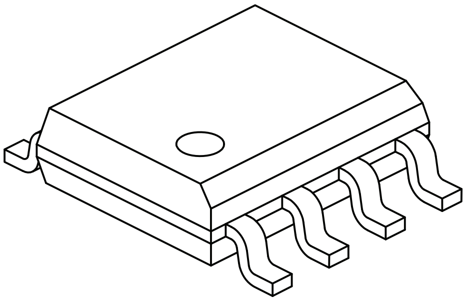


VIEW A-A

Microchip Technology Drawing No. C04-057C Sheet 1 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	1.27 BSC		
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	4.90 BSC		
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1	1.04 REF		
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

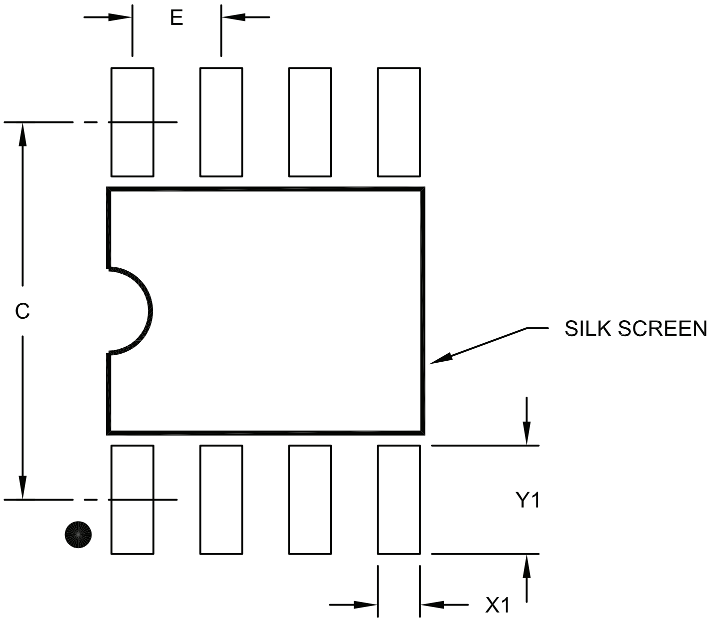
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-057C Sheet 2 of 2

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

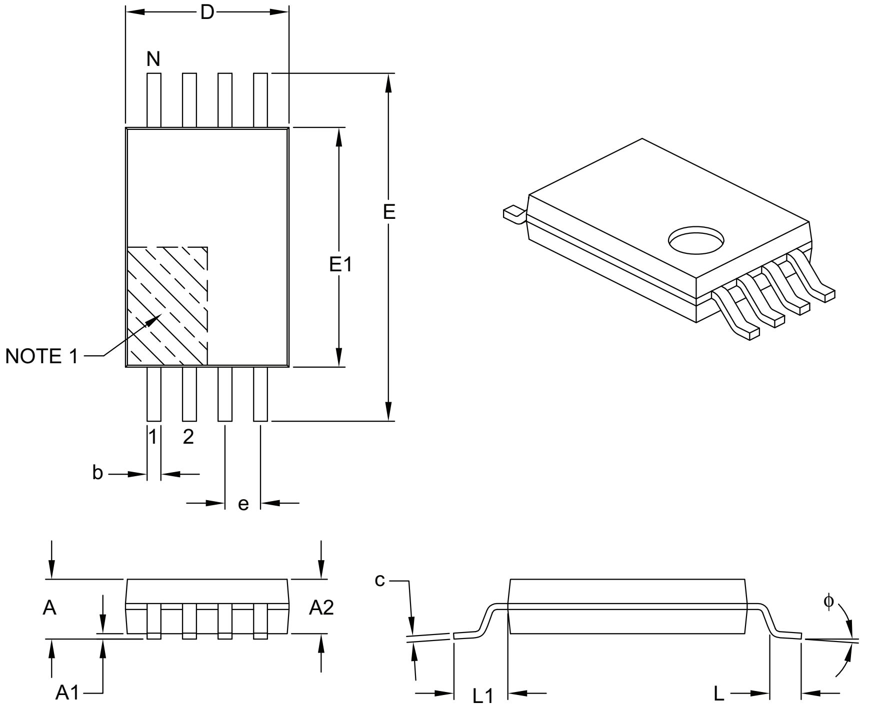
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

8-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	–	0.15
Overall Width	E		6.40 BSC	
Molded Package Width	E1	4.30	4.40	4.50
Molded Package Length	D	2.90	3.00	3.10
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	φ	0°	–	8°
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.19	–	0.30

Notes:

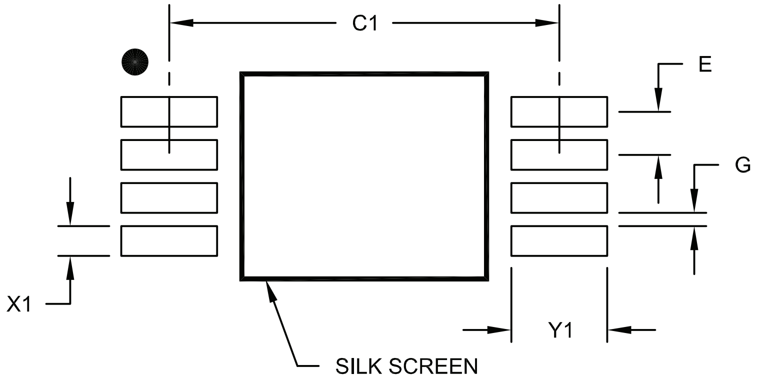
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-086B

8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C1		5.90	
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.45
Distance Between Pads	G	0.20		

Notes:

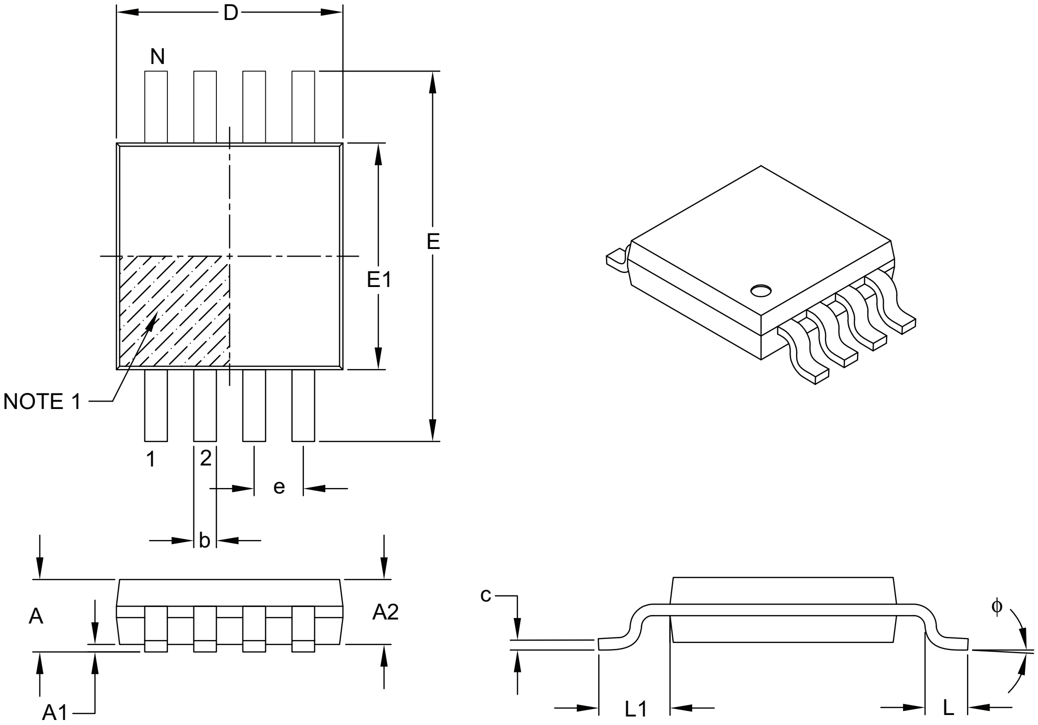
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2086A

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	0.65 BSC		
Overall Height	A	–	–	1.10
Molded Package Thickness	A2	0.75	0.85	0.95
Standoff	A1	0.00	–	0.15
Overall Width	E	4.90 BSC		
Molded Package Width	E1	3.00 BSC		
Overall Length	D	3.00 BSC		
Foot Length	L	0.40	0.60	0.80
Footprint	L1	0.95 REF		
Foot Angle	φ	0°	–	8°
Lead Thickness	c	0.08	–	0.23
Lead Width	b	0.22	–	0.40

Notes:

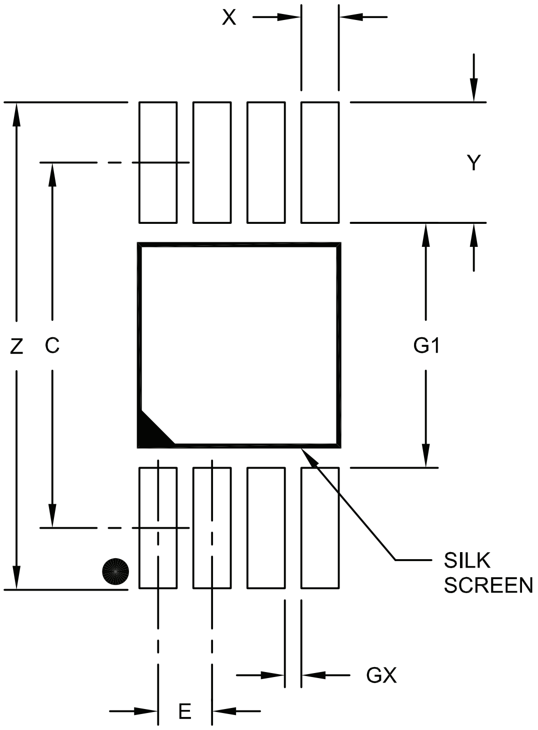
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111B

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		4.40	
Overall Width	Z			5.85
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.45
Distance Between Pads	G1	2.95		
Distance Between Pads	GX	0.20		

Notes:

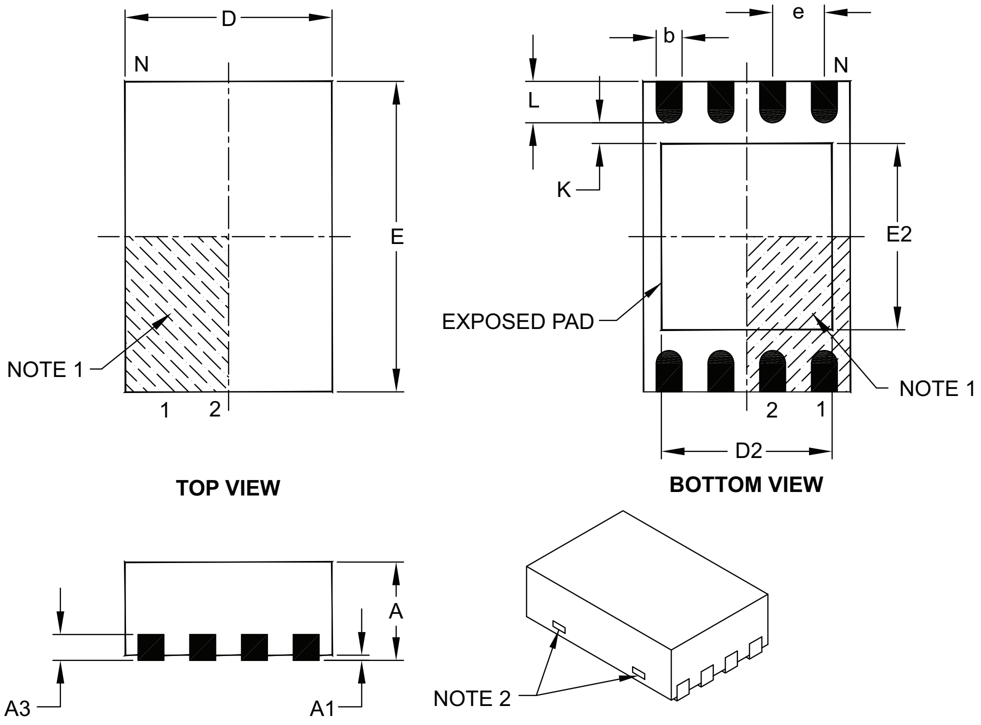
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2111A

8-Lead Plastic Dual Flat, No Lead Package (MC) – 2x3x0.9 mm Body [DFN]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		2.00 BSC	
Overall Width	E		3.00 BSC	
Exposed Pad Length	D2	1.30	–	1.55
Exposed Pad Width	E2	1.50	–	1.75
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	–	–

Notes:

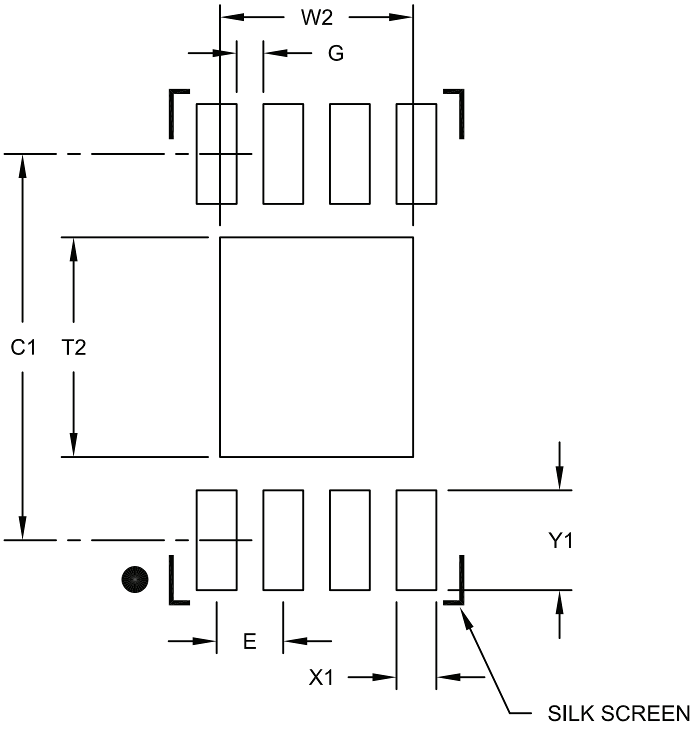
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-123C

8-Lead Plastic Dual Flat, No Lead Package (MC) - 2x3x0.9mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	W2			1.45
Optional Center Pad Length	T2			1.75
Contact Pad Spacing	C1		2.90	
Contact Pad Width (X8)	X1			0.30
Contact Pad Length (X8)	Y1			0.75
Distance Between Pads	G	0.20		

Notes:

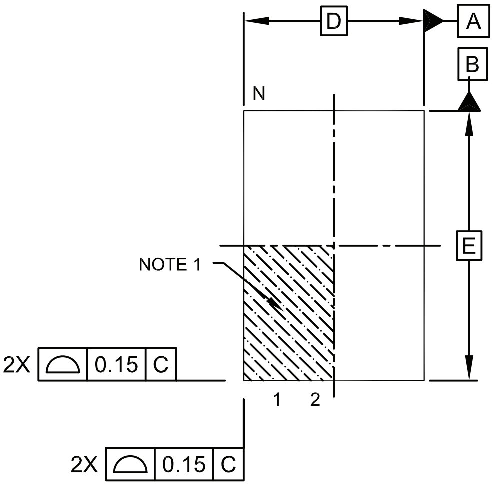
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

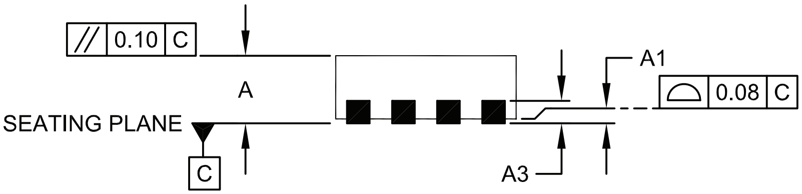
Microchip Technology Drawing No. C04-2123B

8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.75mm Body [TDFN]

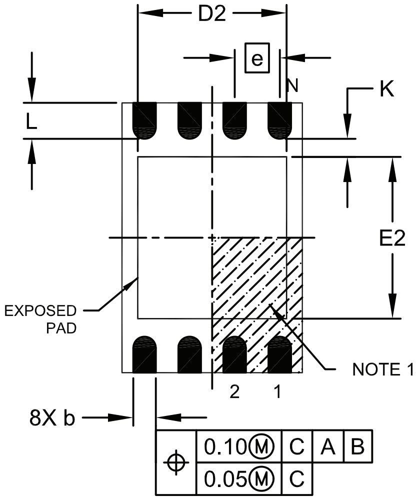
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

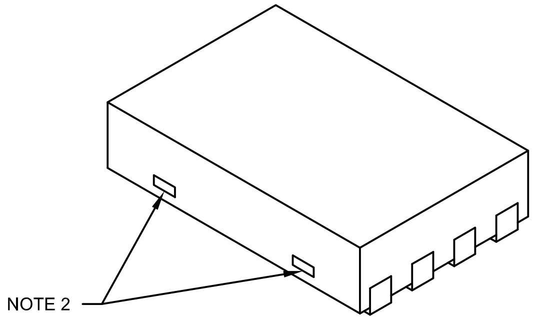


BOTTOM VIEW

Microchip Technology Drawing No. C04-129C Sheet 1 of 2

8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.75mm Body [TDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	0.50 BSC		
Overall Height	A	0.70	0.75	0.80
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3	0.20 REF		
Overall Length	D	2.00 BSC		
Overall Width	E	3.00 BSC		
Exposed Pad Length	D2	1.20	-	1.60
Exposed Pad Width	E2	1.20	-	1.60
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.25	0.30	0.45
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

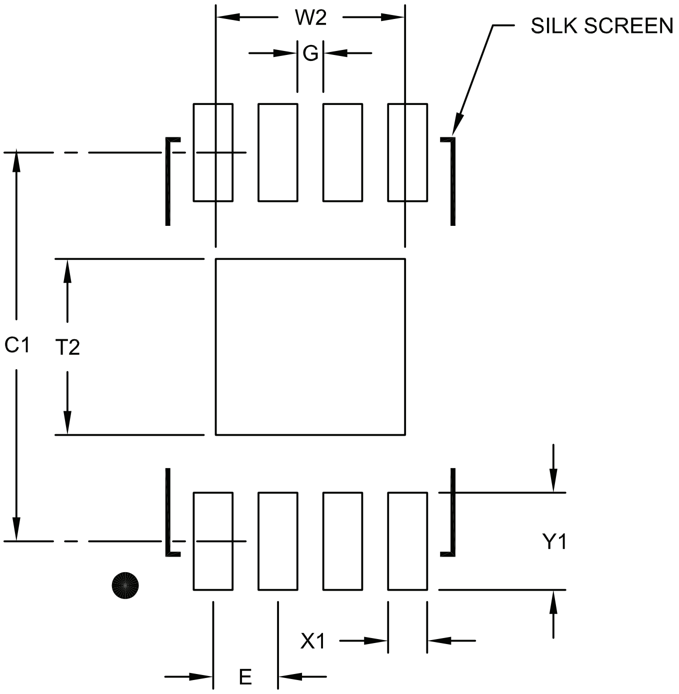
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-129C Sheet 2 of 2

8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.75 mm Body [TDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	W2			1.46
Optional Center Pad Length	T2			1.36
Contact Pad Spacing	C1		3.00	
Contact Pad Width (X8)	X1			0.30
Contact Pad Length (X8)	Y1			0.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2129A

APPENDIX A: REVISION HISTORY

Revision G

Added 2.2V to document; Revised Features section to include Standard and Pb-free finishes.
Corrections to Section 1.0, Electrical Characteristics; Product ID System, added lead finish info.

Revision H

Added Reset Software Write-Protect feature.
Added 2x3 DFN package option.

Revision J

Revised Sections 6.3 and 8.4. Revised DFN Package Drawing.

Revision K (11/2011)

Added TDFN package.

NOTES:

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5. What deletions from the document could be made without affecting the overall usefulness?

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____

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	**X**	**/XX**	**X**
Device	**Temperature Range**	**Package**	**Lead Finish**

Device:
24AA52: = 1.8V, 2 Kbit I^2C Serial EEPROM
24AA52T: = 1.8V, 2 Kbit I^2C Serial EEPROM (Tape and Reel)
24LCS52: = 2.2V, 2 Kbit I^2C Serial EEPROM
24LCS52T: = 2.2V, 2 Kbit I^2C Serial EEPROM (Tape and Reel)

Temperature Range:
I = -40°C to +85°C

Package:
P = Plastic DIP (300 mil body), 8-lead
SN = Plastic SOIC (150 mil body), 8-lead
ST = Plastic TSSOP (4.4 mm), 8-lead
MS = Plastic Micro Small Outline (MSOP), 8-lead
MC = Micro Lead Frame (2x3 mm body), 8-lead
MNY(1) = TDFN (2x3x0.75 mm body), 8-lead (Tape and Reel only)

Note 1: "Y" indicates a Nickel Palladium Gold (NiPdAu) finish.

Examples:

a) 24AA52-I/P: Industrial Temperature, 1.8V, PDIP package
b) 24AA52-I/SN: Industrial Temperature, 1.8V, SOIC package
c) 24AA52T-I/MS: Tape and Reel, Industrial Temperature, 1.8V, MSOP package
d) 24LCS52-I/P: Industrial Temperature, 2.2V, PDIP package
e) 24LCS52-I/MC: Industrial Temperature, 2.2V, DFN package
f) 24LCS52T-I/MS: Tape and Reel, Industrial Temperature, 2.2V, MSOP package
g) 24LCS52T-I/MNY: Tape and Reel, Industrial Temperature, 2.2V, TDFN package

NOTES:

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ISBN: 978-1-61341-786-7

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Тел: +7 (812) 336 43 04 (многоканальный)
Email: org@lifeelectronics.ru

www.lifeelectronics.ru