

**SCOPE: CMOS, BUFFERED, MULTIPLYING 8-BIT D/A CONVERTER**

<u>Device Type</u>	<u>Generic Number</u>	<u>Circuit Function</u>
01	MX7528S(x)/883B	DAC with $\pm 4$ LSB
02	MX7528T(x)/883B	DAC with $\pm 2$ LSB
03	MX7528U(x)/883B	DAC with $\pm 1$ LSB

**Case Outline(s).** The case outlines shall be designated in Mil-Std-1835 and as follows:

<u>Outline Letter</u>	<u>Mil-Std-1835</u>	<u>Case Outline</u>	<u>Package Code</u>
Q	GDIP1-T20 or CDIP2-T20	20 LEAD CERDIP	J20

**Absolute Maximum Ratings:**

$V_{DD}$ to AGND .....	0V, +17V
$V_{DD}$ to DGND .....	0V, +17V
$V_{RFBA}$ , $V_{RFBB}$ to DGND .....	$\pm 25$ V
$V_{REFA}$ , $V_{REFB}$ to AGND .....	$\pm 25$ V
Digital Input Voltage to DGND .....	-0.3V to $V_{DD}+0.3$ V
V pin 1 to DGND .....	-0.3V to $V_{DD}$
V pin 2, V pin 20 to AGND .....	-0.3V to $V_{DD}+0.3$ V
AGND to DGND .....	-0.3V, $V_{DD}+0.3$ V
DGND to AGND .....	+0.3V
Lead Temperature (soldering, 10 seconds) .....	+300°C
Storage Temperature .....	-65°C to +150°C
Continuous Power Dissipation .....	$T_A=+70^\circ\text{C}$
20 pin CERDIP(derate 11.1mW/°C above +70°C) .....	889mW
Junction Temperature $T_J$ .....	+150°C
Thermal Resistance, Junction to Case, $\theta_{JC}$	
20 pin CERDIP.....	40°C/W
Thermal Resistance, Junction to Ambient, $\theta_{JA}$ :	
16 pin CERDIP.....	90°C/W

**Recommended Operating Conditions**

Ambient Operating Range ( $T_A$ ) .....	-55°C to +125°C
Supply Voltage Range ( $V_{DD}$ ) .....	+4.75V to +5.25V and +14.25V to +15.75V
$V_{REF}$ DAC A= $V_{REF}$ DAC B .....	+10V
OUT DAC A=OUT DAC B .....	0V

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**TABLE 1. ELECTRICAL TESTS:**

TEST	Symbol	CONDITIONS	Group A Subgroup	Device type	Limits Min	Limits Max	Units
		-55 °C ≤ T <sub>A</sub> ≤ +125 °C <u>1</u> / Unless otherwise specified					
<b>ACCURACY</b>							
Resolution NOTE 4	RES	V <sub>DD</sub> =+5V and V <sub>DD</sub> =+15V	1,2,3	All	8.0		Bits
Relative Accuracy	RA	V <sub>DD</sub> =+5V and V <sub>DD</sub> =+15V	1,2,3	01		±1.0	LSB
Relative Accuracy	RA	V <sub>DD</sub> =+5V and V <sub>DD</sub> =+15V	1,2,3	02,03		±0.5	LSB
Differential Nonlinearity	DNL	V <sub>DD</sub> =+5V and V <sub>DD</sub> =+15V Monotonic to 8-Bits	1,2,3	All	-1	1	LSB
Gain Error NOTE 2	AE	V <sub>DD</sub> =+5V and V <sub>DD</sub> =+15V DAC register loaded with 1111 1111 1111	1	01 02 03		±4.0 ±2.0 ±1.0	LSB
Gain Error NOTE 2	AE	V <sub>DD</sub> =+5V V <sub>DD</sub> =+15V	2,3	01		±6.0 ±5.0	LSB
Gain Error NOTE 2	AE	V <sub>DD</sub> =+5V V <sub>DD</sub> =+15V	2,3	02		±4.0 ±3.0	LSB
Gain Error NOTE 2	AE	V <sub>DD</sub> =+5V V <sub>DD</sub> =+15V	2,3	03		±3.0 ±1.0	LSB
Power Supply Rejection	PSRR	V <sub>DD</sub> =+5V, ΔV <sub>DD</sub> =±5%	1 2,3	All		±0.02 ±0.04	%/%
Power Supply Rejection	PSRR	V <sub>DD</sub> =+15V, ΔV <sub>DD</sub> =±5%	1 2,3	All		±0.01 ±0.02	%/%
Output Leakage Current OUTA, OUTB	I <sub>OL</sub>	V <sub>DD</sub> =+5V, DAC latches loaded with 0000 0000	1 2,3	All		±50 ±400	nA
Output Leakage Current OUTA, OUTB	I <sub>OL</sub>	V <sub>DD</sub> =+15V, DAC latches loaded with 0000 0000	1 2,3	All		±50 ±200	nA
Reference Input Resistance VREFA, VREFB	R <sub>IN</sub>	V <sub>DD</sub> =+5V and +15V	4,5,6	All	8	15	kΩ
Digital Input High Voltage	V <sub>IH</sub>	V <sub>DD</sub> =+5V V <sub>DD</sub> =+15V	1,2,3	All	2.4 13.5		V
Digital Input Low Voltage	V <sub>IL</sub>	V <sub>DD</sub> =+5V V <sub>DD</sub> =+15V	1,2,3	All		0.8 1.5	V
Digital Input Leakage Current	I <sub>IN</sub>	V <sub>DD</sub> =+5V V <sub>IN</sub> =0V or V <sub>DD</sub>	1 2,3	All		±1.0 ±10	μA
Digital Input Leakage Current	I <sub>IN</sub>	V <sub>DD</sub> =+15V V <sub>IN</sub> =0V or V <sub>DD</sub>	1 2,3	All		±1.0 ±10	μA
Supply Current	I <sub>DD</sub>	V <sub>DD</sub> =+5V All digital inputs V <sub>DD</sub> =+15V V <sub>IL</sub> or V <sub>IH</sub>	1,2,3	All		2.0 2.0	mA
Supply Current	I <sub>DD</sub>	V <sub>DD</sub> =+5V & +15V. All digital inputs 0V or V <sub>DD</sub>	1 2,3	All		100 500	μA
Gain Temperature Coefficient NOTE 3	TC <sub>AE</sub>	V <sub>DD</sub> =+5V V <sub>DD</sub> =+15V	1,2,3	All		±70 ±35	ppm/°C
Feedthrough Error V <sub>REFA</sub> to OUTA and V <sub>REFB</sub> to OUTB	FT <sub>REFA</sub>	V <sub>DD</sub> =+5V or V <sub>DD</sub> =+15V, V <sub>REF</sub> =+10V, 100kHz sinewave, DAC latches loaded with 0000 0000 NOTE 3, NOTE 5	4,5,6	All		-55	dB

TEST	Symbol	CONDITIONS		Group A Subgroup	Device type	Limits Min	Limits Max	Units
		-55 °C ≤ T <sub>A</sub> ≤ +125 °C 1/ Unless otherwise specified						
Digital Input Capacitance NOTE 3, 6	C <sub>IN</sub>	V <sub>DD</sub> =+5V and V <sub>DD</sub> =+15V, DB0-DB7		4	All		10	pF
Digital Input Capacitance NOTE 3, 6	C <sub>IN</sub>	V <sub>DD</sub> =+5V _____ & WR, CS, DACA/DACB V <sub>DD</sub> =+15V		4	All		15	pF
<b>ANALOG INPUTS</b>								
Digital Output pin 2 Capacitance 3/ pin 20	C <sub>OUTA</sub> C <sub>OUTB</sub>	V <sub>DD</sub> =+5V and 15V, DAC latches loaded with 0000 0000		4	All		50 50	pF
Digital Output pin 2 Capacitance 3/ pin 20	C <sub>OUTA</sub> C <sub>OUTB</sub>	V <sub>DD</sub> =+5V and 15V, DAC latches loaded with 1111 1111		4	All		120 120	pF
<b>TIMING</b>								
Chip select to write setup time NOTE 3, 7	t <sub>CS</sub>	V <sub>DD</sub> =+5V V <sub>DD</sub> =+15V		9,10,11	All	250 180		ns
Chip select to write hold time NOTE 3, 7	t <sub>CH</sub>	V <sub>DD</sub> =+5V V <sub>DD</sub> =+15V		9,10,11	All	20 10		ns
Write pulse width NOTE 3, 7	t <sub>WR</sub>	V <sub>DD</sub> =+5V, t <sub>CS</sub> ≥ t <sub>WR</sub> , t <sub>CH</sub> ≥ 0 V <sub>DD</sub> =+15V, t <sub>CS</sub> ≥ t <sub>WR</sub> , t <sub>CH</sub> ≥ 0		9,10,11	All	220 180		ns
Data valid to write setup time NOTE 3, 7	t <sub>DS</sub>	V <sub>DD</sub> =+5V V <sub>DD</sub> =+15V		9,10,11	All	220 180		ns
Data valid to write hold time NOTE 3, 7	t <sub>DH</sub>	V <sub>DD</sub> =+5V V <sub>DD</sub> =+15V		9,10,11	All	10 10		ns
Data select to write setup time NOTE 3,7	t <sub>AS</sub>	V <sub>DD</sub> =+5V V <sub>DD</sub> =+15V		9,10,11	All	250 180		ns
Data select to write hold time NOTE 7	t <sub>AH</sub>	V <sub>DD</sub> =+5V V <sub>DD</sub> =+15V		9,10,11	All	20 10		ns
Reference input resistance match	R <sub>MIN</sub> ΔV <sub>REF</sub>	V <sub>DD</sub> =+5V V <sub>DD</sub> =+15V		4,5,6	All		±1 ±1	%
Channel to Channel isolation NOTE 3 V <sub>REFA</sub> to OUTB	CHISO	V <sub>DD</sub> =+5V or +15V. V <sub>REFA</sub> =±10V, 100kHz sinewave, V <sub>REFB</sub> =0V		4,5,6	All		-60	dB
Channel to Channel isolation NOTE 3 V <sub>REFB</sub> to OUTA	CHISO	V <sub>DD</sub> =+5V or +15V. V <sub>REFB</sub> =±10V, 100kHz sinewave, DAC, V <sub>REFA</sub> =0V		4,5,6	All		-60	dB
Output Current Settling Time NOTE 3, NOTE 8	t <sub>SL</sub>	V <sub>DD</sub> =+5V V <sub>DD</sub> =+15V		9,10,11	All		600 350	ns

NOTE 1: V<sub>OUT1</sub>=0V; V<sub>REF</sub>=+10V, AGND=DGND unless otherwise specified.

NOTE 2: Measured using internal RFBA and RFBB. Gain error is adjustable.

NOTE 3: Characteristics supplied for use as a typical design limit, but not production tested.

- NOTE 4: Guaranteed, if not tested.  
 NOTE 5: Feedthrough error can be reduced by connecting the metal lid to ground.  
 NOTE 6: Subgroup 4 ( $C_{IN}$  and  $C_{OUT}$  measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance.  
 NOTE 7: Timing in accordance with Write Cycle Timing Diagram in Commercial Data Sheet.  
 NOTE 8: To 0.5LSB,  $OUTA/OUTB=100\Omega$  in parallel with 13pF.  $\overline{CS}$   $\overline{WR}$   
 $DB0-DB7=0V$  to  $V_{DD}$  or  $V_{DD}$  to  $0V$ ,  $WR=CS=0V$

**MODE SELECTION TABLE:**

$\overline{CS}$	$\overline{WR}$	$\overline{DACA/DACB}$	DACA	DACB
L	L	L	Write	Hold
L	L	H	Hold	Write
H	X	X	Hold	Hold
X	H	X	Hold	Hold

L = Low state, H = High state, X = Don't care

**ORDERING INFORMATION:**

	Package	Pkg. Code	
01	20 pin CERDIP	J20	MX7528SQ/883B
02	20 pin CERDIP	J20	MX7528TQ/883B
03	20 pin CERDIP	J20	MX7528UQ/883B

**TERMINAL CONNECTIONS:**

J20	
Pin	
1	AGND
2	OUTA
3	RFBA
4	VREFA
5	DGND
6	$\overline{DACA/DACB}$
7	(MSB)DB7
8	DB6
9	DB5
10	DB4
11	DB3
12	DB2
13	DB1
14	DB0(LSB)
15	$\overline{CS}$
16	$\overline{WR}$
17	$V_{DD}$
18	VREFB
19	RFBB
20	OUTB

**QUALITY ASSURANCE**

Sampling and inspection procedures shall be in accordance with MIL-Prf-38535, Appendix A as specified in Mil-Std-883.

Screening shall be in accordance with Method 5004 of Mil-Std-883. Burn-in test Method 1015:

1. Test Condition, A, B, C, or D.
2. TA = +125°C minimum.
3. Interim and final electrical test requirements shall be specified in Table 2.

Quality conformance inspection shall be in accordance with Method 5005 of Mil-Std-883, including Groups A, B, C, and D inspection.

Group A inspection:

1. Tests as specified in Table 2.
2. Selected subgroups in Table 1, Method 5005 of Mil-Std-883 shall be omitted.

Group C and D inspections:

- a. End-point electrical parameters shall be specified in Table 1.
- b. Steady-state life test, Method 1005 of Mil-Std-883:
  1. Test condition A, B, C, D.
  2. TA = +125°C, minimum.
  3. Test duration, 1000 hours, except as permitted by Method 1005 of Mil-Std-883.

**TABLE 2. ELECTRICAL TEST REQUIREMENTS**

Mil-Std-883 Test Requirements	Subgroups per Method 5005, Table 1
Interim Electric Parameters Method 5004	1
Final Electrical Parameters Method 5005	1*, 2, 3
Group A Test Requirements Method 5005	1, 2, 3, 4, 5, 6, 9**, 10**, 11**
Group C and D End-Point Electrical Parameters Method 5005	1

\* PDA applies to Subgroup 1 only.

\*\* Subgroups 9, 10 and 11, if not tested shall be guaranteed to the limits specified in Table 1.

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- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.



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