

# MC10EP445, MC100EP445

## 3.3V/5V ECL 8-Bit Serial/Parallel Converter

### Description

The MC10/100EP445 is an integrated 8-bit differential serial to parallel data converter with asynchronous data synchronization. The device has two modes of operation. CKSEL HIGH mode is designed to operate NRZ data rates of up to 3.3 Gb/s, while CKSEL LOW mode is designed to operate at twice the internal clock data rate of up to 5.0 Gb/s. The conversion sequence was chosen to convert the first serial bit to Q0, the second bit to Q1, etc. Two selectable differential serial inputs, which are selected by SINSEL, provide this device with loop-back testing capability. The MC10/100EP445 has a SYNC pin which, when held high for at least two consecutive clock cycles, will swallow one bit of data shifting the start of the conversion data from  $D_n$  to  $D_{n+1}$ . Each additional shift requires an additional pulse to be applied to the SYNC pin.

Control pins are provided to reset and disable internal clock circuitry. Additionally,  $V_{BB}$  pin is provided for single-ended input condition.

The 100 Series contains temperature compensation.

### Features

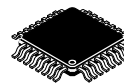
- 1530 ps Propagation Delay
- 5.0 Gb/s Typical Data Rate for CLKSEL LOW Mode
- Differential Clock and Serial Inputs
- $V_{BB}$  Output for Single-Ended Input Applications
- Asynchronous Data Synchronization (SYNC)
- Asynchronous Master Reset (RESET)
- PECL Mode Operating Range:  $V_{CC} = 3.0\text{ V}$  to  $5.5\text{ V}$  with  $V_{EE} = 0\text{ V}$
- NECL Mode Operating Range:  $V_{CC} = 0\text{ V}$  with  $V_{EE} = -3.0\text{ V}$  to  $-5.5\text{ V}$
- Open Input Default State
- CLK ENABLE Immune to Runt Pulse Generation
- Pb-Free Packages are Available\*



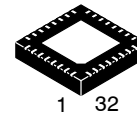
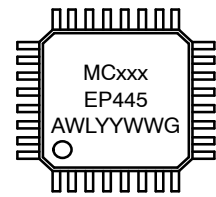
ON Semiconductor®

<http://onsemi.com>

### MARKING DIAGRAM\*



LQFP-32  
FA SUFFIX  
CASE 873A



QFN32  
MN SUFFIX  
CASE 488AM



xxx = 10 or 100  
A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week  
G or ■ = Pb-Free Package  
(Note: Microdot may be in either location)

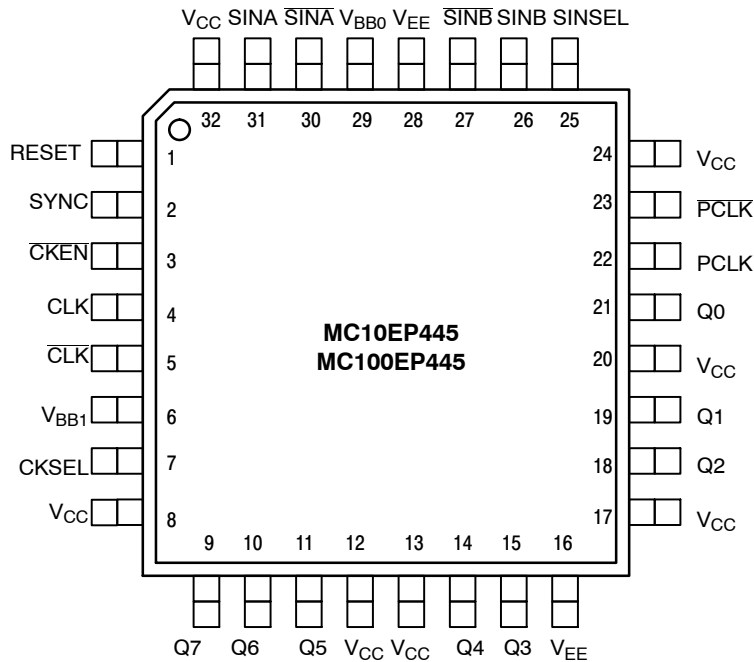
\*For additional marking information, refer to Application Note AND8002/D.

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 17 of this data sheet.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# MC10EP445, MC100EP445



Warning: All V<sub>CC</sub> and V<sub>EE</sub> pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. 32-Lead LQFP Pinout (Top View)

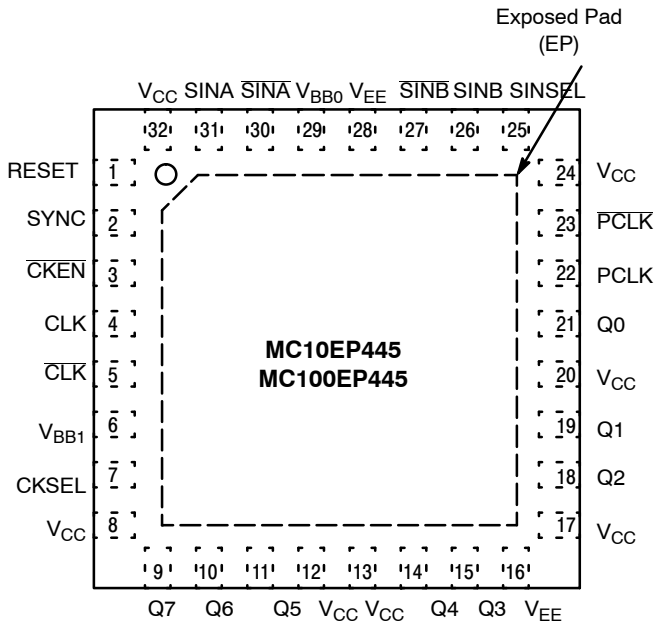


Figure 2. 32-Lead QFN Pinout (Top View)

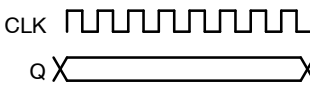
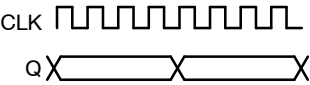
Table 1. PIN DESCRIPTION

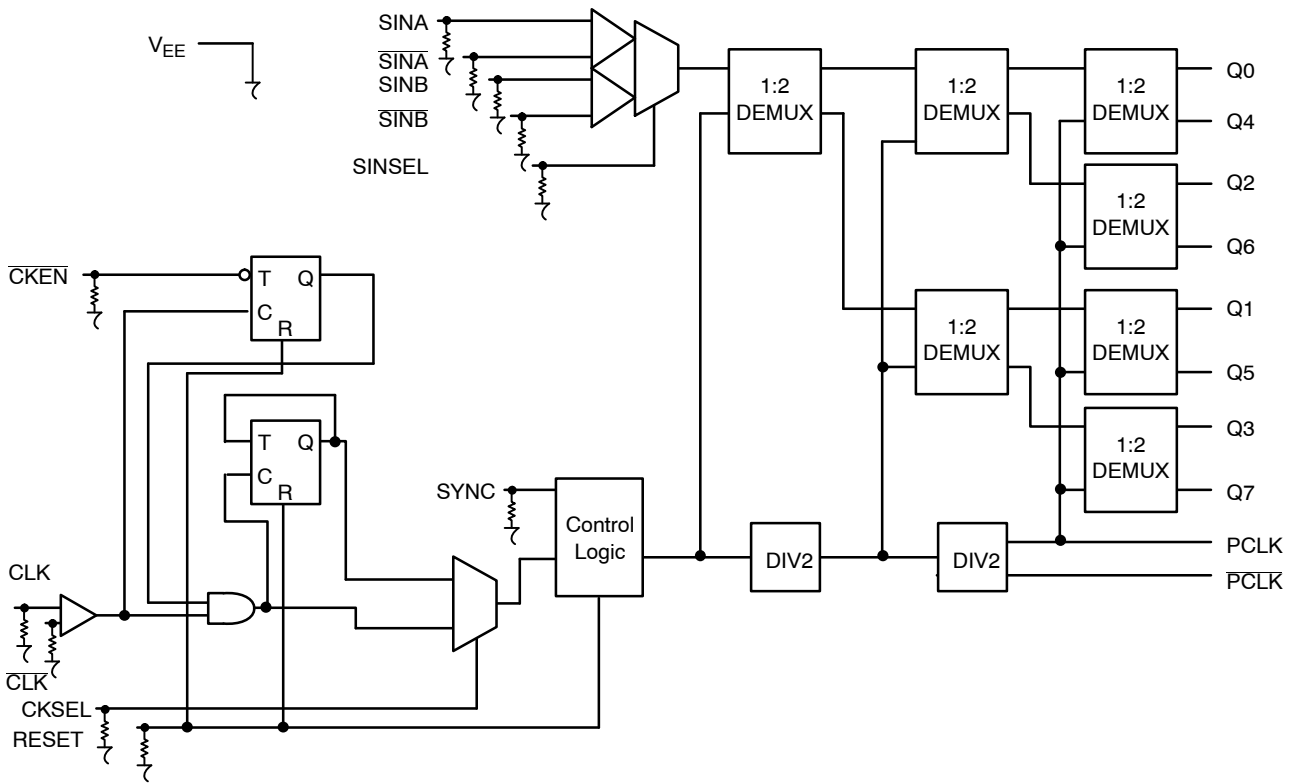
| Pin                                 | Function  |
|-------------------------------------|---|
| SINA*, $\overline{\text{SINA}}^*$   | ECL Differential Serial Data Input A  |
| SINB*, $\overline{\text{SINB}}^*$   | ECL Differential Serial Data Input B  |
| SINSEL*                             | ECL Serial Input Selector Pin   |
| Q0-Q7                               | ECL Parallel Data Outputs   |
| CLK*, $\overline{\text{CLK}}^*$     | ECL Differential Clock Inputs   |
| PCLK, $\overline{\text{PCLK}}$      | ECL Differential Parallel Clock Output  |
| SYNC*                               | ECL Conversion Synchronizing Input  |
| CKSEL*                              | ECL Clock Input Selector Pin  |
| $\overline{\text{CKEN}}^*$          | ECL Clock Enable Pin  |
| RESET*                              | ECL Reset Pin   |
| V <sub>BB0</sub> , V <sub>BB1</sub> | Output Reference Voltage  |
| V <sub>CC</sub>                     | Positive Supply   |
| V <sub>EE</sub>                     | Negative Supply   |
| EP                                  | The exposed pad (EP) on the QFN-32 package bottom is thermally connected to the die for improved heat transfer out of the package. The exposed pad must be attached to a heat-sinking conduit. The pad is electrically connected to V <sub>EE</sub> . |

\* Pins will default logic LOW or differential logic LOW when left open.

# MC10EP445, MC100EP445

**Table 2. TRUTH TABLE**

| PIN    | FUNCTION   |  |
|--------|--|--|
|        | High   | Low  |
| SINSEL | Select SINB Input  | Select SINA Input  |
| CKSEL  | Q: PCLK = 8:1<br>CLK: Q = 1:1<br> | Q: PCLK = 8:1<br>CLK: Q = 1:2<br> |
| CKEN   | Synchronously Disable Internal Clock Circuitry   | Synchronously Enable Internal Clock Circuitry  |
| RESET  | Asynchronous Master Reset  | Synchronous Enable   |
| SYNC   | Asynchronously Applied to Swallow a Data Bit   | Normal Conversion Process  |



**Figure 3. Logic Diagram**

# MC10EP445, MC100EP445

**Table 3. ATTRIBUTES**

| Characteristics   | Value                  |                      |
|---|------------------------|----------------------|
| Internal Input Pulldown Resistor                              | 75 kΩ                  |                      |
| Internal Input Pull-up Resistor                               | N/A                    |                      |
| ESD Protection  | Human Body Model       | > 2 kV               |
|   | Machine Model          | > 200 V              |
|   | Charged Device Model   | > 2 kV               |
| Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1) | Pb Pkg                 | Pb-Free Pkg          |
|   | LQFP-32<br>QFN-32      | Level 2<br>N/A       |
| Flammability Rating   | Oxygen Index: 28 to 34 | UL 94 V-0 @ 0.125 in |
| Transistor Count  | 993 Devices            |                      |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test        |                        |                      |

1. For additional information, see Application Note AND8003/D.

**Table 4. MAXIMUM RATINGS**

| Symbol           | Parameter                                | Condition 1           | Condition 2                                | Rating      | Unit |
|------------------|--|-----------------------|--|-------------|------|
| V <sub>CC</sub>  | PECL Mode Power Supply                   | V <sub>EE</sub> = 0 V |  | 6           | V    |
| V <sub>EE</sub>  | NECL Mode Power Supply                   | V <sub>CC</sub> = 0 V |  | -6          | V    |
| V <sub>I</sub>   | PECL Mode Input Voltage                  | V <sub>EE</sub> = 0 V | V <sub>I</sub> ≤ V <sub>CC</sub>           | 6           | V    |
|                  | NECL Mode Input Voltage                  | V <sub>CC</sub> = 0 V | V <sub>I</sub> ≥ V <sub>EE</sub>           | -6          | V    |
| I <sub>out</sub> | Output Current                           | Continuous<br>Surge   |  | 50          | mA   |
|                  |  |                       |  | 100         | mA   |
| I <sub>BB</sub>  | V <sub>BB</sub> Sink/Source              |                       |  | ± 0.5       | mA   |
| T <sub>A</sub>   | Operating Temperature Range              |                       |  | -40 to +85  | °C   |
| T <sub>stg</sub> | Storage Temperature Range                |                       |  | -65 to +150 | °C   |
| θ <sub>JA</sub>  | Thermal Resistance (Junction-to-Ambient) | 0 lfpm                | 32 LQFP                                    | 80          | °C/W |
|                  |  | 500 lfpm              | 32 LQFP                                    | 55          | °C/W |
| θ <sub>JC</sub>  | Thermal Resistance (Junction-to-Case)    | Standard Board        | 32 LQFP                                    | 12 to 17    | °C/W |
| θ <sub>JA</sub>  | Thermal Resistance (Junction-to-Ambient) | 0 lfpm<br>500 lfpm    | QFN-32                                     | 31          | °C/W |
|                  |  |                       | QFN-32                                     | 27          | °C/W |
| θ <sub>JC</sub>  | Thermal Resistance (Junction-to-Case)    | 2S2P                  | QFN-32                                     | 12          | °C/W |
| T <sub>sol</sub> | Wave Solder                              | Pb<br>Pb-Free         | <2 to 3 sec @ 248°C<br><2 to 3 sec @ 260°C | 265         | °C   |
|                  |  |                       |  | 265         |      |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

# MC10EP445, MC100EP445

**Table 5. 10EP DC CHARACTERISTICS, PECL  $V_{CC} = 3.3\text{ V}$ ,  $V_{EE} = 0\text{ V}$  (Note 2)**

| Symbol      | Characteristic   | -40°C |      |      | 25°C |      |      | 85°C |      |      | Unit          |
|-------------|--|-------|------|------|------|------|------|------|------|------|---------------|
|             |  | Min   | Typ  | Max  | Min  | Typ  | Max  | Min  | Typ  | Max  |               |
| $I_{EE}$    | Power Supply Current   | 95    | 119  | 143  | 98   | 122  | 146  | 100  | 125  | 150  | mA            |
| $V_{OH}$    | Output HIGH Voltage (Note 3)   | 2165  | 2290 | 2415 | 2230 | 2355 | 2480 | 2290 | 2415 | 2540 | mV            |
| $V_{OL}$    | Output LOW Voltage (Note 3)  | 1365  | 1490 | 1615 | 1430 | 1555 | 1680 | 1490 | 1615 | 1740 | mV            |
| $V_{IH}$    | Input HIGH Voltage (Single-Ended)  | 2090  |      | 2415 | 2155 |      | 2480 | 2215 |      | 2540 | mV            |
| $V_{IL}$    | Input LOW Voltage (Single-Ended)   | 1365  |      | 1690 | 1460 |      | 1755 | 1490 |      | 1815 | mV            |
| $V_{BB}$    | Output Voltage Reference   | 1790  | 1890 | 1990 | 1855 | 1955 | 2055 | 1915 | 2015 | 2115 | mV            |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 4) | 2.0   |      | 3.3  | 2.0  |      | 3.3  | 2.0  |      | 3.3  | V             |
| $I_{IH}$    | Input HIGH Current   |       |      | 150  |      |      | 150  |      |      | 150  | $\mu\text{A}$ |
| $I_{IL}$    | Input LOW Current  | 0.5   |      |      | 0.5  |      |      | 0.5  |      |      | $\mu\text{A}$ |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.3 V to -2.2 V.
- All loading with 50  $\Omega$  to  $V_{CC} - 2.0\text{ V}$ .
- $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ .  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

**Table 6. 10EP DC CHARACTERISTICS, PECL  $V_{CC} = 5.0\text{ V}$ ,  $V_{EE} = 0\text{ V}$  (Note 5)**

| Symbol      | Characteristic   | -40°C |      |      | 25°C |      |      | 85°C |      |      | Unit          |
|-------------|--|-------|------|------|------|------|------|------|------|------|---------------|
|             |  | Min   | Typ  | Max  | Min  | Typ  | Max  | Min  | Typ  | Max  |               |
| $I_{EE}$    | Power Supply Current (Note 6)  | 95    | 119  | 143  | 98   | 122  | 146  | 100  | 125  | 150  | mA            |
| $V_{OH}$    | Output HIGH Voltage (Note 7)   | 3865  | 3990 | 4115 | 3930 | 4055 | 4180 | 3990 | 4115 | 4240 | mV            |
| $V_{OL}$    | Output LOW Voltage (Note 7)  | 3065  | 3190 | 3315 | 3130 | 3255 | 3380 | 3190 | 3315 | 3440 | mV            |
| $V_{IH}$    | Input HIGH Voltage (Single-Ended)  | 3790  |      | 4115 | 3855 |      | 4180 | 3915 |      | 4240 | mV            |
| $V_{IL}$    | Input LOW Voltage (Single-Ended)   | 3065  |      | 3390 | 3130 |      | 3455 | 3190 |      | 3515 | mV            |
| $V_{BB}$    | Output Voltage Reference   | 3490  | 3590 | 3690 | 3555 | 3655 | 3755 | 3615 | 3715 | 3815 | mV            |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 8) | 2.0   |      | 5.0  | 2.0  |      | 5.0  | 2.0  |      | 5.0  | V             |
| $I_{IH}$    | Input HIGH Current   |       |      | 150  |      |      | 150  |      |      | 150  | $\mu\text{A}$ |
| $I_{IL}$    | Input LOW Current  | 0.5   |      |      | 0.5  |      |      | 0.5  |      |      | $\mu\text{A}$ |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +2.0 V to -0.5 V.
- Required 500 lfm air flow when using +5 V power supply. For  $(V_{CC} - V_{EE}) > 3.3\text{ V}$ , 5  $\Omega$  to 10  $\Omega$  in line with  $V_{EE}$  required for maximum thermal protection at elevated temperatures. Recommend  $V_{CC} - V_{EE}$  operation at  $\leq 3.3\text{ V}$ .
- All loading with 50  $\Omega$  to  $V_{CC} - 2.0\text{ V}$ .
- $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ .  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

# MC10EP445, MC100EP445

**Table 7. 10EP DC CHARACTERISTICS, NECL**  $V_{CC} = 0\text{ V}$ ,  $V_{EE} = -5.5\text{ V}$  to  $-3.0\text{ V}$  (Note 9)

| Symbol      | Characteristic  | -40°C        |       |       | 25°C         |       |       | 85°C         |       |       | Unit          |
|-------------|---|--------------|-------|-------|--------------|-------|-------|--------------|-------|-------|---------------|
|             |   | Min          | Typ   | Max   | Min          | Typ   | Max   | Min          | Typ   | Max   |               |
| $I_{EE}$    | Power Supply Current (Note 10)  | 95           | 119   | 143   | 98           | 122   | 146   | 100          | 125   | 150   | mA            |
| $V_{OH}$    | Output HIGH Voltage (Note 11)   | -1135        | -1010 | -885  | -1070        | -945  | -820  | -1010        | -885  | -760  | mV            |
| $V_{OL}$    | Output LOW Voltage (Note 11)  | -1935        | -1810 | -1685 | -1870        | -1745 | -1620 | -1810        | -1685 | -1560 | mV            |
| $V_{IH}$    | Input HIGH Voltage (Single-Ended)   | -1210        |       | -885  | -1145        |       | -820  | -1085        |       | -760  | mV            |
| $V_{IL}$    | Input LOW Voltage (Single-Ended)  | -1935        |       | -1610 | -1870        |       | -1545 | -1810        |       | -1485 | mV            |
| $V_{BB}$    | Output Voltage Reference  | -1510        | -1410 | -1310 | -1445        | -1345 | -1245 | -1385        | -1285 | -1185 | mV            |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 12) | $V_{EE}+2.0$ |       | 0.0   | $V_{EE}+2.0$ |       | 0.0   | $V_{EE}+2.0$ |       | 0.0   | V             |
| $I_{IH}$    | Input HIGH Current  |              |       | 150   |              |       | 150   |              |       | 150   | $\mu\text{A}$ |
| $I_{IL}$    | Input LOW Current   | 0.5          |       |       | 0.5          |       |       | 0.5          |       |       | $\mu\text{A}$ |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

9. Input and output parameters vary 1:1 with  $V_{CC}$ .

10. Required 500 lfm air flow when using  $-5\text{ V}$  power supply. For  $(V_{CC} - V_{EE}) > 3.3\text{ V}$ ,  $5\ \Omega$  to  $10\ \Omega$  in line with  $V_{EE}$  required for maximum thermal protection at elevated temperatures. Recommend  $V_{CC}-V_{EE}$  operation at  $\leq 3.3\text{ V}$ .

11. All loading with  $50\ \Omega$  to  $V_{CC} - 2.0\text{ V}$ .

12.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

**Table 8. 100EP DC CHARACTERISTICS, PECL**  $V_{CC} = 3.3\text{ V}$ ,  $V_{EE} = 0\text{ V}$  (Note 13)

| Symbol      | Characteristic  | -40°C |      |      | 25°C |      |      | 85°C |      |      | Unit          |
|-------------|---|-------|------|------|------|------|------|------|------|------|---------------|
|             |   | Min   | Typ  | Max  | Min  | Typ  | Max  | Min  | Typ  | Max  |               |
| $I_{EE}$    | Power Supply Current  | 95    | 119  | 143  | 98   | 122  | 146  | 100  | 125  | 150  | mA            |
| $V_{OH}$    | Output HIGH Voltage (Note 14)   | 2155  | 2280 | 2405 | 2155 | 2280 | 2405 | 2155 | 2280 | 2405 | mV            |
| $V_{OL}$    | Output LOW Voltage (Note 14)  | 1355  | 1480 | 1605 | 1355 | 1480 | 1605 | 1355 | 1480 | 1605 | mV            |
| $V_{IH}$    | Input HIGH Voltage (Single-Ended)   | 2075  |      | 2420 | 2075 |      | 2420 | 2075 |      | 2420 | mV            |
| $V_{IL}$    | Input LOW Voltage (Single-Ended)  | 1355  |      | 1675 | 1355 |      | 1675 | 1355 |      | 1675 | mV            |
| $V_{BB}$    | Output Voltage Reference  | 1775  | 1875 | 1975 | 1775 | 1875 | 1975 | 1775 | 1875 | 1975 | mV            |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 15) | 2.0   |      | 3.3  | 2.0  |      | 3.3  | 2.0  |      | 3.3  | V             |
| $I_{IH}$    | Input HIGH Current  |       |      | 150  |      |      | 150  |      |      | 150  | $\mu\text{A}$ |
| $I_{IL}$    | Input LOW Current   | 0.5   |      |      | 0.5  |      |      | 0.5  |      |      | $\mu\text{A}$ |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

13. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary  $+0.3\text{ V}$  to  $-2.2\text{ V}$ .

14. All loading with  $50\ \Omega$  to  $V_{CC} - 2.0\text{ V}$ .

15.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

# MC10EP445, MC100EP445

**Table 9. 100EP DC CHARACTERISTICS, PECL**  $V_{CC} = 5.0\text{ V}$ ,  $V_{EE} = 0\text{ V}$  (Note 16)

| Symbol      | Characteristic  | -40°C |      |      | 25°C |      |      | 85°C |      |      | Unit          |
|-------------|---|-------|------|------|------|------|------|------|------|------|---------------|
|             |   | Min   | Typ  | Max  | Min  | Typ  | Max  | Min  | Typ  | Max  |               |
| $I_{EE}$    | Power Supply Current (Note 17)  | 95    | 119  | 143  | 98   | 122  | 146  | 100  | 125  | 150  | mA            |
| $V_{OH}$    | Output HIGH Voltage (Note 18)   | 3855  | 3980 | 4105 | 3855 | 3980 | 4105 | 3855 | 3980 | 4105 | mV            |
| $V_{OL}$    | Output LOW Voltage (Note 18)  | 3055  | 3180 | 3305 | 3055 | 3180 | 3305 | 3055 | 3180 | 3305 | mV            |
| $V_{IH}$    | Input HIGH Voltage (Single-Ended)   | 3775  |      | 4120 | 3775 |      | 4120 | 3775 |      | 4120 | mV            |
| $V_{IL}$    | Input LOW Voltage (Single-Ended)  | 3055  |      | 3375 | 3055 |      | 3375 | 3055 |      | 3375 | mV            |
| $V_{BB}$    | Output Voltage Reference  | 3475  | 3575 | 3675 | 3475 | 3575 | 3675 | 3475 | 3575 | 3675 | mV            |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 19) | 2.0   |      | 5.0  | 2.0  |      | 5.0  | 2.0  |      | 5.0  | V             |
| $I_{IH}$    | Input HIGH Current  |       |      | 150  |      |      | 150  |      |      | 150  | $\mu\text{A}$ |
| $I_{IL}$    | Input LOW Current   | 0.5   |      |      | 0.5  |      |      | 0.5  |      |      | $\mu\text{A}$ |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

16. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +2.0 V to -0.5 V.

17. Required 500 lfm air flow when using +5 V power supply. For  $(V_{CC} - V_{EE}) > 3.3\text{ V}$ , 5  $\Omega$  to 10  $\Omega$  in line with  $V_{EE}$  required for maximum thermal protection at elevated temperatures. Recommend  $V_{CC} - V_{EE}$  operation at  $\leq 3.3\text{ V}$ .

18. All loading with 50  $\Omega$  to  $V_{CC} - 2.0\text{ V}$ .

19.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

**Table 10. 100EP DC CHARACTERISTICS, NECL**  $V_{CC} = 0\text{ V}$ ,  $V_{EE} = -5.5\text{ V}$  to  $-3.0\text{ V}$  (Note 20)

| Symbol      | Characteristic  | -40°C          |       |       | 25°C           |       |       | 85°C           |       |       | Unit          |
|-------------|---|----------------|-------|-------|----------------|-------|-------|----------------|-------|-------|---------------|
|             |   | Min            | Typ   | Max   | Min            | Typ   | Max   | Min            | Typ   | Max   |               |
| $I_{EE}$    | Power Supply Current (Note 21)  | 95             | 119   | 143   | 98             | 122   | 146   | 100            | 125   | 150   | mA            |
| $V_{OH}$    | Output HIGH Voltage (Note 22)   | -1145          | -1020 | -895  | -1145          | -1020 | -895  | -1145          | -1020 | -895  | mV            |
| $V_{OL}$    | Output LOW Voltage (Note 22)  | -1945          | -1820 | -1695 | -1945          | -1820 | -1695 | -1945          | -1820 | -1695 | mV            |
| $V_{IH}$    | Input HIGH Voltage (Single-Ended)   | -1225          |       | -880  | -1225          |       | -880  | -1225          |       | -880  | mV            |
| $V_{IL}$    | Input LOW Voltage (Single-Ended)  | -1945          |       | -1625 | -1945          |       | -1625 | -1945          |       | -1625 | mV            |
| $V_{BB}$    | Output Voltage Reference  | -1525          | -1425 | -1325 | -1525          | -1425 | -1325 | -1525          | -1425 | -1325 | mV            |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 23) | $V_{EE} + 2.0$ |       | 0.0   | $V_{EE} + 2.0$ |       | 0.0   | $V_{EE} + 2.0$ |       | 0.0   | V             |
| $I_{IH}$    | Input HIGH Current  |                |       | 150   |                |       | 150   |                |       | 150   | $\mu\text{A}$ |
| $I_{IL}$    | Input LOW Current   | 0.5            |       |       | 0.5            |       |       | 0.5            |       |       | $\mu\text{A}$ |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

20. Input and output parameters vary 1:1 with  $V_{CC}$ .

21. Required 500 lfm air flow when using -5.0 V power supply. For  $(V_{CC} - V_{EE}) > 3.3\text{ V}$ , 5  $\Omega$  to 10  $\Omega$  in line with  $V_{EE}$  required for maximum thermal protection at elevated temperatures. Recommend  $V_{CC} - V_{EE}$  operation at  $\leq 3.3\text{ V}$ .

22. All loading with 50  $\Omega$  to  $V_{CC} - 2.0\text{ V}$ .

23.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

# MC10EP445, MC100EP445

**Table 11. AC CHARACTERISTICS**  $V_{CC} = 0\text{ V}$ ;  $V_{EE} = -3.0\text{ V}$  to  $-5.5\text{ V}$  or  $V_{CC} = 3.0\text{ V}$  to  $5.5\text{ V}$ ;  $V_{EE} = 0\text{ V}$  (Note 24)

| Symbol                                 | Characteristic   | -40°C        |              |                   | 25°C         |              |                   | 85°C         |              |                   | Unit |
|--|--|--------------|--------------|-------------------|--------------|--------------|-------------------|--------------|--------------|-------------------|------|
|  |  | Min          | Typ          | Max               | Min          | Typ          | Max               | Min          | Typ          | Max               |      |
| $f_{\max}$                             | Maximum Input CLK Frequency<br>(See Figure 13. $F_{\max}/\text{JITTER}$ )<br>CKSEL = LOW<br>CKSEL = HIGH | 2.0<br>2.8   | 2.5<br>3.3   |                   | 2.0<br>2.8   | 2.5<br>3.3   |                   | 1.7<br>2.8   | 2.2<br>3.3   |                   | GHz  |
| $t_{\text{PLH}}$ ,<br>$t_{\text{PHL}}$ | Propagation Delay to<br>Output Differential<br>CLK to Q<br>CLK TO PCLK                                   | 1280<br>1000 | 1475<br>1240 | 1710<br>1490      | 1335<br>1050 | 1557<br>1310 | 1795<br>1580      | 1450<br>1140 | 1663<br>1420 | 1950<br>1710      | ps   |
| $t_s$                                  | Setup Time<br>SINA, B+ TO CLK+ (Figure 5)<br>CKEN+ TO CLK- (Figure 6)                                    | -400<br>100  | -459<br>50   |                   | -420<br>100  | -479<br>50   |                   | -440<br>100  | -492<br>50   |                   | ps   |
| $t_h$                                  | Hold Time<br>CLK+ TO SINA, B- (Figure 5)<br>CLK- TO CKEN (Figure 6)                                      | 533<br>45    | 474<br>-35   |                   | 550<br>45    | 490<br>-35   |                   | 560<br>45    | 508<br>-35   |                   | ps   |
| $t_{\text{RR}}/t_{\text{RR2}}$         | Reset Recovery (Figure 4)  | 350          | 180          |                   | 350          | 180          |                   | 350          | 180          |                   | ps   |
| $t_{\text{PW}}$                        | Minimum Pulse Width<br>RESET   | 400          |              |                   | 400          |              |                   | 400          |              |                   | ps   |
| $t_{\text{JITTER}}$                    | RMS Random Clock Jitter<br>@ 2.0 GHz CLK_SEL LOW<br>@ 2.5 GHz CLK_SELF HIGH<br>@ 3.0 GHz CLK_SEL HIGH    |              |              | 1.5<br>1.0<br>1.5 |              |              | 1.5<br>1.0<br>2.0 |              |              | 1.5<br>1.5<br>2.5 | ps   |
| $V_{\text{PP}}$                        | Input Voltage Swing (Differential Configuration)<br>(Note 25)  | 150          | 800          | 1200              | 150          | 800          | 1200              | 150          | 800          | 1200              | mV   |
| $t_r$ ,<br>$t_f$                       | Output Rise/Fall Times<br>(20% – 80%)<br>Q/Q<br>PCLK/PCLK  | 100<br>100   | 180<br>180   | 400<br>250        | 100<br>100   | 200<br>200   | 400<br>300        | 125<br>125   | 230<br>230   | 425<br>325        | ps   |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

24. Measured using a 750 mV source, 50% duty cycle clock source. All loading with 50  $\Omega$  to  $V_{CC} - 2.0\text{ V}$ .

25.  $V_{\text{PP}}(\text{min})$  is the minimum input swing for which AC parameters are guaranteed.



# MC10EP445, MC100EP445

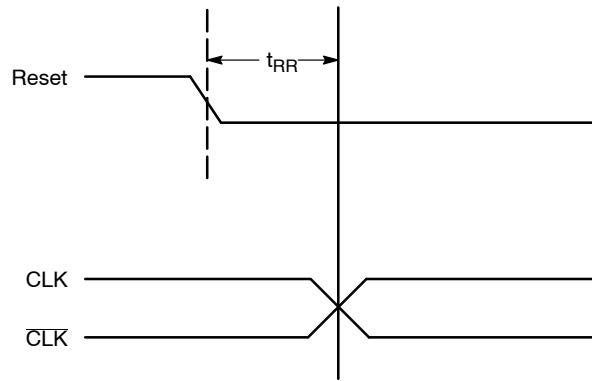


Figure 4. Reset Recovery

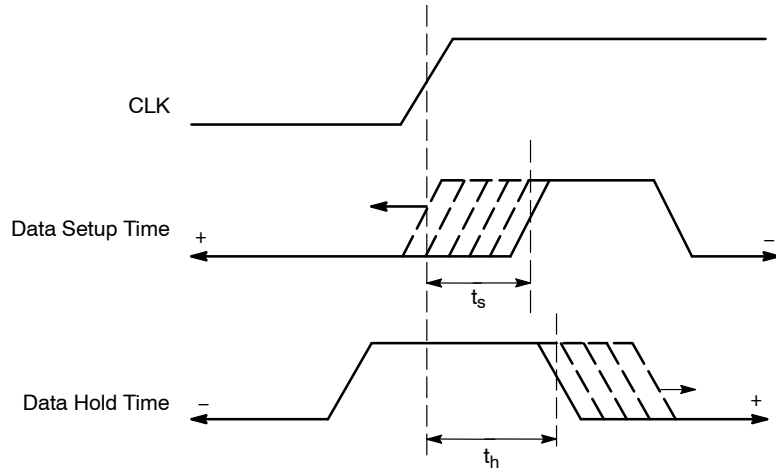


Figure 5. Data Setup and Hold Time

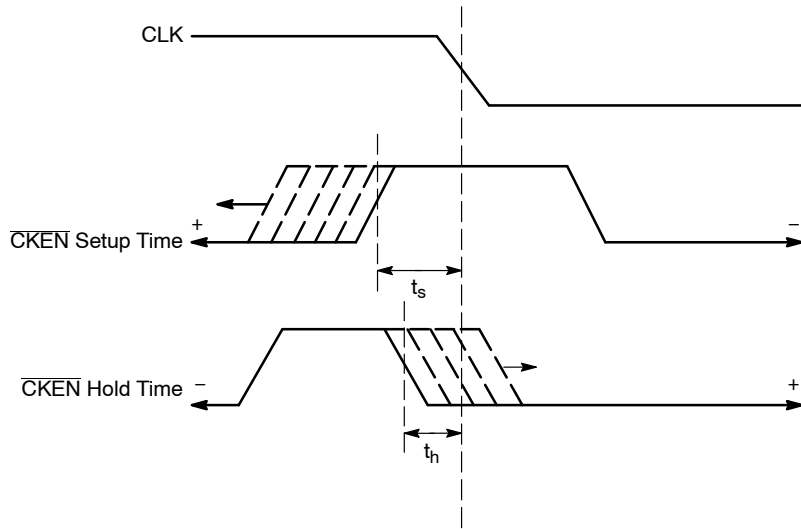


Figure 6.  $\overline{CKEN}$  Setup and Hold Time

# MC10EP445, MC100EP445

## APPLICATION INFORMATION

The MC10/100EP445 is an integrated 1:8 serial to parallel converter with two modes of operation selected by CKSEL (Pin 7). CKSEL HIGH mode only latches data on the rising edge of the input CLK and CKSEL LOW mode latches data on both the rising and falling edge of the input CLK. CKSEL LOW is the open default state. Either of the two differential input serial data path provided for this device, SINA and SINB, can be chosen with the SINSEL pin (pin 25). SINA is the default input path when SINSEL pin is left floating. Because of internal pull-downs on the input pins, all input pins will default to logic low when left open.

The two selectable serial data paths can be used for loop-back testing as well as the bit error testing.

Upon power-up, the internal flip-flops will attain a random state. To synchronize multiple flip-flops in the device, the Reset (pin 1) must be asserted. The reset pin will disable the internal clock signal irrespective of the CKEN state (CKEN disables the internal clock circuitry). The device will grab the first stream of data after the falling edge of RESET<sup>①</sup>, followed by the falling edge of CLK<sup>②</sup>, on second rising edge of CLK<sup>③</sup> in either CKSEL modes. (See Figure 6)

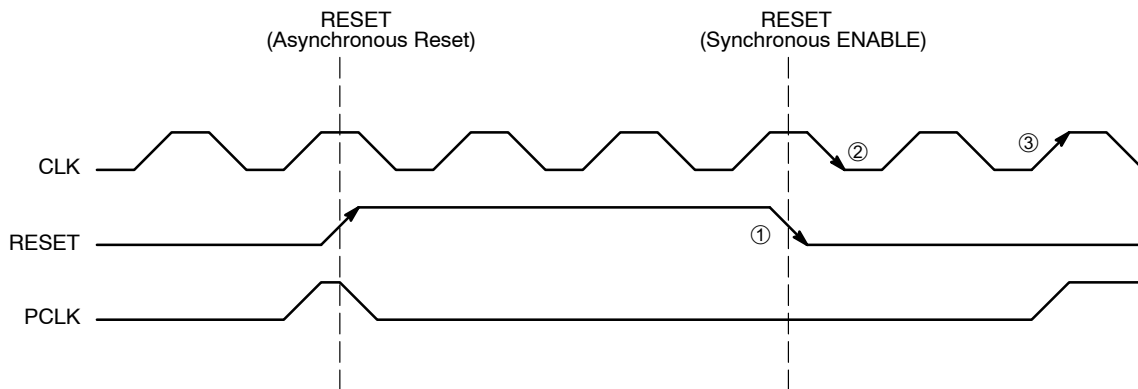


Figure 7. Reset Timing Diagram

# MC10EP445, MC100EP445

For CKSEL LOW operation, the data is latched on both the rising edge and the falling edge of the clock and the time from when the serial data is latched<sup>①</sup> to when the data is seen on the parallel output<sup>②</sup> is 6 clock cycles (see Figure 8).

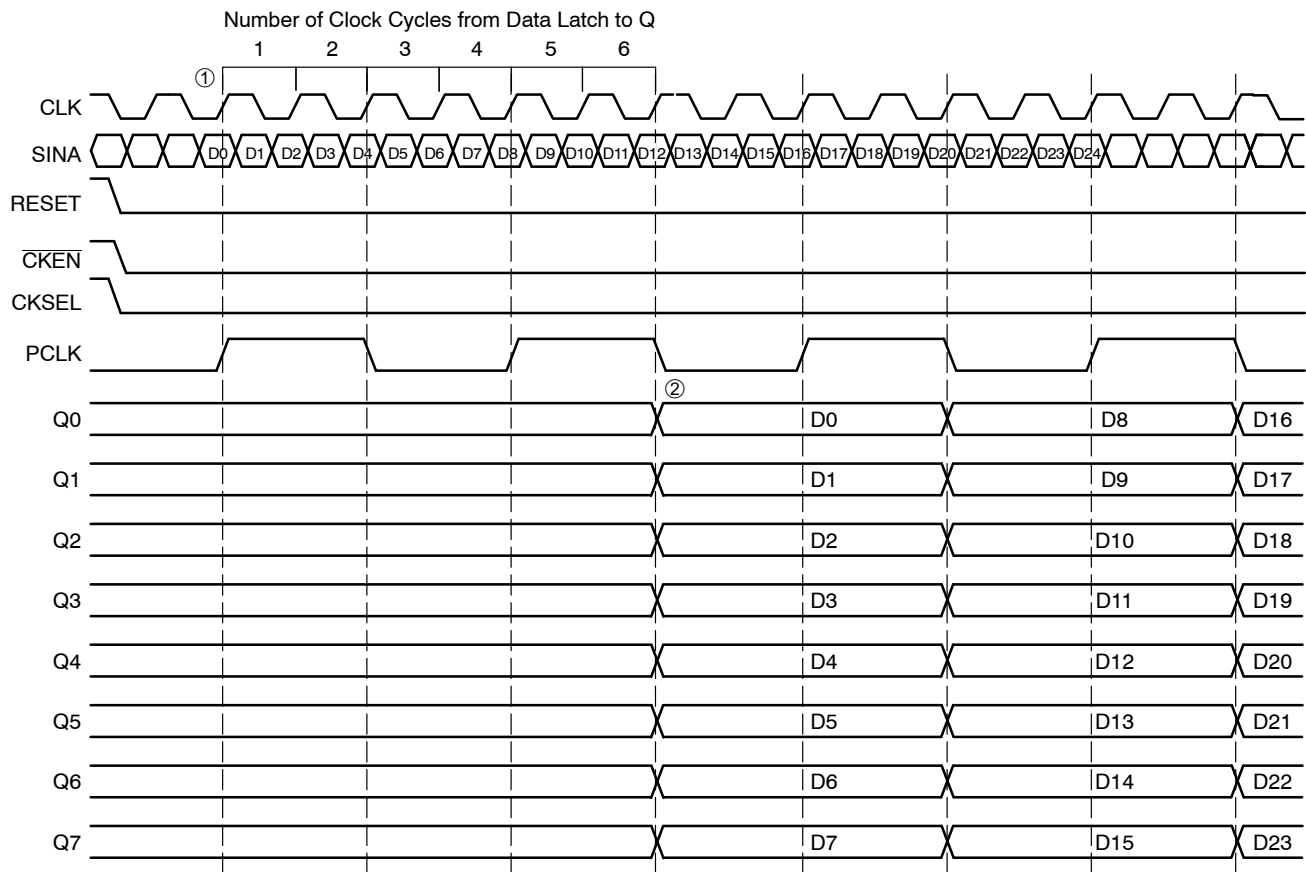


Figure 8. Timing Diagram A. 1:8 Serial to Parallel Conversion with CKSEL LOW

# MC10EP445, MC100EP445

Similarly, for CKSEL HIGH operation, the data is latched only on the rising edge of the clock and the time from when the serial data is latched<sup>①</sup> to when the data is seen on the parallel output<sup>②</sup> is 12 clock cycles (see Figure 9).

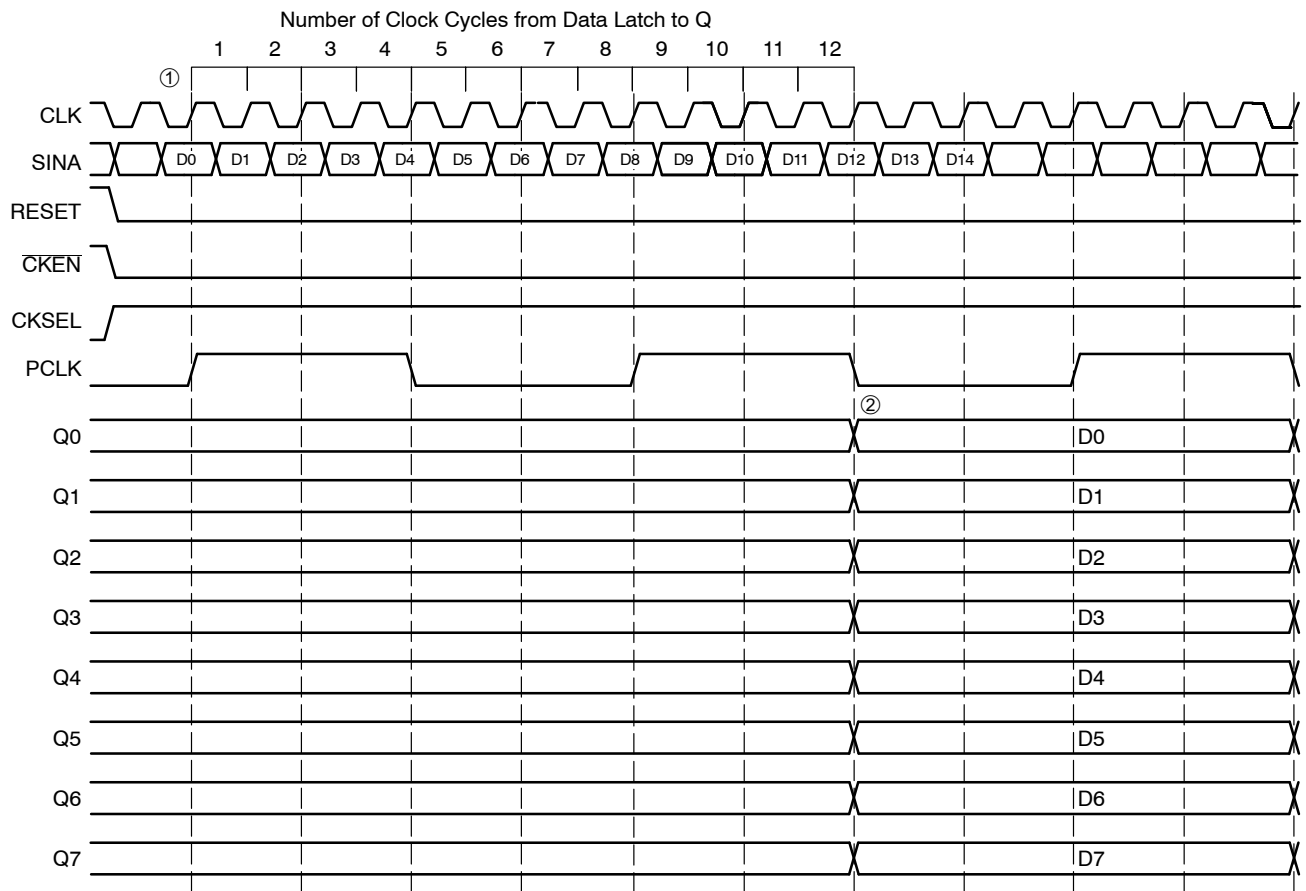


Figure 9. Timing Diagram A. 1:8 Serial to Parallel Conversion with CKSEL HIGH

## MC10EP445, MC100EP445

To allow the user to synchronize the output byte data correctly, the start bit for conversion can be moved using the SYNC input pin (pin 2). Asynchronously asserting the SYNC pin will force the internal clock to swallow a clock pulse, effectively shifting a bit from the  $Q_n$  to the  $Q_{n-1}$  output as shown in Figure 10 and Figure 11. For CKSEL LOW, a single pulse applied asynchronously for two consecutive

clock cycles shifts the start bit for conversion from  $Q_n$  to  $Q_{n-1}$ . The bit is swallowed following the two clock cycle pulse width of SYNC<sup>①</sup> on the next triggering edge of clock<sup>②</sup> (either on the rising or the falling edge of the clock). Each additional shift requires an additional pulse to be applied to the SYNC pin. (See Figure 10)

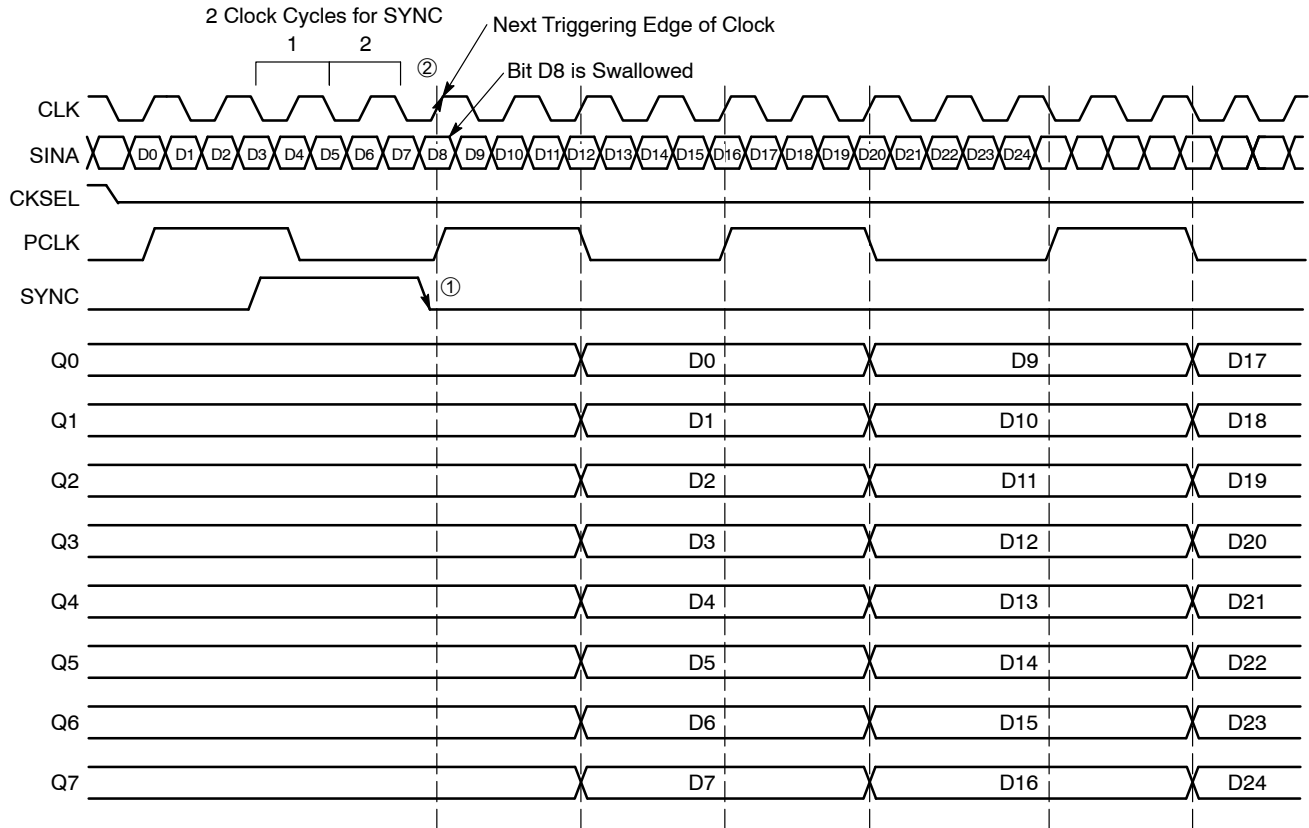


Figure 10. Timing Diagram A. 1:8 Serial to Parallel Conversion with SYNC Pulse at CKSEL LOW

## MC10EP445, MC100EP445

For CKSEL HIGH, a single pulse applied asynchronously for three consecutive clock cycles shifts the start bit for conversion from  $Q_n$  to  $Q_{n-1}$ . The bit is swallowed following the three clock cycle pulse width of SYNC on the next

triggering edge of clock<sup>②</sup> (on the rising edge of the clock only). Each additional shift requires an additional pulse to be applied to the SYNC pin. (See Figure 11)

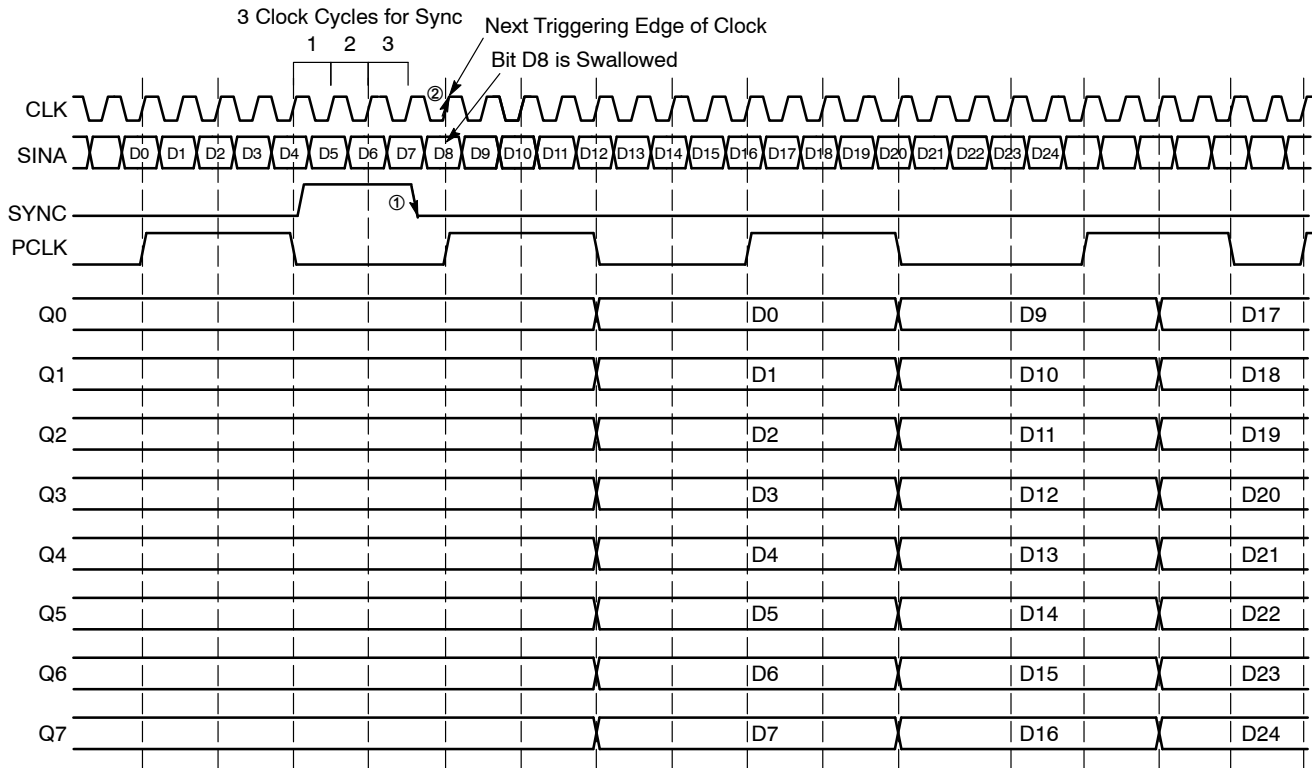
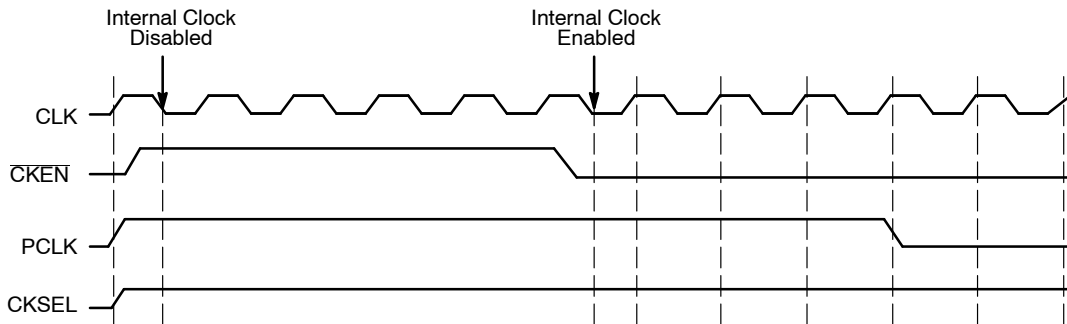


Figure 11. Timing Diagram A. 1:8 Serial to Parallel Conversion with SYNC Pulse at CKSEL HIGH

## MC10EP445, MC100EP445

The synchronous  $\overline{\text{CKEN}}$  (pin 3) applied with at least one clock cycle pulse length will disable the internal clock signal. The synchronous  $\overline{\text{CKEN}}$  will suspend all of the device activities and prevent runt pulses from being generated. The rising edge of  $\overline{\text{CKEN}}$  followed by the falling

edge of CLK will suspend all activities. The first data bit will clock on the rising edge, since the falling edge of  $\overline{\text{CKEN}}$  followed by the falling edge of the incoming clock triggers the enabling of the internal process. (See Figure 12)



**Figure 12. Timing Diagram with CKEN with CKSEL HIGH**

The differential PCLK output (pins 22 and 23) is a word framer and can help the user to synchronize the parallel data outputs. During CKSEL LOW operation, the PCLK will provide a divide by 4–clock frequency, which frames the serial data in period of PCLK output. Likewise during CKSEL HIGH operation, the PCLK will provide a divide by 8–clock frequency.

The  $V_{\text{BB}}$  pin, an internally generated voltage supply, is available to this device only. For single-ended input

conditions, the unused differential input is connected to  $V_{\text{BB}}$  as a switching reference voltage.  $V_{\text{BB}}$  may also rebias AC coupled inputs. When used, decouple  $V_{\text{BB}}$  and  $V_{\text{CC}}$  via a  $0.01 \mu\text{F}$  capacitor, which will limit the current sourcing or sinking to  $0.5\text{mA}$ . When not used,  $V_{\text{BB}}$  should be left open. Also, both outputs of the differential pair must be terminated ( $50 \Omega$  to  $V_{\text{TT}} = V_{\text{CC}} - 2 \text{V}$ ) even if only one output is used.

# MC10EP445, MC100EP445

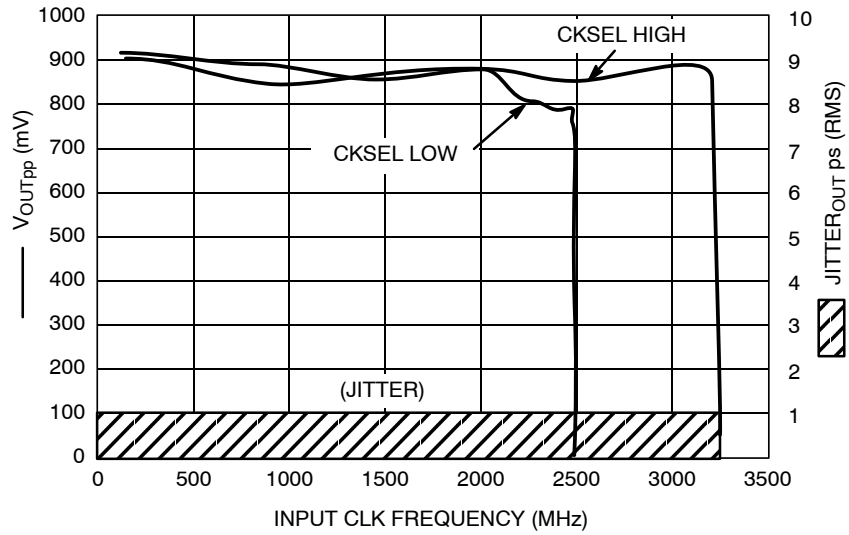


Figure 13.  $F_{max}/Jitter$

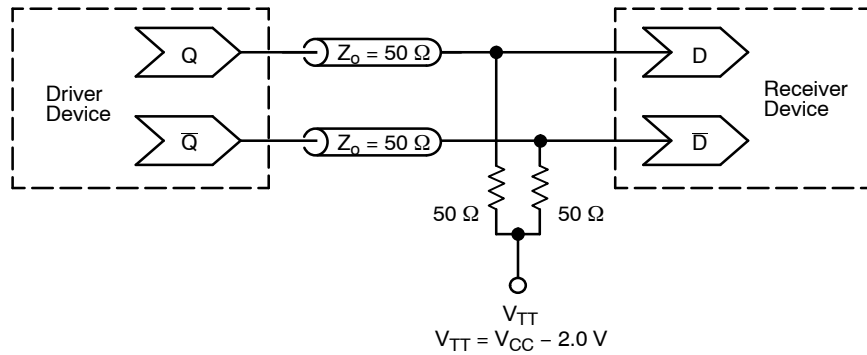


Figure 14. Typical Termination for Output Driver and Device Evaluation  
(See Application Note AND8020/D – Termination of ECL Logic Devices.)



# MC10EP445, MC100EP445

## ORDERING INFORMATION

| Device          | Package              | Shipping†          |
|-----------------|----------------------|--------------------|
| MC10EP445FA     | LQFP-32              | 250 Units / Tray   |
| MC10EP445FAG    | LQFP-32<br>(Pb-Free) | 250 Units / Tray   |
| MC10EP445FAR2   | LQFP-32              | 2000 / Tape & Reel |
| MC10EP445FAR2G  | LQFP-32<br>(Pb-Free) | 2000 / Tape & Reel |
| MC10EP445MNG    | QFN-32<br>(Pb-Free)  | 74 Units / Rail    |
| MC10EP445MNR4G  | QFN-32<br>(Pb-Free)  | 1000 / Tape & Reel |
| MC100EP445FAG   | LQFP-32<br>(Pb-Free) | 250 Units / Tray   |
| MC100EP445FAR2  | LQFP-32              | 2000 / Tape & Reel |
| MC100EP445FAR2G | LQFP-32<br>(Pb-Free) | 2000 / Tape & Reel |
| MC100EP445MNG   | QFN-32<br>(Pb-Free)  | 74 Units / Rail    |
| MC100EP445MNR4G | QFN-32<br>(Pb-Free)  | 1000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

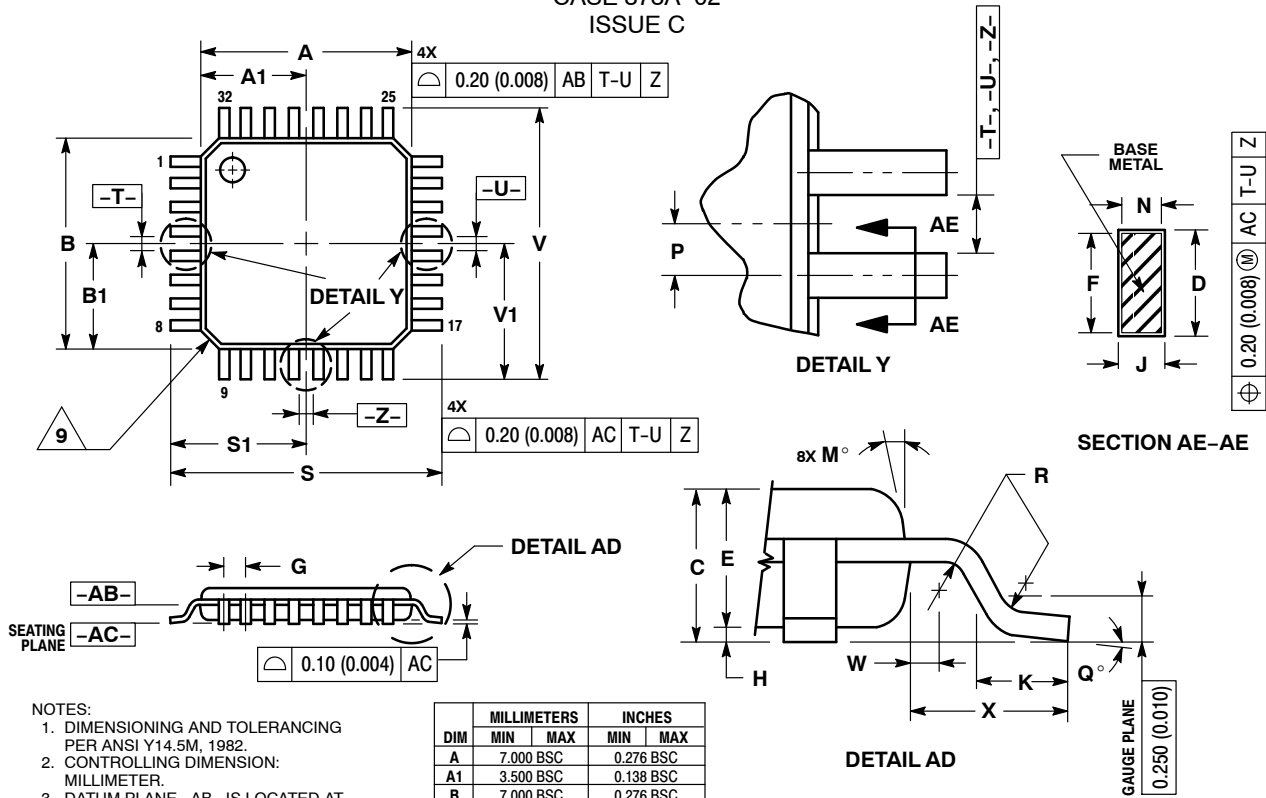
### Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPiCE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

# MC10EP445, MC100EP445

## PACKAGE DIMENSIONS

32 LEAD LQFP  
CASE 873A-02  
ISSUE C



**NOTES:**

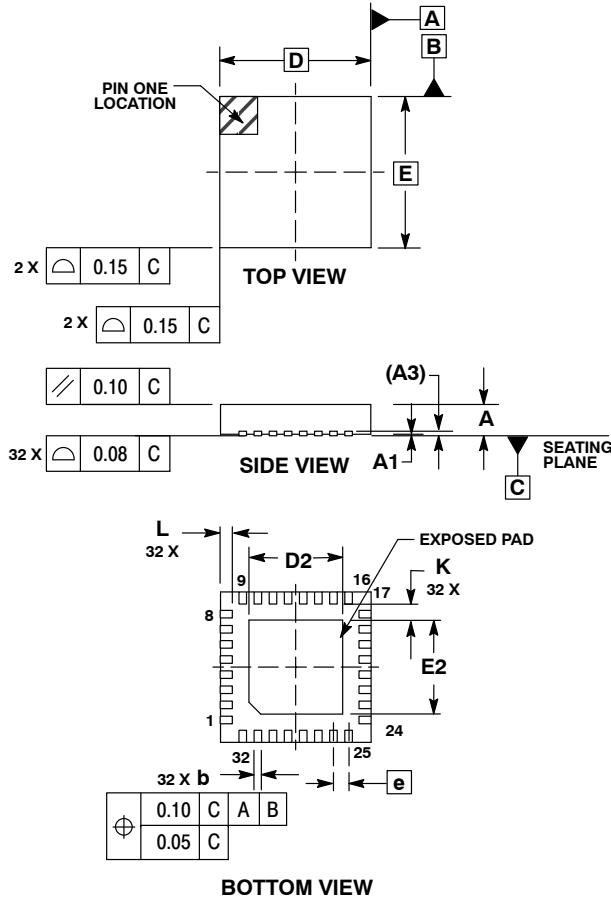
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -AB- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -T-, -U-, AND -Z- TO BE DETERMINED AT DATUM PLANE -AB-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -AC-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -AB-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

| DIM | MILLIMETERS |       | INCHES |       |
|-----|-------------|-------|--------|-------|
|     | MIN         | MAX   | MIN    | MAX   |
| A   | 7.000       | BSC   | 0.276  | BSC   |
| A1  | 3.500       | BSC   | 0.138  | BSC   |
| B   | 7.000       | BSC   | 0.276  | BSC   |
| B1  | 3.500       | BSC   | 0.138  | BSC   |
| C   | 1.400       | 1.600 | 0.055  | 0.063 |
| D   | 0.300       | 0.450 | 0.012  | 0.018 |
| E   | 1.350       | 1.450 | 0.053  | 0.057 |
| F   | 0.300       | 0.400 | 0.012  | 0.016 |
| G   | 0.800       | BSC   | 0.031  | BSC   |
| H   | 0.050       | 0.150 | 0.002  | 0.006 |
| J   | 0.090       | 0.200 | 0.004  | 0.008 |
| K   | 0.450       | 0.750 | 0.018  | 0.030 |
| M   | 12°         | REF   | 12°    | REF   |
| N   | 0.090       | 0.160 | 0.004  | 0.006 |
| P   | 0.400       | BSC   | 0.016  | BSC   |
| Q   | 1°          | 5°    | 1°     | 5°    |
| R   | 0.150       | 0.250 | 0.006  | 0.010 |
| S   | 9.000       | BSC   | 0.354  | BSC   |
| S1  | 4.500       | BSC   | 0.177  | BSC   |
| V   | 9.000       | BSC   | 0.354  | BSC   |
| V1  | 4.500       | BSC   | 0.177  | BSC   |
| W   | 0.200       | REF   | 0.008  | REF   |
| X   | 1.000       | REF   | 0.039  | REF   |

# MC10EP445, MC100EP445

## PACKAGE DIMENSIONS

QFN32 5\*5\*1 0.5 P  
CASE 488AM-01  
ISSUE O

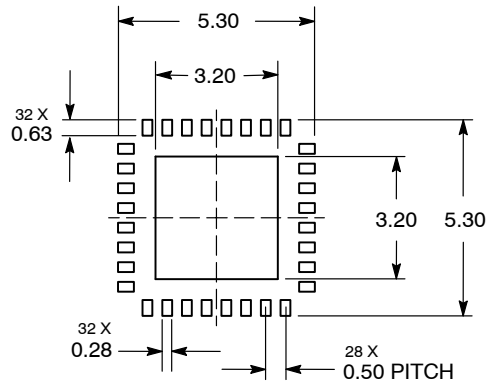


**NOTES:**

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| MILLIMETERS |           |       |       |
|-------------|-----------|-------|-------|
| DIM         | MIN       | NOM   | MAX   |
| A           | 0.800     | 0.900 | 1.000 |
| A1          | 0.000     | 0.025 | 0.050 |
| A3          | 0.200 REF |       |       |
| b           | 0.180     | 0.250 | 0.300 |
| D           | 5.00 BSC  |       |       |
| D2          | 2.950     | 3.100 | 3.250 |
| E           | 5.00 BSC  |       |       |
| E2          | 2.950     | 3.100 | 3.250 |
| e           | 0.500 BSC |       |       |
| K           | 0.200     | ---   | ---   |
| L           | 0.300     | 0.400 | 0.500 |

**SOLDERING FOOTPRINT\***



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.



Тел: +7 (812) 336 43 04 (многоканальный)

Email: [org@lifeelectronics.ru](mailto:org@lifeelectronics.ru)