Dual Serial 12-Bit Multiplying DAC

FEATURES

- **DNL and INL Over Temperature: ±0.5LSB Max**
- **Gain Error: ±1LSB Max**
- **Low Supply Current: 10μA Max**
- 4-Quadrant Multiplication
- Power-On Reset
- Asynchronous Clear Input
- Daisy-Chain 3-Wire Serial Interface
- 16-Pin Narrow SO and PDIP Packages

APPLICATIONS

- Process Control and Industrial Automation
- Software Controlled Gain Adjustment
- Digitally Controlled Filter and Power Supplies
- Automatic Test Equipment

DESCRIPTION

The LTC®1590 is a dual, serial input 12-bit multiplying digital-to-analog converter (DAC). It includes two current output multiplying CMOS DACs and an easy SPI compatible serial interface with daisy-chain output. An asynchronous $\overline{CLR}$ pin sets both DACs to zero scale.

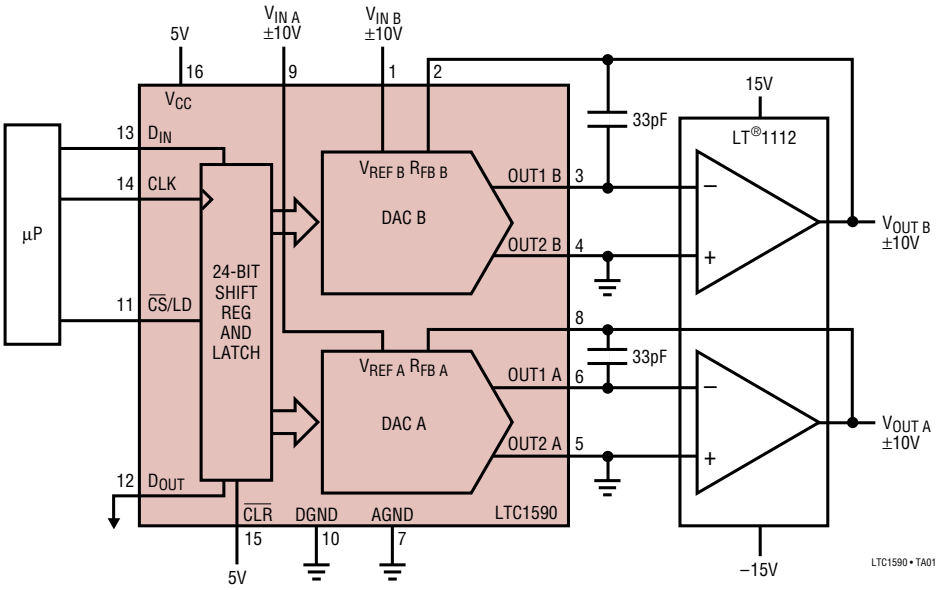
Excellent accuracy, stability and versatility are combined with the smallest package available for a dual 12-bit multiplying DAC.

Parts are available in 16-pin PDIP and narrow SO packages and are specified over the commercial and industrial temperature ranges.

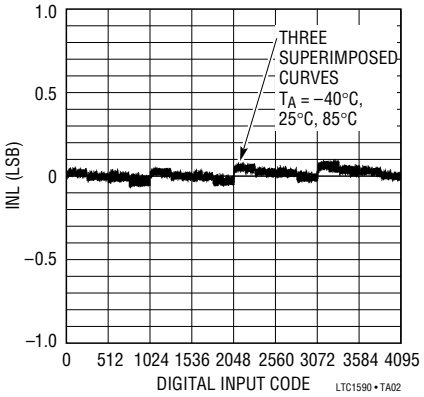
LT, LTC and LT are registered trademarks of Linear Technology Corporation.

TYPICAL APPLICATION

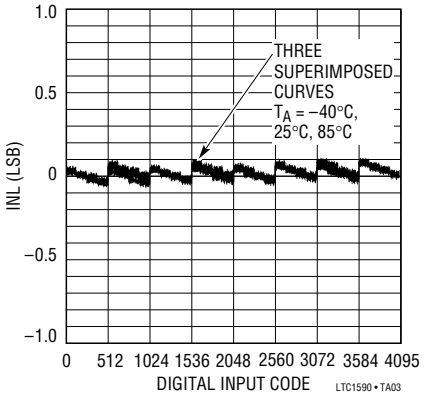
Dual 12-Bit 2-Quadrant Multiplying DAC



Integral Nonlinearity Over Temperature DAC A



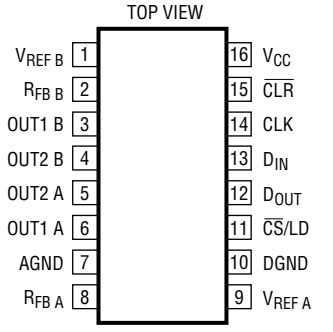
Integral Nonlinearity Over Temperature DAC B



ABSOLUTE MAXIMUM RATINGS

V_{CC} to AGND ..... −0.5V to 7V
V_{CC} to DGND ..... −0.5V to 7V
AGND to DGND ..... V_{CC} + 0.5V
DGND to AGND ..... V_{CC} + 0.5V
V_{REF} to AGND ..... ±25V
R_{FB} to AGND ..... ±25V
Digital Inputs to DGND ..... −0.5V to V_{CC} + 0.5V
V_{OUT1}, V_{OUT2} to AGND ..... −0.5V to V_{CC} + 0.5V
Maximum Junction Temperature ..... 150°C
Operating Temperature Range
LTC1590C ..... 0°C to 70°C
LTC1590I ..... −40°C to 85°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



N PACKAGE 16-LEAD PDIP
S PACKAGE 16-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 100°C/W (N)
T_{JMAX} = 150°C, θ_{JA} = 150°C/W (S)

ORDER PART NUMBER
LTC1590CN
LTC1590CS
LTC1590IN
LTC1590IS

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

V_{CC} = 4.5V to 5.5V, V_{REF} = 10V, V_{OUT1} = V_{OUT2} = AGND = DGND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Accuracy							
	Resolution		●	12			Bits
INL	Integral Nonlinearity	(Note 1)	●			±0.5	LSB
DNL	Differential Nonlinearity	Guaranteed Monotonic, T_{MIN} to T_{MAX}	●			±0.5	LSB
GE	Gain Error	(Note 2), T_A = 25°C				±1	LSB
		T_{MIN} to T_{MAX}	●			±2	LSB
	Gain Temperature Coefficient	(Note 3) ΔGain/ΔTemperature	●		1	5	ppm/°C
$I_{LEAKAGE}$	OUT1 A, OUT1 B Leakage Current	(Note 4), T_A = 25°C				±5	nA
		T_{MIN} to T_{MAX}	●			±25	nA
	Zero-Scale Error	T_A = 25°C				±0.03	LSB
		T_{MIN} to T_{MAX}	●			±0.15	LSB
PSRR	Power Supply Rejection	V_{CC} = 5V ±10%	●		±0.0001	±0.002	%/%
Reference Input							
R_{REF}	V_{REF} Input Resistance		●	8	11	15	kΩ
	V_{REFA}, V_{REFB} Input Resistance Match		●			3	%
AC Performance (Note 3)							
	Digital-to-Analog Glitch Impulse	(Notes 5, 6)			1		nV-s
	Multiplying Feedthrough Error	(Note 11)			−89	−80	dB
	Output Current Settling Time	(Note 5) To 0.01% for Full-Scale Change			0.3	0.8	µs
	Channel-to-Channel Isolation	(Note 7)				−90	dB
	Digital Crosstalk	(Notes 5, 8)			1		nV-s
	Output Noise Voltage Density	(Note 9)			13		nV/√Hz
THD	Total Harmonic Distortion	(Note 10)			−108	−92	dB
	Multiplying Bandwidth	(Note 12)			1		MHz

ELECTRICAL CHARACTERISTICS

V_{CC} = 4.5V to 5.5V, V_{REF} = 10V, V_{OUT1} = V_{OUT2} = AGND = DGND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Analog Outputs							
C_{OUT}	Output Capacitance (Note 3)	DAC Register Loaded to All 1s DAC Register Loaded to All 0s	● ●		60 30	90 60	pF pF
Digital Input							
V_{IH}	Digital Input High Voltage		●	2.4			V
V_{IL}	Digital Input Low Voltage		●			0.8	V
I_{IN}	Digital Input Current		●		0.001	±1	µA
C_{IN}	Digital Input Capacitance	(Note 3) V_{IN} = 0V	●			8	pF
Digital Output							
V_{OH}	Digital Output High Voltage	I_{OH} = 200µA	●	4			V
V_{OL}	Digital Output Low Voltage	I_{OH} = 1.6mA	●			0.4	V
Timing Characteristics							
t_1	D_{IN} to CLK Setup Time		●	50			ns
t_2	D_{IN} to CLK Setup Hold Time		●	0			ns
t_3	CLK High Time		●	40			ns
t_4	CLK Low Time		●	40			ns
t_5	$\overline{CS}$/LD High Time		●	50			ns
t_6	LSB CLK to $\overline{CS}$/LD		●	40			ns
t_7	$\overline{CS}$/LD Low to CLK High		●	20			ns
t_8	CLK Low to $\overline{CS}$/LD Low		●	20			ns
t_9	CLK to D_{OUT} Delay		●	10		160	ns
Power Supply							
V_{CC}	Operating Supply Range		●	4.5	5	5.5	V
I_{CC}	Supply Current	Digital Inputs = 0V or V_{CC}	●			10	µA

The ● denotes specifications which apply over the full operating temperature range.

Note 1: ±0.5LSB = ±0.012% of full scale.

Note 2: Using internal feedback resistor.

Note 3: Guaranteed by design, not subject to test.

Note 4: I_{OUT1} with DAC register loaded with all 0s.

Note 5: OUT1 load = 100Ω in parallel with 13pF.

Note 6: V_{REF} = 0V. DAC register contents changed from all 0s to all 1s or all 1s to all 0s.

Note 7: DAC A output with $V_{REF\,A}$ = 0V and $V_{REF\,B}$ = 10kHz $20V_{P-P}$, or DAC B output with $V_{REF\,B}$ = 0V, $V_{REF\,A}$ = 10kHz $20V_{P-P}$. Both DAC registers loaded with all 1s.

Note 8: Glitch on DAC A or DAC B output when the other DAC makes a full-scale transition.

Note 9: 10Hz to 100kHz. Calculation from $e_n = \sqrt{4KTRB}$ where:
K = Boltzmann constant (J/K°); R = resistance (Ω); T = resistor temperature (°K); B = bandwidth (Hz).

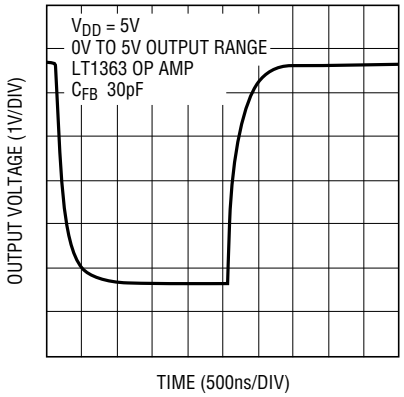
Note10: V_{REF} = $6V_{RMS}$ at 1kHz. DAC register loaded with all 1s, using LT®1124 op amp.

Note 11: V_{REF} = ±10V, 10kHz sine wave, DAC register loaded with all 0s, using LT1358 op amp.

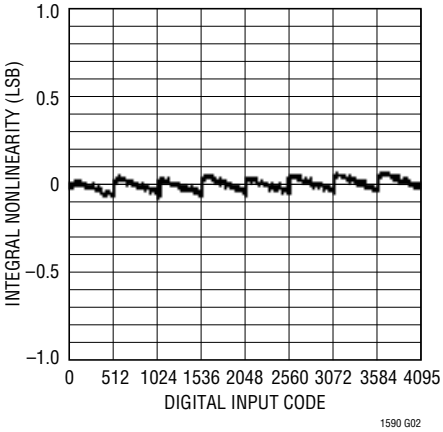
Note 12: –3dB bandwidth using LT1358 op amp.

TYPICAL PERFORMANCE CHARACTERISTICS

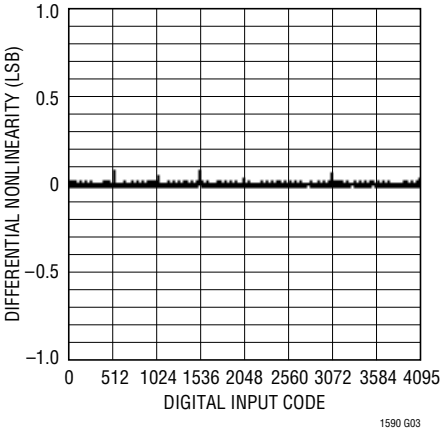
Full-Scale Settling Waveform



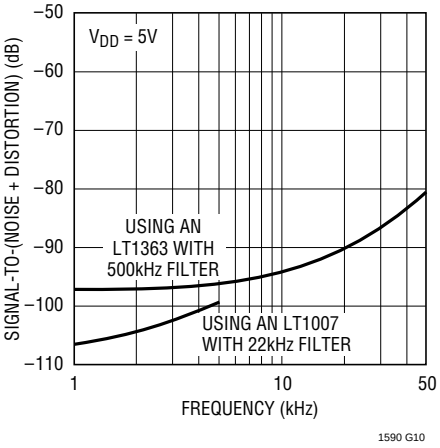
Integral Nonlinearity (INL)



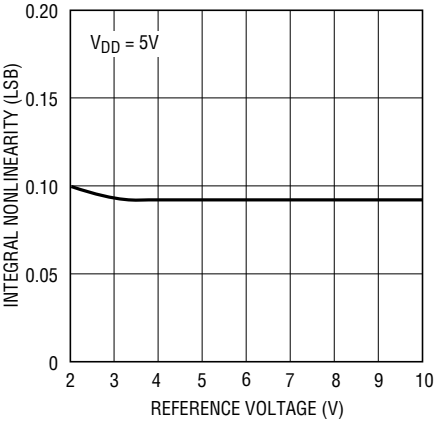
Differential Nonlinearity (DNL)



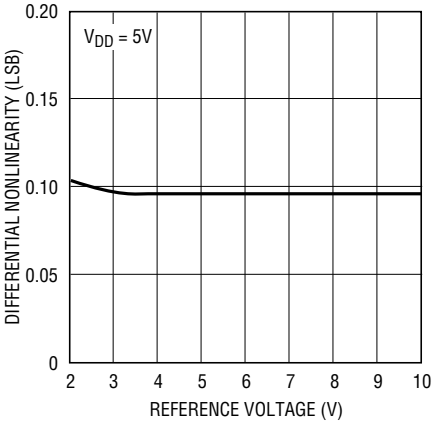
Multiplying Mode Signal-to-(Noise + Distortion) vs Frequency



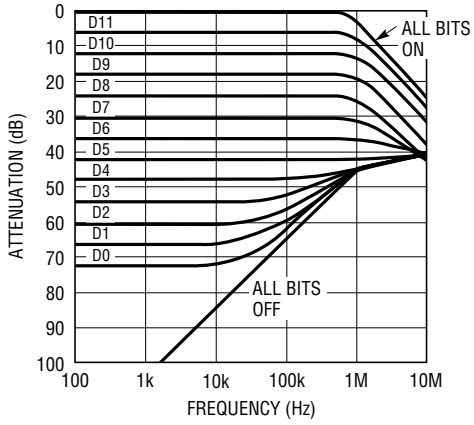
Integral Nonlinearity vs Reference Voltage



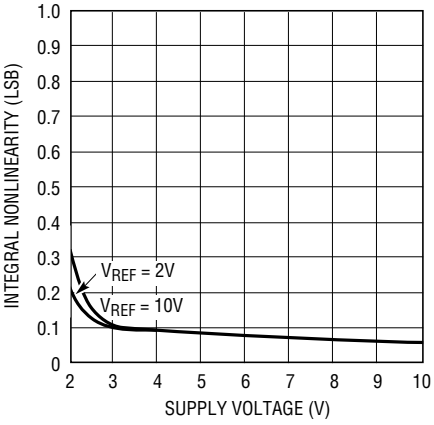
Differential Nonlinearity vs Reference Voltage



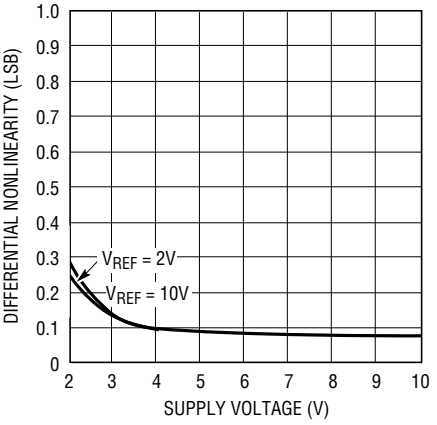
Multiplying Mode Frequency Response vs Digital Code



Integral Nonlinearity vs Supply Voltage

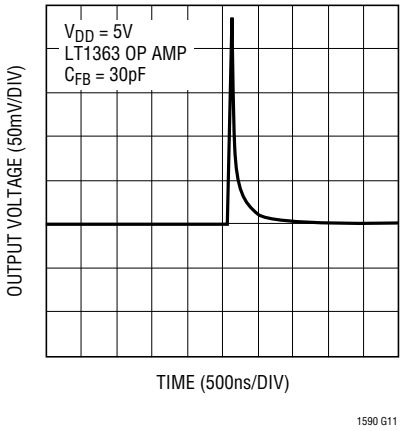


Differential Nonlinearity vs Supply Voltage

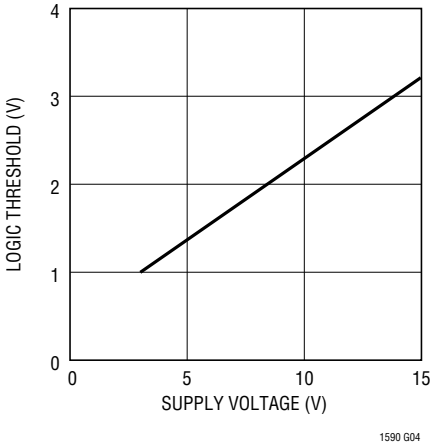


TYPICAL PERFORMANCE CHARACTERISTICS

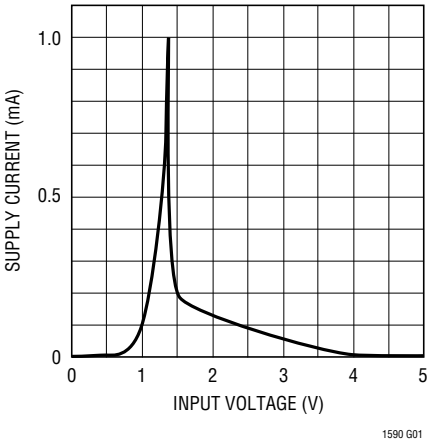
Midscale Glitch Impulse



Logic Threshold vs Supply Voltage



Supply Current vs Logic Input Voltage



PIN FUNCTIONS

$V_{REF\ B}$, $V_{REF\ A}$ (Pins 1, 9): Reference Inputs for DAC A/B. Typically ±10V, accepts up to ±25V.

$R_{FB\ B}$, $R_{FB\ A}$ (Pins 2, 8): Feedback Resistors for DAC A/B. Normally tied to the output of current to voltage converter op amp. Typically swings to ±10V. Swings from 0V to $-V_{REF}$.

OUT1 B, OUT1 A (Pins 3, 6): True Current Output for DAC A/B. Normally tied to inverting input of current to voltage converter op amp.

OUT2 B, OUT2 A (Pins 4, 5): Complement Current Output for DAC A/B. Normally tied to ground.

AGND (Pin 7): Analog Ground Pin. Tie to ground.

DGND (Pin 10): Digital Ground Pin. Tie to ground.

$\overline{CS}$/LD (Pin 11): The Serial Interface Enable and Load Control Input. When $\overline{CS}$/LD is low the CLK signal is enabled so the data can be clocked in. When $\overline{CS}$/LD is pulled high, data is loaded from the shift register into the DAC register, updating the DAC output.

D_{OUT} (Pin 12): The Serial Data Output. Data becomes valid on the rising edge of the CLK.

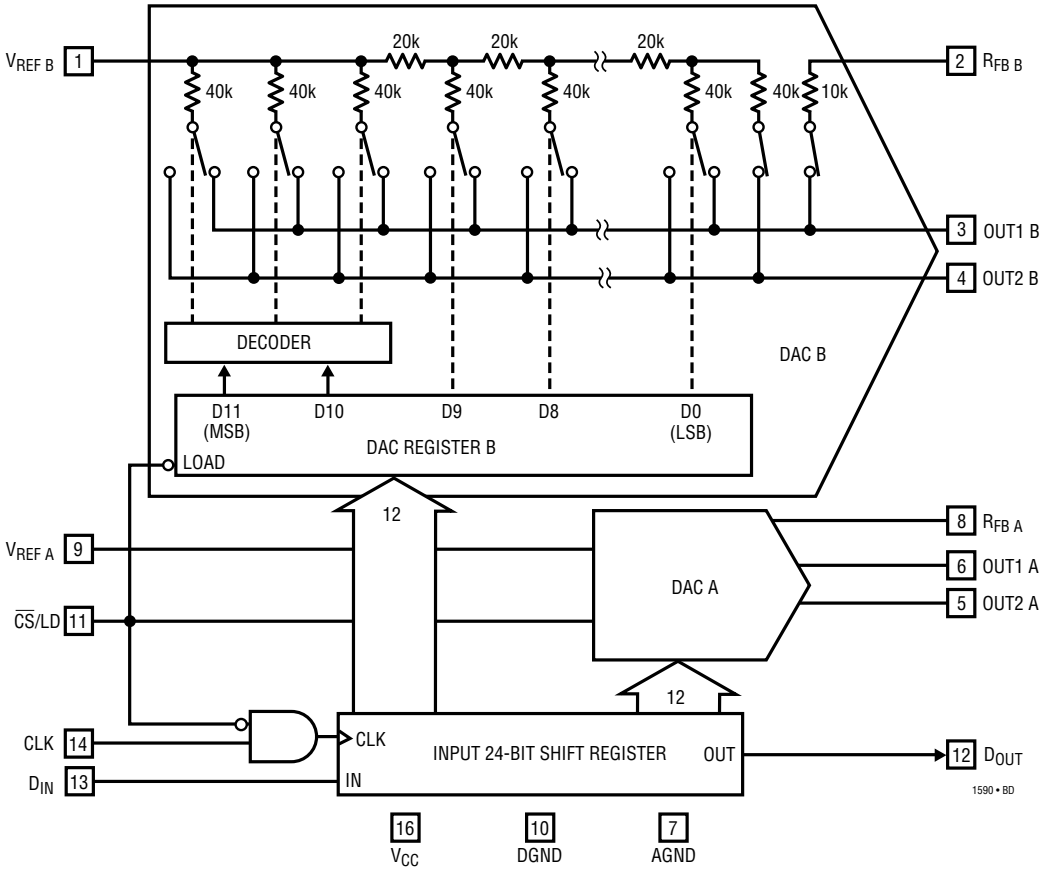
D_{IN} (Pin 13): The Serial Data Input. Data on the D_{IN} pin is latched into the shift register on the rising edge of the serial clock. Data is loaded as one 24-bit word. The first 12 bits are for DAC A, MSB-first and the second 12 bits are for DAC B, MSB-first.

CLK (Pin 14): The Serial Interface Clock Input.

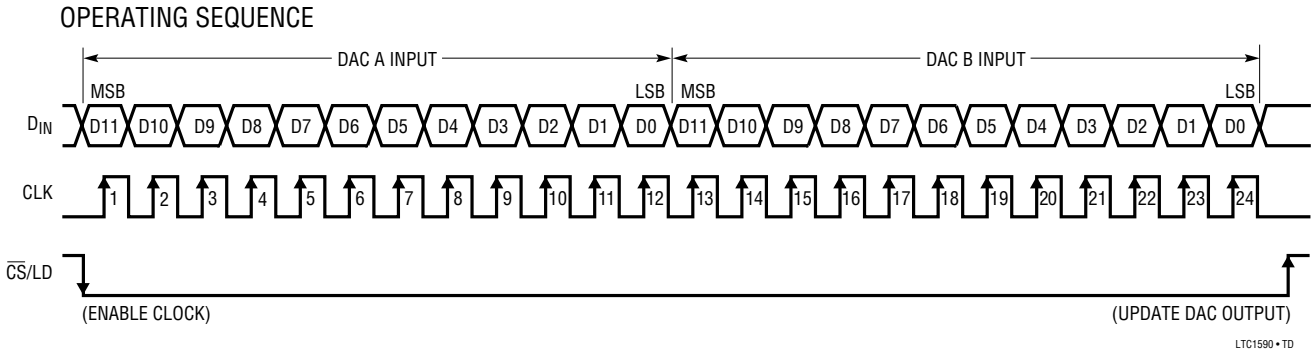
$\overline{CLR}$ (Pin 15): The Clear Pin for the DAC. Clears both DACs to zero scale when pulled low. This pin should be tied to V_{CC} for normal operation.

V_{CC} (Pin 16): The Positive Supply Input. $4.5 \leq V_{CC} \leq 5.5V$. Requires a bypass capacitor to ground.

BLOCK DIAGRAM

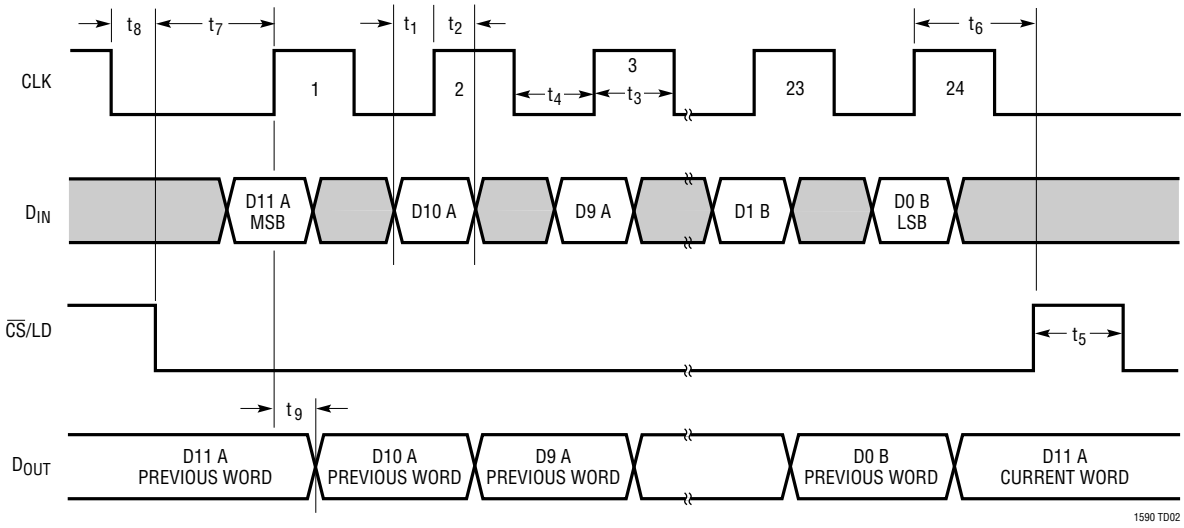


TIMING DIAGRAMS



TIMING DIAGRAMS

TIMING DIAGRAM



APPLICATIONS INFORMATION

Description

The LTC1590 is a dual 12-bit multiplying DAC that has serial inputs and current outputs. It uses precision R/2R resistor ladder technology to provide exceptional linearity and stability. The device operates from a single 5V supply and provides a ±10V reference input and voltage output range when used with an external op amp.

Serial I/O

The LTC1590 has a 3-wire SPI/MICROWIRE™ compatible serial port that accepts 24-bit serial words. Data is loaded MSB first with the first 12 bits controlling DAC A and the second 12 bits controlling DAC B. Data is shifted into the D_{IN} input on the rising edge of CLK. The $\overline{CS}$/LD input must be taken low before transferring data to enable the CLK input. After transferring data, $\overline{CS}$/LD is pulled high to load data from the shift register to the DAC registers which updates both DACs.

The buffered output of the 24-bit shift register is available on the D_{OUT} pin. Multiple DACs can be daisy-chained on one 3-wire interface by connecting the D_{OUT} pin to the D_{IN} pin of the next DAC (see the Timing Diagrams section).

MICROWIRE is a trademark of National Semiconductor Corporation.

Equivalent Circuit

Figure 1 shows an equivalent analog circuit for the LTC1590 DACs. R is the reference input, R_{REF}, which is nominally 11k. The DAC output is represented by the Thevinin equivalent current source with a value of:

$$(Code/4096)(V_{REF}/R)$$

The current source I_{LKG} models the junction leakage of the DAC output switches. I_{LKG} is typically less than 5nA at 85°C and decreases by roughly two times for every 10°C reduction in temperature. C_{OUT} is the output capacitance, and it also comes from the DAC output switches and varies from 30pF at zero scale to 60pF at full scale. R_O is the equivalent output resistance, which varies with digital input code (see Op Amp Selection section).

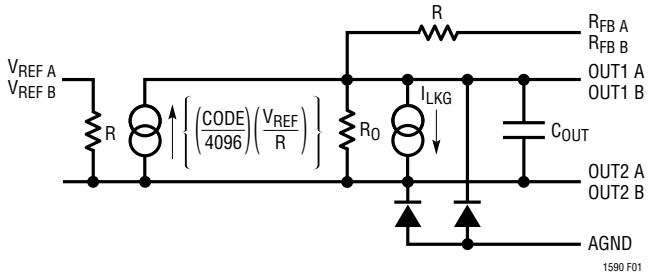


Figure 1. Equivalent Circuit

APPLICATIONS INFORMATION

Unipolar 2-Quadrant Multiplying Mode (V_{OUT} = 0V to $-V_{REF}$)

The LTC1590 can be used with a dual op amp to provide a dual 2-quadrant multiplying DAC as shown in Figure 2. The unipolar DAC transfer function is shown in Table 1. The 33pF feedback capacitor is recommended to compensate for the pole caused by the internal feedback resistor and the OUT1 output capacitance. For high speed op amps this feedback capacitor is required for stability, and a smaller value, 8pF to 15pF, may be desired to get the fastest transient response and shortest settling time. A larger feedback capacitor can be used to reduce wideband noise, glitch impulse and distortion for lower frequency signals. A pole is introduced in the DAC transfer function at approximately $(C_{FB})(R_{FB})$. For example, a 100pF feedback capacitor will typically give a pole at:

$$145kHz = \frac{1}{2\pi(100pF)(11k\Omega)}$$

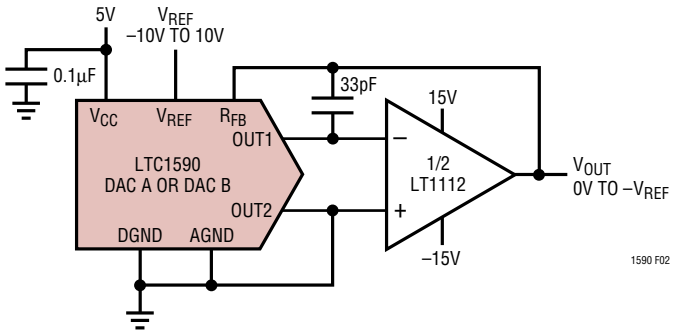


Figure 2. Unipolar Operation (2-Quadrant Multiplication)

Table 1. Unipolar Binary Code Table

DIGITAL INPUT BINARY NUMBER IN DAC REGISTER			ANALOG OUTPUT V_{OUT}
MSB		LSB	
1111	1111	1111	$-V_{REF}$ (4095/4096)
1000	0000	0000	$-V_{REF}$ (2048/4096) = $-V_{REF}/2$
0000	0000	0001	$-V_{REF}$ (1/4096)
0000	0000	0000	0V

Bipolar 4-Quadrant Multiplying Mode ($V_{OUT} = -V_{REF}$ to $+V_{REF}$)

The circuit of Figure 3 can be used to provide a dual 4-quadrant multiplying DAC. This circuit starts with the unipolar application circuit and adds three resistors and an op amp. These extra devices provide a gain of –2 from the unipolar output to the bipolar output, plus an offset of $(-1)(V_{REF})$ to produce the transfer function shown in Table 2. A pack of matched 20k resistors, with two resistors in parallel forming the 10k resistor, is recommended.

Table 2. Bipolar Offset Binary Code Table

DIGITAL INPUT BINARY NUMBER IN DAC REGISTER			ANALOG OUTPUT V_{OUT}
MSB		LSB	
1111	1111	1111	$+V_{REF}$ (2047/2048)
1000	0000	0001	$+V_{REF}$ (1/2048)
1000	0000	0000	0V
0111	1111	1111	$-V_{REF}$ (1/2048)
0000	0000	0000	$-V_{REF}$ (2048/2048) = $-V_{REF}$

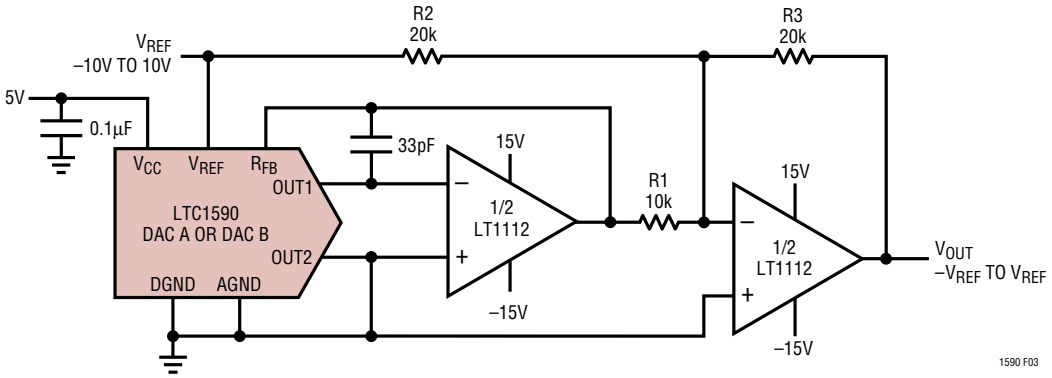


Figure 3. Bipolar Operation (4-Quadrant Multiplication)

APPLICATIONS INFORMATION

Op Amp Selection

To maintain the excellent accuracy and stability of the LTC1590 thought should be given to op amp selection. Fortunately, the sensitivity of INL and DNL to op amp offset has been significantly reduced compared to competing parts of this type. The op amp's V_{OS} causes DAC output offset. In addition, because the DAC's equivalent output resistance R_O changes as a function of code, there is a code-dependent DAC output error proportional to V_{OS}. For fixed reference applications this causes gain, INL and DNL error. For multiplying applications, a code-dependent, DC output voltage error is seen. At zero scale the DAC output error is equal to the op amp offset, and at full scale the output error is equal to twice the op amp offset. For example, a 1mV op amp offset will cause a 0.41LSB zero-scale error and a 0.82LSB full-scale error with a 10V full-scale range. The offset caused INL error is approximately 0.4 times the op amp V_{OS} and DNL error is 0.07 times op amp V_{OS}. For the same example of 1mV op amp V_{OS} and 10V full-scale range, the INL degradation will be 0.17LSB and DNL degradation will be 0.03LSB.

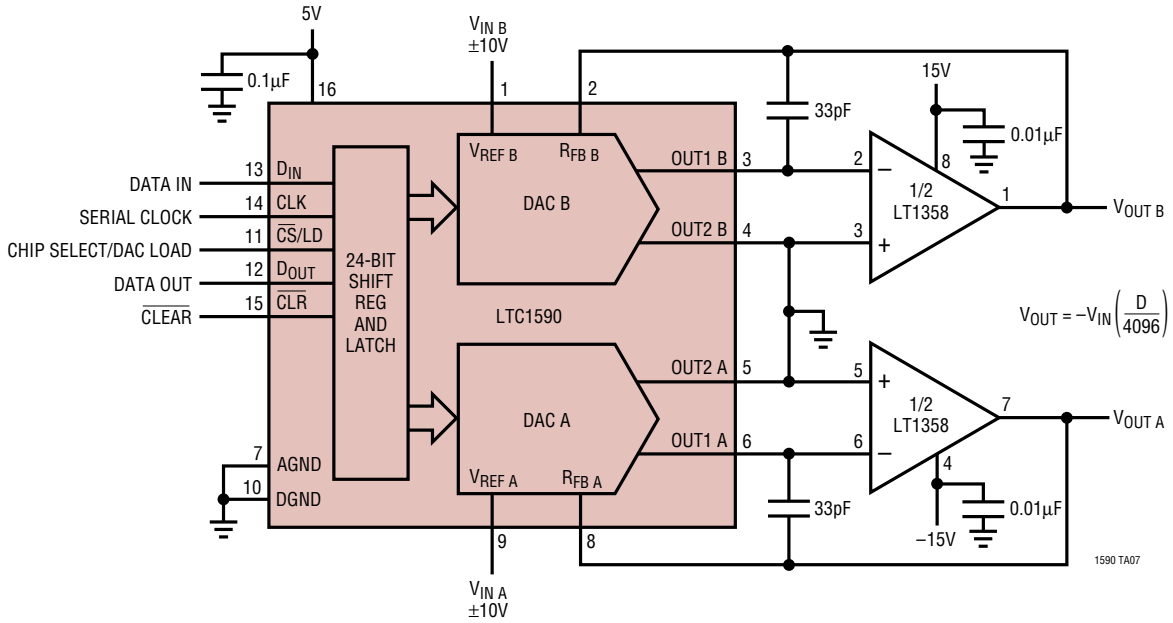
Op amp bias current causes only an offset error equal to $(I_{BIAS})(R_{FB}) \approx (I_{BIAS})(11k\Omega)$. For example, a 100nA op amp bias current causes a 1.1mV DAC offset, or 0.45LSB for a 10V full-scale range. It is important to note that connecting the op amp noninverting input to ground through a resistor will not cancel bias current errors and should never be done! Similarly an offset caused by op amp bias current should not be adjusted by using the op amp null pins since this increases offset between DAC OUT1 and OUT2 pins, causing INL, DNL and gain errors. If op amp offset error adjustment is required, the op amp input offset voltage (the voltage difference between OUT1 and OUT2) should be nulled.

Grounding

As with any high precision data converter, clean grounding is important. A low impedance analog ground plane and star grounding should be used. OUT2 carries the complementary DAC output current and should be tied to the star ground with as low a resistance as possible. Other ground points that must be tied to the star ground point include the V_{REF} input ground, the op amp noninverting input(s) and the V_{OUT} ground reference point.

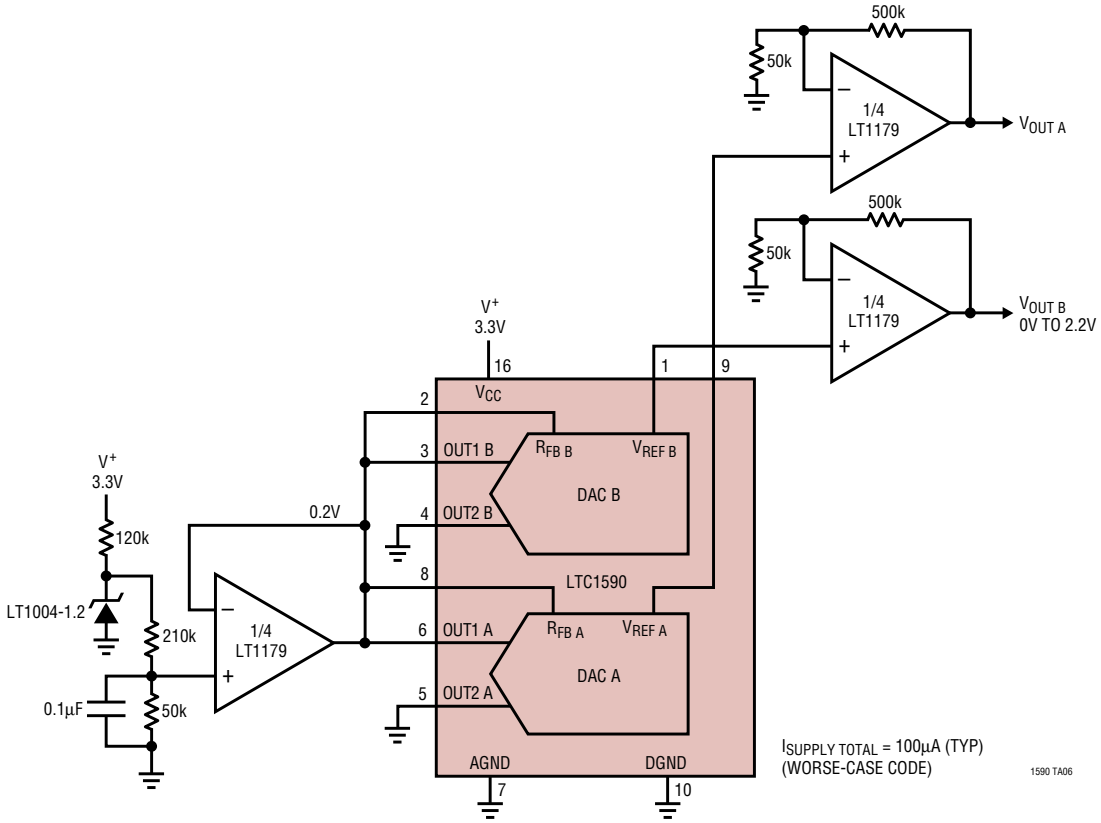
TYPICAL APPLICATIONS

Dual Programmable Attenuator

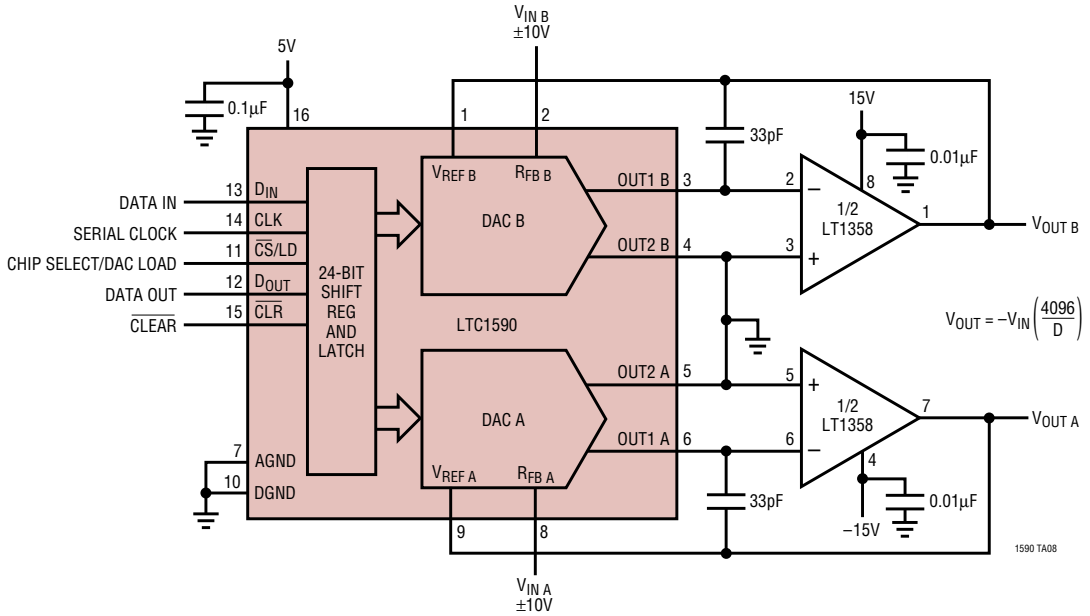


TYPICAL APPLICATIONS

Very Low Power Single Supply Dual V_{OUT} DAC

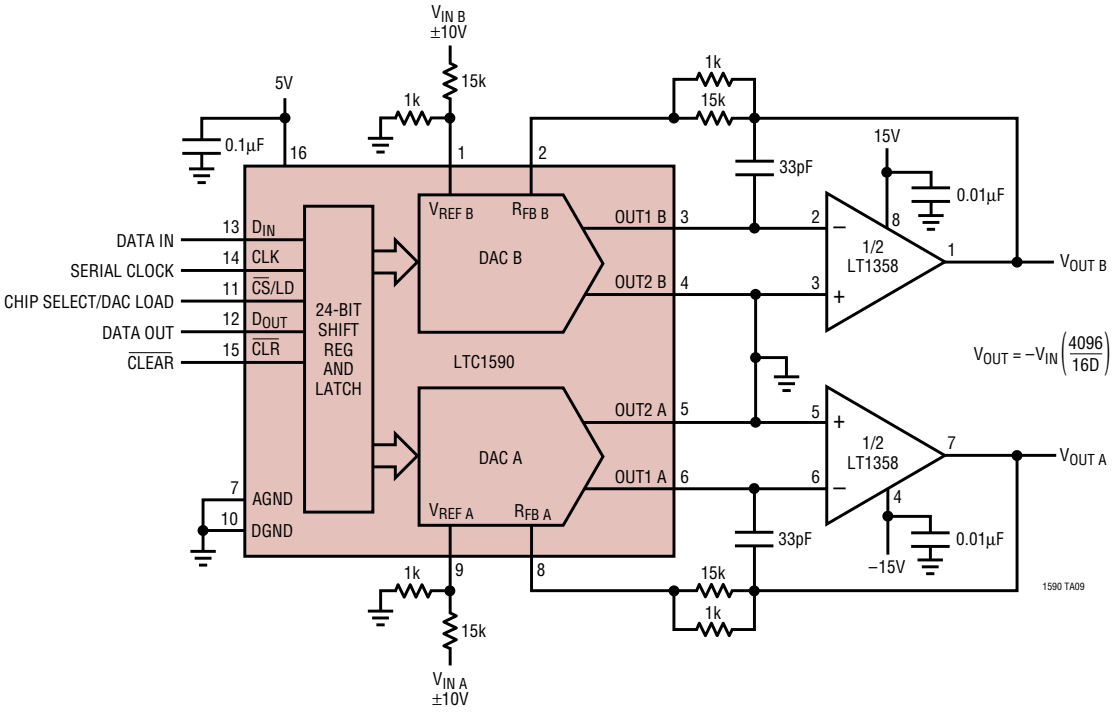


Dual Programmable Gain Amplifier



TYPICAL APPLICATIONS

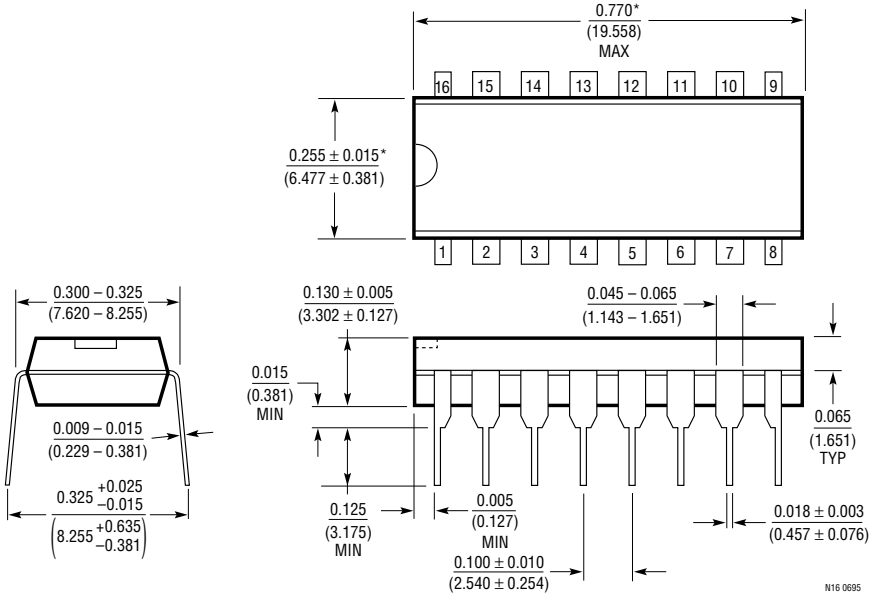
Dual Programmable Gain Amplifier with Input Attenuation



PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

N Package
16-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)



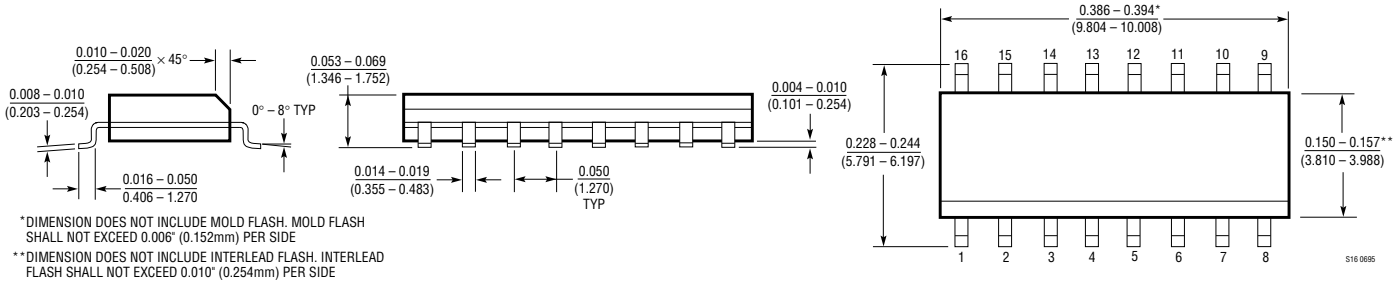
*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

S Package
16-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)

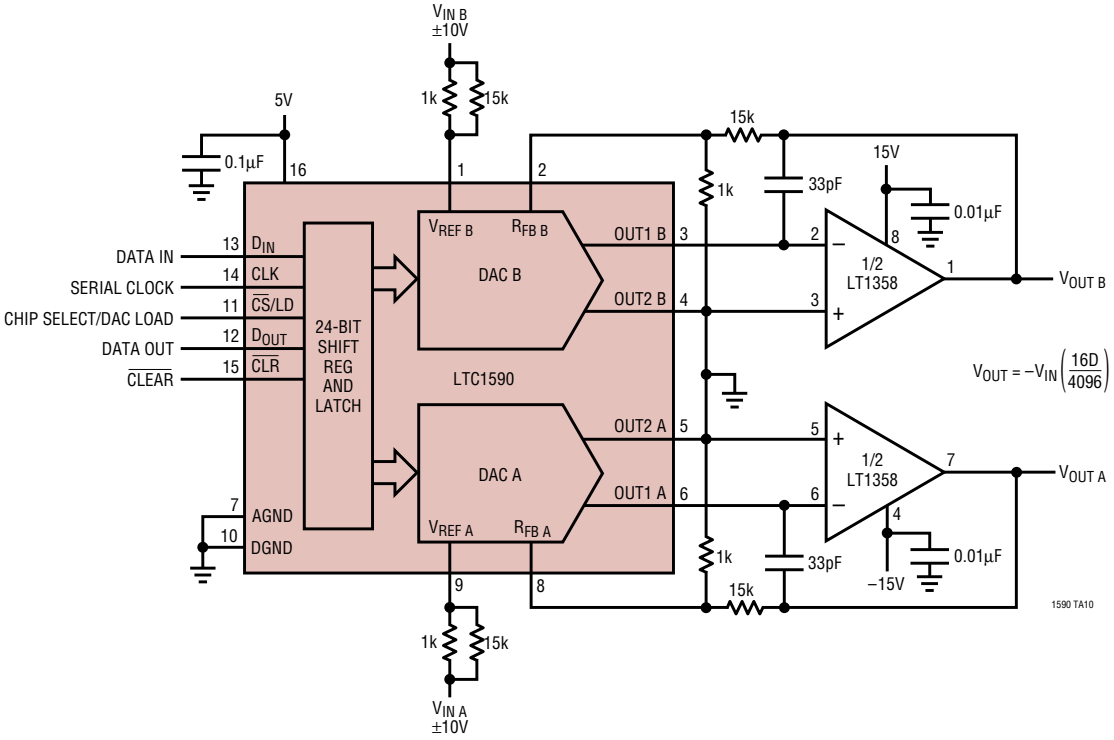


*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

TYPICAL APPLICATION

Dual Programmable Attenuator with Gain



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1595	16-Bit Multiplying I_{OUT} DAC in SO-8	True 16-Bit Upgrade for DAC8043
LTC1596	16-Bit Multiplying I_{OUT} DAC	True 16-Bit Upgrade for DAC8143 and AD7543
LTC7541A	Parallel I/O Multiplying I_{OUT} 12-Bit DAC	12-Bit Wide Parallel Input
LTC7543/LTC8143	Serial I/O Multiplying I_{OUT} 12-Bit DACs	Clear Pin and Serial Data Output (LTC8143)
LTC7545A	Parallel I/O Multiplying I_{OUT} 12-Bit DAC	12-Bit Wide Latched Parallel Input
LTC8043	Serial I/O Multiplying I_{OUT} 12-Bit DAC	8-Pin SO and PDIP

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LifeElectronics
Живое партнерство

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- *Входной контроль качества.*
- *Наличие сертификата ISO.*

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- *Защиту от снятия компонента с производства.*
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