

## 7A V•I Chip™ EMI Filter SIP

### Description:

The QPI-11 EMI filter is specifically designed to attenuate conducted common-mode (CM) and differential-mode (DM) noise of Vicor's V•I Chip™ PRM/VTM factorized power products to comply with the CISPR22 standard requirements for conducted noise measurements. The filter is designed to operate up to 50 Vdc, 100 Vdc surge, and supports 7A loads up to 85°C (T<sub>A</sub>) without de-rating.

Designed for the industrial bus range, the V•I Chip™ EMI Filter supports the PICMG® 3.0 specification for filtering system boards to the EN55022 Class B limits.



Figure 1 - QPI-11LZ (~1/2 in<sup>2</sup> area)

### Features:

- >60 dB CM attenuation at 1 MHz (50Ω)
- >70 dB DM attenuation at 1 MHz (50Ω)
- 50 Vdc (max input)
- 100 Vdc surge 100 ms
- 750 Vdc hi-pot hold off to shield plane
- 7 A rating
- 12.9 x 25.3 x 5.0 mm Lidded SiP (System-in-Package)
- 12.4 x 24.9 x 3.4 mm Open-frame SiP
- Low profile LGA package
- -40° to +125°C PCB temperature (see Figure 6)
- Efficiency >99%
- TÜV Certified

### Applications

- V•I Chip™ input EMI filter

### Typical Applications:

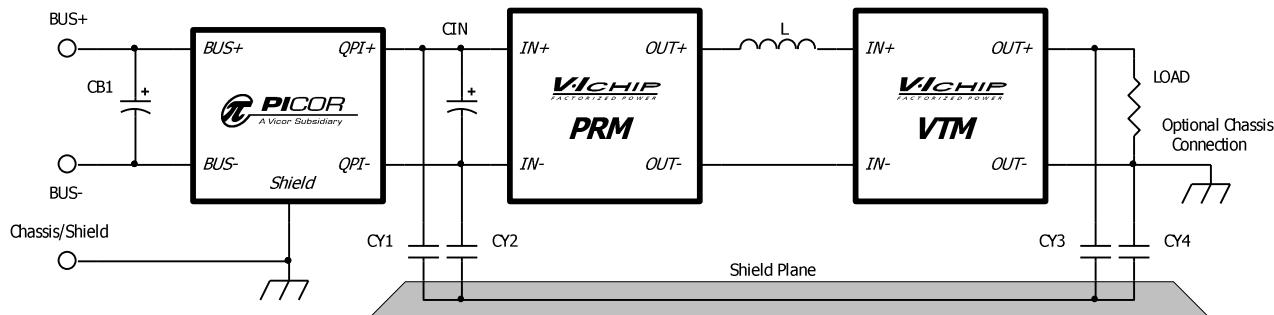


Figure 2 – Typical QPI-11 application schematic with Vicor's PRM and VTM modules in a base-plate configuration.<sup>(1)</sup>

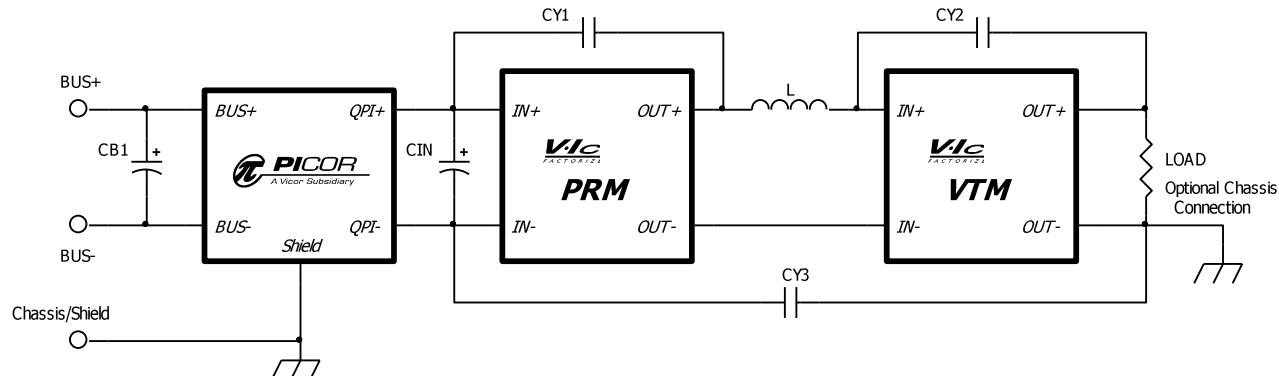


Figure 3 – Typical QPI-11 application schematic with Vicor's PRM and VTM modules in an open-frame configuration.<sup>(1)</sup>

**Note 1:** CB1 capacitor, referenced in all schematics, is a 47uF electrolytic; United Chemi-Con EMVE101ARA470MKE05 or equivalent.  
 CY1 to CY4, referenced in all schematics, are 4.7nF hi-voltage safety capacitors; Vishay VY1472M63Y5UQ63V0 or equivalent.

**Absolute Maximum Ratings** – Exceeding these parameters may result in permanent damage to the product.

|  |                 |
|--|-----------------|
| Input Voltage, BUS+ to BUS-, continuous  | -50 to 50 Vdc   |
| Input Voltage, BUS+ to BUS-, 100ms transient   | -100 to 100 Vdc |
| BUS+/ BUS- to Shield pads, hi-pot  | -750 to 750 Vdc |
| Input to output current, continuous @ 25°C $T_A$                                     | 7 Adc           |
| Power dissipation, @ 85°C $T_A$ , 7A <sup>(2)</sup>                                  | 1.85 W          |
| Operating temperature - $T_A$  | -40 to 125 °C   |
| Thermal resistance <sup>(2)</sup> - $R_{\theta H-A}$ , using PCB layout in Figure 20 | 30 °C/W         |
| Thermal resistance <sup>(2)</sup> - $R_{\theta H-PCB}$                               | 18 °C/W         |
| Storage temperature, JEDEC Standard J-STD-033B                                       | -55 to 125 °C   |
| Reflow temperature, 20 s exposure  | 245 °C          |
| ESD, Human body model (HBM)  | -2000 to 2000 V |

**Electrical Characteristics** – Parameter limits apply over the operating temp. range, unless otherwise noted.

| Parameter                     | Notes  | Min | Typ | Max | Units |
|-------------------------------|--|-----|-----|-----|-------|
| BUS+ to BUS- input range      | Measured at 7 A, 85°C ambient temperature <sup>(2)</sup> |     |     | 50  | Vdc   |
| BUS+ to QPI+ voltage drop     | Measured at 7 A, 85°C ambient temperature <sup>(2)</sup> |     |     | 130 | mVdc  |
| BUS- to QPI- voltage drop     | Measured at 7 A, 85°C ambient temperature <sup>(2)</sup> |     |     | 130 | mVdc  |
| Common mode attenuation       | VBUS = 24 V, Frequency = 1.0 MHz, line impedance = 50Ω   | 60  |     |     | dB    |
| Differential mode attenuation | VBUS = 24 V, Frequency = 1.0 MHz, line impedance = 50Ω   | 70  |     |     | dB    |
| Input bias current at 50 V    | Input current from BUS+ to BUS-                          |     |     | 10  | uA    |

**Note 2:** See Figure 6 for current de-rating curve.

**Pad Descriptions**

| Pad Number | Name   | Description   | LGA Pattern (Top View) |    |   |      |
|------------|--------|---|------------------------|----|---|------|
| 8, 9       | BUS+   | Positive bus potential                                  | BUS+                   | 9  | 8 | 7    |
| 1, 10      | BUS-   | Negative bus potential                                  | BUS-                   | 10 |   | 6    |
| 6, 7       | QPI+   | Positive input to the converter                         |                        |    |   | QPI+ |
| 4, 5       | QPI-   | Negative input to the converter                         |                        |    |   | QPI- |
| 2, 3       | Shield | Shield connects to the system chassis or safety ground. |                        | 1  | 2 | 3    |
|            |        |   |                        |    | 4 | QPI- |

**Ordering Information**

| Part Number             | Description  |
|-------------------------|--|
| QPI-11LZ <sup>(3)</sup> | QPI-11 LGA Package, RoHS Compliant                     |
| QPI-11LZ-01             | QPI-11 LGA Package, RoHS Compliant, Open Frame Package |

**Note 3:** QPI-11LZ is a non-hermetically sealed package. Please read the "Post Solder Cleaning" section on page 10.

**QPI-11 Evaluation Boards**

| Part #     | Description:  |
|------------|---|
| QPI-11-CB1 | A QPI-11LZ mounted on a carrier board that can hold either a stand-alone BCM or a paired PRM/VTM evaluation board available from Vicor. |

## Applications Information

### EMI Sources

Many of the components in today's power conversion modules are sources of high-frequency EMI noise generation. Diodes, high-frequency switching devices, transformers and inductors, and circuit layouts passing high dv/dt or di/dt signals are all potential sources of EMI.

EMI is propagated either by radiated or conductive means. Radiated EMI can be sourced from these components as well as by circuit loops that act like antennas and broadcast the noise signals to neighboring circuit paths. This also means that these loops can act as receivers of a broadcasted signal. This radiated EMI noise can be reduced by proper circuit layout and by shielding potential sources of EMI transmission.

There are two basic forms of conducted EMI that typically need to be filtered; namely common-mode (CM) and differential-mode (DM) EMI. Differential-mode resides in the normal power loop of a power source and its load; where the signal travels from the source to the load and then returns to the source.

Common-mode is a signal that travels through both leads of the source and is returned to earth via parasitic pathways, either capacitively or inductively coupled.

Figure 10 to Figure 13 are the resulting EMI plots of the total noise, both common and differential mode, of Vicor's PRM/VTM evaluation modules, under various loads, after filtering by the QPI-11LZ. The red and blue traces represent the positive and negative branches of total noise, as measured using an industry standard LISN setup, shown in Figures 4 and 5. The PRM and VTM evaluation boards are mounted to a Picor QPI-11-CB1 board for testing.

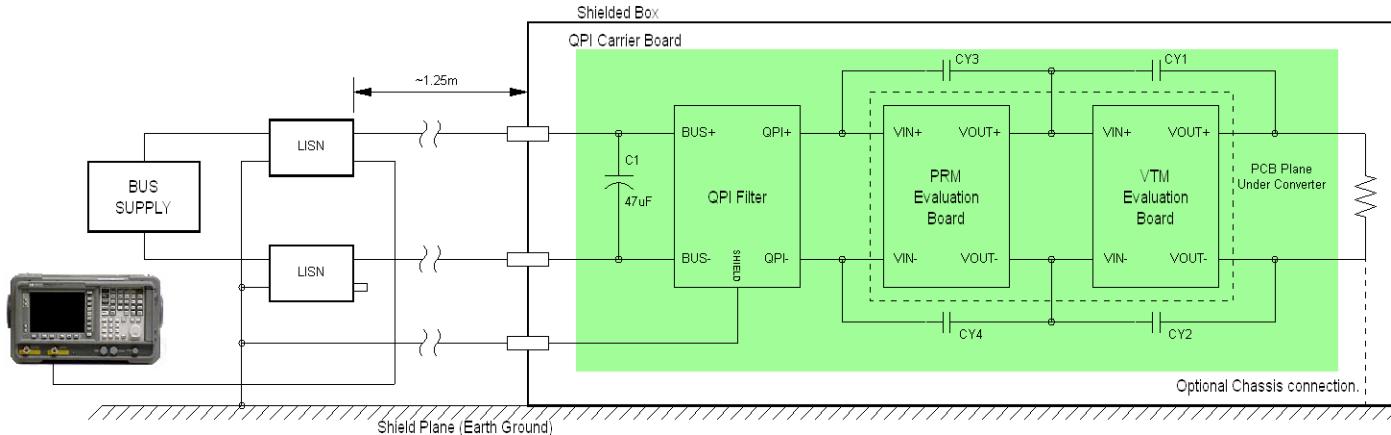
The Differential-mode EMI is typically larger in magnitude than common-mode, since common-mode is created by the physical imbalances in the differential loop path. Reducing differential EMI will cause a reduction in common-mode EMI.

### EMI Filtering

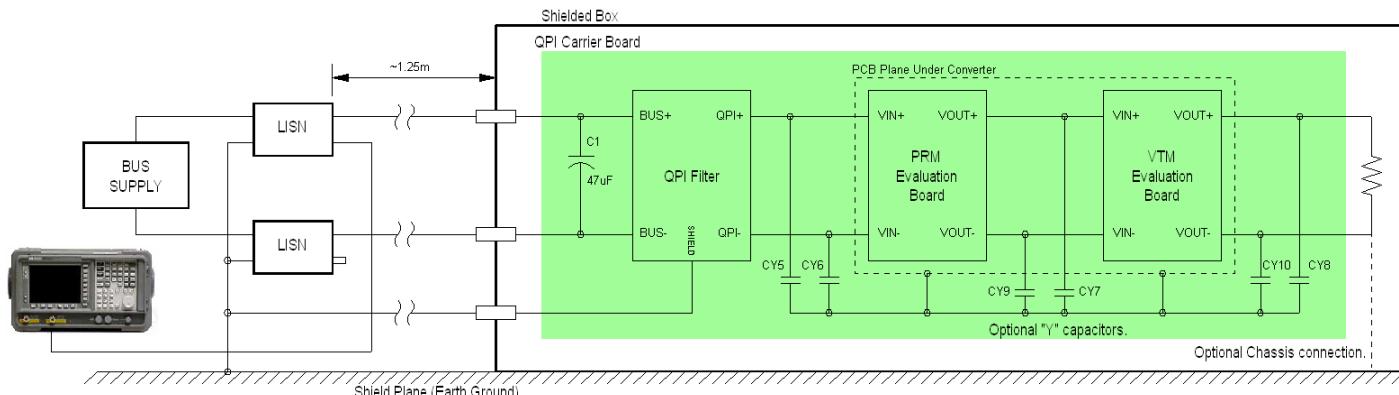
The basic premise of filtering EMI is to insert a high-impedance, at the EMI's base frequency, in both the differential and common-mode paths as it returns to the power source.

Passive filters use common-mode chokes and "Y" capacitors to filter out common-mode EMI. These chokes are designed to present a high-impedance at the EMI frequency in series with the return path, and a low impedance path to the earth signal via the "Y" caps. This network will force the EMI signals to re-circulate within a confined area and not to propagate to the outside world. Often two common-mode networks are required to filter EMI within the frequency span required to pass the EN55022 class B limits.

The other component of the passive filter is the differential LC network. Again, the inductor is chosen such that it will present a high-impedance in the differential EMI loop at the EMI's base frequency. The differential capacitor will then shunt the EMI back to its source. The QPI-11 was specifically designed to work with higher switching frequency converters like Vicor's V•I Chip™ products; PRM and VTM modules; as well as their newer VI Brick™ product series.



**Figure 4 - Open-frame EMI test setup using the QPI-11-CB1 carrier board with V•I Chip™ evaluation boards.**



**Figure 5 - Base-plate EMI test setup using the QPI-11-CB1 carrier board with V•I Chip™ evaluation boards.**

### EMI Management

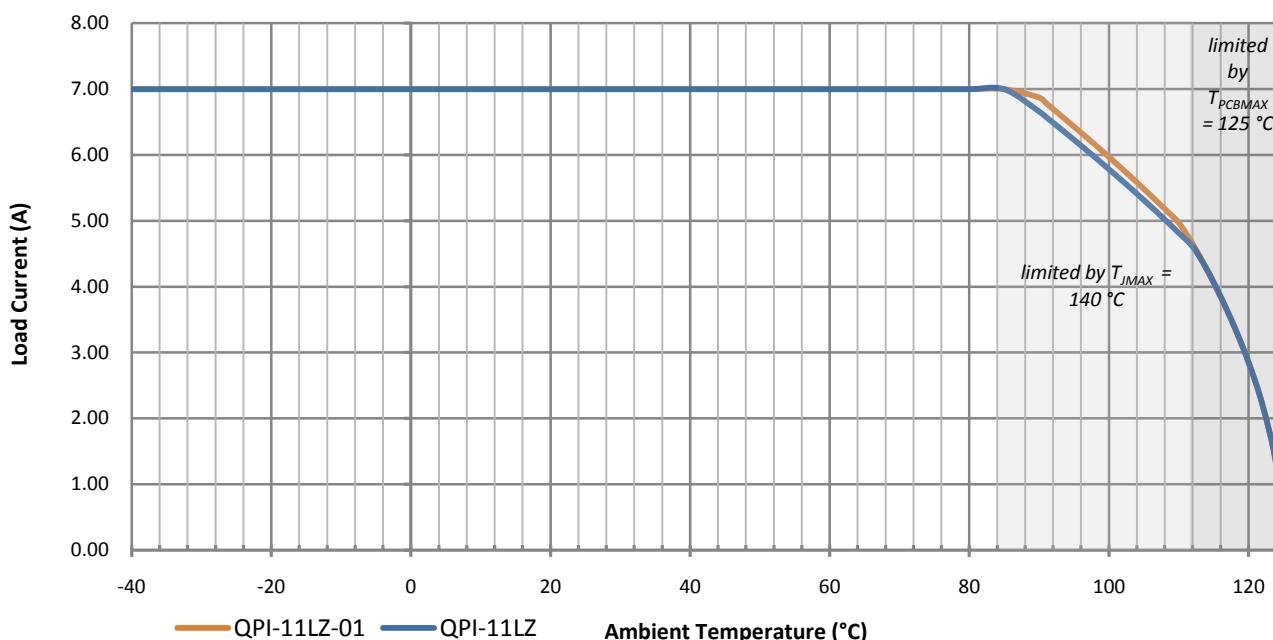
The more effectively EMI is managed at the source, namely the power converter, the less EMI attenuation the filter will have to do. The addition of "Y" capacitors to the input and output power nodes of the converter will help to limit the amount of EMI that tries to propagate to the input source.

There are two basic topologies for the connection of the re-circulating "Y" capacitors. In Figure 4 the open-frame topology is shown in Picor's EMI test setup. The "Y" capacitors (CY1 to CY4) re-circulate the EMI signals between the positive input and output, and the negative input and output of the power conversion stage.

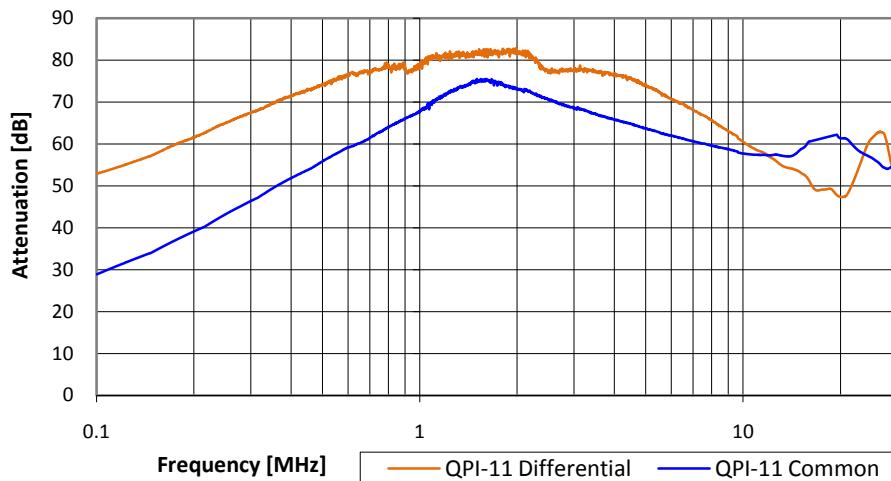
**Current De-Rating:** mounted to QPI-11-CB1 evaluation board.

Figure 5 shows the base-plate topology of re-circulating "Y" caps. Here, CY5 to CY10 are connected to each power node of the PRM and VTM, and then are commoned together on a copper shield plane created under the converter. The addition of the copper shield plane helps in the containment of the radiated EMI, converting it back to conducted EMI and shunting it back to its source.

Both of these topologies work well with the PRM/VTM combination shown above in attenuating noise levels well below class B EMI limits.



**Figure 6 - Current de-rating over ambient temperature range.**

**QPI Insertion Loss Measurements**

**QPI Insertion Loss Equation:**

$$\text{Insertion Loss} = 20 * \log * \left[ \frac{I_{INA}}{I_{INB}} \right]$$

Figure 7 - Attenuation curves into a 50Ω line impedance, bias from a 24V bus.

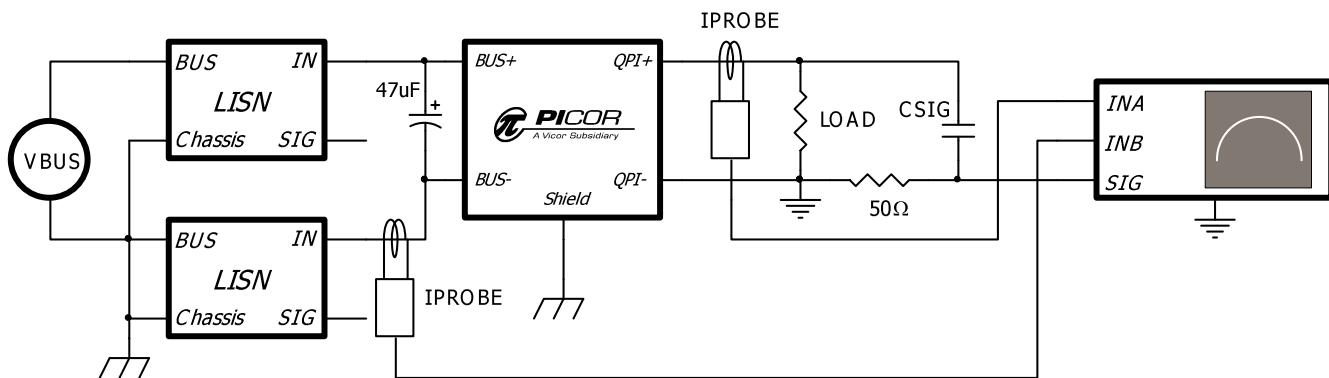
**QPI Insertion Loss Test Circuits**


Figure 8 – Test Set-up to measure Differential Mode EMI currents in Figure 7.

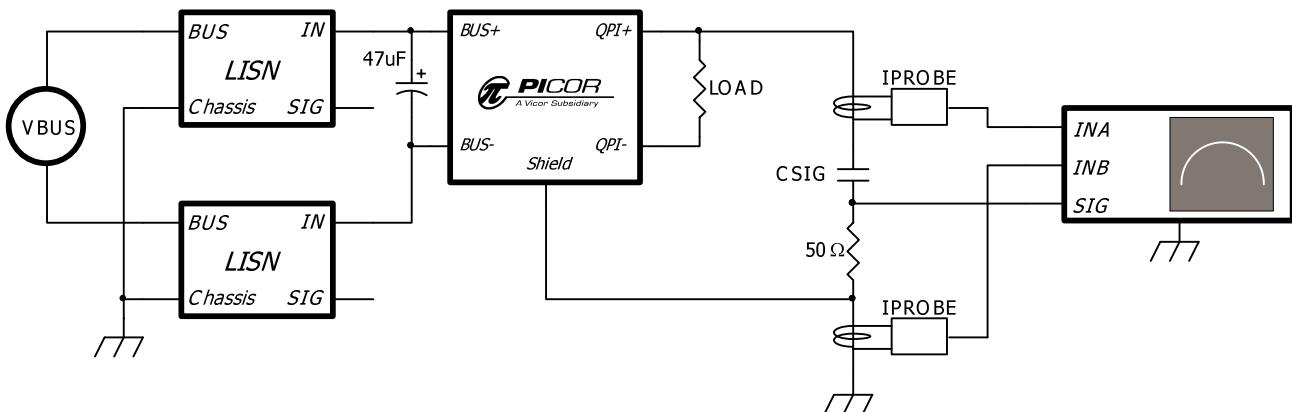


Figure 9 - Test Set-up to measure Common Mode EMI currents in Figure 7.

**Attenuation Plots:**

QPI-11 with PRM P024F048T12AL-CB and various VTM modules, connected in Base-plate configuration, as shown in Figure 2.

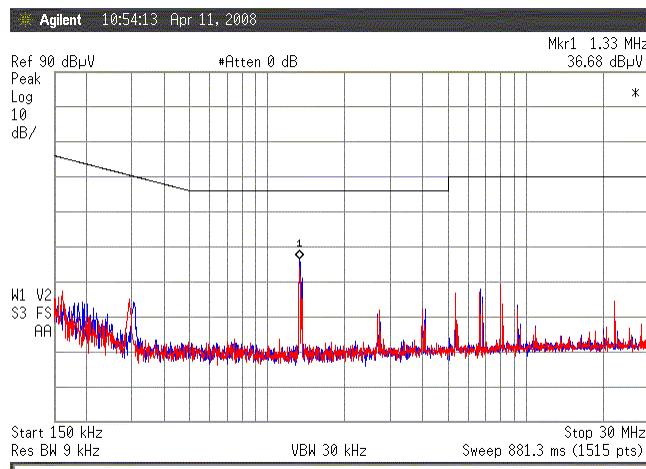


Figure 10 - VTM V048F030T070-CB with 111W Load.

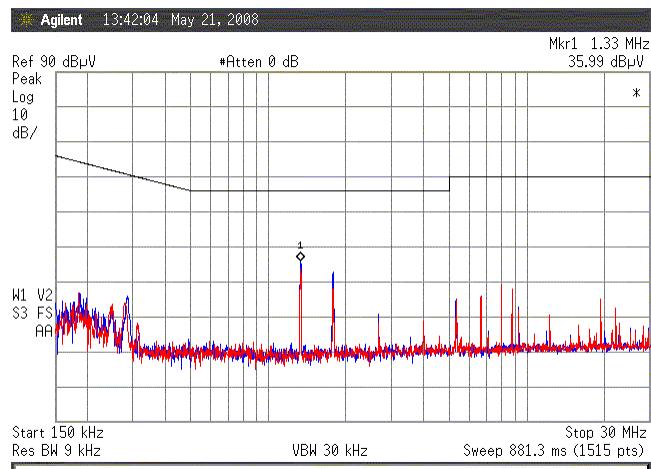


Figure 12 - VTM V048F240T012-CB with 86W Output Load.

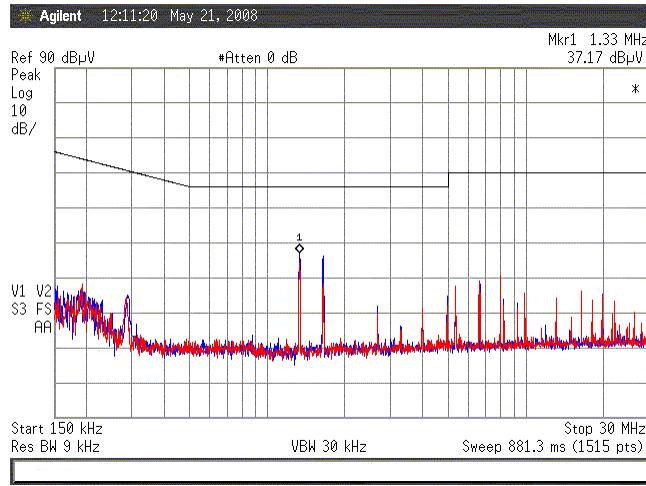


Figure 11 - VTM V048F120T025-CB with 90W Load.

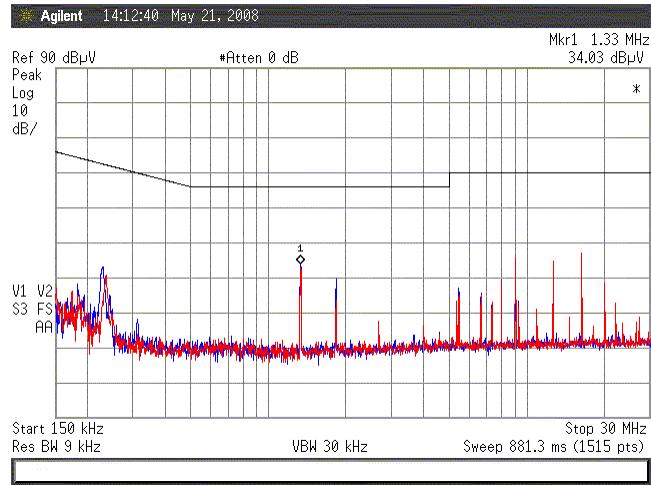


Figure 13 - VTM V048F480T006-CB with 76W Load.

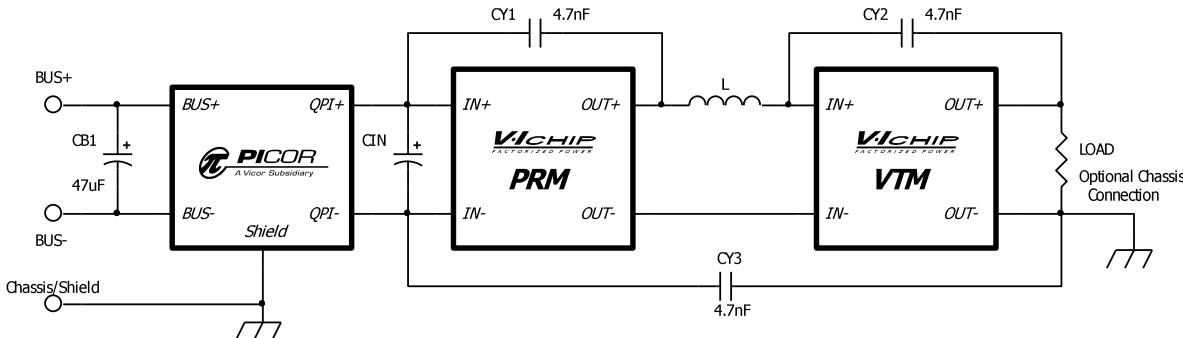
**Converter Output Grounding: Recommended configuration.**


Figure 14 – PRM/VTM converter in base-plate configuration with output connected to chassis/earth.

When using the QPI-11 with a Vicor PRM/VTM, in a power system that requires the converter's output to be connected to chassis/earth, Picor recommends using the open-frame

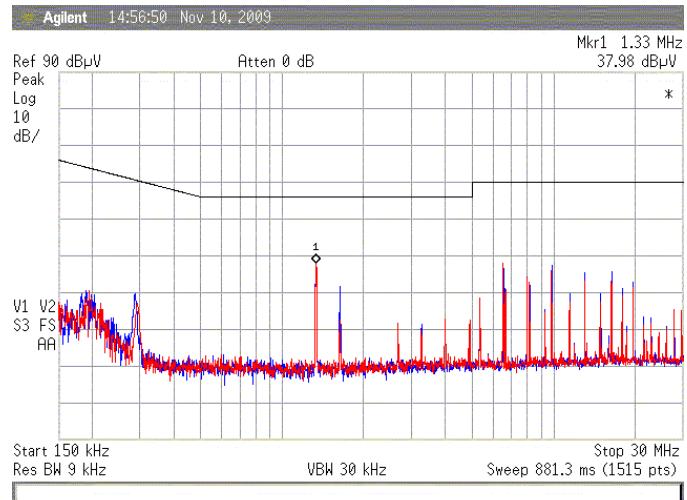
configuration of "Y" capacitors, shown in Figure 14, to recirculate EMI currents. A base-plate configuration could also be used with a slight decrease in EMI attenuation, but with

peaks well below class B limits.

The plot in Figure 15 is of a P024F048T12AL-CB and a V048F240T012-CB, an 86W load with the output ground connected to the chassis. When using the open-frame configuration of "Y" caps, the EMI shield plane is not used by the "Y" capacitors for re-circulating the EMI currents.

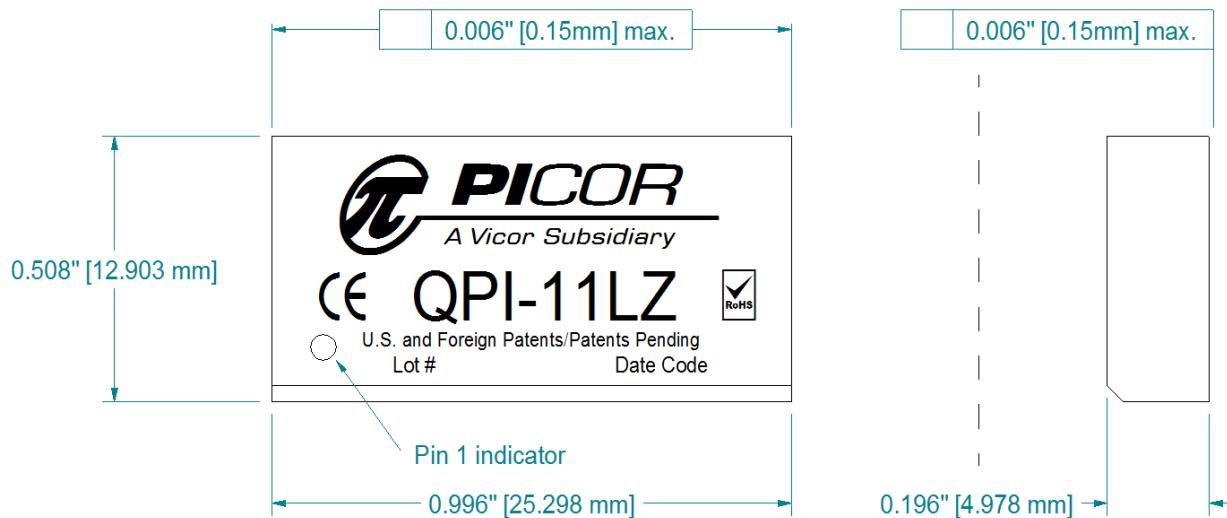
The QPI-11 is not designed to be used in parallel with another QPI-11 to achieve a higher current rating, but it can be used multiple times within a system design.

The red and blue traces in Figure 10 through Figure 13, and Figure 15, are the measurements of total EMI, in both the positive and negative branches. The test setups shown in Figure 4 and Figure 5 are representative of measuring the positive branch of the total EMI for the unit under test.

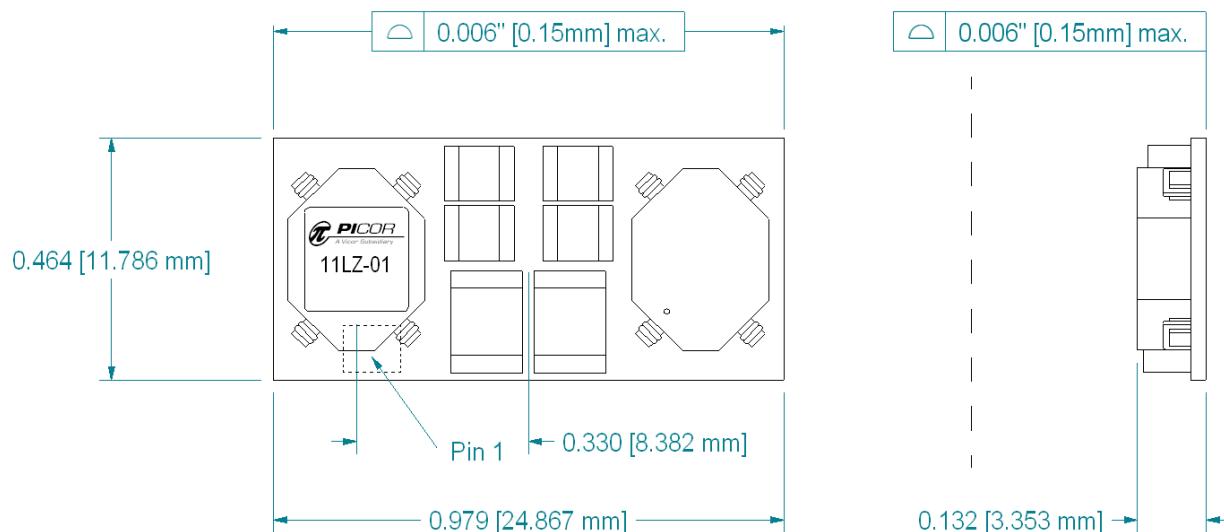


**Figure 15 – Total noise plot of PRM/VTM with its output return connected to chassis, as shown in Figure 14.**

**Mechanicals**



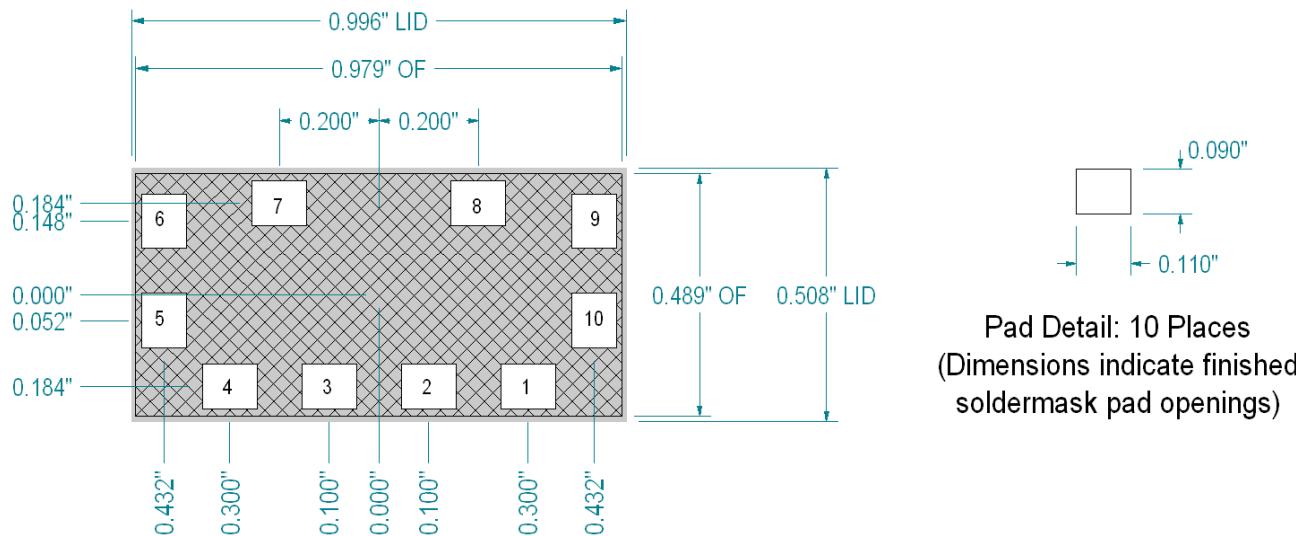
**Figure 16 - Lidded Package Dimensions, tolerance of  $\pm 0.004"$**



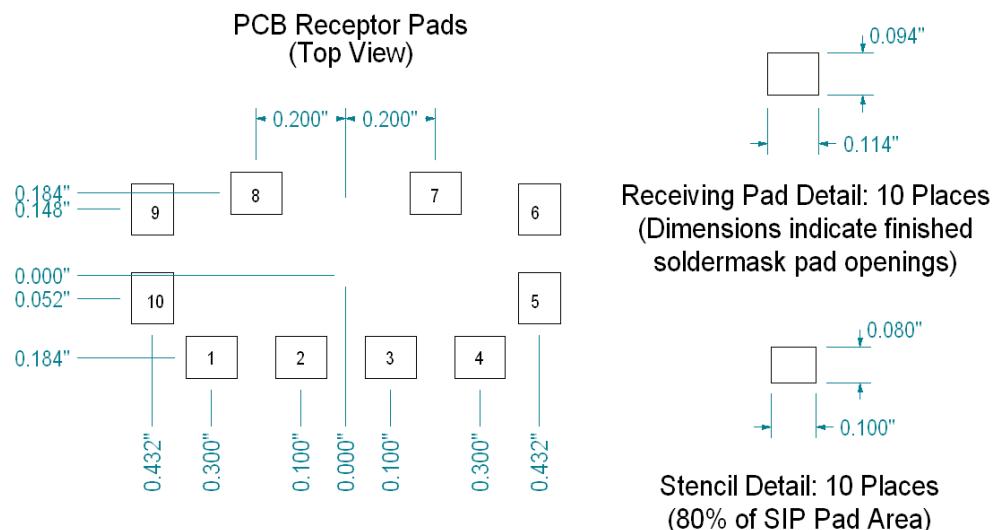
**Figure 17 - Open Open-frame Package dimensions, tolerance of  $\pm 0.004"$ . Pick and Place from label center.**

**QPI-11 Mechanical Data**

| Datum                   | Units                | QPI-11LZ | QPI-11LZ-01 | Notes                                       |
|-------------------------|----------------------|----------|-------------|---|
| FITS                    | Failure/Billion Hrs. | 16       | 16          | FITS based on the BellCore Standard TR-332  |
| MTBF                    | Million Hrs.         | 62.5     | 62.5        | MTBFs based on the BellCore Standard TR-332 |
| Weight                  | grams                | 2.4      | 2.075       |   |
| MSL                     |                      | 3        | 3           |   |
| Peak reflow Temperature | °C/20 seconds        | 245      | 245         | IPC/JEDEC J-STD-020D                        |

**Pad and Stencil Definitions:**


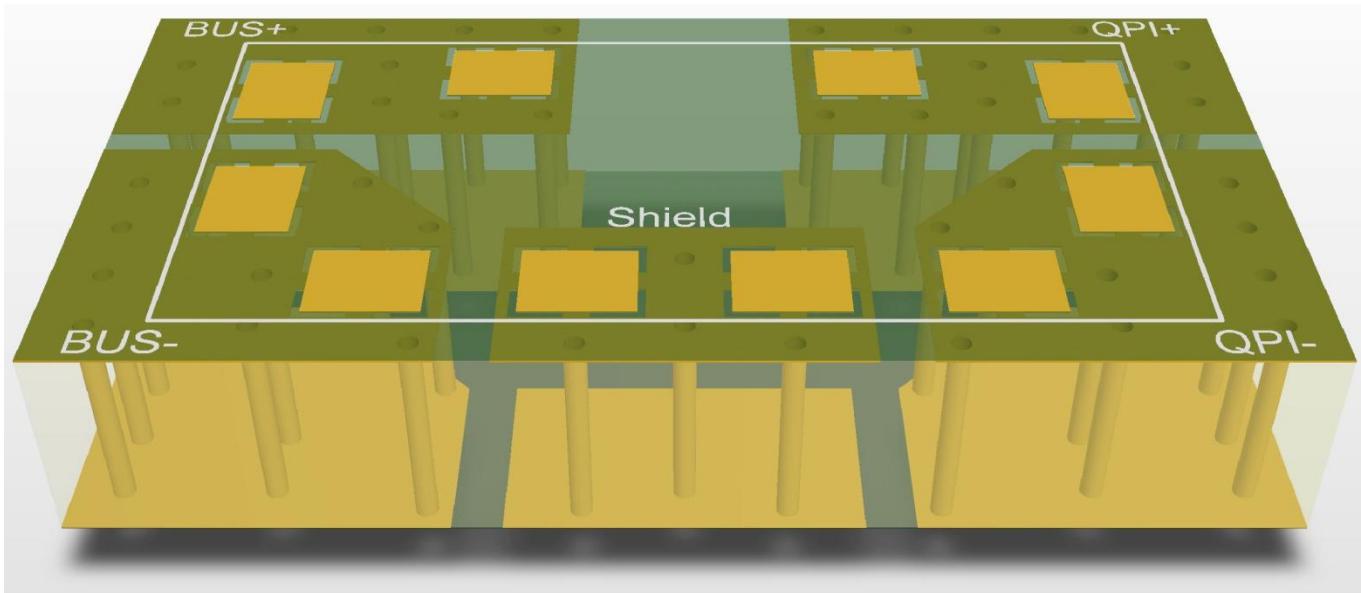
**Figure 18** - Bottom view of open-frame (OF) and lidded products. (All dimensions are in inches.)



**Figure 19** - Recommended receptor and stencil patterns. (All dimensions are in inches.)

Stencil definition is based on a 6mil stencil thickness, 80% of LGA pad area coverage. LGA Package dimensions are for both the Open-Frame and Lidded versions of the QPI-11.

**QPI-11 PCB Layout Recommendations:**



**Figure 20 - 3D view of paralleling planes underneath the QPI-11.**

The filtering performance of the QPI-11 is sensitive to capacitive coupling between its input and output pins. Parasitic plane capacitance must be kept below 1 pico-Farad between inputs and outputs using the layout shown above and the recommendations described below to achieve maximum conducted EMI performance.

To avoid capacitive coupling between input and output pins, there should not be any planes or large traces that run under both input and output pins, such as a ground plane or power plane. For example, if there are two signal planes or large traces where one trace runs under the input pins, and the other under the output pins, and both planes overlap in another area, they will cause capacitive coupling between input and output pins. Also, planes that run under both input and output pins, but do not cross, can cause capacitive coupling if they are capacitively bypassed together. Figure 20

shows the recommended PCB layout on a 2 layer board. Here, the top layer planes are duplicated on the bottom layer so that there can be no overlapping of input and output planes. This method can be used for boards of greater layer count.

**Post Solder Cleaning**

Picor's LZ version QP SIPs are not hermetically sealed and must not be exposed to liquid, including but not limited to cleaning solvents, aqueous washing solutions or pressurized sprays. When soldering, it is recommended that no-clean flux solder be used, as this will ensure that potentially corrosive mobile ions will not remain on, around, or under the module following the soldering process. For applications where the end product must be cleaned in a liquid solvent, Picor recommends using the QPI-11LZ-01, open-frame version of the EMI filter.

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