

74ALVC573

Octal D-type transparent latch; 3-state

Rev. 03 — 26 October 2007

Product data sheet

1. General description

The 74ALVC573 is an octal D-type transparent latch featuring separate D-type inputs for each latch and 3-state true outputs for bus-oriented applications. A latch enable (LE) input and an outputs enable (\overline{OE}) input are common to all latches.

When pin LE is HIGH, data at the D-inputs (pins D0 to D7) enters the latches. In this condition, the latches are transparent, that is, a latch output will change each time its corresponding D-input changes. When pin LE is LOW, the latches store the information that was present at the D-inputs one set-up time preceding the HIGH-to-LOW transition of pin LE.

When pin \overline{OE} is LOW, the contents of the eight latches are available at the Q-outputs (pins Q0 to Q7). When pin \overline{OE} is HIGH, the outputs go to the high-impedance OFF-state. Operation of input pin \overline{OE} does not affect the state of the latches.

The 74ALVC573 is functionally identical to the 74ALVC373, but has a different pin arrangement.

2. Features

- Wide supply voltage range from 1.65 V to 3.6 V
- 3.6 V tolerant inputs/outputs
- CMOS low power consumption
- Direct interface with TTL levels (2.7 V to 3.6 V)
- Power-down mode
- Latch-up performance exceeds 250 mA
- Complies with JEDEC standards:
 - ◆ JESD8-7 (1.65 V to 1.95 V)
 - ◆ JESD8-5 (2.3 V to 2.7 V)
 - ◆ JESD8B/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - ◆ HBM JESD22-A114E exceeds 2000 V
 - ◆ MM JESD22-A 115-A exceeds 200 V

3. Ordering information

Table 1. Ordering information

| Type number | Package | | | Version |
|-------------|-------------------|----------|--|----------|
| | Temperature range | Name | Description | |
| 74ALVC573D | -40 °C to +85 °C | SO20 | plastic small outline package; 20 leads; body width 7.5 mm | SOT163-1 |
| 74ALVC573PW | -40 °C to +85 °C | TSSOP20 | plastic thin shrink small outline package; 20 leads; body width 4.4 mm | SOT360-1 |
| 74ALVC573BQ | -40 °C to +85 °C | DHVQFN20 | plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm | SOT764-1 |

4. Functional diagram

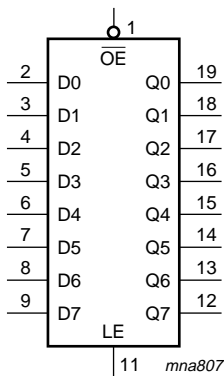


Fig 1. Logic symbol

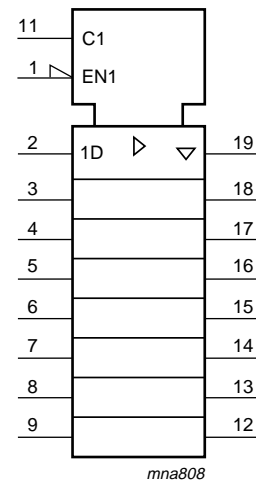


Fig 2. IEC logic symbol

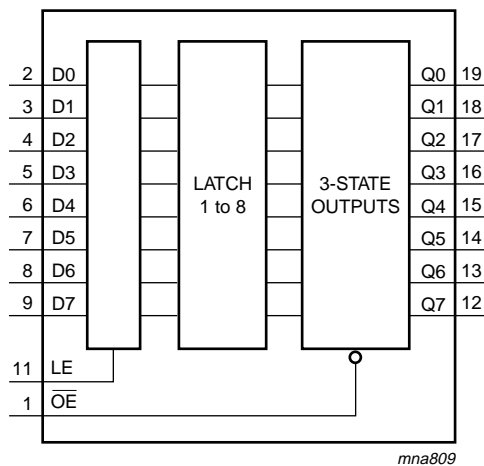


Fig 3. Functional diagram

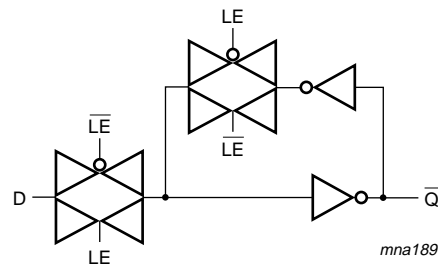


Fig 4. Logic diagram (one latch)

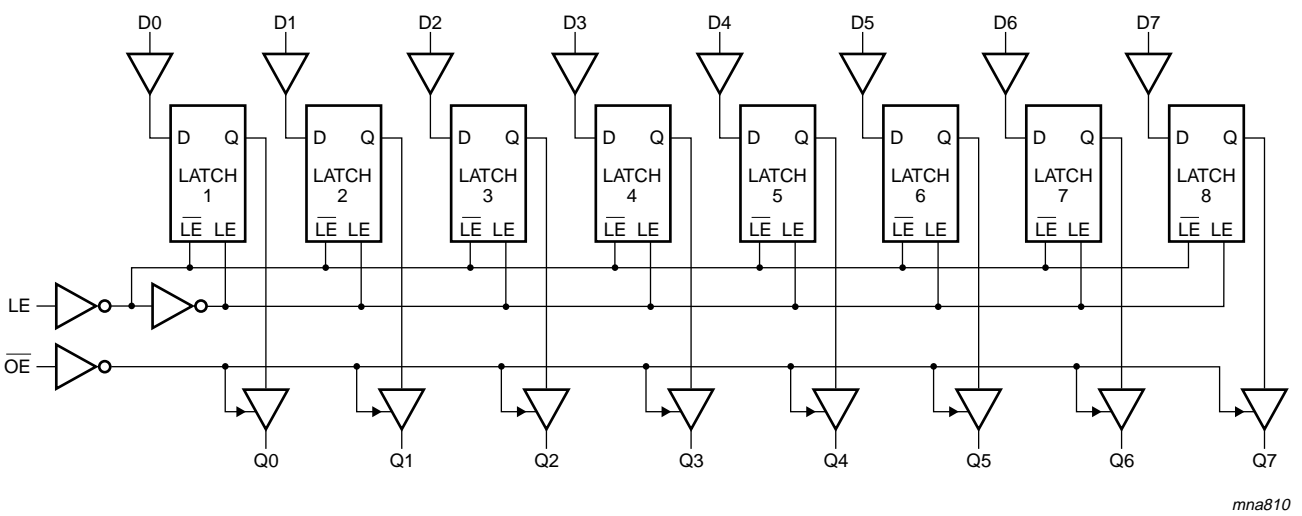


Fig 5. Logic diagram

5. Pinning information

5.1 Pinning

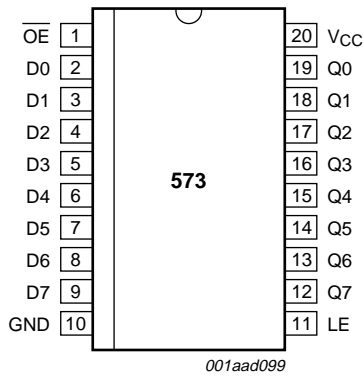
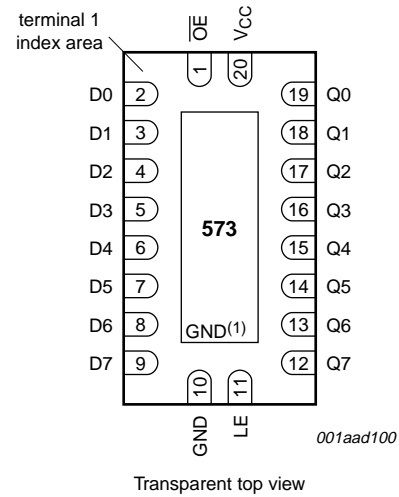


Fig 6. Pin configuration SO20 and TSSOP20



(1) The die substrate is attached to this pad using conductive die attach material. It can not be used as a supply pin or input.

Fig 7. Pin configuration DHVQFN20

5.2 Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|-----------------|--------------------------------|----------------------------------|
| D[0:7] | 2, 3, 4, 5, 6, 7, 8, 9 | data input |
| LE | 11 | latch enable input (active HIGH) |
| OE | 1 | output enable input (active LOW) |
| Q[0:7] | 19, 18, 17, 16, 15, 14, 13, 12 | 3-state latch output |
| V _{CC} | 20 | supply voltage |
| GND | 10 | ground (0 V) |

6. Functional description

Table 3. Functional table^[1]

| Operating modes | Input | | | Internal latch | Output Qn |
|--|------------------------|----|----|----------------|--------------|
| | $\overline{\text{OE}}$ | LE | Dn | | |
| Enable and read register (transparent mode) | L | H | L | L | L |
| | L | H | H | H | H |
| Latch and read register | L | L | l | L | L |
| | L | L | h | H | H |
| Latch register and disable outputs | H | L | l | L | Z |
| | H | L | h | H | Z |

- [1] H = HIGH voltage level
 h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition
 L = LOW voltage level
 l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition
 Z = High-impedance OFF-state

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------------|-------------------------|--|------------------------------------|-----------------------|------|
| V_{CC} | supply voltage | | -0.5 | +4.6 | V |
| I_{IK} | input clamping current | $V_{\text{I}} < 0 \text{ V}$ | -50 | - | mA |
| V_{I} | input voltage | | -0.5 | +4.6 | V |
| I_{OK} | output clamping current | $V_{\text{O}} > V_{\text{CC}}$ or $V_{\text{O}} < 0 \text{ V}$ | - | ± 50 | mA |
| V_{O} | output voltage | output HIGH or LOW state | ^[1] ^[2] -0.5 | $V_{\text{CC}} + 0.5$ | V |
| | | output 3-state | -0.5 | +4.6 | V |
| | | power-down mode, $V_{\text{CC}} = 0 \text{ V}$ | ^[2] -0.5 | +4.6 | V |
| I_{O} | output current | $V_{\text{O}} = 0 \text{ V}$ to V_{CC} | - | ± 50 | mA |
| I_{CC} | supply current | | - | 100 | mA |
| I_{GND} | ground current | | -100 | - | mA |
| T_{stg} | storage temperature | | -65 | +150 | °C |
| P_{tot} | total power dissipation | $T_{\text{amb}} = -40 \text{ °C}$ to $+85 \text{ °C}$ | ^[3] - | 500 | mW |

- [1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 [2] When $V_{\text{CC}} = 0 \text{ V}$ (power-down mode), the output voltage can be 3.6 V in normal operation.
 [3] For SO20 packages: above 70 °C derate linearly with 8 mW/K.
 For TSSOP20 packages: above 60 °C derate linearly with 5.5 mW/K.
 For DHVQFN20 packages: above 60 °C derate linearly with 4.5 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---------------------|-------------------------------------|---------------------------------|------|----------|------|
| V_{CC} | supply voltage | | 1.65 | 3.6 | V |
| V_I | input voltage | | 0 | 3.6 | V |
| V_O | output voltage | output HIGH or LOW state | 0 | V_{CC} | V |
| | | output 3-state | 0 | 3.6 | V |
| | | power-down mode; $V_{CC} = 0$ V | 0 | 3.6 | V |
| T_{amb} | ambient temperature | in free air | -40 | +85 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC} = 1.65$ V to 2.7 V | - | 20 | ns/V |
| | | $V_{CC} = 2.7$ V to 3.6 V | - | 10 | ns/V |

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | Unit |
|----------|---------------------------|--|----------------------|--------------------|----------------------|---------|
| | | | Min | Typ ^[1] | Max | |
| V_{IH} | HIGH-level input voltage | $V_{CC} = 1.65$ V to 1.95 V | $0.65 \times V_{CC}$ | - | - | V |
| | | $V_{CC} = 2.3$ V to 2.7 V | 1.7 | - | - | V |
| | | $V_{CC} = 2.7$ V to 3.6 V | 2.0 | - | - | V |
| V_{IL} | LOW-level input voltage | $V_{CC} = 1.65$ V to 1.95 V | - | - | $0.35 \times V_{CC}$ | V |
| | | $V_{CC} = 2.3$ V to 2.7 V | - | - | 0.7 | V |
| | | $V_{CC} = 2.7$ V to 3.6 V | - | - | 0.8 | V |
| V_{OH} | HIGH-level output voltage | $V_I = V_{IH}$ or V_{IL} | | | | |
| | | $I_O = -100$ μ A; $V_{CC} = 1.65$ V to 3.6 V | $V_{CC} - 0.2$ | - | - | V |
| | | $I_O = -6$ mA; $V_{CC} = 1.65$ V | 1.25 | - | - | V |
| | | $I_O = -12$ mA; $V_{CC} = 2.3$ V | 1.8 | - | - | V |
| | | $I_O = -18$ mA; $V_{CC} = 2.3$ V | 1.7 | - | - | V |
| | | $I_O = -12$ mA; $V_{CC} = 2.7$ V | 2.2 | - | - | V |
| | | $I_O = -18$ mA; $V_{CC} = 3.0$ V | 2.4 | - | - | V |
| | | $I_O = -24$ mA; $V_{CC} = 3.0$ V | 2.2 | - | - | V |
| V_{OL} | LOW-level output voltage | $V_I = V_{IH}$ or V_{IL} | | | | |
| | | $I_O = 100$ μ A; $V_{CC} = 1.65$ V to 3.6 V | - | - | 0.2 | V |
| | | $I_O = 6$ mA; $V_{CC} = 1.65$ V | - | - | 0.3 | V |
| | | $I_O = 12$ mA; $V_{CC} = 2.3$ V | - | - | 0.4 | V |
| | | $I_O = 18$ mA; $V_{CC} = 2.3$ V | - | - | 0.6 | V |
| | | $I_O = 12$ mA; $V_{CC} = 2.7$ V | - | - | 0.4 | V |
| | | $I_O = 18$ mA; $V_{CC} = 3.0$ V | - | - | 0.4 | V |
| | | $I_O = 24$ mA; $V_{CC} = 3.0$ V | - | - | 0.55 | V |
| I_I | input leakage current | $V_{CC} = 3.6$ V; $V_I = 3.6$ V or GND | - | ± 0.1 | ± 5 | μ A |

Table 6. Static characteristics ...continued

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | Unit |
|------------------|---------------------------|--|------------------|--------------------|-----|------|
| | | | Min | Typ ^[1] | Max | |
| I _{OZ} | OFF-state output current | V _I = V _{IH} or V _{IL} ; V _{CC} = 1.65 V to 3.6 V; V _O = 3.6 V or GND; | - | ±0.1 | ±10 | μA |
| I _{OFF} | power-off leakage supply | V _{CC} = 0 V; V _I or V _O = 0 V to 3.6 V | - | ±0.1 | ±10 | μA |
| I _{CC} | supply current | V _{CC} = 3.6 V; V _I = V _{CC} or GND; I _O = 0 A | - | 0.2 | 10 | μA |
| ΔI _{CC} | additional supply current | per input pin; V _{CC} = 3.0 V to 3.6 V; V _I = V _{CC} - 0.6 V; I _O = 0 A | - | 5 | 750 | μA |
| C _I | input capacitance | | - | 3.5 | - | pF |

[1] All typical values are measured at V_{CC} = 3.3 V (unless stated otherwise) and T_{amb} = 25 °C.

10. Dynamic characteristics

Table 7. Dynamic characteristicsVoltages are referenced to GND (ground = 0 V). For test circuit see [Figure 12](#).

| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | Unit | | |
|----------------------------------|-------------------|--|------------------|--|-----|------|-----|----|
| | | | Min | Typ ^[1] | Max | | | |
| t _{pd} | propagation delay | Dn to Qn; see Figure 8 ^[2] | | | | | | |
| | | V _{CC} = 1.65 V to 1.95 V | 1.0 | 2.5 | 5.4 | ns | | |
| | | V _{CC} = 2.3 V to 2.7 V | 1.0 | 2.0 | 3.5 | ns | | |
| | | V _{CC} = 2.7 V | 1.0 | 2.3 | 3.6 | ns | | |
| | | V _{CC} = 3.0 V to 3.6 V | 1.0 | 2.2 | 3.3 | ns | | |
| | | LE to Qn; see Figure 9 | | | | | | |
| | | V _{CC} = 1.65 V to 1.95 V | 1.0 | 2.8 | 6.0 | ns | | |
| | | V _{CC} = 2.3 V to 2.7 V | 1.0 | 2.1 | 3.8 | ns | | |
| | | V _{CC} = 2.7 V | 1.0 | 2.4 | 3.7 | ns | | |
| | | V _{CC} = 3.0 V to 3.6 V | 1.0 | 2.3 | 3.3 | ns | | |
| | | t _{en} | enable time | $\overline{\text{OE}}$ to Qn; see Figure 10 ^[2] | | | | |
| | | | | V _{CC} = 1.65 V to 1.95 V | 1.5 | 3.0 | 6.4 | ns |
| V _{CC} = 2.3 V to 2.7 V | 1.0 | | | 2.4 | 4.5 | ns | | |
| V _{CC} = 2.7 V | 1.5 | | | 3.0 | 4.6 | ns | | |
| V _{CC} = 3.0 V to 3.6 V | 1.0 | | | 2.3 | 4.0 | ns | | |
| t _{dis} | disable time | $\overline{\text{OE}}$ to Qn; see Figure 10 ^[2] | | | | | | |
| | | V _{CC} = 1.65 V to 1.95 V | 1.5 | 3.4 | 7.0 | ns | | |
| | | V _{CC} = 2.3 V to 2.7 V | 1.0 | 2.2 | 4.4 | ns | | |
| | | V _{CC} = 2.7 V | 1.5 | 2.8 | 4.4 | ns | | |
| | | V _{CC} = 3.0 V to 3.6 V | 1.0 | 2.7 | 4.4 | ns | | |

Table 7. Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 12](#).

| Symbol | Parameter | Conditions | –40 °C to +85 °C | | | Unit |
|-----------------|-------------------------------|---|------------------|--------------------|-----|------|
| | | | Min | Typ ^[1] | Max | |
| t _W | pulse width | LE pulse width HIGH; see Figure 9 | | | | |
| | | V _{CC} = 1.65 V to 1.95 V | 3.8 | - | - | ns |
| | | V _{CC} = 2.3 V to 2.7 V | 3.3 | - | - | ns |
| | | V _{CC} = 2.7 V | 3.3 | - | - | ns |
| t _{su} | set-up time | Dn to LE; see Figure 11 | | | | |
| | | V _{CC} = 1.65 V to 1.95 V | 0.8 | - | - | ns |
| | | V _{CC} = 2.3 V to 2.7 V | 0.8 | - | - | ns |
| | | V _{CC} = 2.7 V | 0.8 | - | - | ns |
| t _h | hold time | Dn to LE; see Figure 11 | | | | |
| | | V _{CC} = 1.65 V to 1.95 V | 0.8 | - | - | ns |
| | | V _{CC} = 2.3 V to 2.7 V | 0.8 | - | - | ns |
| | | V _{CC} = 2.7 V | 0.8 | - | - | ns |
| C _{PD} | power dissipation capacitance | per latch; V _I = GND to V _{CC} ; V _{CC} = 3.3 V ^[3] | | | | |
| | | outputs HIGH or LOW state | - | 37 | - | pF |
| | | outputs 3-state | - | 7 | - | pF |

[1] Typical values are measured at T_{amb} = 25 °C

[2] t_{pd} is the same as t_{PHL} and t_{PLH}.

t_{en} is the same as t_{PZH} and t_{PZL}.

t_{dis} is the same as t_{PHZ} and t_{PLZ}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz; f_o = output frequency in MHz

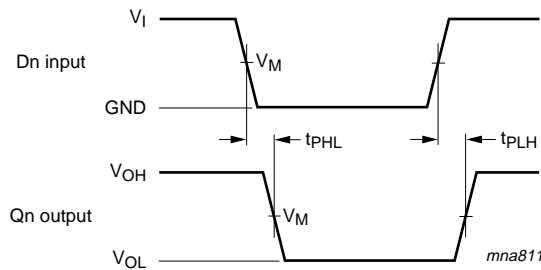
C_L = output load capacitance in pF

V_{CC} = supply voltage in Volts

N = number of inputs switching

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs

11. Waveforms



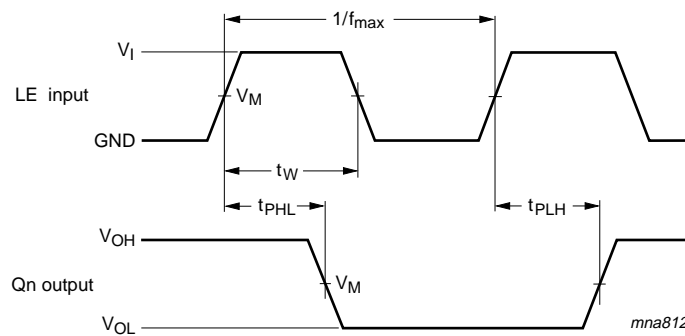
Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are the typical output voltage levels that occur with the output load.

Fig 8. Input Dn to output Qn propagation delay times

Table 8. Measurement points

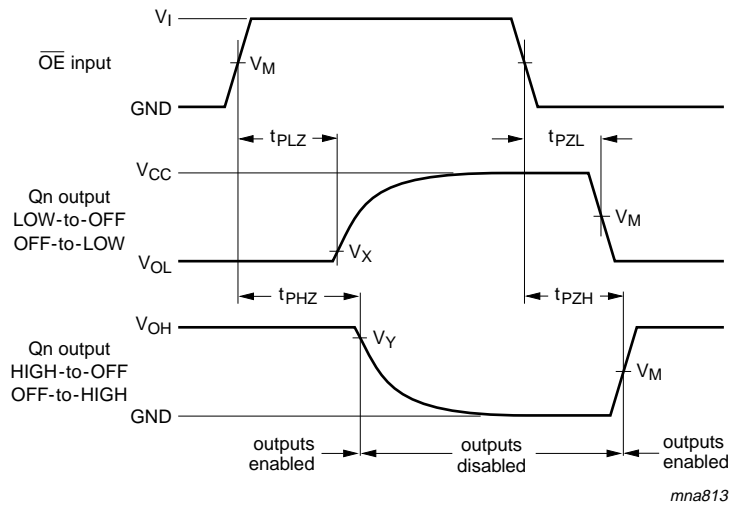
| Supply voltage V_{CC} | V_M | Output | |
|-------------------------|-------------|-------------------|-------------------|
| | | V_X | V_Y |
| 1.65 V to 1.95 V | $0.5V_{CC}$ | $V_{OL} + 0.15 V$ | $V_{OH} - 0.15 V$ |
| 2.3 V to 2.7 V | $0.5V_{CC}$ | $V_{OL} + 0.15 V$ | $V_{OH} - 0.15 V$ |
| 2.7 V | 1.5 V | $V_{OL} + 0.3 V$ | $V_{OH} - 0.3 V$ |
| 3.0 V to 3.6 V | 1.5 V | $V_{OL} + 0.3 V$ | $V_{OH} - 0.3 V$ |



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are the typical output voltage levels that occur with the output load.

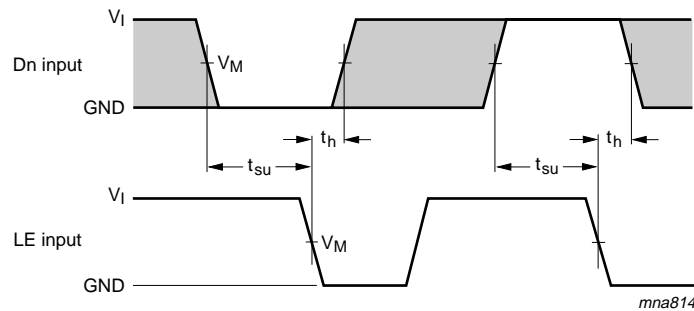
Fig 9. Latch enable (LE) pulse width and latch enable input to output (Qn) propagation delays



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are the typical output voltage levels that occur with the output load.

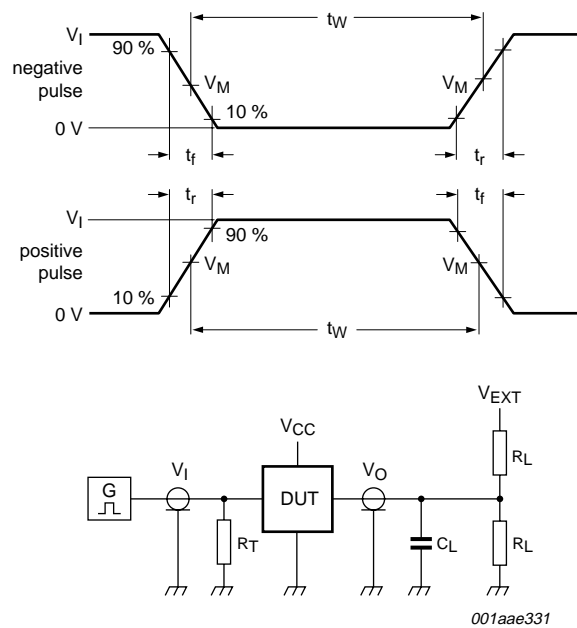
Fig 10. Enable and disable times



Measurement points are given in [Table 8](#).

The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig 11. The data set-up and hold times for Dn input to LE input



Test data is given in [Table 9](#).

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig 12. Test circuitry for switching times

Table 9. Test data

| Supply voltage | Input | | Load | | V_{EXT} | | |
|------------------|----------|---------------|-------|--------------|--------------------|--------------------|--------------------|
| | V_I | t_r, t_f | C_L | R_L | t_{PLH}, t_{PHL} | t_{PLZ}, t_{PZL} | t_{PHZ}, t_{PZH} |
| 1.65 V to 1.95 V | V_{CC} | ≤ 2.0 ns | 30 pF | 1 k Ω | open | $2V_{CC}$ | GND |
| 2.3 V to 2.7 V | V_{CC} | ≤ 2.0 ns | 30 pF | 500 Ω | open | $2V_{CC}$ | GND |
| 2.7 V | 2.7 V | ≤ 2.5 ns | 50 pF | 500 Ω | open | 6 V | GND |
| 3.0 V to 3.6 V | 2.7 V | ≤ 2.5 ns | 50 pF | 500 Ω | open | 6 V | GND |

12. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



Fig 13. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

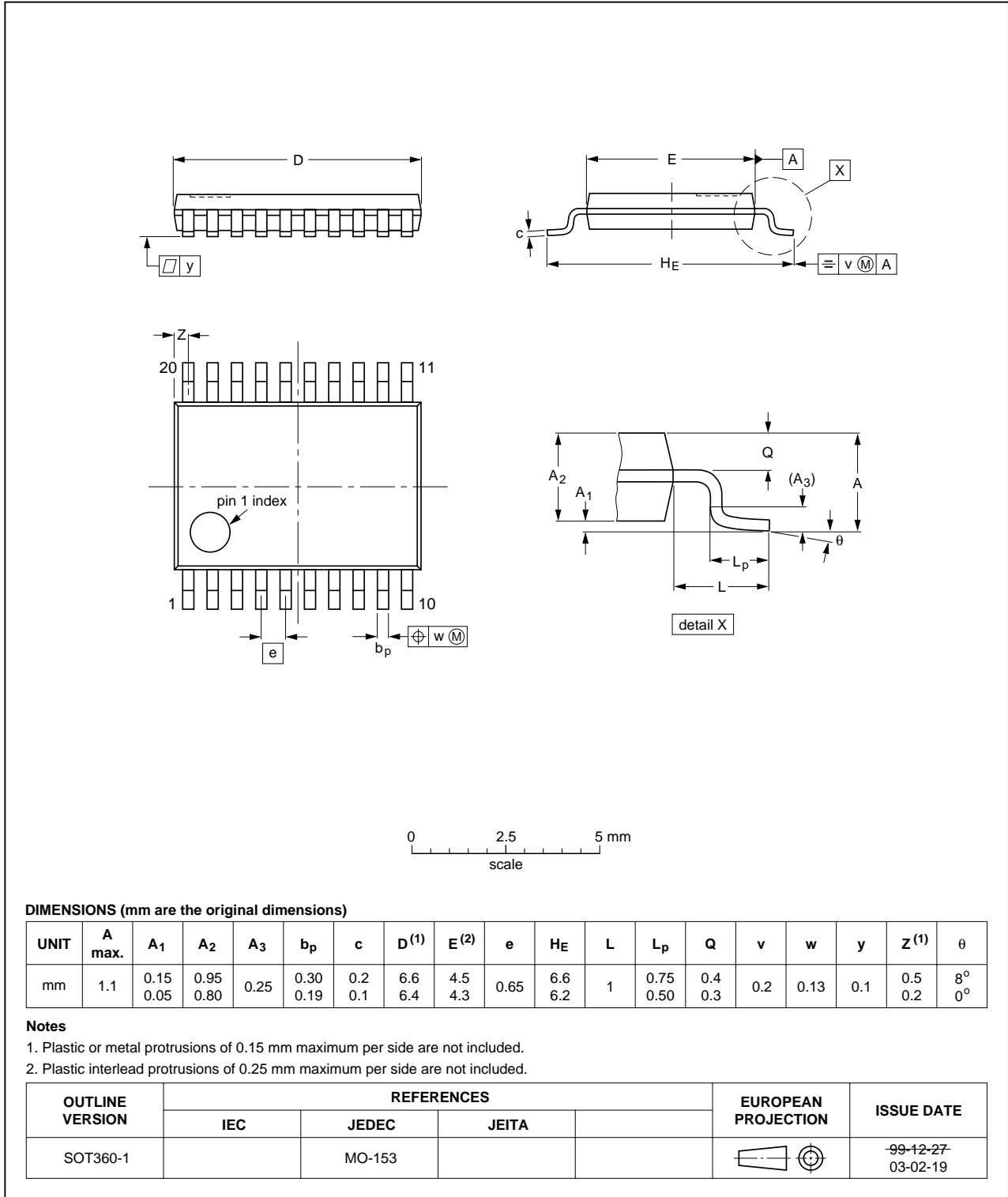


Fig 14. Package outline SOT360-1 (TSSOP20)

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm

SOT764-1

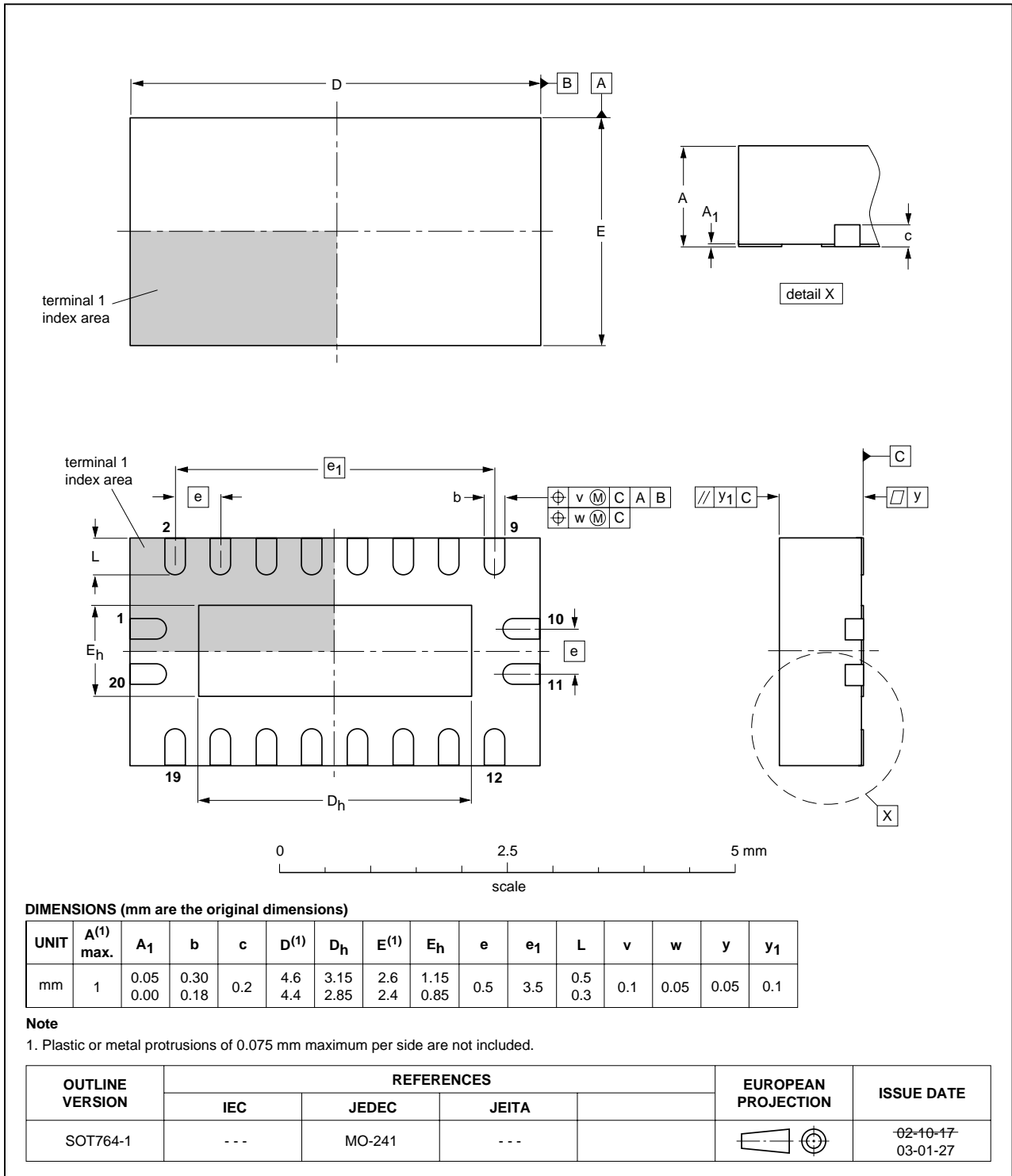


Fig 15. Package outline SOT764-1 (DHVQFN20)

13. Abbreviations

Table 10. Abbreviations

| Acronym | Description |
|---------|-----------------------------|
| CDM | Charged Device Model |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MM | Machine Model |
| TTL | Transistor-Transistor Logic |

14. Revision history

Table 11. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|----------------|--|-----------------------|---------------|-------------|
| 74ALVC573_3 | 20071026 | Product data sheet | - | 74ALVC573_2 |
| Modifications: | <ul style="list-style-type: none"> • The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Section 3: DHVQFN20 package added. • Section 8: derating values added for DHVQFN20 package. • Section 12: outline drawing added for DHVQFN20 package. | | | |
| 74ALVC573_2 | 20030625 | Product specification | - | 74ALVC573_1 |
| 74ALVC573_1 | 20020301 | Product specification | - | - |

15. Legal information

15.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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Компания «Life Electronics» занимается поставками электронных компонентов импортного и отечественного производства от производителей и со складов крупных дистрибьюторов Европы, Америки и Азии.

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- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.



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