R1WV6416R Series

64Mb Advanced LPSRAM (4M word x 16bit / 8M word x 8bit)

REJ03C0368-0100
Rev.1.00
2009.05.07

Description

The R1WV6416R Series is a family of low voltage 64-Mbit static RAMs organized as 4,194,304-word by 16-bit, fabricated by Renesas's high-performance 0.15um CMOS and TFT technologies.
The R1WV6416R Series is suitable for memory applications where a simple interfacing, battery operating and battery backup are the important design objectives.
The R1WV6416R Series is provided in 48-pin thin small outline package [TSOP (I): 12mm x 20mm with pin pitch of 0.5mm], 52-pin micro thin small outline package [μTSOP (II): 10.79mm x 10.49mm with pin pitch of 0.4mm] and 48-ball fine pitch ball grid array [f-BGA] package. It gives the best solution for compaction of mounting area as well as flexibility of wiring pattern of printed circuit boards.

Features

- Single 2.7~3.6V power supply
- Small stand-by current: 8 µA (3.0V, typical)
- No clocks, No refresh
- All inputs and outputs are TTL compatible.
- Easy memory expansion by CS1#, CS2, LB# and UB#
- Common Data I/O
- Three-state outputs: OR-tie Capability
- OE# prevents data contention on the I/O bus

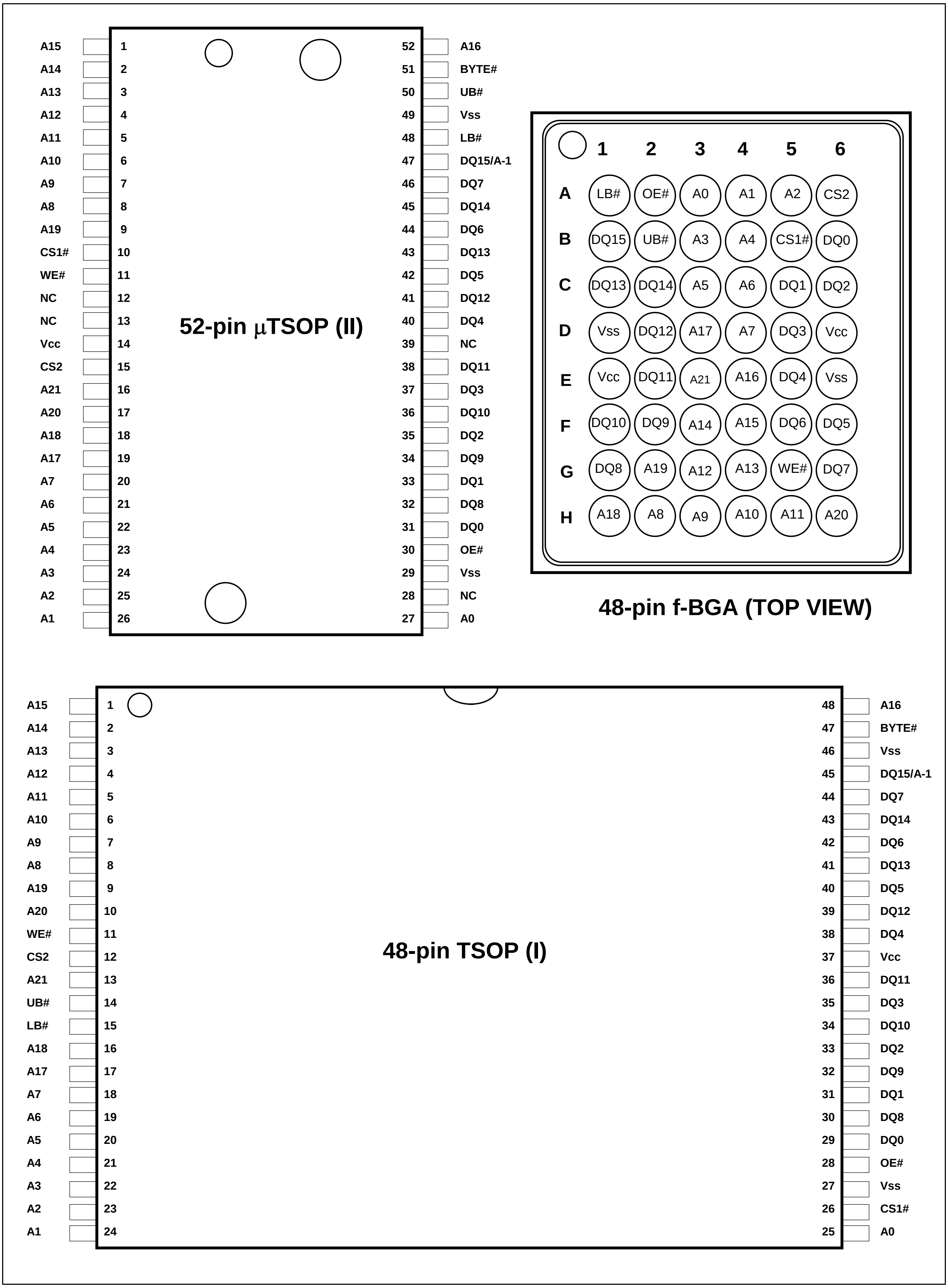
Ordering Information

Type No.	Access time	Package
R1WV6416RSA-5S%	55 ns	12mm x 20mm 48-pin plastic TSOP (I) (normal-bend type) (48P3R)
R1WV6416RSA-7S%	70 ns	
R1WV6416RSD-5S%	55 ns	350 mil 52-pin plastic µ-TSOP (II) (normal-bend type) (52PTG)
R1WV6416RSD-7S%	70 ns	
R1WV6416RBG-5S%	55 ns	f-BGA 0.75mm pitch 48-ball
R1WV6416RBG-7S%	70 ns	

% - Temperature version; see table below

%	Temperature Range
R	0 ~ +70 °C
I	-40 ~ +85 °C

Pin Arrangement

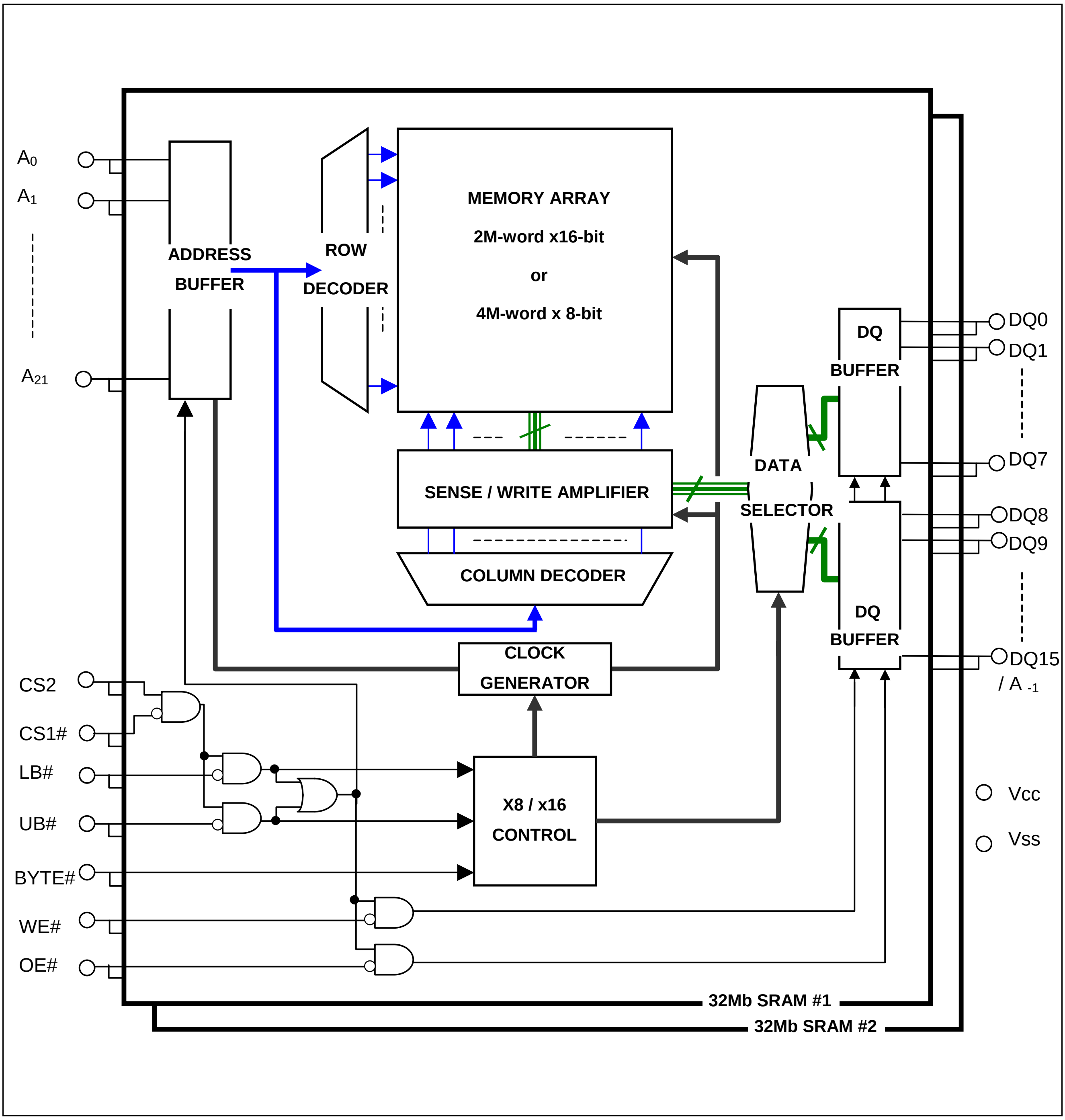


Pin Description

Pin name	Function
Vcc	Power supply
Vss	Ground
A0 to A21	Address input (word mode)
A-1 to A21	Address input (byte mode)
DQ0 to DQ15	Data input/output
CS1#	Chip select 1
CS2	Chip select 2
WE#	Write enable
OE#	Output enable
LB#	Lower byte enable
UB#	Upper byte enable
BYTE#	Byte control mode enable
NC	Non connection

Note: BYTE# pin is supported for 48-pin TSOP (I) and 52-pin µTSOP (II) packages.

Block Diagram



Note: BYTE# pin is supported for 48-pin TSOP (I) and 52-pin µTSOP (II) packages.

Operation Table

CS1#	CS2	BYTE#	LB#	UB#	WE#	OE#	DQ0~7	DQ8~14	DQ15	Operation
H	X	X	X	X	X	X	High-Z	High-Z	High-Z	Stand-by
X	L	X	X	X	X	X	High-Z	High-Z	High-Z	Stand-by
X	X	H	H	H	X	X	High-Z	High-Z	High-Z	Stand-by
L	H	H	L	H	L	X	Din	High-Z	High-Z	Write in lower byte
L	H	H	L	H	H	L	Dout	High-Z	High-Z	Read in lower byte
L	H	H	L	H	H	H	High-Z	High-Z	High-Z	Output disable
L	H	H	H	L	L	X	High-Z	Din	Din	Write in upper byte
L	H	H	H	L	H	L	High-Z	Dout	Dout	Read in upper byte
L	H	H	H	L	H	H	High-Z	High-Z	High-Z	Output disable
L	H	H	L	L	L	X	Din	Din	Din	Word write
L	H	H	L	L	H	L	Dout	Dout	Dout	Word read
L	H	H	L	L	H	H	High-Z	High-Z	High-Z	Output disable
L	H	L	L	L	L	X	Din	High-Z	A-1	Byte write
L	H	L	L	L	H	L	Dout	High-Z	A-1	Byte read
L	H	L	L	L	H	H	High-Z	High-Z	A-1	Output disable

Note1. H: V_{IH} L:V_{IL} X: V_{IH} or V_{IL}
2. BYTE# pin is supported for 48-pin TSOP (I) and 52-pin µTSOP (II) packages.
3. When apply BYTE# ="L", please assign LB#=UB#="L".

Absolute Maximum Ratings

Parameter	Symbol	Value		unit
Power supply voltage relative to Vss	Vcc	-0.5 to +4.6		V
Terminal voltage on any pin relative to Vss	V_T	-0.5*1 to Vcc+0.3*2		V
Power dissipation	P_T	0.7		W
Operation temperature	Topr*3	R ver.	0 to +70	°C
		I ver.	-40 to +85	°C
Storage temperature range	Tstg	-65 to 150		°C
Storage temperature range under bias	Tbias*3	R ver.	0 to +70	°C
		I ver.	-40 to +85	°C

Note 1. –2.0V in case of AC (Pulse width ≤30ns)
2. Maximum voltage is +4.6V.
3. Ambient temperature range depends on R/I-version. Please see table on page 1.

Recommended Operating Conditions

Parameter		Symbol	Min.	Typ.	Max.	Unit	Note
Supply voltage		Vcc	2.7	3.0	3.6	V	
		Vss	0	0	0	V	
Input high voltage		V_{IH}	2.4	-	Vcc+0.2	V	
Input low voltage		V_{IL}	-0.2	-	0.4	V	1
Ambient temperature range	R ver.	Ta	0	-	+70	°C	2
	I ver.		-40	-	+85	°C	2

Note 1. –2.0V in case of AC (Pulse width ≤ 30ns)
2. Ambient temperature range depends on R/I-version. Please see table on page 1.

DC Characteristics

<table>
<tr><th>Parameter</th><th>Symbol</th><th>Min.</th><th>Typ.</th><th>Max.</th><th>Unit</th><th colspan="2">Test conditions*3</th></tr>
<tr><td>Input leakage current</td><td>| I_{LI} |</td><td>-</td><td>-</td><td>1</td><td>µA</td><td colspan="2">Vin = Vss to Vcc</td></tr>
<tr><td>Output leakage current</td><td>| I_{LO} |</td><td>-</td><td>-</td><td>1</td><td>µA</td><td colspan="2">BYTE# ≥ Vcc -0.2V or BYTE# ≤ 0.2V
CS1# =V_{IH} or CS2 =V_{IL} or
OE# =V_{IH} or WE# =V_{IL} or
LB# = UB# =V_{IH}, VI/O =Vss to Vcc</td></tr>
<tr><td rowspan="2">Average operating current</td><td>I_{CC1}</td><td>-</td><td>45*1</td><td>60</td><td>mA</td><td colspan="2">Min. cycle, duty =100%, II/O = 0mA
BYTE# ≥ Vcc -0.2V or BYTE# ≤ 0.2V
CS1# =V_{IL}, CS2 =V_{IH}, Others = V_{IH}/V_{IL}</td></tr>
<tr><td>I_{CC2}</td><td>-</td><td>5*1</td><td>10</td><td>mA</td><td colspan="2">Cycle =1µs, duty =100%, II/O = 0mA
BYTE# ≥ Vcc -0.2V or BYTE# ≤ 0.2V
CS1# ≤ 0.2V, CS2 ≥ V_{CC}-0.2V,
V_{IH} ≥ V_{CC}-0.2V, V_{IL} ≤ 0.2V</td></tr>
<tr><td>Standby current</td><td>I_{SB}</td><td>-</td><td>0.1*1</td><td>0.3</td><td>mA</td><td colspan="2">BYTE# ≥ Vcc -0.2V or BYTE# ≤ 0.2V
CS2 =V_{IL}</td></tr>
<tr><td rowspan="4">Standby current</td><td rowspan="4">I_{SB1}</td><td>-</td><td>8*1</td><td>24</td><td>µA</td><td>~+25°C</td><td rowspan="4">Vin ≥ 0V
BYTE# ≥ Vcc -0.2V or
BYTE# ≤ 0.2V
(1) 0V ≤ CS2 ≤ 0.2V or
(2) CS1# ≥ V_{CC}-0.2V,
CS2 ≥ V_{CC}-0.2V or
(3) LB# = UB# ≥ V_{CC}-0.2V,
CS1# ≤ 0.2V,
CS2 ≥ V_{CC}-0.2V</td></tr>
<tr><td>-</td><td>14*2</td><td>48</td><td>µA</td><td>~+40°C</td></tr>
<tr><td>-</td><td>-</td><td>100</td><td>µA</td><td>~+70°C</td></tr>
<tr><td>-</td><td>-</td><td>160</td><td>µA</td><td>~+85°C</td></tr>
<tr><td>Output high voltage</td><td>V_{OH}</td><td>2.4</td><td>-</td><td>-</td><td>V</td><td colspan="2">BYTE# ≥ Vcc -0.2V or BYTE# ≤ 0.2V
I_{OH} = -0.5mA</td></tr>
<tr><td>Output low voltage</td><td>V_{OL}</td><td>-</td><td>-</td><td>0.4</td><td>V</td><td colspan="2">BYTE# ≥ Vcc -0.2V or BYTE# ≤ 0.2V
I_{OL} = 2mA</td></tr>
</table>

Note 1. Typical parameter indicates the value for the center of distribution at 3.0V (Ta= 25ºC), and not 100% tested.
2. Typical parameter indicates the value for the center of distribution at 3.0V (Ta= 40ºC), and not 100% tested.
3. BYTE# pin is supported for 48-pin TSOP (I) and 52-pin µTSOP (II) packages.

Capacitance

(Ta =25°C, f =1MHz)

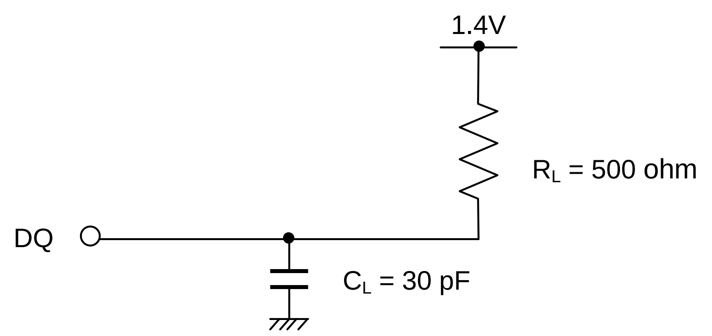
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions	Note
Input capacitance	C in	-	-	20	pF	Vin =0V	1
Input / output capacitance	$C_{I/O}$	-	-	20	pF	$V_{I/O}$ =0V	1

Note1.This parameter is sampled and not 100% tested.

AC Characteristics

Test Conditions (Vcc = 2.7V ~ 3.6V, Ta = 0 ~ +70°C / -40 ~ +85°C*1)

- Input pulse levels: V_{IL} = 0.4V, V_{IH} = 2.4V
- Input rise and fall time: 5ns
- Input and output timing reference level: 1.4V
- Output load: See figures (Including scope and jig)



Note1. Ambient temperature range depends on R/I-version. Please see table on page 1.

Read Cycle

Parameter	Symbol	R1WV6416R**-5S		R1WV6416R**-7S		Unit	Note
		Min.	Max.	Min.	Max.		
Read cycle time	t_{RC}	55	-	70	-	ns	
Address access time	t_{AA}	-	55	-	70	ns	
Chip select access time	t_{ACS1}	-	55	-	70	ns	
	t_{ACS2}	-	55	-	70	ns	
Output enable to output valid	t_{OE}	-	25	-	35	ns	
Output hold from address change	t_{OH}	10	-	10	-	ns	
LB#, UB# access time	t_{BA}	-	55	-	70	ns	
Chip select to output in low-Z	t_{CLZ1}	10	-	10	-	ns	2,3
	t_{CLZ2}	10	-	10	-	ns	2,3
LB#, UB# enable to low-Z	t_{BLZ}	5	-	5	-	ns	2,3
Output enable to output in low-Z	t_{OLZ}	5	-	5	-	ns	2,3
Chip deselect to output in high-Z	t_{CHZ1}	0	20	0	25	ns	1,2,3
	t_{CHZ2}	0	20	0	25	ns	1,2,3
LB#, UB# disable to high-Z	t_{BHZ}	0	20	0	25	ns	1,2,3
Output disable to output in high-Z	t_{OHZ}	0	20	0	25	ns	1,2,3

Write Cycle

Parameter	Symbol	R1WV6416R**-5S		R1WV6416R**-7S		Unit	Note
		Min.	Max.	Min.	Max.		
Write cycle time	t_{WC}	55	-	70	-	ns	
Address valid to end of write	t_{AW}	50	-	65	-	ns	
Chip select to end of write	t_{CW}	50	-	65	-	ns	5
Write pulse width	t_{WP}	40	-	55	-	ns	4
LB#, UB# valid to end of write	t_{BW}	50	-	65	-	ns	
Address setup time	t_{AS}	0	-	0	-	ns	6
Write recovery time	t_{WR}	0	-	0	-	ns	7
Data to write time overlap	t_{DW}	25	-	35	-	ns	
Data hold from write time	t_{DH}	0	-	0	-	ns	
Output enable from end of write	t_{OW}	5	-	5	-	ns	2
Output disable to output in high-Z	t_{OHZ}	0	20	0	25	ns	1,2
Write to output in high-Z	t_{WHZ}	0	20	0	25	ns	1,2

Note1. t_{CHZ}, t_{OHZ}, t_{WHZ} and t_{BHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.

2. This parameter is sampled and not 100% tested.

3. At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.

4. A write occurs during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#.

A write begins at the latest transition among CS1# going low, CS2 going high, WE# going low and LB# going low or UB# going low .

A write ends at the earliest transition among CS1# going high, CS2 going low, WE# going high and LB# going high or UB# going high. t_{WP} is measured from the beginning of write to the end of write.

5. t_{CW} is measured from the later of CS1# going low or CS2 going high to end of write.

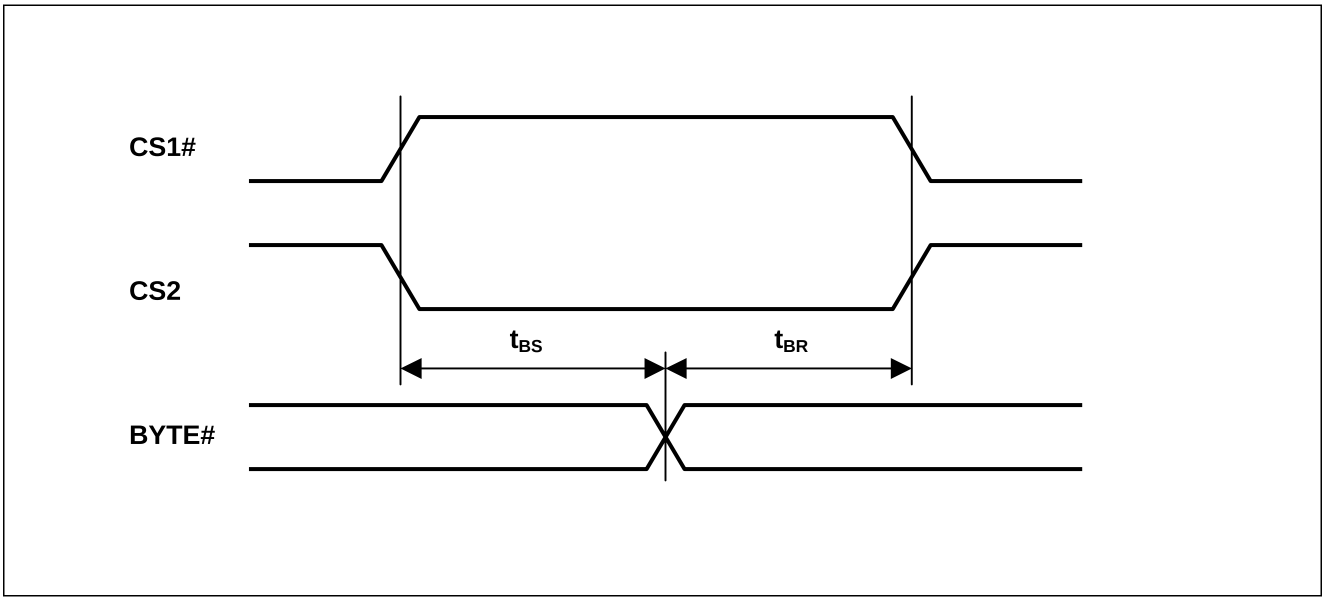
6. t_{AS} is measured the address valid to the beginning of write.

7. t_{WR} is measured from the earliest of CS1# or WE# going high or CS2 going low to the end of write cycle.

BYTE# Timing Conditions

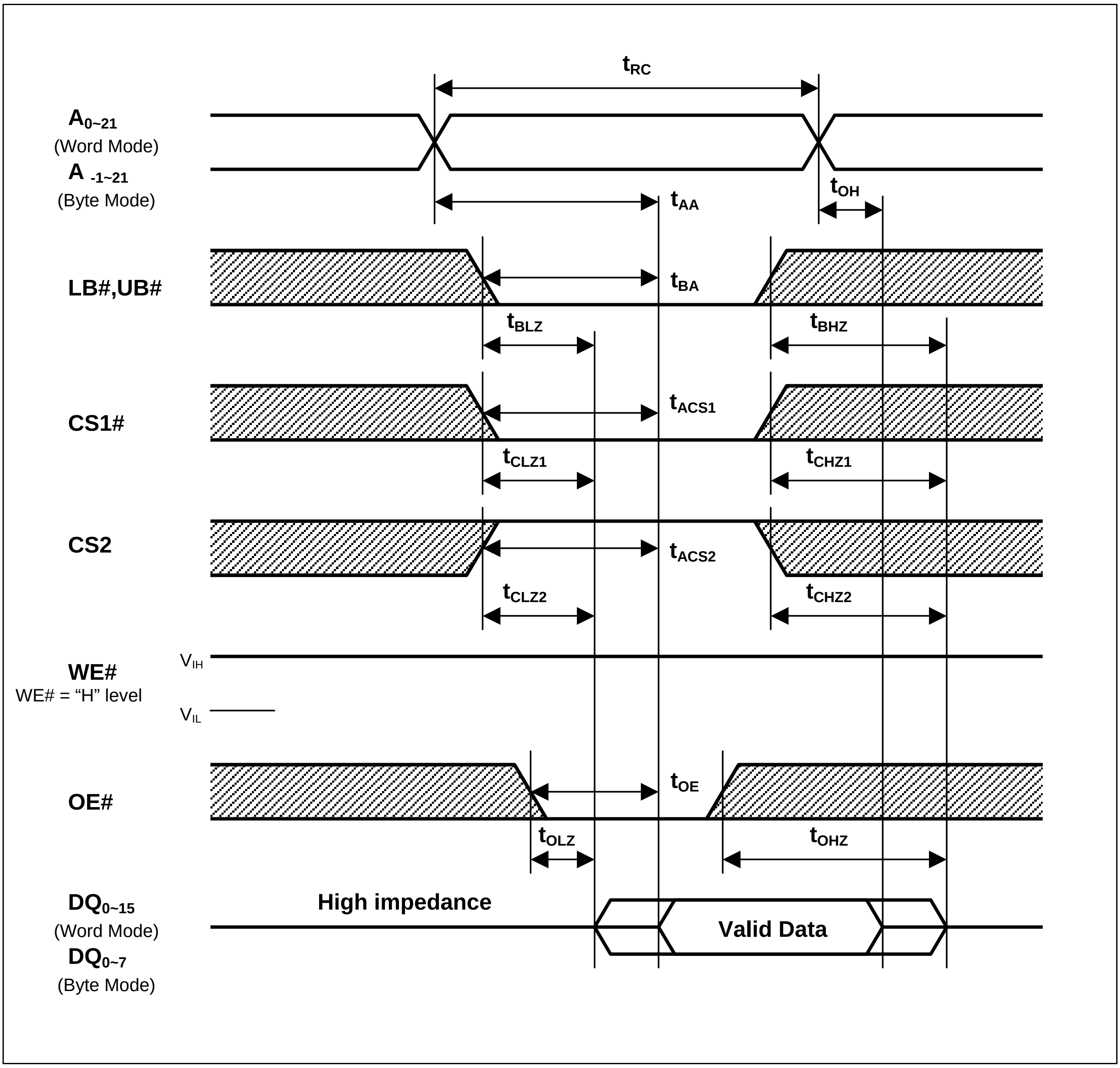
Parameter	Symbol	R1WV6416R**-5S		R1WV6416R**-7S		Unit	Note
		Min.	Max.	Min.	Max.		
Byte setup time	t_{BS}	5	-	5	-	ms	
Byte recovery time	t_{BR}	5	-	5	-	ms	

BYTE# Timing Waveforms



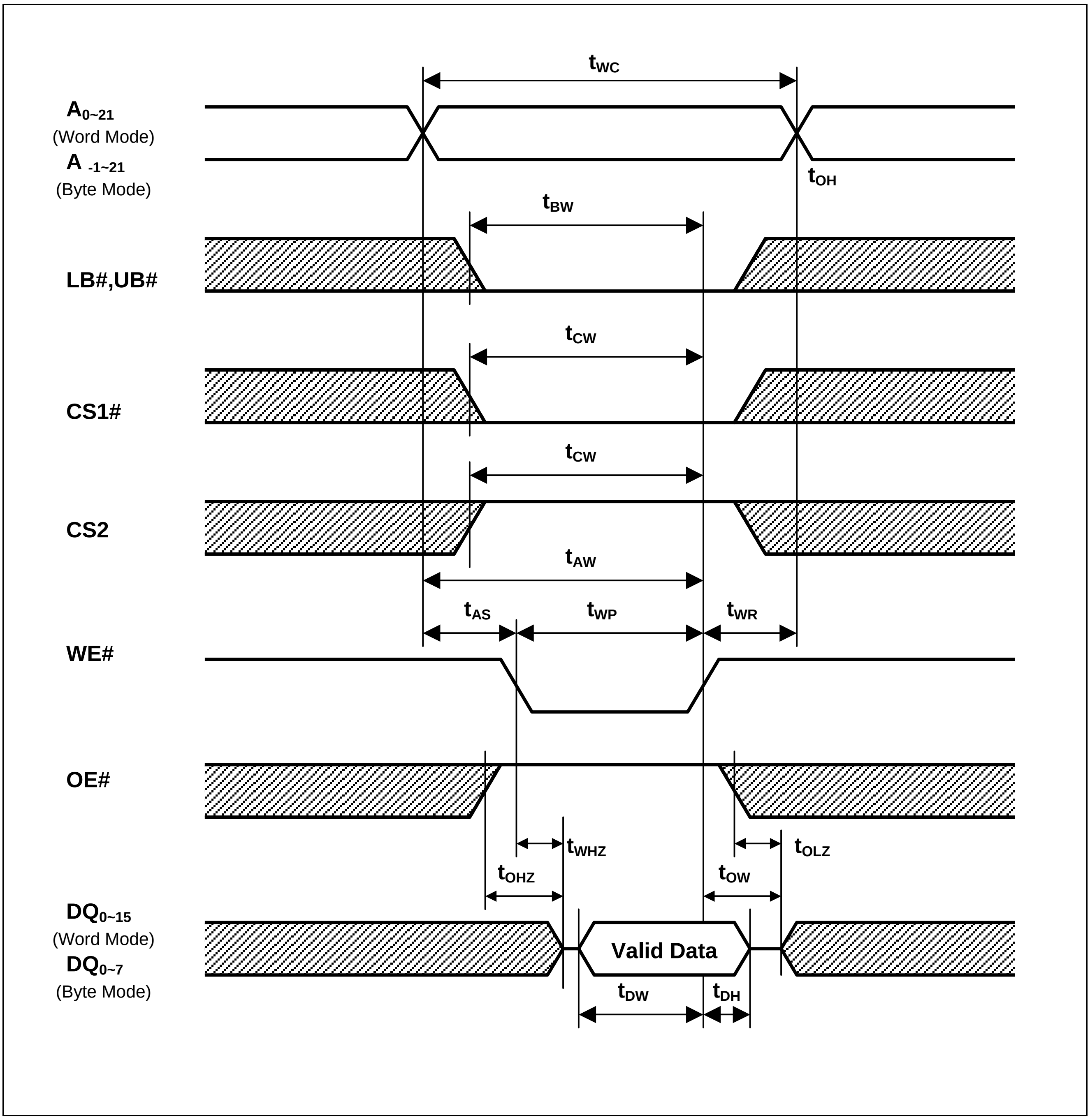
Timing Waveforms

Read Cycle*1



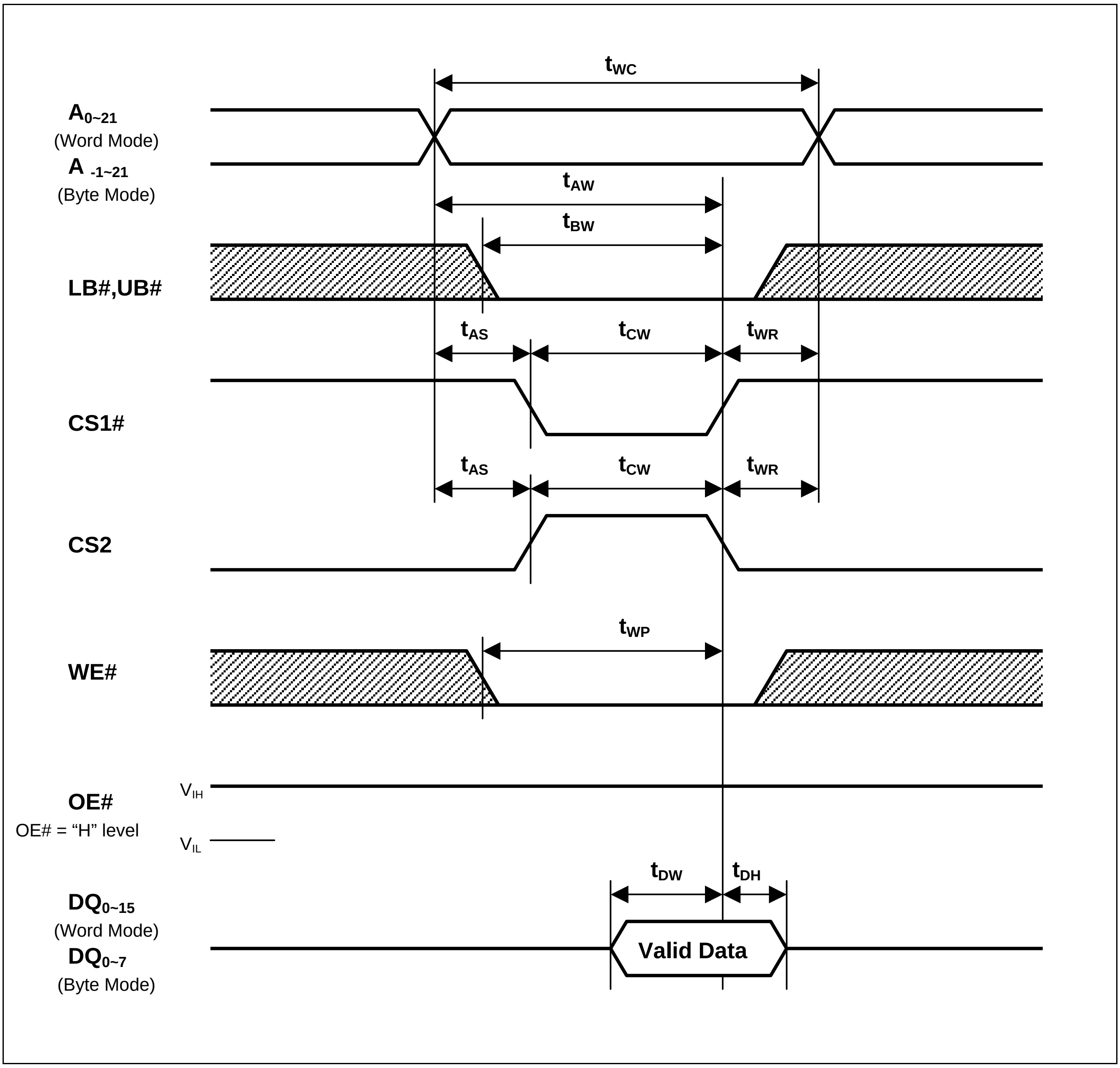
Note1. BYTE# ≥ Vcc – 0.2V or BYTE# ≤ 0.2V

Write Cycle (1)[*1] (WE# CLOCK)



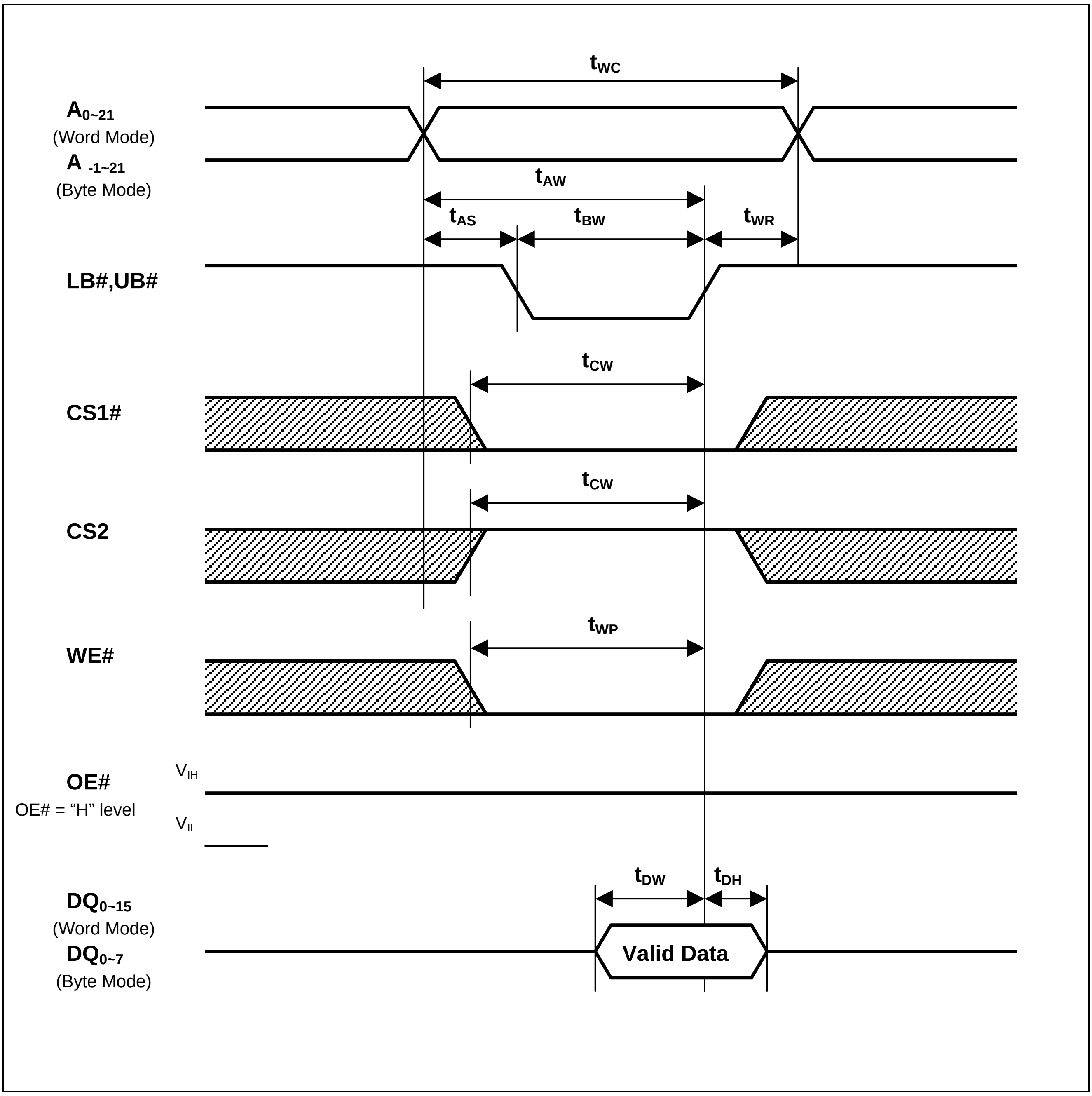
Note1. BYTE# ≥ Vcc – 0.2V or BYTE# ≤ 0.2V

Write Cycle (2)[*1] (CS1#, CS2 CLOCK)



Note1. BYTE# ≥ Vcc – 0.2V or BYTE# ≤ 0.2V

Write Cycle (3)[*1] (LB#, UB# CLOCK)



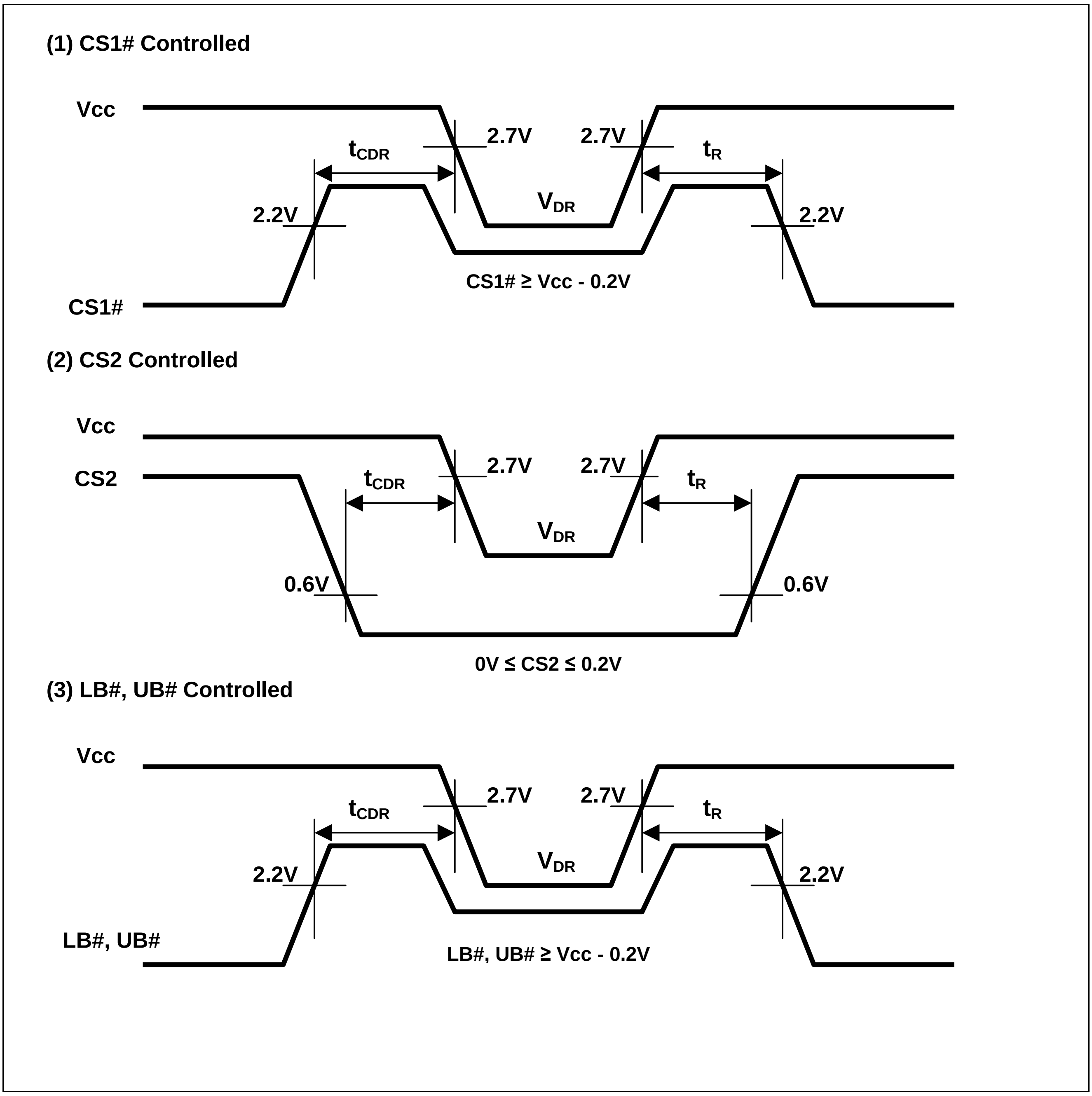
Note1. BYTE# ≥ Vcc – 0.2V or BYTE# ≤ 0.2V

Low Vcc Data Retention Characteristics

Parameter	Symbol	Min.	Typ	Max.	Unit	Test conditions[3,4]	
V_{CC} for data retention	V_{DR}	2.0	-	3.6	V	Vin ≥ 0V BYTE# ≥ Vcc -0.2V or BYTE# ≤ 0.2V (1) 0V ≤ CS2 ≤ 0.2V or (2) CS1# ≥ V_{CC}-0.2V, CS2 ≥ V_{CC}-0.2V or (3) LB# = UB# ≥ V_{CC}-0.2V, CS1# ≤ 0.2V, CS2 ≥ V_{CC}-0.2V	
Data retention current	I_{CCDR}	-	8[1]	24	µA	~+25°C	Vin ≥ 0V BYTE# ≥ Vcc -0.2V or BYTE# ≤0.2V (1) 0V ≤ CS2 ≤ 0.2V or (2) CS1# ≥ V_{CC}-0.2V, CS2 ≥ V_{CC}-0.2V or (3) LB# = UB# ≥ V_{CC}-0.2V, CS1# ≤ 0.2V, CS2 ≥ V_{CC}-0.2V
		-	14[2]	48	µA	~+40°C	
		-	-	100	µA	~+70°C	
		-	-	160	µA	~+85°C	
Chip select to data retention time	t_{CDR}	0	-	-	ns	See retention waveform.	
Operation recovery time	t_R	5	-	-	ms		

Note 1. Typical parameter indicates the value for the center of distribution at 3.0V (Ta= 25ºC), and not 100% tested.
2. Typical parameter indicates the value for the center of distribution at 3.0V (Ta= 40ºC), and not 100% tested.
3. BYTE# pin is supported for 48-pin TSOP (I) and 52-pin µTSOP (II) packages.
4. CS2 also controls address buffer, WE# buffer ,CS1# buffer ,OE# buffer ,LB# ,UB# buffer and Din buffer. If CS2 controls data retention mode, Vin levels (address, WE# ,OE#,CS1#,LB#,UB#,I/O) can be in the high impedance state. If CS1# controls data retention mode, CS2 must be CS2 ≥ Vcc-0.2V or0V ≤ CS2 ≤ 0.2V. The other input levels (address, WE# ,OE#,CS1#,LB#,UB#,I/O) can be in the high impedance state.

Low Vcc Data Retention Timing Waveforms*1



Note1. BYTE# ≥ Vcc – 0.2V or BYTE# ≤ 0.2V

Revision History	R1WV6416R Data Sheet

Rev.	Date	Contents pf Revision	
		Page	Description
0.01	Mar.24, 2008	-	Initial issue: Preliminary Data Sheet
1.00	May 07, 2009	-	Finalized
		5	Operation Table corrected
		6	Error corrected: I_{SB} Test condition CS2=V_{IH}->V_{IL}

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

RENESAS SALES OFFICES http://www.renesas.com

Refer to "**http://www.renesas.com/en/network**" for the latest and detailed information.

Renesas Technology America, Inc.
450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology (Shanghai) Co., Ltd.
Unit 204, 205, AZIACenter, No.1233 Lujiazui Ring Rd, Pudong District, Shanghai, China 200120
Tel: <86> (21) 5877-1818, Fax: <86> (21) 6887-7858/7898

Renesas Technology Hong Kong Ltd.
7th Floor, North Tower, World Finance Centre, Harbour City, Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2377-3473

Renesas Technology Taiwan Co., Ltd.
10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 3518-3399

Renesas Technology Singapore Pte. Ltd.
1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Renesas Technology Korea Co., Ltd.
Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

Renesas Technology Malaysia Sdn. Bhd
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510

Colophon .7.2

To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

RENESAS

ООО "ЛайфЭлектроникс" "LifeElectronics" LLC

ИНН 7805602321 КПП 780501001 Р/С 40702810122510004610 ФАКБ "АБСОЛЮТ БАНК" (ЗАО) в г.Санкт-Петербурге К/С 30101810900000000703 БИК 044030703

Компания «Life Electronics» занимается поставками электронных компонентов импортного и отечественного производства от производителей и со складов крупных дистрибьюторов Европы, Америки и Азии.

С конца 2013 года компания активно расширяет линейку поставок компонентов по направлению коаксиальный кабель, кварцевые генераторы и конденсаторы (керамические, пленочные, электролитические), за счёт заключения дистрибьюторских договоров

Мы предлагаем:

- *Конкурентоспособные цены и скидки постоянным клиентам.*
- *Специальные условия для постоянных клиентов.*
- *Подбор аналогов.*
- *Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.*

- *Приемлемые сроки поставки, возможна ускоренная поставка.*
- *Доставку товара в любую точку России и стран СНГ.*
- *Комплексную поставку.*
- *Работу по проектам и поставку образцов.*
- *Формирование склада под заказчика.*

- *Сертификаты соответствия на поставляемую продукцию (по желанию клиента).*
- *Тестирование поставляемой продукции.*
- *Поставку компонентов, требующих военную и космическую приемку.*
- *Входной контроль качества.*
- *Наличие сертификата ISO.*

В составе нашей компании организован Конструкторский отдел, призванный помогать разработчикам, и инженерам.

Конструкторский отдел помогает осуществить:

- *Регистрацию проекта у производителя компонентов.*
- *Техническую поддержку проекта.*
- *Защиту от снятия компонента с производства.*
- *Оценку стоимости проекта по компонентам.*
- *Изготовление тестовой платы монтаж и пусконаладочные работы.*

Тел: +7 (812) 336 43 04 (многоканальный)
Email: org@lifeelectronics.ru

www.lifeelectronics.ru