

# R1WV6416R Series

64Mb Advanced LPSRAM (4M word x 16bit / 8M word x 8bit)

REJ03C0368-0100

Rev.1.00

2009.05.07

## Description

The R1WV6416R Series is a family of low voltage 64-Mbit static RAMs organized as 4,194,304-word by 16-bit, fabricated by Renesas's high-performance 0.15um CMOS and TFT technologies.

The R1WV6416R Series is suitable for memory applications where a simple interfacing, battery operating and battery backup are the important design objectives.

The R1WV6416R Series is provided in 48-pin thin small outline package [TSOP (I): 12mm x 20mm with pin pitch of 0.5mm], 52-pin micro thin small outline package [ $\mu$ TSOP (II): 10.79mm x 10.49mm with pin pitch of 0.4mm] and 48-ball fine pitch ball grid array [f-BGA] package. It gives the best solution for compaction of mounting area as well as flexibility of wiring pattern of printed circuit boards.

## Features

- Single 2.7~3.6V power supply
- Small stand-by current: 8  $\mu$ A (3.0V, typical)
- No clocks, No refresh
- All inputs and outputs are TTL compatible.
- Easy memory expansion by CS1#, CS2, LB# and UB#
- Common Data I/O
- Three-state outputs: OR-tie Capability
- OE# prevents data contention on the I/O bus

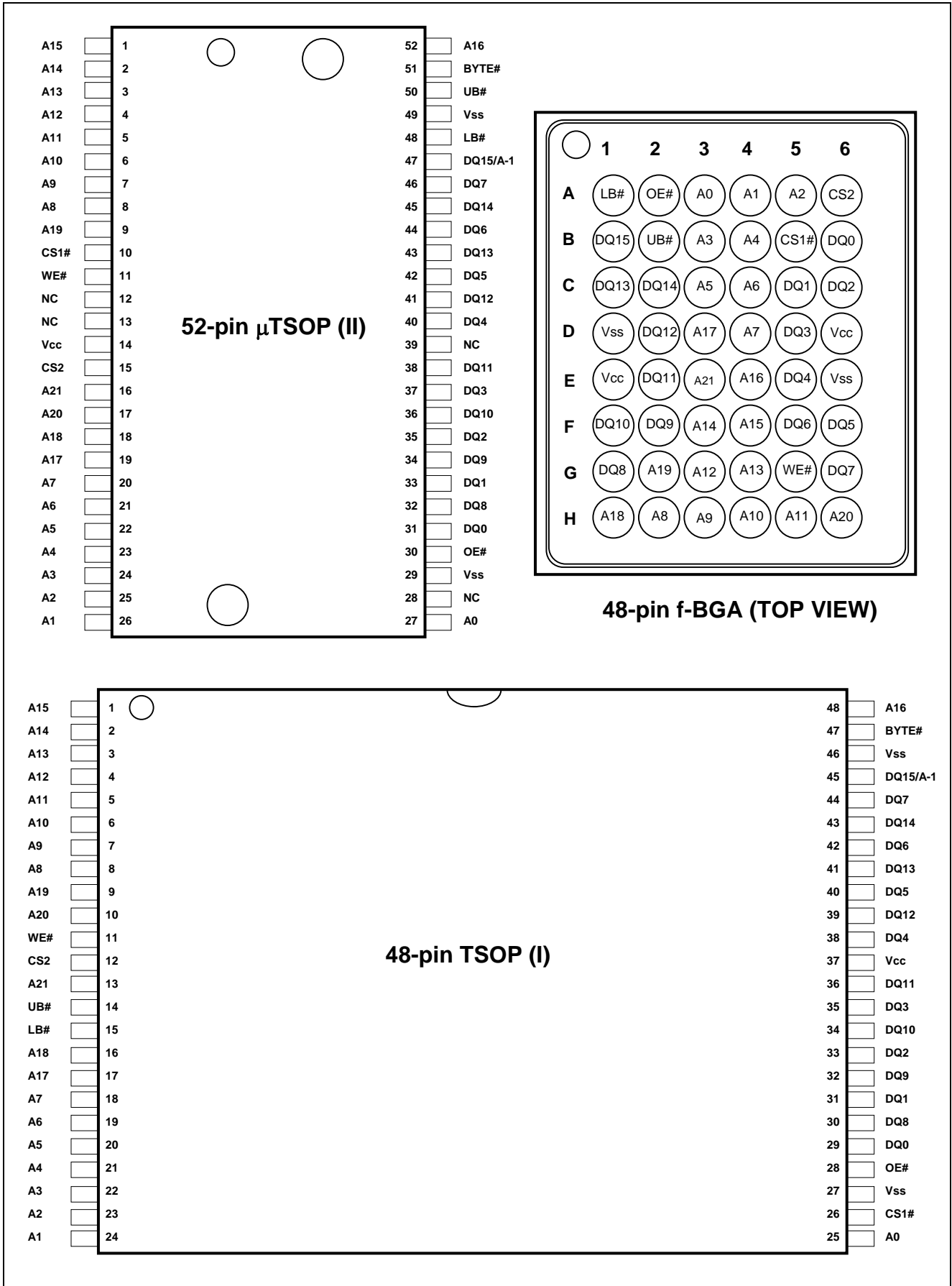
## Ordering Information

Type No.	Access time	Package
R1WV6416RSA-5S%	55 ns	12mm x 20mm 48-pin plastic TSOP (I) (normal-bend type) (48P3R)
R1WV6416RSA-7S%	70 ns	
R1WV6416RSD-5S%	55 ns	350 mil 52-pin plastic $\mu$ -TSOP (II) (normal-bend type) (52PTG)
R1WV6416RSD-7S%	70 ns	
R1WV6416RBG-5S%	55 ns	f-BGA 0.75mm pitch 48-ball
R1WV6416RBG-7S%	70 ns	

% - Temperature version; see table below

%	Temperature Range
R	0 ~ +70 °C
I	-40 ~ +85 °C

Pin Arrangement

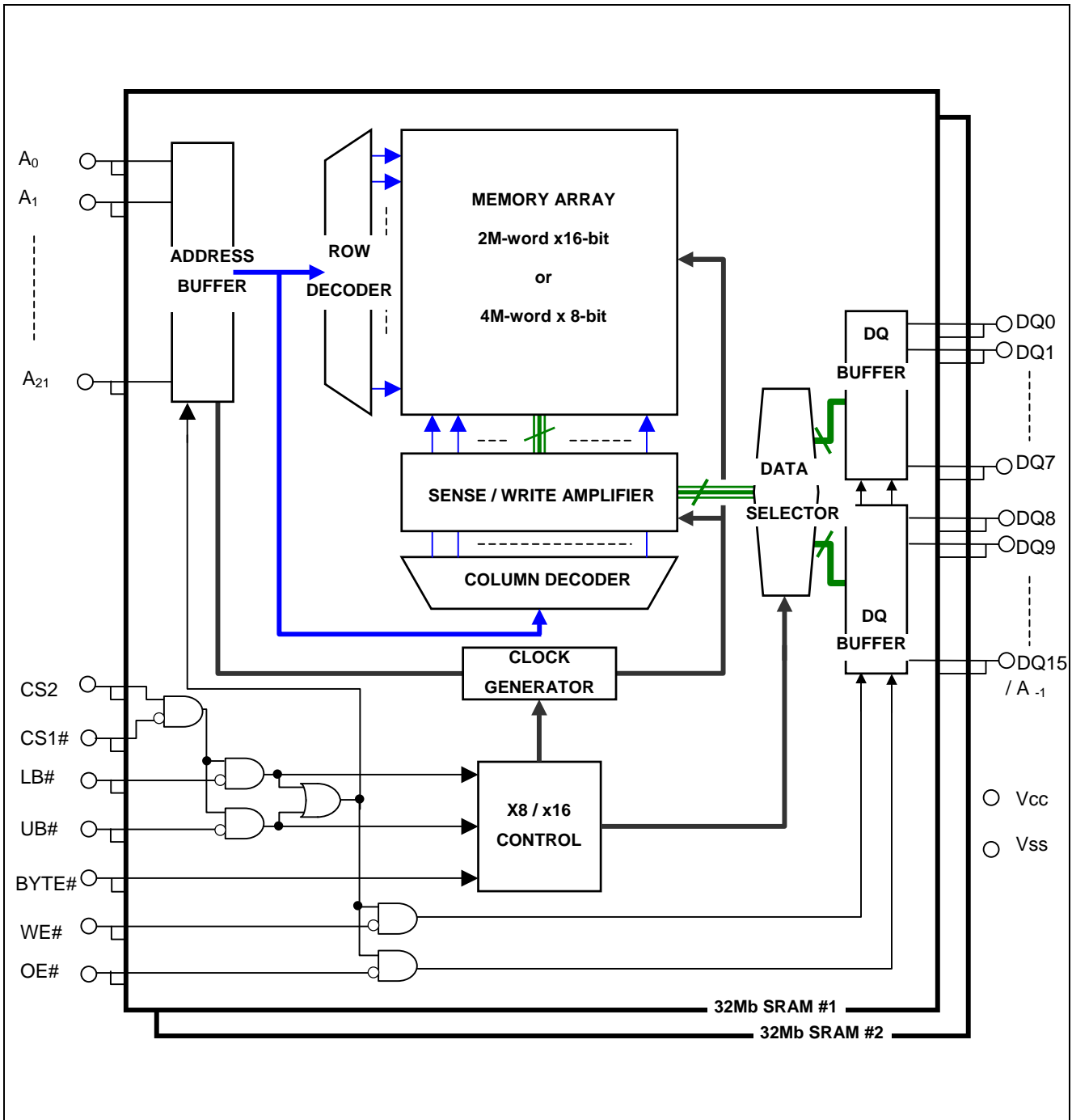


## Pin Description

Pin name	Function
Vcc	Power supply
Vss	Ground
A0 to A21	Address input (word mode)
A-1 to A21	Address input (byte mode)
DQ0 to DQ15	Data input/output
CS1#	Chip select 1
CS2	Chip select 2
WE#	Write enable
OE#	Output enable
LB#	Lower byte enable
UB#	Upper byte enable
BYTE#	Byte control mode enable
NC	Non connection

Note: BYTE# pin is supported for 48-pin TSOP (I) and 52-pin  $\mu$ TSOP (II) packages.

Block Diagram



Note: BYTE# pin is supported for 48-pin TSOP (I) and 52-pin  $\mu$ TSOP (II) packages.

## Operation Table

CS1#	CS2	BYTE#	LB#	UB#	WE#	OE#	DQ0~7	DQ8~14	DQ15	Operation
H	X	X	X	X	X	X	High-Z	High-Z	High-Z	Stand-by
X	L	X	X	X	X	X	High-Z	High-Z	High-Z	Stand-by
X	X	H	H	H	X	X	High-Z	High-Z	High-Z	Stand-by
L	H	H	L	H	L	X	Din	High-Z	High-Z	Write in lower byte
L	H	H	L	H	H	L	Dout	High-Z	High-Z	Read in lower byte
L	H	H	L	H	H	H	High-Z	High-Z	High-Z	Output disable
L	H	H	H	L	L	X	High-Z	Din	Din	Write in upper byte
L	H	H	H	L	H	L	High-Z	Dout	Dout	Read in upper byte
L	H	H	H	L	H	H	High-Z	High-Z	High-Z	Output disable
L	H	H	L	L	L	X	Din	Din	Din	Word write
L	H	H	L	L	H	L	Dout	Dout	Dout	Word read
L	H	H	L	L	H	H	High-Z	High-Z	High-Z	Output disable
L	H	L	L	L	L	X	Din	High-Z	A-1	Byte write
L	H	L	L	L	H	L	Dout	High-Z	A-1	Byte read
L	H	L	L	L	H	H	High-Z	High-Z	A-1	Output disable

Note1. H:  $V_{IH}$  L:  $V_{IL}$  X:  $V_{IH}$  or  $V_{IL}$

2. BYTE# pin is supported for 48-pin TSOP (I) and 52-pin  $\mu$ TSOP (II) packages.

3. When apply BYTE# = "L", please assign LB#=UB#="L".

## Absolute Maximum Ratings

Parameter	Symbol	Value	unit
Power supply voltage relative to Vss	Vcc	-0.5 to +4.6	V
Terminal voltage on any pin relative to Vss	$V_T$	$-0.5^{*1}$ to $V_{cc}+0.3^{*2}$	V
Power dissipation	$P_T$	0.7	W
Operation temperature	$T_{opr}^{*3}$	R ver.	0 to +70
		I ver.	-40 to +85
Storage temperature range	Tstg	-65 to 150	°C
Storage temperature range under bias	$T_{bias}^{*3}$	R ver.	0 to +70
		I ver.	-40 to +85

Note 1. -2.0V in case of AC (Pulse width  $\leq 30$ ns)

2. Maximum voltage is +4.6V.

3. Ambient temperature range depends on R/I-version. Please see table on page 1.

## Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note	
Supply voltage	V <sub>CC</sub>	2.7	3.0	3.6	V		
	V <sub>SS</sub>	0	0	0	V		
Input high voltage	V <sub>IH</sub>	2.4	-	V <sub>CC</sub> +0.2	V		
Input low voltage	V <sub>IL</sub>	-0.2	-	0.4	V	1	
Ambient temperature range	R ver.	T <sub>a</sub>	0	-	+70	°C	2
	I ver.		-40	-	+85	°C	2

Note 1. -2.0V in case of AC (Pulse width ≤ 30ns)

2. Ambient temperature range depends on R/I-version. Please see table on page 1.

## DC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions <sup>3</sup>
Input leakage current	I <sub>LI</sub>	-	-	1	μA	V <sub>in</sub> = V <sub>SS</sub> to V <sub>CC</sub>
Output leakage current	I <sub>LO</sub>	-	-	1	μA	BYTE# ≥ V <sub>CC</sub> -0.2V or BYTE# ≤ 0.2V CS1# =V <sub>IH</sub> or CS2 =V <sub>IL</sub> or OE# =V <sub>IH</sub> or WE# =V <sub>IL</sub> or LB# = UB# =V <sub>IH</sub> , VI/O =V <sub>SS</sub> to V <sub>CC</sub>
Average operating current	I <sub>CC1</sub>	-	45 <sup>*1</sup>	60	mA	Min. cycle, duty =100%, I/I/O = 0mA BYTE# ≥ V <sub>CC</sub> -0.2V or BYTE# ≤ 0.2V CS1# =V <sub>IL</sub> , CS2 =V <sub>IH</sub> , Others = V <sub>IH</sub> /V <sub>IL</sub>
	I <sub>CC2</sub>	-	5 <sup>*1</sup>	10	mA	Cycle =1μs, duty =100%, I/I/O = 0mA BYTE# ≥ V <sub>CC</sub> -0.2V or BYTE# ≤ 0.2V CS1# ≤ 0.2V, CS2 ≥ V <sub>CC</sub> -0.2V, V <sub>IH</sub> ≥ V <sub>CC</sub> -0.2V, V <sub>IL</sub> ≤ 0.2V
Standby current	I <sub>SB</sub>	-	0.1 <sup>*1</sup>	0.3	mA	BYTE# ≥ V <sub>CC</sub> -0.2V or BYTE# ≤ 0.2V CS2 =V <sub>IL</sub>
Standby current	I <sub>SB1</sub>	-	8 <sup>*1</sup>	24	μA	~+25°C V <sub>in</sub> ≥ 0V BYTE# ≥ V <sub>CC</sub> -0.2V or BYTE# ≤ 0.2V
		-	14 <sup>*2</sup>	48	μA	~+40°C (1) 0V ≤ CS2 ≤ 0.2V or (2) CS1# ≥ V <sub>CC</sub> -0.2V, CS2 ≥ V <sub>CC</sub> -0.2V or
		-	-	100	μA	~+70°C (3) LB# = UB# ≥ V <sub>CC</sub> -0.2V, CS1# ≤ 0.2V, CS2 ≥ V <sub>CC</sub> -0.2V
		-	-	160	μA	~+85°C
Output high voltage	V <sub>OH</sub>	2.4	-	-	V	BYTE# ≥ V <sub>CC</sub> -0.2V or BYTE# ≤ 0.2V I <sub>OH</sub> = -0.5mA
Output low voltage	V <sub>OL</sub>	-	-	0.4	V	BYTE# ≥ V <sub>CC</sub> -0.2V or BYTE# ≤ 0.2V I <sub>OL</sub> = 2mA

Note 1. Typical parameter indicates the value for the center of distribution at 3.0V (T<sub>a</sub> = 25°C), and not 100% tested.

2. Typical parameter indicates the value for the center of distribution at 3.0V (T<sub>a</sub> = 40°C), and not 100% tested.

3. BYTE# pin is supported for 48-pin TSOP (I) and 52-pin μTSOP (II) packages.

## Capacitance

(Ta =25°C, f =1MHz)

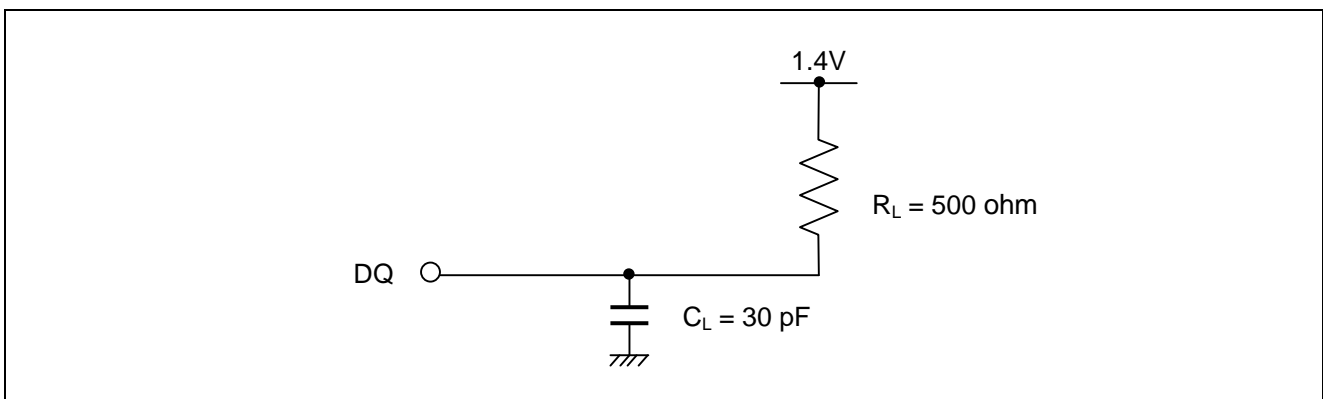
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions	Note
Input capacitance	C <sub>in</sub>	-	-	20	pF	V <sub>in</sub> =0V	1
Input / output capacitance	C <sub>I/O</sub>	-	-	20	pF	V <sub>I/O</sub> =0V	1

Note1. This parameter is sampled and not 100% tested.

## AC Characteristics

Test Conditions (V<sub>cc</sub> = 2.7V ~ 3.6V, Ta = 0 ~ +70°C / -40 ~ +85°C\*1)

- Input pulse levels: V<sub>IL</sub> = 0.4V, V<sub>IH</sub> = 2.4V
- Input rise and fall time: 5ns
- Input and output timing reference level: 1.4V
- Output load: See figures (Including scope and jig)



Note1. Ambient temperature range depends on R/I-version. Please see table on page 1.

## Read Cycle

Parameter	Symbol	R1WV6416R**-5S		R1WV6416R**-7S		Unit	Note
		Min.	Max.	Min.	Max.		
Read cycle time	t <sub>RC</sub>	55	-	70	-	ns	
Address access time	t <sub>AA</sub>	-	55	-	70	ns	
Chip select access time	t <sub>ACS1</sub>	-	55	-	70	ns	
	t <sub>ACS2</sub>	-	55	-	70	ns	
Output enable to output valid	t <sub>OE</sub>	-	25	-	35	ns	
Output hold from address change	t <sub>OH</sub>	10	-	10	-	ns	
LB#, UB# access time	t <sub>BA</sub>	-	55	-	70	ns	
Chip select to output in low-Z	t <sub>CLZ1</sub>	10	-	10	-	ns	2,3
	t <sub>CLZ2</sub>	10	-	10	-	ns	2,3
LB#, UB# enable to low-Z	t <sub>BLZ</sub>	5	-	5	-	ns	2,3
Output enable to output in low-Z	t <sub>OLZ</sub>	5	-	5	-	ns	2,3
Chip deselect to output in high-Z	t <sub>CHZ1</sub>	0	20	0	25	ns	1,2,3
	t <sub>CHZ2</sub>	0	20	0	25	ns	1,2,3
LB#, UB# disable to high-Z	t <sub>BHZ</sub>	0	20	0	25	ns	1,2,3
Output disable to output in high-Z	t <sub>OHZ</sub>	0	20	0	25	ns	1,2,3



## Write Cycle

Parameter	Symbol	R1WV6416R**-5S		R1WV6416R**-7S		Unit	Note
		Min.	Max.	Min.	Max.		
Write cycle time	$t_{WC}$	55	-	70	-	ns	
Address valid to end of write	$t_{AW}$	50	-	65	-	ns	
Chip select to end of write	$t_{CW}$	50	-	65	-	ns	5
Write pulse width	$t_{WP}$	40	-	55	-	ns	4
LB#, UB# valid to end of write	$t_{BW}$	50	-	65	-	ns	
Address setup time	$t_{AS}$	0	-	0	-	ns	6
Write recovery time	$t_{WR}$	0	-	0	-	ns	7
Data to write time overlap	$t_{DW}$	25	-	35	-	ns	
Data hold from write time	$t_{DH}$	0	-	0	-	ns	
Output enable from end of write	$t_{OW}$	5	-	5	-	ns	2
Output disable to output in high-Z	$t_{OHZ}$	0	20	0	25	ns	1,2
Write to output in high-Z	$t_{WHZ}$	0	20	0	25	ns	1,2

Note1.  $t_{CHZ}$ ,  $t_{OHZ}$ ,  $t_{WHZ}$  and  $t_{BHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.

2. This parameter is sampled and not 100% tested.

3. At any given temperature and voltage condition,  $t_{HZ}$  max is less than  $t_{LZ}$  min both for a given device and from device to device.

4. A write occurs during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#.

A write begins at the latest transition among CS1# going low, CS2 going high, WE# going low and LB# going low or UB# going low .

A write ends at the earliest transition among CS1# going high, CS2 going low, WE# going high and LB# going high or UB# going high.  $t_{WP}$  is measured from the beginning of write to the end of write.

5.  $t_{CW}$  is measured from the later of CS1# going low or CS2 going high to end of write.

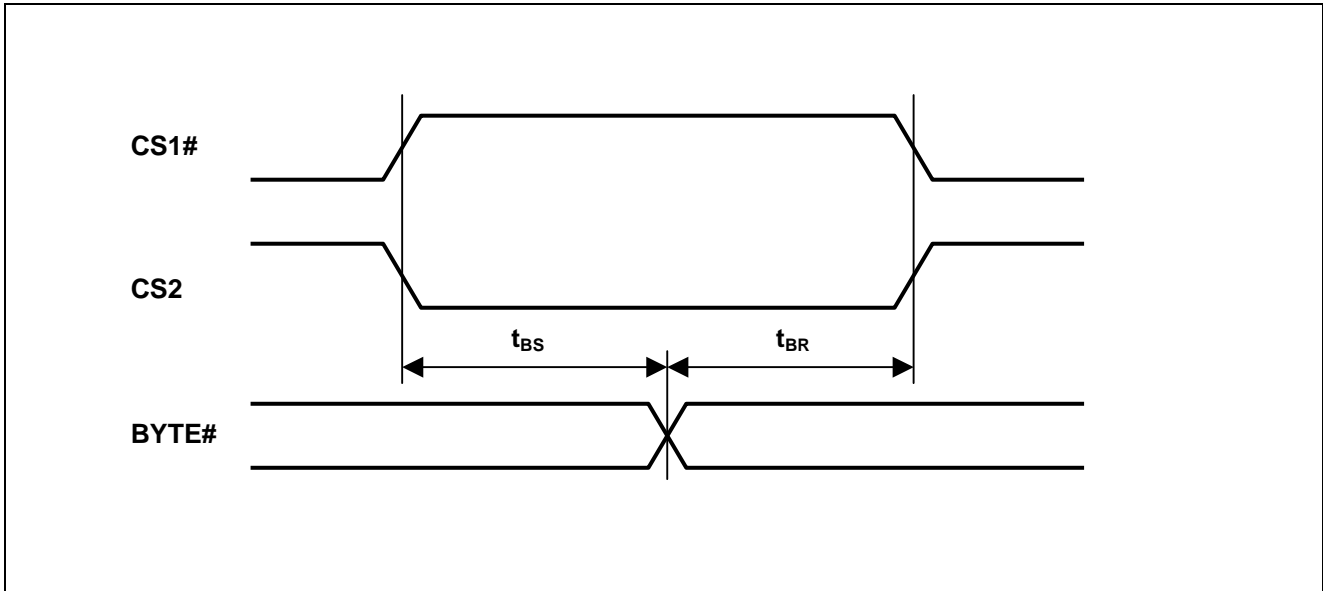
6.  $t_{AS}$  is measured the address valid to the beginning of write.

7.  $t_{WR}$  is measured from the earliest of CS1# or WE# going high or CS2 going low to the end of write cycle.

## BYTE# Timing Conditions

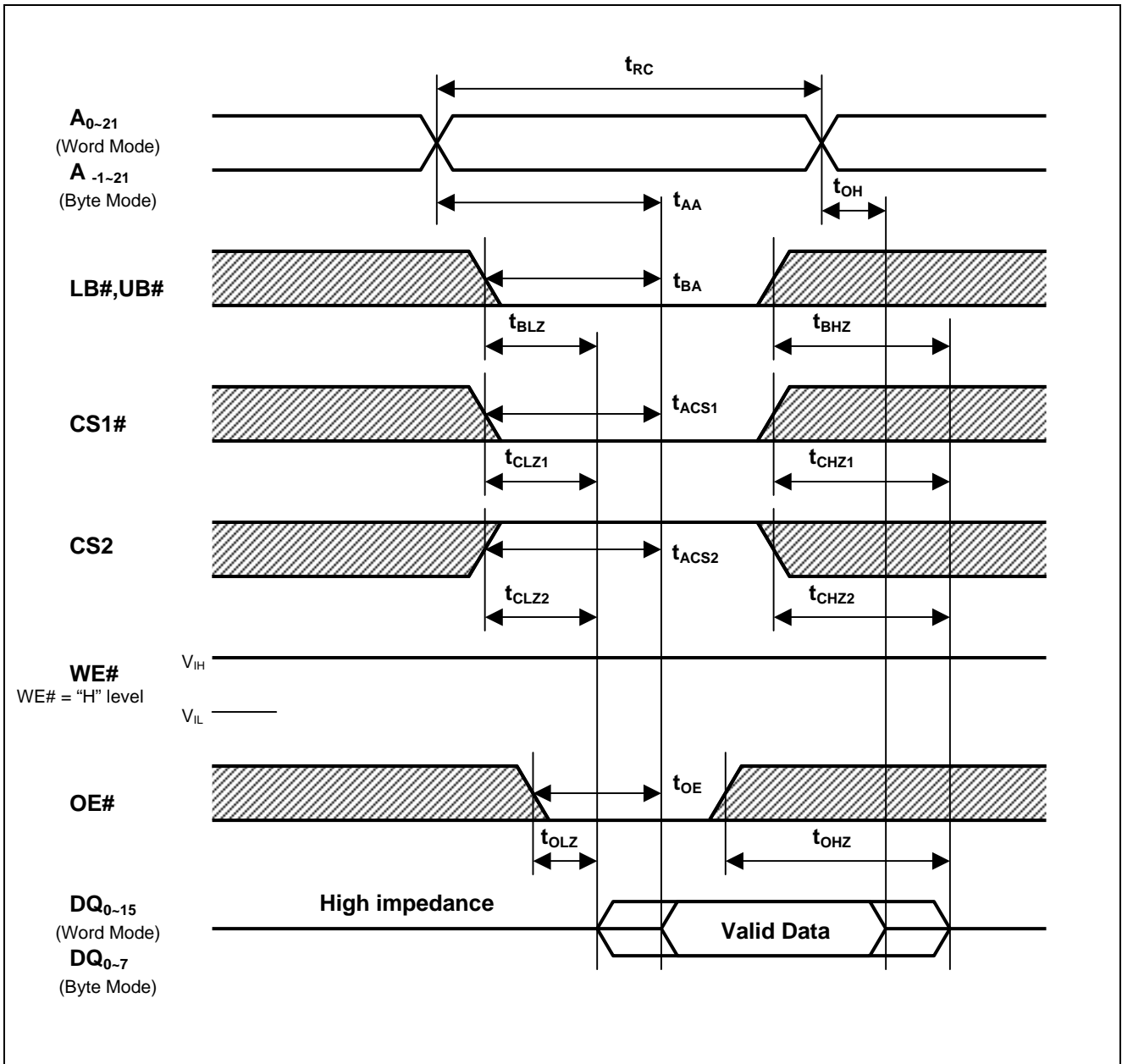
Parameter	Symbol	R1WV6416R**-5S		R1WV6416R**-7S		Unit	Note
		Min.	Max.	Min.	Max.		
Byte setup time	$t_{BS}$	5	-	5	-	ms	
Byte recovery time	$t_{BR}$	5	-	5	-	ms	

## BYTE# Timing Waveforms



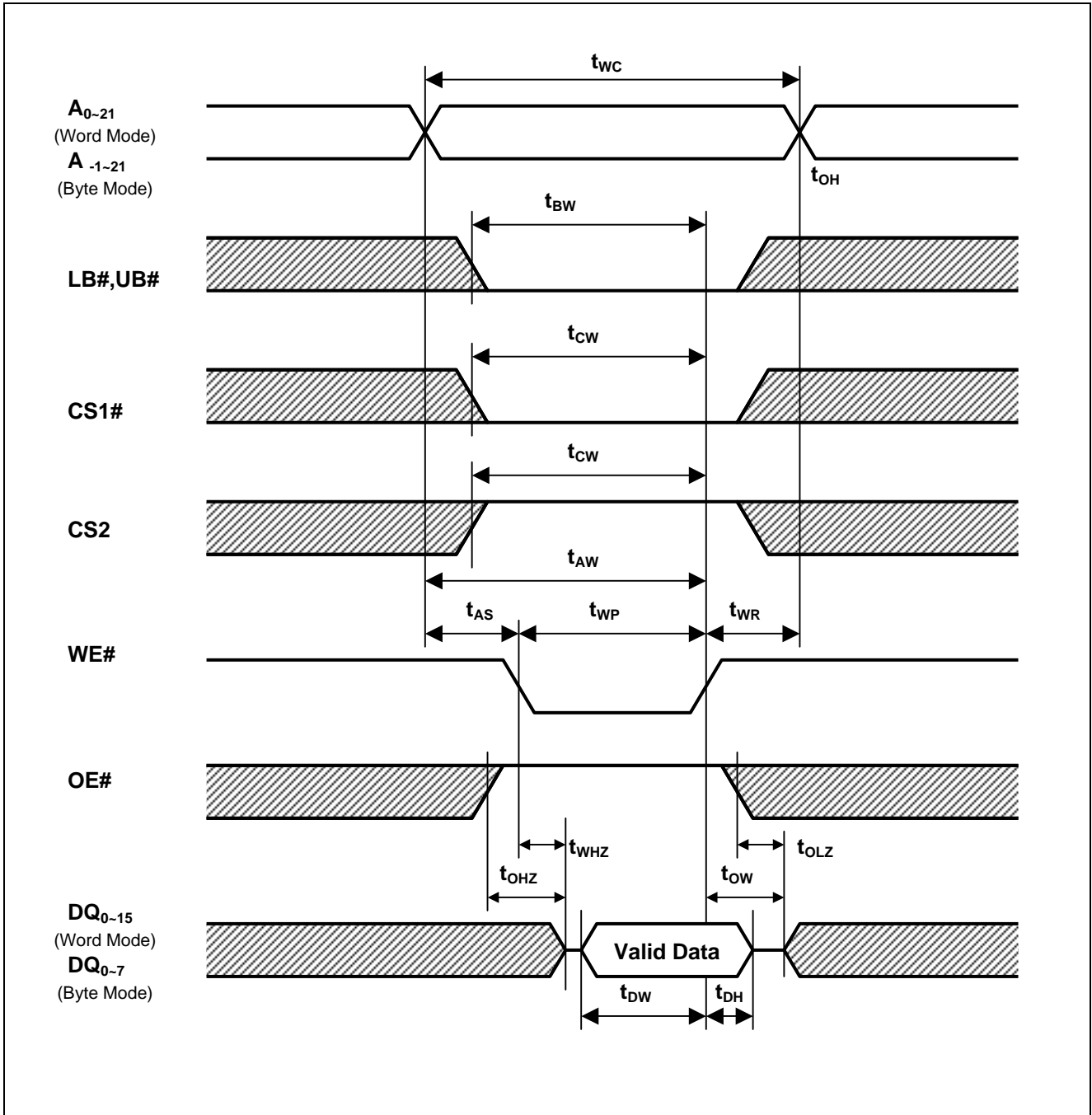
Timing Waveforms

Read Cycle<sup>\*1</sup>



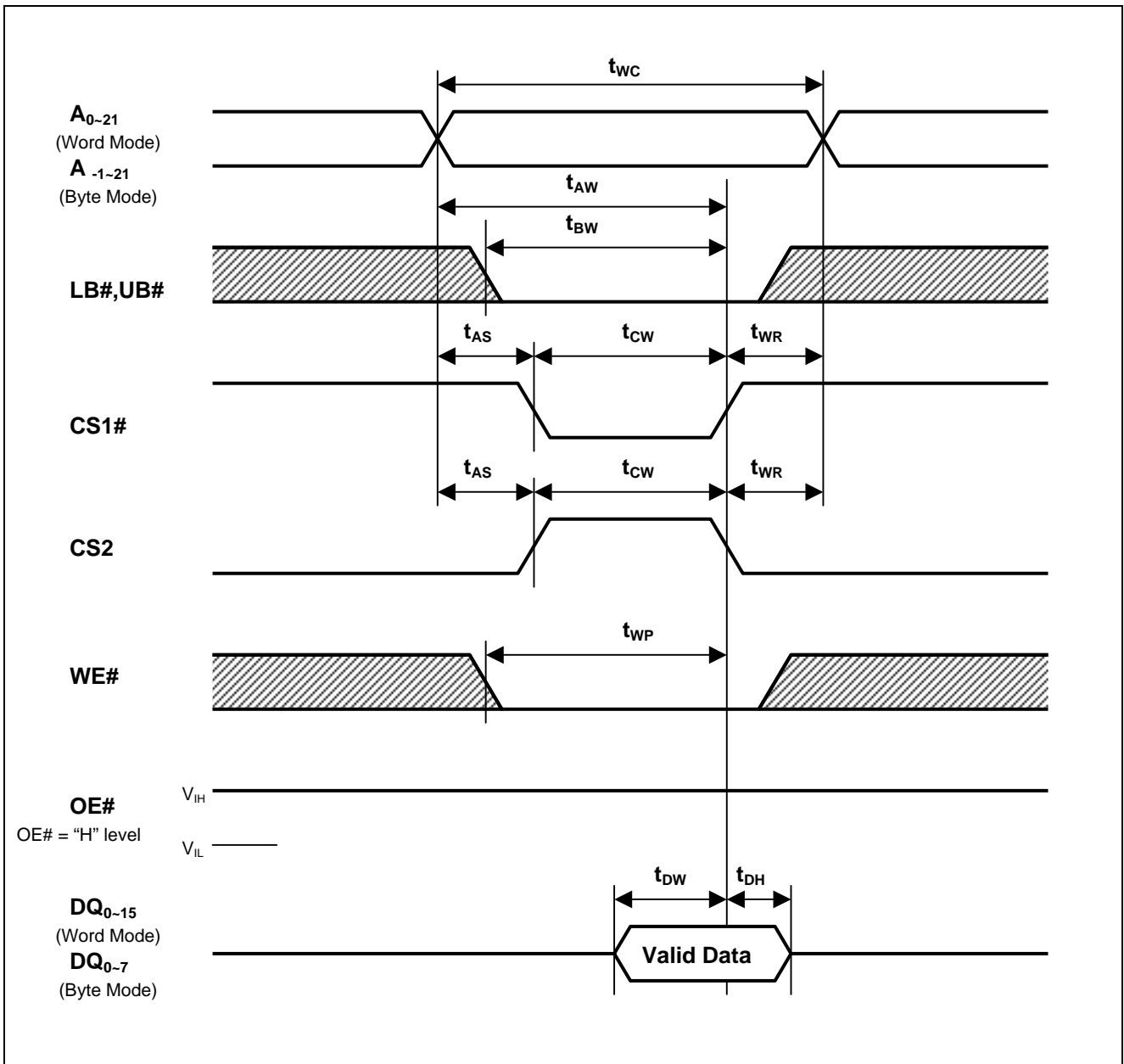
Note1. BYTE#  $\geq V_{CC} - 0.2V$  or BYTE#  $\leq 0.2V$

Write Cycle (1)<sup>\*1</sup> (WE# CLOCK)



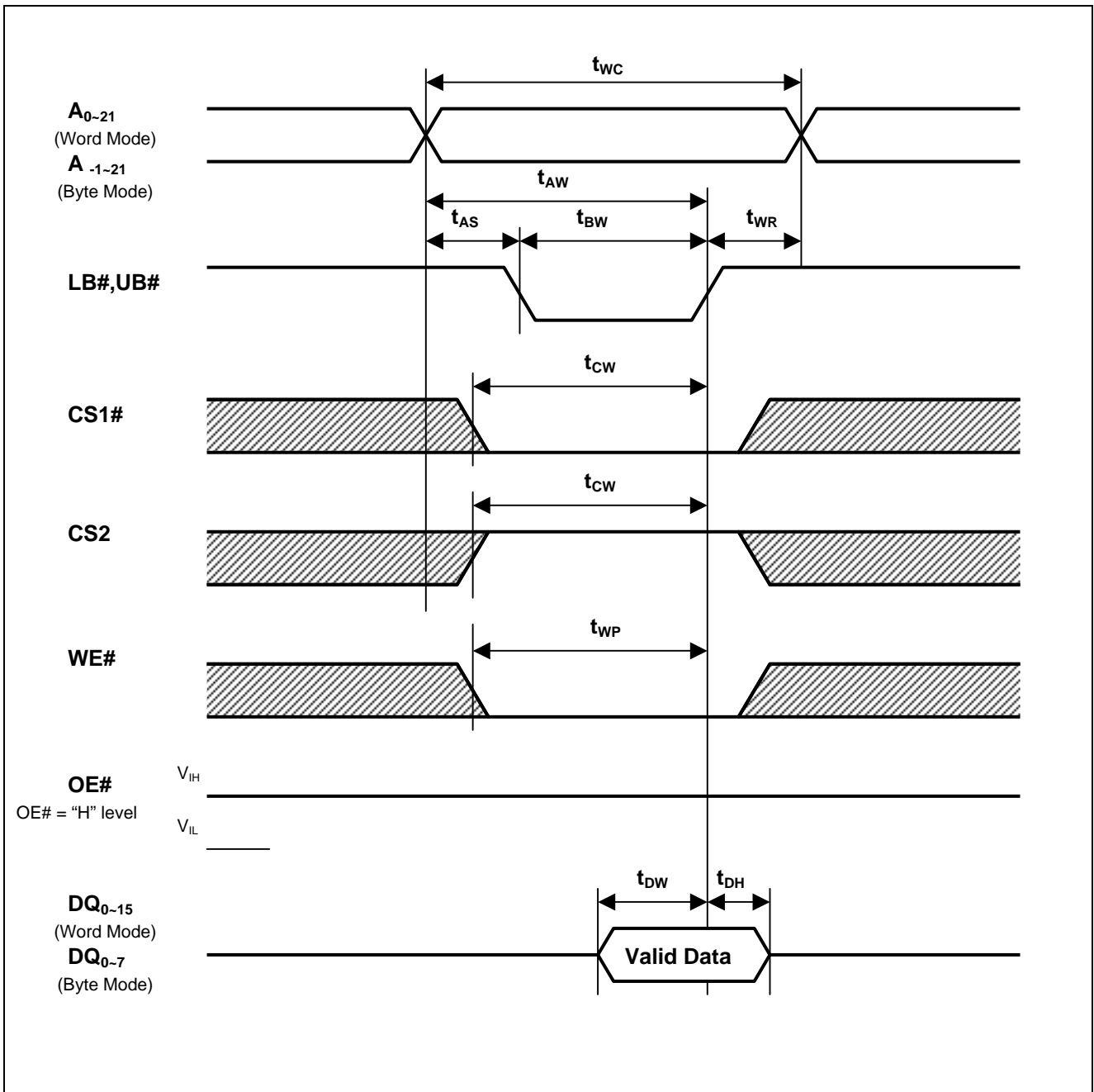
Note1. BYTE# ≥ V<sub>CC</sub> - 0.2V or BYTE# ≤ 0.2V

Write Cycle (2)<sup>\*1</sup> (CS1#, CS2 CLOCK)



Note1. BYTE#  $\geq V_{CC} - 0.2V$  or BYTE#  $\leq 0.2V$

Write Cycle (3)<sup>\*1</sup> (LB#, UB# CLOCK)



Note1. BYTE#  $\geq V_{CC} - 0.2V$  or BYTE#  $\leq 0.2V$

## Low Vcc Data Retention Characteristics

Parameter	Symbol	Min.	Typ	Max.	Unit	Test conditions <sup>3,4</sup>	
V <sub>CC</sub> for data retention	V <sub>DR</sub>	2.0	-	3.6	V	Vin ≥ 0V BYTE# ≥ V <sub>CC</sub> -0.2V or BYTE# ≤ 0.2V (1) 0V ≤ CS2 ≤ 0.2V or (2) CS1# ≥ V <sub>CC</sub> -0.2V, CS2 ≥ V <sub>CC</sub> -0.2V or (3) LB# = UB# ≥ V <sub>CC</sub> -0.2V, CS1# ≤ 0.2V, CS2 ≥ V <sub>CC</sub> -0.2V	
Data retention current	I <sub>CCDR</sub>	-	8 <sup>*1</sup>	24	μA	~+25°C	Vin ≥ 0V BYTE# ≥ V <sub>CC</sub> -0.2V or BYTE# ≤ 0.2V
		-	14 <sup>*2</sup>	48	μA	~+40°C	(1) 0V ≤ CS2 ≤ 0.2V or (2) CS1# ≥ V <sub>CC</sub> -0.2V, CS2 ≥ V <sub>CC</sub> -0.2V or
		-	-	100	μA	~+70°C	(3) LB# = UB# ≥ V <sub>CC</sub> -0.2V, CS1# ≤ 0.2V, CS2 ≥ V <sub>CC</sub> -0.2V
		-	-	160	μA	~+85°C	CS1# ≤ 0.2V, CS2 ≥ V <sub>CC</sub> -0.2V
Chip select to data retention time	t <sub>CDR</sub>	0	-	-	ns	See retention waveform.	
Operation recovery time	t <sub>R</sub>	5	-	-	ms		

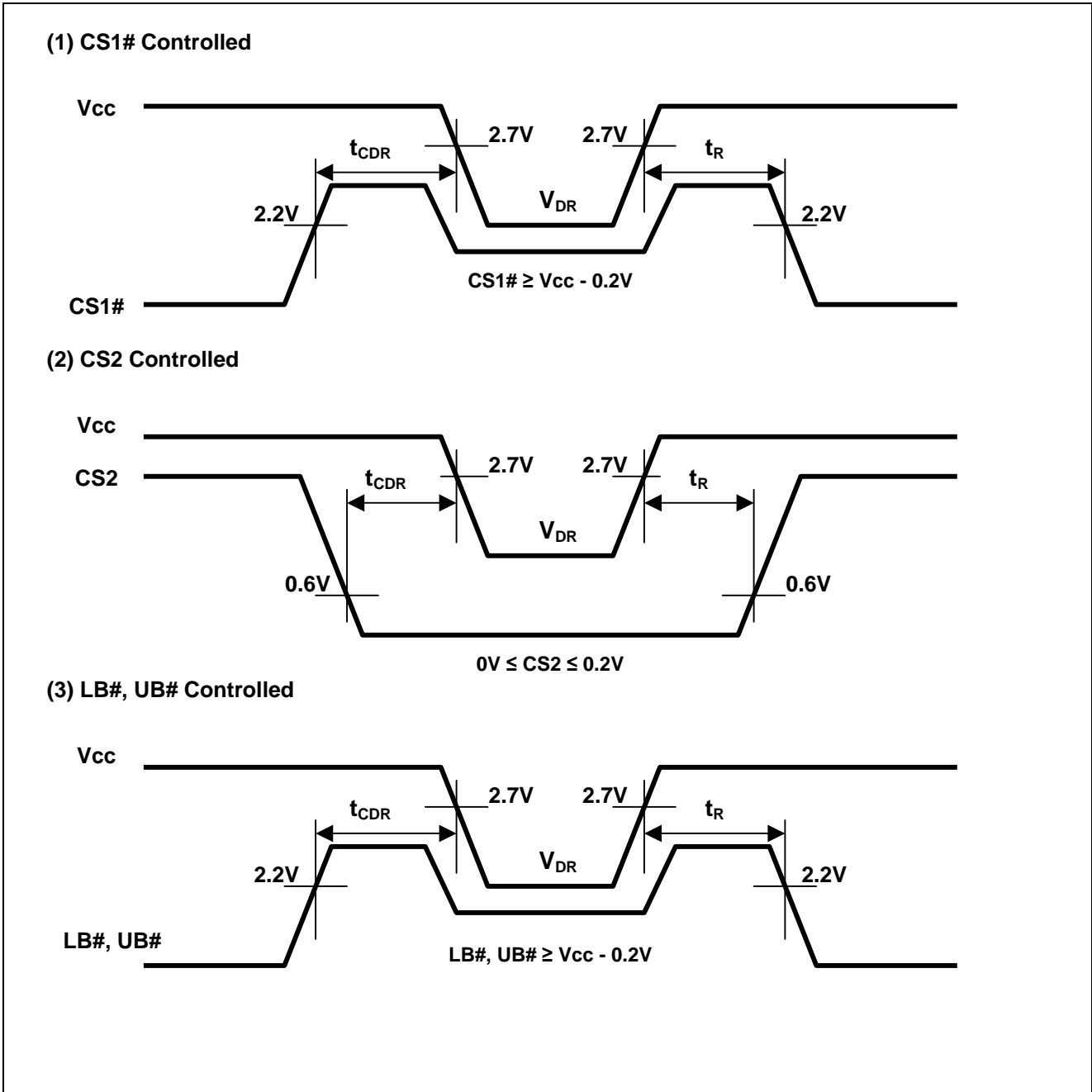
Note 1. Typical parameter indicates the value for the center of distribution at 3.0V (Ta= 25°C), and not 100% tested.

2. Typical parameter indicates the value for the center of distribution at 3.0V (Ta= 40°C), and not 100% tested.

3. BYTE# pin is supported for 48-pin TSOP (I) and 52-pin μTSOP (II) packages.

4. CS2 also controls address buffer, WE# buffer, CS1# buffer, OE# buffer, LB#, UB# buffer and Din buffer. If CS2 controls data retention mode, Vin levels (address, WE#, OE#, CS1#, LB#, UB#, I/O) can be in the high impedance state. If CS1# controls data retention mode, CS2 must be CS2 ≥ V<sub>CC</sub>-0.2V or 0V ≤ CS2 ≤ 0.2V. The other input levels (address, WE#, OE#, CS1#, LB#, UB#, I/O) can be in the high impedance state.

Low Vcc Data Retention Timing Waveforms\*1



Note1. BYTE#  $\geq V_{CC} - 0.2V$  or BYTE#  $\leq 0.2V$



## Revision History

## R1WV6416R Data Sheet

Rev.	Date	Contents of Revision	
		Page	Description
0.01	Mar.24, 2008	-	Initial issue: Preliminary Data Sheet
1.00	May 07, 2009	-	Finalized
		5	Operation Table corrected
		6	Error corrected: $I_{SB}$ Test condition $CS2=V_{IH} \rightarrow V_{IL}$

Notes:

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Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

**Renesas Technology Europe Limited**  
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.  
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

**Renesas Technology (Shanghai) Co., Ltd.**  
Unit 204, 205, AZIACenter, No.1233 Lujiazui Ring Rd, Pudong District, Shanghai, China 200120  
Tel: <86> (21) 5877-1818, Fax: <86> (21) 6887-7858/7898

**Renesas Technology Hong Kong Ltd.**  
7th Floor, North Tower, World Finance Centre, Harbour City, Canton Road, Tsimshatsui, Kowloon, Hong Kong  
Tel: <852> 2265-6688, Fax: <852> 2377-3473

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1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632  
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Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea  
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

**Renesas Technology Malaysia Sdn. Bhd**  
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia  
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On April 1<sup>st</sup>, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: <http://www.renesas.com>

April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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Тел: +7 (812) 336 43 04 (многоканальный)

Email: [org@lifeelectronics.ru](mailto:org@lifeelectronics.ru)