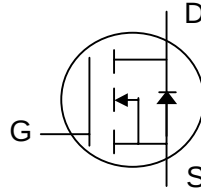


N-channel Enhancement-mode Power MOSFET

Dynamic dv/dt rating
 Repetitive Avalanche Rated
 Fast Switching
 Simple Drive Requirement

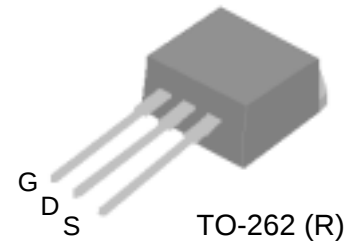
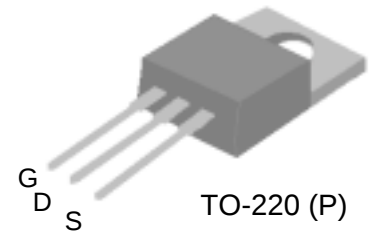


BV_{DSS} 675V
 $R_{DS(ON)}$ 1.2Ω
 I_D 7A

DESCRIPTION

The SSM07N70C series is specially designed as a main switching device for universal 90~265VAC off-line AC/DC converter applications. Both TO-220 and TO-262 type provide high blocking voltage to overcome voltage surge and sag in the toughest power system with the best combination of fast switching, ruggedized design and cost-effectiveness.

The TO-220 and TO-262 packages are widely preferred for all commercial and industrial applications. The device is well suited for switch-mode power supplies, AC-DC converters and high-current high-speed switching circuits.



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	675	V
V_{GS}	Gate-Source Voltage	± 30	V
$I_D @ T_C=25^{\circ}C$	Continuous Drain Current, $V_{GS} @ 10V$	7	A
$I_D @ T_C=100^{\circ}C$	Continuous Drain Current, $V_{GS} @ 10V$	4.4	A
I_{DM}	Pulsed Drain Current ¹	18	A
$P_D @ T_C=25^{\circ}C$	Total Power Dissipation	89	W
	Linear Derating Factor	0.7	W/°C
E_{AS}	Single Pulse Avalanche Energy ²	140	mJ
I_{AR}	Avalanche Current	7	A
E_{AR}	Repetitive Avalanche Energy	7	mJ
T_{STG}	Storage Temperature Range	-55 to 150	°C
T_J	Operating Junction Temperature Range	-55 to 150	°C

THERMAL DATA

Symbol	Parameter	Value	Unit
Rthj-c	Thermal Resistance Junction-case Max.	1.4	°C/W
Rthj-a	Thermal Resistance Junction-ambient Max.	62	°C/W

Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =1mA	675	-	-	V
ΔBV _{DSS} /ΔT _j	Breakdown Voltage Temperature Coefficient	Reference to 25°C, I _D =1mA	-	0.6	-	V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =3.5A	-	-	1.2	Ω
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	2	-	4	V
g _{fs}	Forward Transconductance	V _{DS} =10V, I _D =3.5A	-	4.5	-	S
I _{DSS}	Drain-Source Leakage Current (T _j =25°C)	V _{DS} =675V, V _{GS} =0V	-	-	10	uA
	Drain-Source Leakage Current (T _j =150°C)	V _{DS} =480V, V _{GS} =0V	-	-	100	uA
I _{GSS}	Gate-Source Leakage	V _{GS} = ± 30V	-	-	±100	nA
Q _g	Total Gate Charge ³	I _D =7A	-	32	-	nC
Q _{gs}	Gate-Source Charge	V _{DS} =480V	-	8.6	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge	V _{GS} =10V	-	9	-	nC
t _{d(on)}	Turn-on Delay Time ³	V _{DD} =300V	-	17	-	ns
t _r	Rise Time	I _D =7A	-	15	-	ns
t _{d(off)}	Turn-off Delay Time	R _G =10Ω, V _{GS} =10V	-	35	-	ns
t _f	Fall Time	R _D =43Ω	-	18	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V	-	2075	-	pF
C _{oss}	Output Capacitance	V _{DS} =25V	-	120	-	pF
C _{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	8	-	pF

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I _S	Continuous Source Current (Body Diode)	V _D =V _G =0V , V _S =1.5V	-	-	7	A
I _{SM}	Pulsed Source Current (Body Diode) ¹		-	-	18	A
V _{SD}	Forward On Voltage ³	T _j =25°C, I _S =7A, V _{GS} =0V	-	-	1.5	V

Notes:

- 1.Pulse width limited by safe operating area.
- 2.Starting T_j=25°C , V_{DD}=50V , L=5mH , R_G=25Ω , I_{AS}=7A.
- 3.Pulse width ≤300us , duty cycle ≤2%.

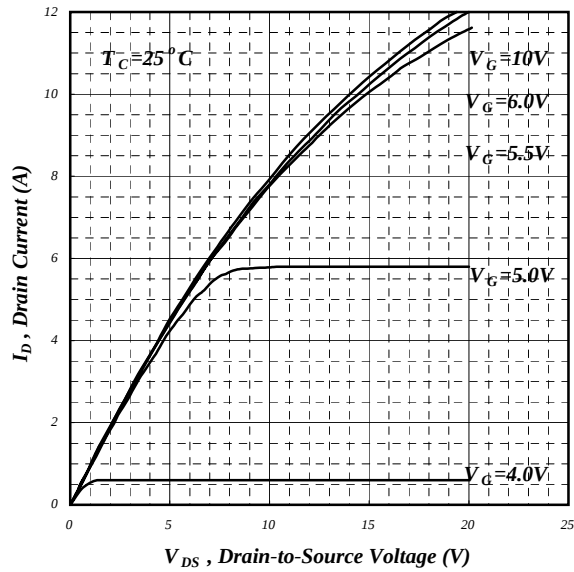


Fig 1. Typical Output Characteristics

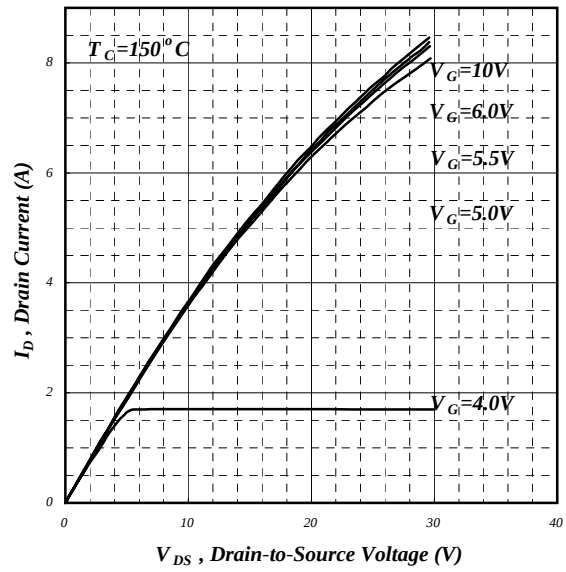


Fig 2. Typical Output Characteristics

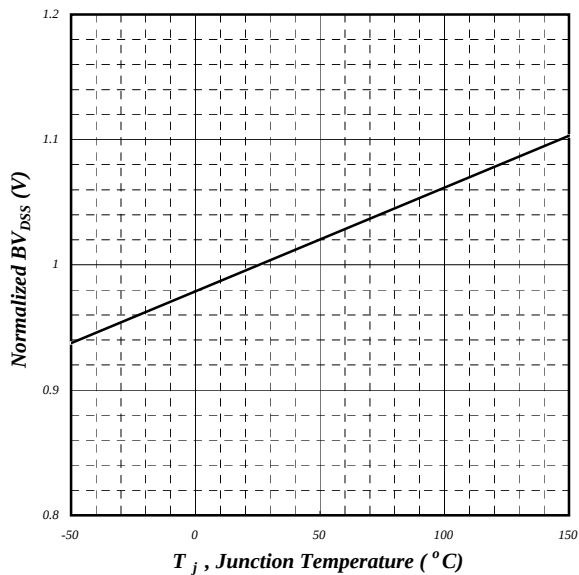


Fig 3. Normalized BV_{DSS} vs. Junction Temperature

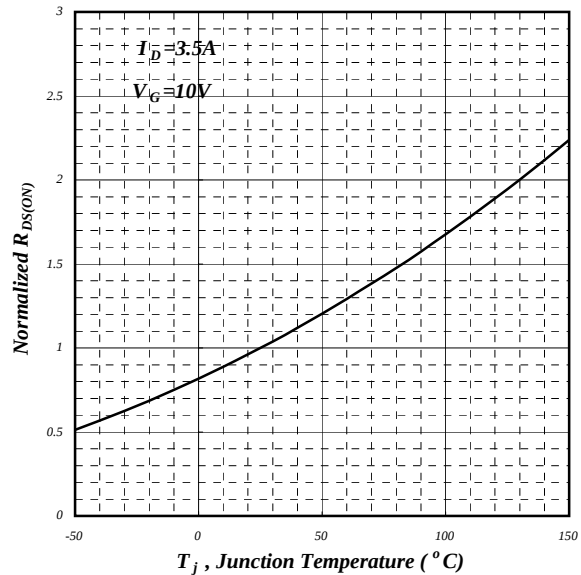


Fig 4. Normalized On-Resistance vs. Junction Temperature

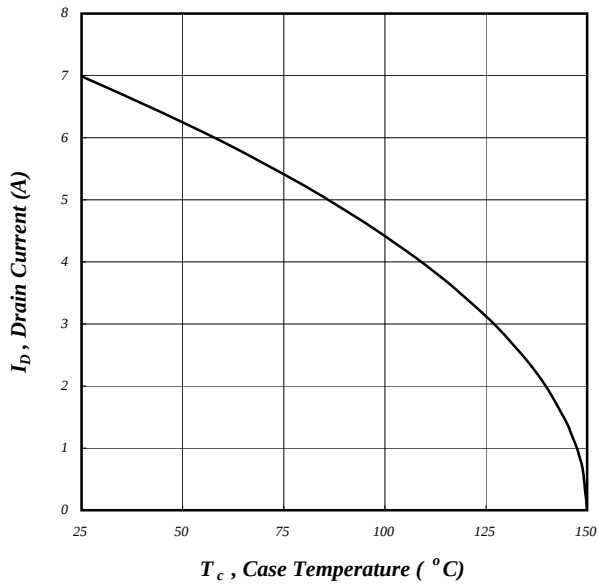


Fig 5. Maximum Drain Current vs. Case Temperature

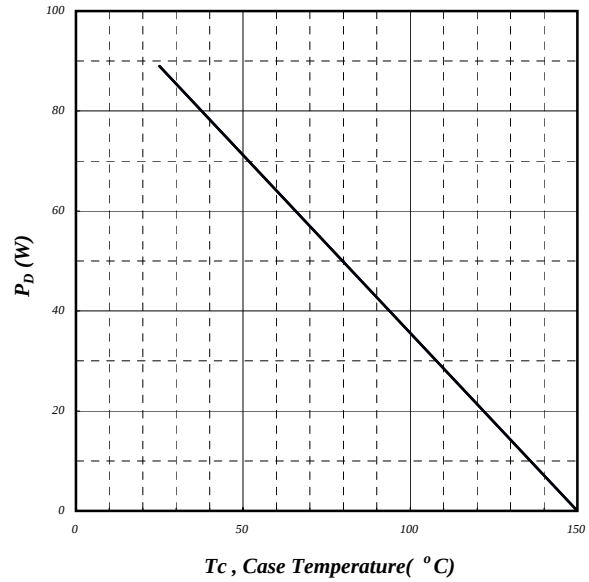


Fig 6. Typical Power Dissipation

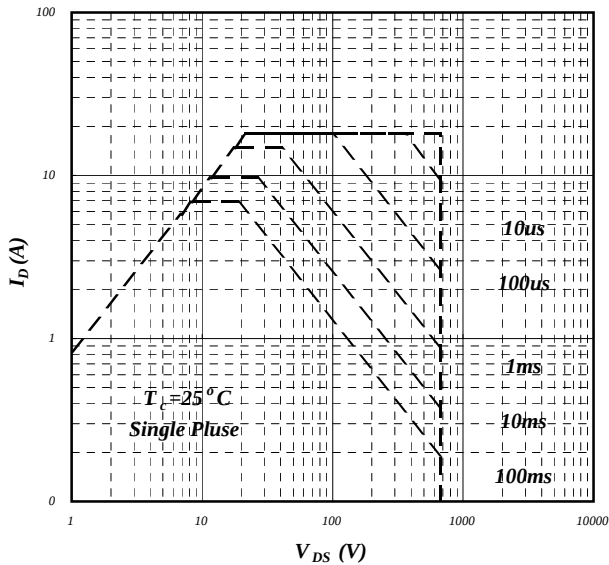


Fig 7. Maximum Safe Operating Area

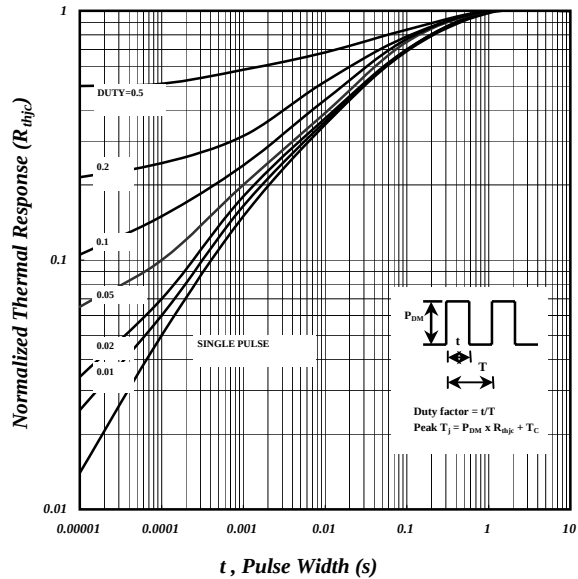


Fig 8. Effective Transient Thermal Impedance

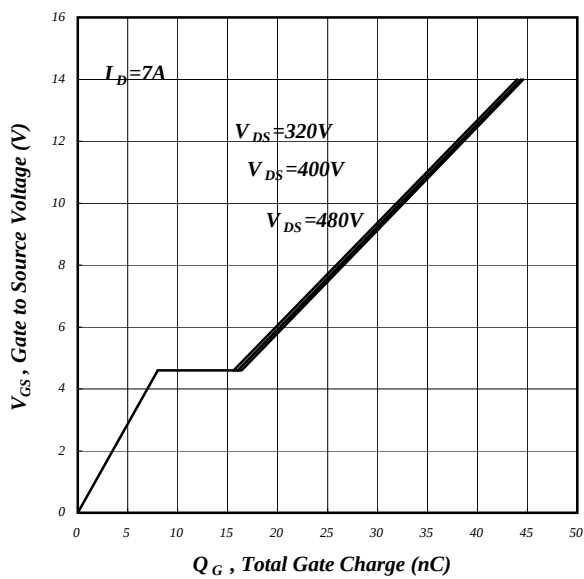


Fig 9. Gate Charge Characteristics

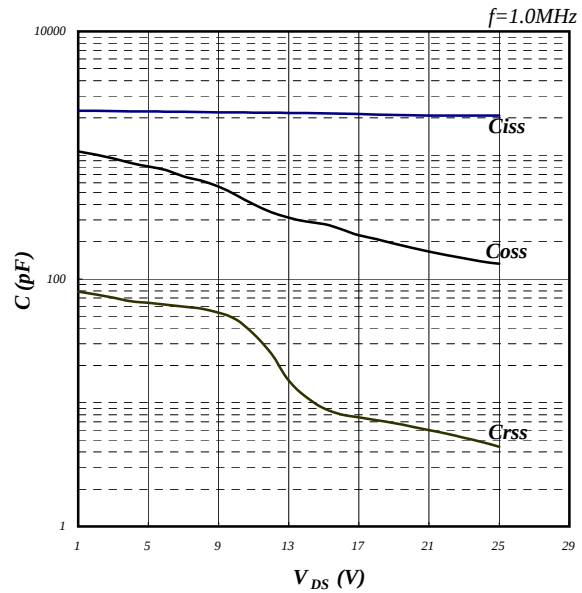


Fig 10. Typical Capacitance Characteristics

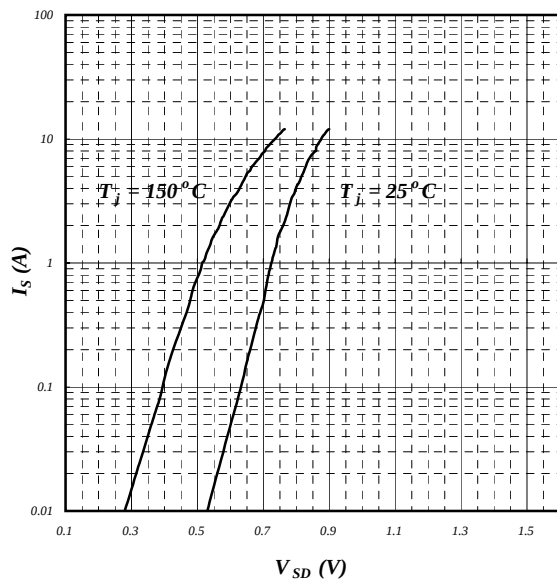


Fig 11. Forward Characteristic of Reverse Diode

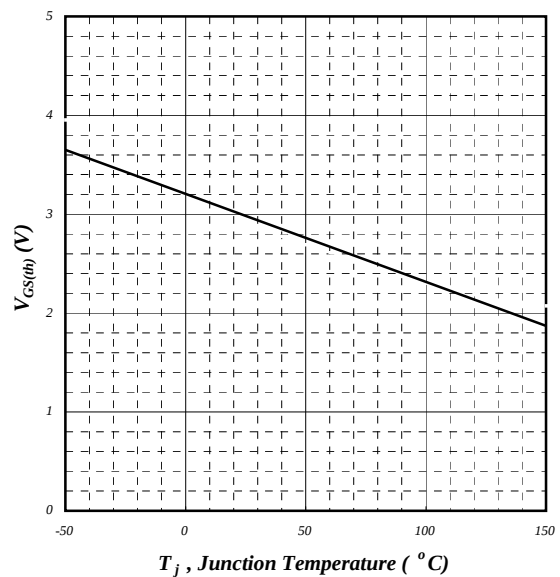


Fig 12. Gate Threshold Voltage vs. Junction Temperature

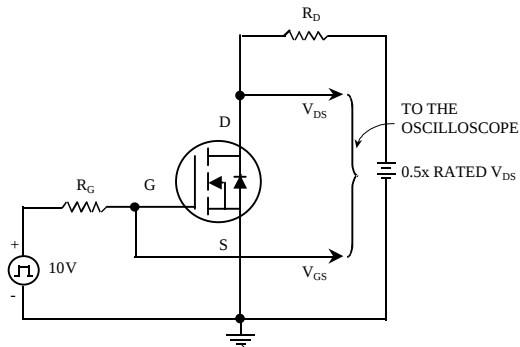


Fig 13. Switching Time Circuit

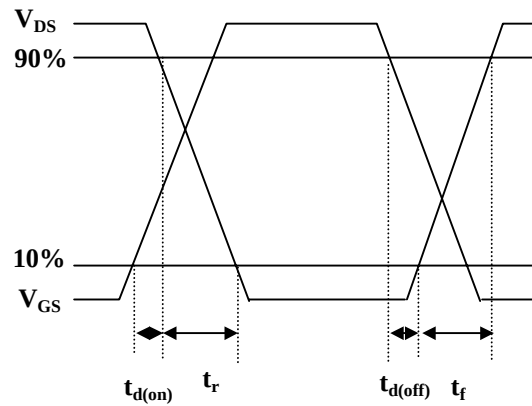


Fig 14. Switching Time Waveform

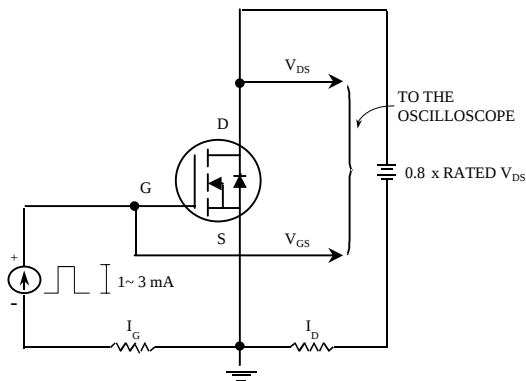


Fig 15. Gate Charge Circuit

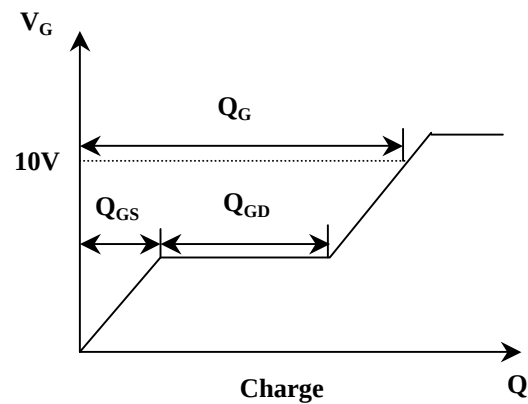


Fig 16. Gate Charge Waveform

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- Техническую поддержку проекта.
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