Power Supply IC Series for TFT-LCD Panels

12V Input Multi-channel System Power Supply IC

BD8166EFV

No.09035EBT14

●Description

The BD8166EFV is a system power supply for the TFT-LCD panels used for liquid crystal TVs.
Incorporates two high-power FETs with low on resistance for large currents that employ high-power packages, thus driving large current loads while suppressing the generation of heat. A charge pump controller is incorporated as well, thus greatly reducing the number of application components.

●Features

1) Step-up and step-down DC/DC converter
2) Incorporates 2-A N-channel FET.
3) Incorporates positive/negative charge pumps.
4) Incorporates a gate shading function.
5) Input voltage limit: 6 V to 18 V
6) Feedback voltage: 1.25 V ± 1.6%
7) Switching frequency: 500 kHz
8) Protection circuit: Undervoltage lockout protection circuit
   Thermal shutdown circuit
   Overcurrent protection circuit
   Short protection circuit of timer latch type
9) HTSSOP-B40 Package

●Applications

Power supply for the TFT-LCD panels used for LCD TVs

●Absolute maximum ratings (Ta = 25℃)

Parameter	Symbol	Limit	Unit
Power supply voltage	Vcc, PVCC	19	V
Vo1 voltage	Vo1	19	V
Vo2 voltage	Vo2	40	V
IG Voltage	IGH	7	V
Maximum junction temperature	Tjmax	150	℃
Power dissipation	Pd	4700*1	mW
Operating temperature range	Topr	-40 to 85	℃
Storage temperature range	Tstg	-55 to 150	℃

* Reduced by 37.6 mW/℃ over 25℃, when mounted on a glass epoxy 4-layer board (70 mm × 70 mm × 1.6 mm)
(Copper foil on back 70 mm × 70 mm).

●Recommended Operating Ranges (Ta = 25℃)

Parameter	Symbol	Limit		Unit
		Min.	Max.	
Power supply voltage	VCC, PVCC	6	18	V
Vo1 voltage	Vo1	8	18	V
Vo2 voltage	Vo2	—	39	V
I G Voltage	IGH	—	5	V
SW current	SW1, SW2	—	2	A

●**Electrical characteristics (Unless otherwise specified, Ta = 25°C, VCC = 15 V, Ta = 25℃)**

1. DC/DC Converter Block

Parameter	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
[Soft start block SS1 and SS2]						
SS source current	I_{SO}	6	10	14	μA	Vss = 1.0 V
SS sinking current	I_{SI}	0.5	2	—	mA	Vss = 1.0 V
Clamp voltage	Vcl	1.7	1.9	2.1	V	
[Error amp block FB1 and FB2]						
FB input bias current 1 and 2	$I_{FB1, 2}$	—	0.4	1.5	μA	VFB = 0.5 V
Feedback voltage 1 and 2	$V_{FB1, 2}$	1.230	1.250	1.270	V	Buffer
Voltage gain	A V	—	200	—	V/V	
COMP sinking current	Iol	1	2	4	mA	V_{FB} = 1.5 V, COMP = 1.5 V
COMP source current	Ioo	-12	-6	-2	mA	V_{FB} = 1.0 V COMP = 1.0 V
[Switch output block SW1 and SW2]						
On resistance on high side	$R_{on\ h}$	—	200	300	mΩ	Io = 1A*
On resistance on low side	$R_{on\ l}$	—	2	3	Ω	Io = 20 mA*
Off current	Ioff	—	0.2	—	mA	
Current limit	Insw	2	—	—	A	*
Maximum duty ratio	DMax	—	97	—	%	

2. Positive/Negative Charge Pump Block

Parameter	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
[Error amp block FB3 and FB4]						
Input bias current 3	I_{FB3}	—	0.1	0.5	μA	
Input bias current 4	I_{FB4}	—	0.1	0.5	μA	
Feedback voltage 3	V_{FB3}	1.18	1.25	1.32	V	
Feedback voltage 4	V_{FB4}	1.18	1.25	1.32	V	
[Delay start block SS3 and SS4]						
SS source current	I_{DSO}	3	5	7	μA	V_{DLS} = 0.5 V
SS sinking current	I_{DSI}	0.2	0.5	—	mA	V_{DLS} = 0.5 V
Startup voltage	V_{ST}	0.52	0.65	0.78	V	
[Switch block C1L, C2L, and C3]						
N-channel on resistance	R_{ON_NC}	—	4	8	Ω	Io = 20 mA*
P-channel on resistance	R_{ON_PC}	—	4	8	Ω	Io = 20 mA*

○Design guarantee (No total shipment inspection is made.)
*This product is not designed for protection against radio active rays.

●**Electrical characteristics (Unless otherwise specified, Ta = 25℃, VCC = 15 V, Ta = 25℃)**

3. Gate Shading Block

Parameter	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
[Output block Vo2GS and GSOUT]						
N-channel on resistance	Ron_NGS	—	10	15	Ω	Io = 20 mA*
P-channel on resistance	Ron_PGS	—	55	80	Ω	Io = 20 mA*
N-channel leak current	ILEAK_NGS	—	—	10	μA	
P-channel leak current	ILEAK_PGS	—	—	10	μA	
[Input block IG]						
IGH voltage	IGH	1.9	2.9	5	V	
IGL voltage	LGL	—	0	0.9	V	
IG sinking current	IIG	8	16.5	25	μA	IG = 3.3 V

4. Overall

Parameter	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
[Reference voltage block VREF]						
Reference voltage	VREF	2.84	2.90	2.96	V	
Load stability	ΔV	—	5	20	mV	IREF = 1 mA
[Regulator circuit block VREG]						
REG output voltage	VREG	4.5	5.0	5.5	V	
Load stability	ΔV	—	50	100	mV	IREG = 10 mA
[Oscillator block]						
Frequency	Fosc	400	500	600	kHz	
[Protection detection block FAULT]						
Off-leak current	IFL	—	—	10	μA	
On resistance	Ron_FL	—	1	—	kΩ	
[Short protection block SCP]						
SCP lease current	Iscp	6	10	14	μA	
Threshold voltage	Vth_scp	0.96	1.2	1.44	V	
Off sinking current	IOFFS	1	3	—	mA	SCP = 0.5 V
[VCOM block]						
Input offset voltage	Voso	-10	0	10	mV	
Input bias current	Ibo	—	0.1	1	μA	
Drive current	Ioo	50	100	350	mA	
Slew rate	SRo	5	12	—	V/MS	
GB product	GBW	—	12	—	MHz	
High output voltage	Voho	Vol-0.3	Vol-0.1	—	V	Io = -5 mA
Low output voltage	Vohl	—	0.1	0.3	V	Io = 5 mA
[Low voltage protection circuit]						
Detection voltage	VUVLO	4.8	5.1	5.4	V	
[Overall]						
Average current consumption	Icc	3.0	4.5	6.0	mA	Standby current

○Design guarantee (No total shipment inspection is made.)
*This product is not designed for protection against radio active rays.

●**Reference Data (Unless otherwise specified, Ta = 25℃)**

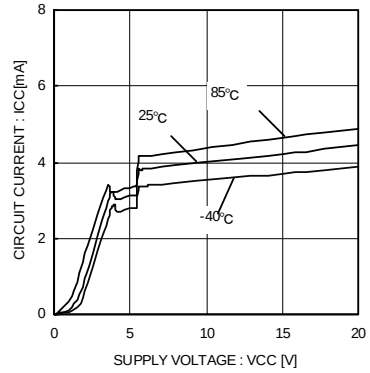


Fig.1 Standby Circuit Current 1

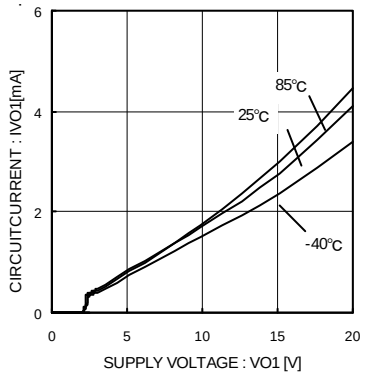


Fig.2 Standby Circuit Current 2

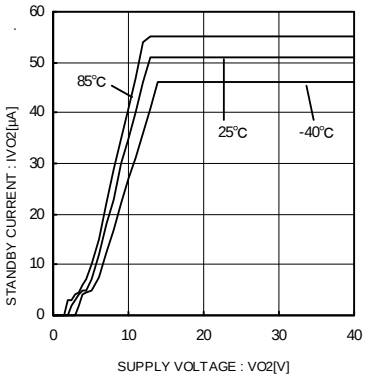


Fig.3 Standby Circuit Current 3

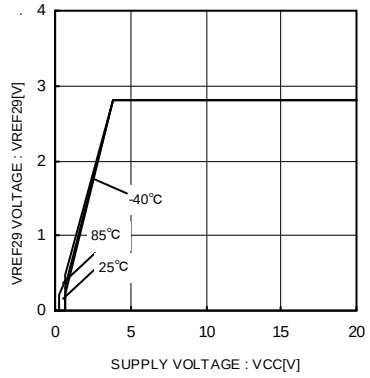


Fig.4 Internal Reference Line Regulation

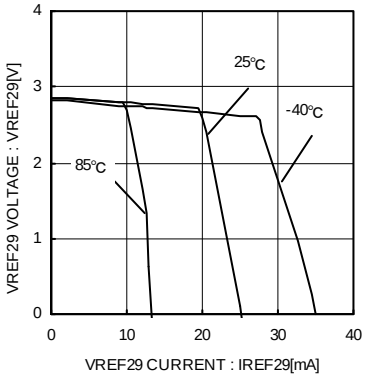


Fig.5 Internal Reference Load Regulation

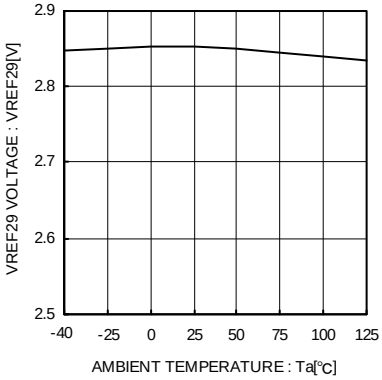


Fig.6 Internal Reference vs Temperature

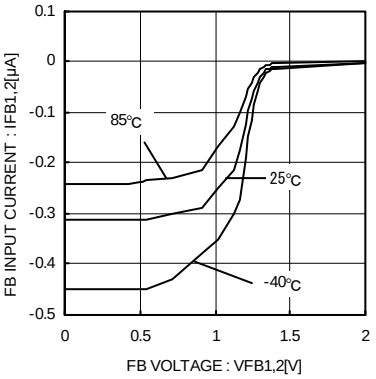


Fig.7 DC/DC Error Amp Input Bias Current

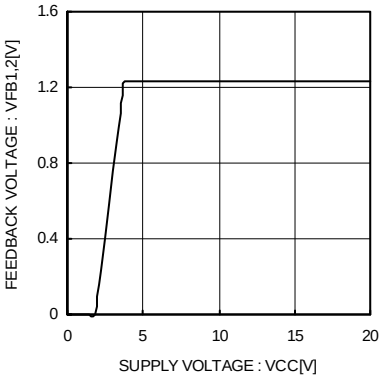


Fig.8 DC/DC Error Amp Feedback Voltage

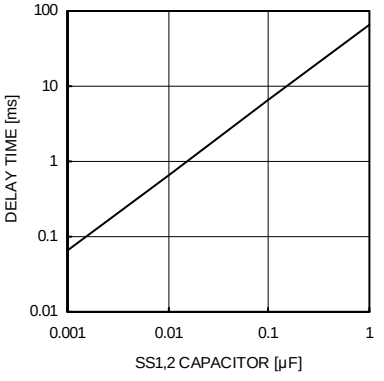


Fig.9 Soft Start Capacity vs Delay Time

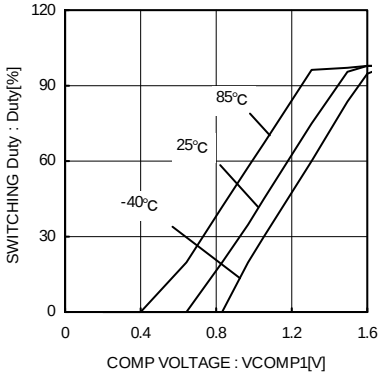


Fig.10 Error Output Voltage vs Duty

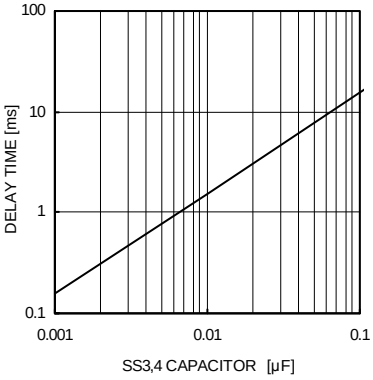


Fig.11 Delay Start Capacity vs Delay Time

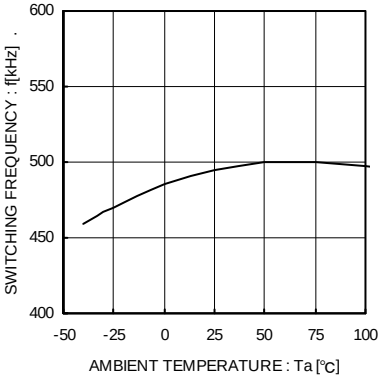


Fig.12 Switching Frequency vs Temperature

●Reference Data (Unless otherwise specified, Ta = 25℃)

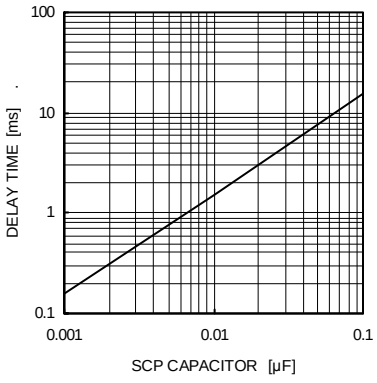


Fig.13 SCP Capacity vs Delay Time

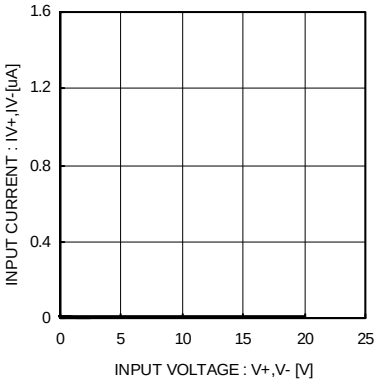


Fig.14 COM Input Bias Current

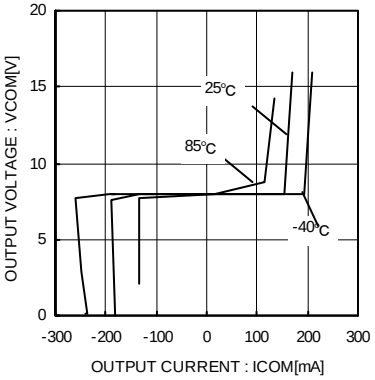


Fig.15 COM Load Regulation

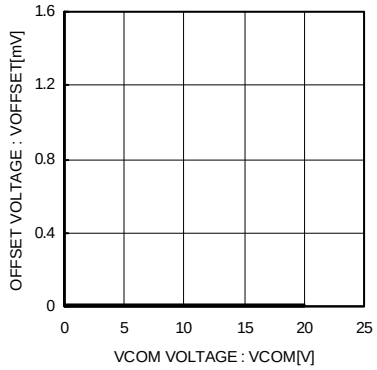


Fig.16 VCOM Offset Voltage

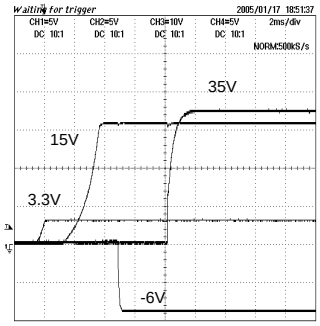


Fig.17 Start-up Sequence

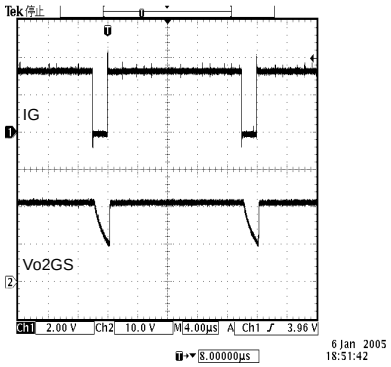


Fig.18 Gate-shading Waveform

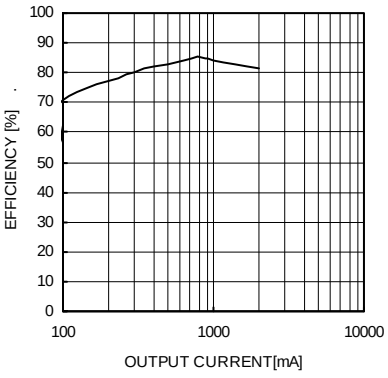


Fig.19 Output Current vs Efficiency (Vo1)

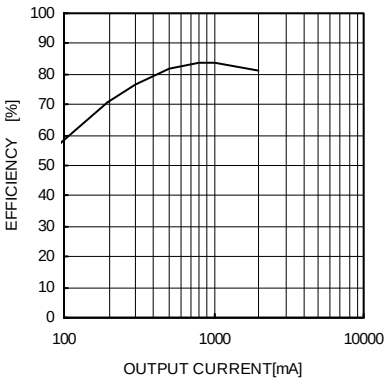


Fig.20 Output Current vs Efficiency (VDD)

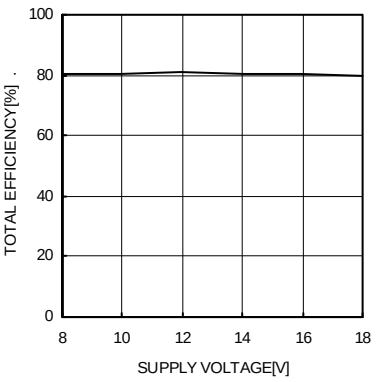


Fig.21 Total Efficiency

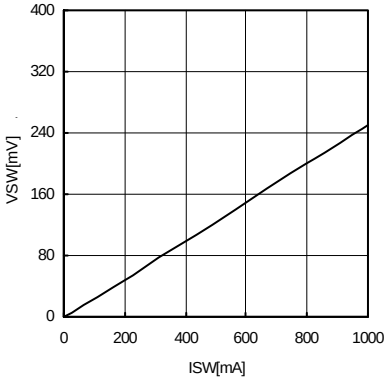


Fig.22 DC/DC SW On Resistance

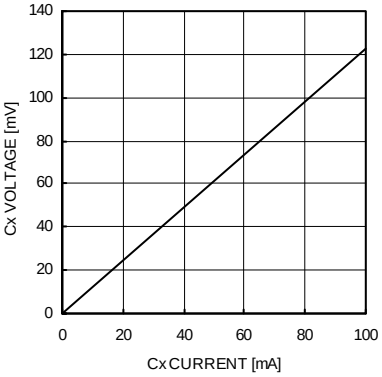


Fig.23 Charge Pump N-channel On Resistance

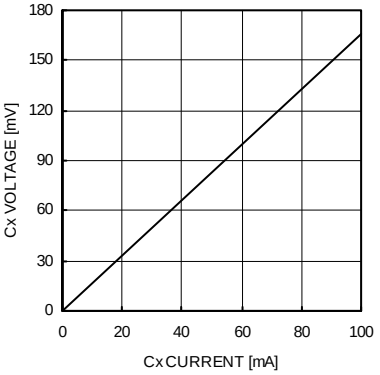
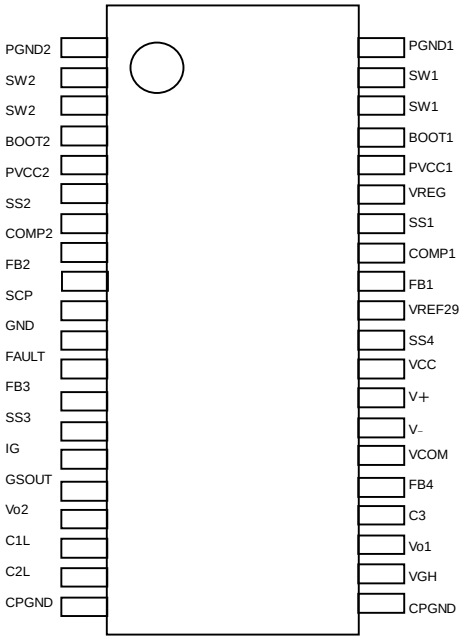


Fig.24 Charge Pump P-channel On Resistance

●Pin Assignment Diagram



●Block Diagram

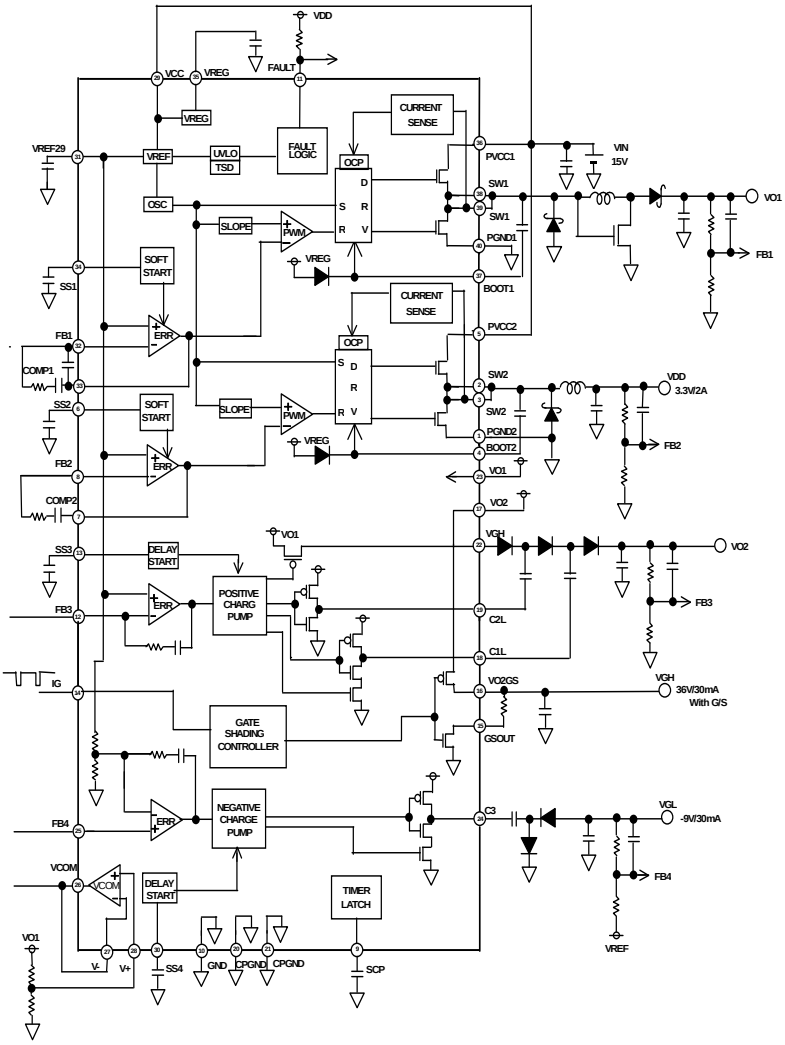


Fig. 25 Pin Assignment Diagram & Block Diagram

●Pin Assignment and Pin Function

Pin No.	Pin name	Function	Pin No.	Pin name	Function
1	PGND2	Ground pin	21	CPGND	Ground pin
2	SW2	Switching pin 2	22	VGH	Positive charge pump diode connection pin
3	SW2	Switching pin 2	23	Vo1	Power supply input pin
4	BOOT2	Capacitance connection pin for booting 2	24	C3	Charge pump clock output 3
5	PVCC2	Power supply input pin	25	FB4	Feedback input 3
6	SS2	Soft start capacitance connection pin 2	26	VCOM	VCOM output
7	COMP2	Error amp output 2	27	V-	VCOM negative input pin
8	FB2	Feedback input 2	28	V+	VCOM positive input pin
9	SCP	Capacitance connection pin for short protection delay	29	VCC	Power supply input pin
10	GND	Ground pin	30	SS4	Delay start capacitance connection pin 4
11	FAULT	Protection detection output pin	31	VREF29	Standard voltage output pin
12	FB3	Feedback input 3	32	FB1	Feedback input 1
13	SS3	Delay start capacitance connection pin 3	33	COMP1	Error amp output 1
14	IG	Gate shading input pin	34	SS1	Soft start capacitance connection pin 1
15	GSOUT	Gate shading sink output pin	35	VREG	Regulator output pin for booting
16	Vo2GS	Gate shading source output pin	36	PVCC1	Power supply input pin
17	Vo2	Power supply input pin	37	BOOT1	Capacitance connection pin for booting 1
18	C1L	Charge pump clock output 1	38	SW1	Switching pin 1
19	C2L	Charge pump clock output 2	39	SW1	Switching pin 1
20	CPGND	Ground pin	40	PGND1	Ground pin

●Block Operation

- VREG
  A block to generate constant-voltage for DC/DC boosting.

- VREF
  A block that generates internal reference voltage of 2.9 V (Typ.).

- TSD/UVLO
  TSD (Thermal shutdown)/UVLO (Under Voltage Lockout) protection block. The TSD circuit shuts down IC at 175°C (Typ.) and recovers at 160°C (Typ.). The UVLO circuit shuts down the IC when the Vcc is 5.1 V (Typ.) or below.

- Error amp block (ERR)
  This is the circuit to compare the reference voltage of 1.25 V (Typ.) and the feedback voltage of output voltage. The COMP pin voltage resulting from this comparison determines the switching duty. At the time of startup, since the soft start is operated by the SS pin voltage, the COMP pin voltage is limited to the SS pin voltage.

- Oscillator block (OSC)
  This block generates the oscillating frequency.

- SLOPE block
  This block generates the triangular waveform from the clock created by OSC. Generated triangular waveform is sent to the PWM comparator.

- PWM block
  The COMP pin voltage output by the error amp is compared to the SLOPE block's triangular waveform to determine the switching duty. Since the switching duty is limited by the maximum duty ratio which is determined internally, it does not become 100%.

- DRV block
  A DC/DC driver block. A signal from the PWM is input to drive the power FETs.

- CURRENT SENSE
  Current flowing to the power FET is detected by voltage at the CURRENT SENSE and the overcurrent protection operates at 3A (Typ.). When the overcurrent protection operates, switching is turned OFF and the SS pin capacitance is discharged.

- DELAY START
  A start delay circuit for positive/negative charge pump.

- Soft start circuit
  Since the output voltage rises gradually while restricting the current at the time of startup, it is possible to prevent the output voltage overshoot or the rush current.

- Positive charge pump
  A controller circuit for the positive-side charge pump. The switching amplitude is controlled so that the feedback voltage FB2 will be set to 1.25 V (Typ.).
  The start delay time can be set in the DLS pin at the time of startup. When the DLS voltage reaches 0.65 V (Typ.), switching waves will be output from the CL1 and CL2 pins.

- Negative charge pump
  A controller circuit for the negative-side charge pump. The switching amplitude is controlled so that the feedback voltage FB3 will be set to 1.25 V (Typ.).

- Gate shading controller
  A controller circuit of gate shading. The Vo2GS and GSOUT are turned on and off according to IG pin input.

- VCOM
  A common amplifier to set output voltage in a range of 0.3 V to Vo1-0.3 V.

- Timer latch
  An output short protection circuit. If at least one output is down after the DC/DC2 and positive/negative charge pump outputs all rise, all the outputs will be shut down.

●Start-up Sequence

The DC/DC converter of this IC incorporates a soft start function, and the charge pump incorporates a delay function, for which independent time settings are possible through external capacitors. As the capacitance, 0.001 µF to 0.1 µF is recommended. If the capacitance is set lower than 0.001 µF, the overshooting may occur on the output voltage. If the capacitance is set larger than 0.1 µF, the excessive back current flow may occur in the internal parasitic elements when the power is turned OFF and it may damage IC. When the capacitor more than 0.1 µF is used, be sure to insert a diode to VCC in series, or a bypass diode between the SS and VCC pins.

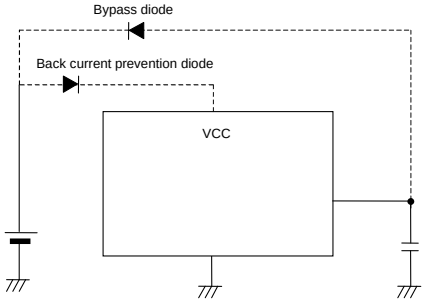


Fig.26 Example of Bypass Diode Use

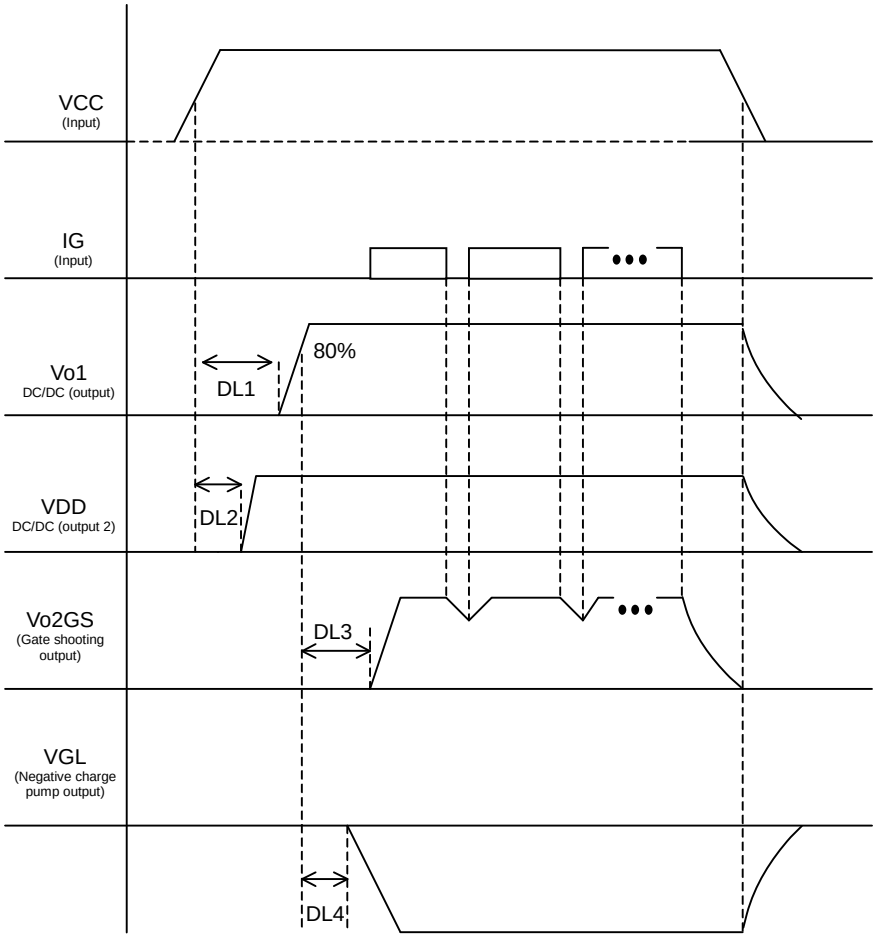
When there is the activation relation (sequences) with other power supplies, be sure to use the high-precision product (such as X5R). Soft start time may vary according to the input voltage, output loads, coils, voltage, and output capacitance. Be sure to verify the operation using the actual product.

A delay of the charge pump starts from a point where Vo1 reaches 80% (Typ.).

Soft start time of DC/DC converter block: tss
Tss = (Css × 0.7 V) / 10 µA [s]
Where, Css is an external capacitor.

Delay time of charge pump block: t DELAY
t DELAY = (Css × 0.65) / 5 µA [s]
Where, Css is an external capacitor.

Startup example



DL1 = SS1 capacitance delay time
DL2 = SS2 capaciance delay time
DL3 = SS3 capacitance delay time
DL4 = SS4 capacitance delay time

Fig. 27

●Selecting Application Components

(1) Output LC constant

The inductance L to use for output is decided by the rated current I_{LR} and input current maximum value I_{OMAX} of the inductance.

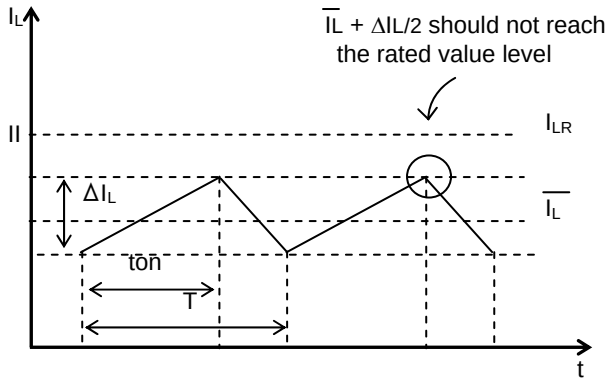


Fig. 28

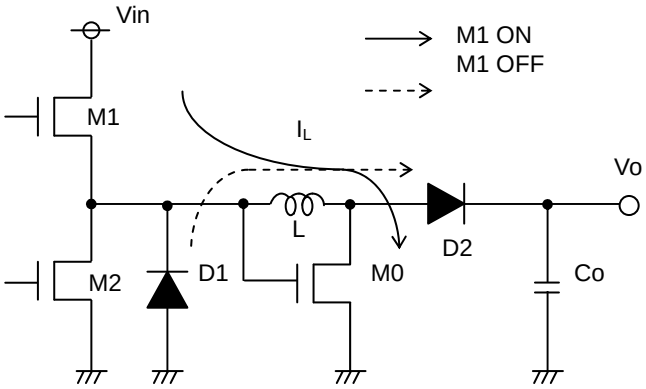


Fig.29

Adjust so that $I_L + \Delta\overline{I_L}/2$ does not reach the rated current value I_{LR}. At this time, $\overline{I_L}$ and ΔI_L can be obtained by the following equation.

$$\overline{I_L} = \left(1 + \frac{Vo}{Vin}\right) Io \times \frac{1}{\eta} \quad [A] \qquad (\eta\text{:efficiency})$$

$$\Delta I_L = \frac{1}{L}\{Vin \times Vo / (Vin + Vo)\} \times \frac{1}{f} \quad [A]$$

Set with sufficient margin because the inductance L value may have the dispersion of ± 30%.

For the capacitor C to use for the output, select the capacitor which has the larger value in the ripple voltage V_{PP} permissible value and the drop voltage permissible value at the time of sudden load change.

Output ripple voltage is decided by the following equation.

$$\Delta V_{PP} = \left(\overline{IL} \frac{\Delta I_L}{2}\right) R_{ESR} + \frac{Io}{Co} (Vin / (Vin + Vo)) \times \frac{1}{f}$$

Perform setting so that the voltage is within the permissible ripple voltage range.
For the drop voltage V_{DR} during sudden load change, please perform the rough calculation by the following equation.

$$VDR = \frac{\Delta I}{Co} \times 10\mu \text{ sec} \quad [V]$$

However, 10 µs is the rough calculation value of the DC/DC response speed.
Make Co settings so that these two values will be within the limit values.

(2) Output LC constant

The inductance L to use for output is decided by the rated current I_{LR} and input current maximum value I_{OMAX} of the inductance.

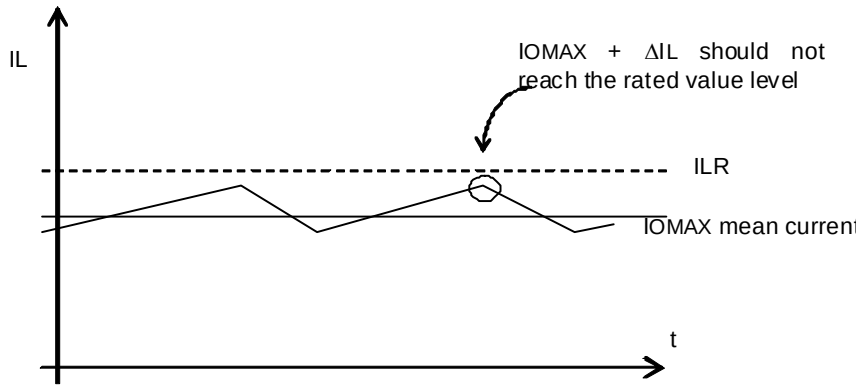


Fig. 28

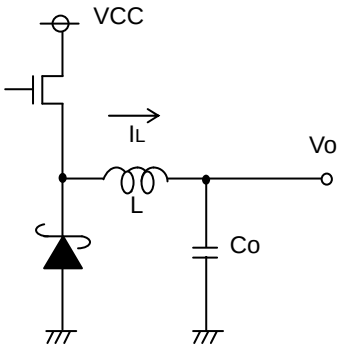


Fig. 29

Adjust so that $I_{OMAX} + \Delta I_L$ does not reach the rated current value I_{LR}. At this time, ΔI_L can be obtained by the following equation.

$$\Delta I_L = \frac{1}{L} \times (Vcc - Vo) \times \frac{Vo}{Vcc} \times \frac{1}{f} \quad [A]$$

Set with sufficient margin because the inductance L value may have the dispersion of ± 30%.

For the capacitor C to use for the output, select the capacitor which has the larger value in the ripple voltage V_{PP} permissible value and the drop voltage permissible value at the time of sudden load change.

Output ripple voltage is decided by the following equation.

$$\Delta V_{PP} = \Delta I_L \times R_{ESR} + \frac{\Delta I_L}{2Co} \times \frac{Vo}{Vcc} \times \frac{1}{f} \quad [V]$$

Perform setting so that the voltage is within the permissible ripple voltage range.
For the drop voltage V_{DR} during sudden load change, please perform the rough calculation by the following equation.

$$VDR = \frac{\Delta I}{Co} \times 10\ \mu s \quad [V]$$

However, 10 µs is the rough calculation value of the DC/DC response speed.
Make Co settings so that these two values will be within the limit values.

(3) Phase compensation

Phase Setting Method

The following conditions are required in order to ensure the stability of the negative feedback circuit.

- Phase lag should be 150° or lower during gain 1 (0 dB) (phase margin of 30° or higher).

Because DC/DC converter applications are sampled using the switching frequency, the overall GBW should be set to 1/10 the switching frequency or lower. The target application characteristics can be summarized as follows:

- Phase lag should be 150° or lower during gain 1 (0 dB) (phase margin of 30° or higher).
- The GBW at that time (i.e., the frequency of a 0-dB gain) is 1/10 of the switching frequency or below.

In other words, because the response is determined by the GBW limitation, it is necessary to use higher switching frequencies to raise response.

One way to maintain stability through phase compensation involves canceling the secondary phase lag (-180°) caused by LC resonance with a secondary phase advance (by inserting 2 phase advances).
The GBW (i.e., the frequency with the gain set to 1) is determined by the phase compensation capacitance connected to the error amp. Increase the capacitance if a GBW reduction is required.

(a) Standard integrator (low-pass filter)

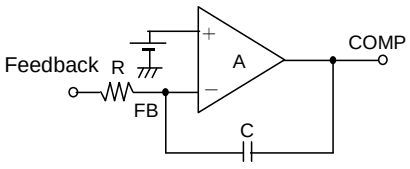


Fig. 30

(b) Open loop characteristics of integrator

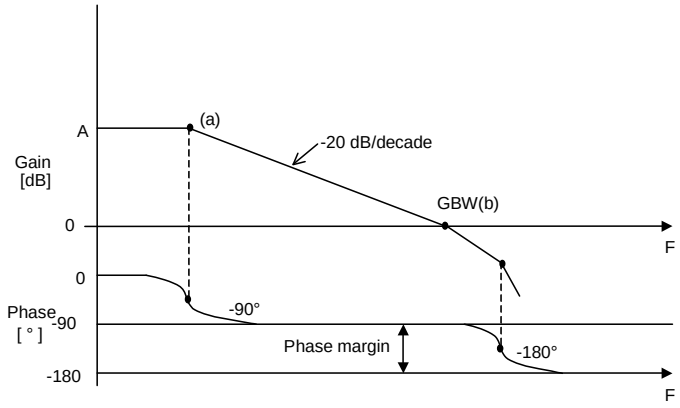
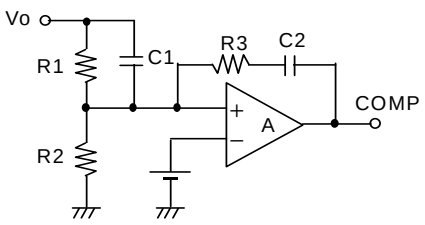


Fig. 31

Point (a) $fa = \frac{1}{2\pi RCA}$ [Hz]

Point (b) $fb = GBW = \frac{1}{2\pi RC}$ [Hz]

The error amp performs phase compensation of types (a) and (b), making it act as a low-pass filter.
For DC/DC converter applications, R refers to feedback resistors connected in parallel.
From the LC resonance of output, the number of phase advances to be inserted is two.



LC resonant frequency $fp = \frac{1}{2\pi\sqrt{LC}}$ [Hz]

Phase advance $fz1 = \frac{1}{2\pi C_1 R_1}$ [Hz]

Phase advance $fz2 = \frac{1}{2\pi C_2 R_3}$ [Hz]

Fig. 32

Set a phase advancing frequency close to the LC resonant frequency for the purpose of canceling the LC resonance.

(4) Short protection of timer latch type

If the overcurrent protection function operates after all the outputs are stable, all the outputs will be shut down by the latch function.

The latch timing is determined by the capacitance connected to the SCP pin. As the capacitance, 0.001 µF to 0.1 µF is recommended. A startup failure may result if the capacitance is 0.001 µF or below. The internal elements may be damaged because an overcurrent state will continue if the capacitance is 1 µF or above.

- t scp = (Cscp × 0.6 V) / 5 µA [s]
- Where, Css is an external capacitor.

(5) Fault function

This IC incorporates a fault function to tell the operating situation of the protection circuit.

If the protection circuit turns on, the fault pin will be pulled up by external pull-up resistance, and high-level voltage will be output.

In a stable operation state, the output will be low-level voltage. As the resistance value, 10 kΩ to 220 kΩ is recommended. Offset voltage due to the internal on resistance will be generated if the resistance is set to 10 Ω or below. In that case, no low-level voltage may be output correctly. No high-level voltage may be output correctly if the resistance is 220 kΩ or over by leak current.

The following conditions will set the fault pin to high level.

- If UVLO operates
- If TSD operates
- If OCP operates
- If SCP operates

(6) Common amp

VCOM operates in a range between 0.3 V and V01-0.3 V. Usually, use the buffer type shown in (a).

To improve the current drive capability, use PNP and NPN transistors as shown in (b).

Use the buffer type specified in (a) if the VCOM is not used, and ground the V+ pin. A resistance setting range of 10 kΩ to 100 kΩ is recommended for R3 and R4. If the resistance is set to 10 kΩ or below, the current consumption will increase and the efficiency of power will be degraded. If the resistance is 100 kΩ or above, the input bias current will be 0.1 µA (Typ.) and the offset voltage may become great.

(a)

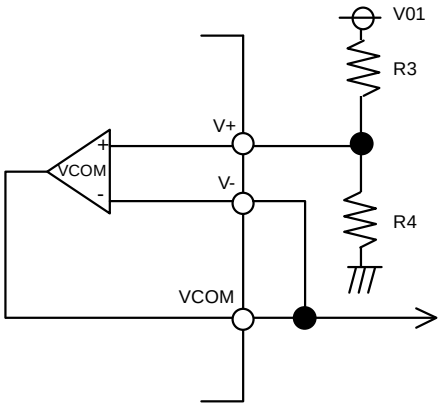


Fig. 33

(b)

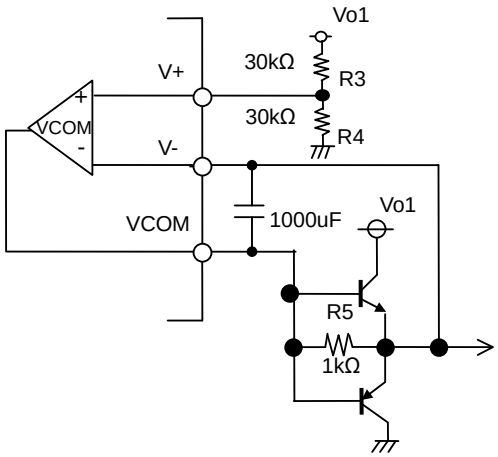
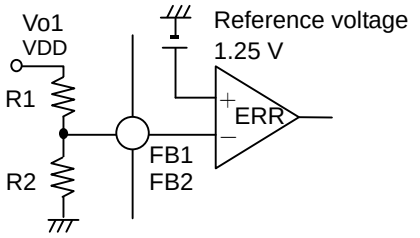


Fig. 34

$$VCOM = \frac{R4}{R3 + R4} \times Vo1\ [V]$$ The recommended R5 value is approximately 1 kΩ.

(7) Design of Feedback Resistance constant

Set the feedback resistance as shown below.

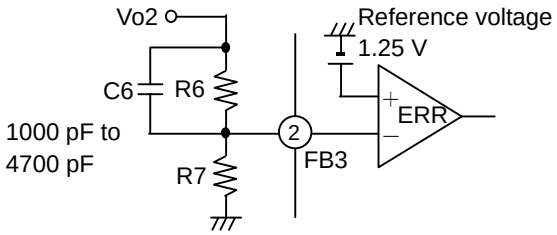


$$Vo1, V_{DD} = \frac{R1 + R2}{R2} \times 1.25 \quad [V]$$

Fig. 35

(8) Positive-side Charge Pump Settings

The IC incorporates a charge pump controller, thus making it possible to generate stable gate voltage.
The output voltage is determined by the following equation. As the setting range, 10 kΩ to 330 kΩ is recommended. If the resistor is set lower than 10 kΩ, it causes reduction of power efficiency. If it is set more than 330 kΩ, the offset voltage becomes larger by the input bias current of 0.4 μA (Typ.) in the internal error amp.



$$Vo2 = \frac{R6 + R7}{R7} \times 1.25 \quad [V]$$

Fig. 36

In order to prevent output voltage overshooting, insert capacitor C6 in parallel with R6.
As the capacitance, 1,000 pF to 4,700 pF is recommended. If the capacitance is not within the range, output voltage oscillation may result. By connecting capacitance to the SS3 pin, the rising delay time can be set for the positive-side charge pump output. The delay time is determined by the following equation. If a capacitance outside this range is inserted, output voltage oscillation may result.

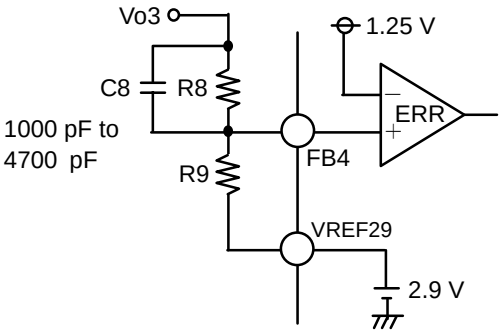
- Delay time of charge pump block t_{DELAY}

  $t_{DELAY} = (C_{DLS} \times 0.65) / 5\ \mu A$ [s]

  Where, C_{DLS} is an external capacitor.

(9) Negative-side Charge Pump Settings

BD8166EFV incorporates a charge pump controller for negative voltage, thus making it possible to generate stable gate voltage.
The output voltage is determined by the following equation. As the setting range, 10 kΩ to 330 kΩ is recommended.
If the resistor is set lower than 10 kΩ, it causes reduction of power efficiency. If it is set more than 330kΩ, the offset voltage becomes larger by the input bias current of 0.4 μA (Typ.) in the internal error amp.



$$Vo3 = -\frac{R8}{R9} \times 1.65 + 1.25\ V \quad [V]$$

Fig.37

Like the positive-side charge pump, the rise delay time can be set by connecting capacitance to the SS4 pin.
In order to prevent output voltage overshooting, insert capacitor C6 in parallel with R6. As the capacitance, 1,000 pF to 4,700 pF is recommended. If a capacitor outside this range is inserted, the output voltage may oscillate.

●Gate Shading Setting Method

The IG input signal allows the high-level and low-level control of the positive-side gate voltage. The slope of output can be set by the external RC. The recommended resistance set value is 200 Ω to 5.1 kΩ and the recommended capacitor set value is 0.001 µF to 0.1 µF. The aggravation of efficiency may be caused if settings outside this range are made.

Determine ΔV by referring to the following value. The following calculation equation is used for ΔV.

$$\Delta V = \quad Vo2GS \quad (1 - \exp(- \frac{tW}{CR})) \quad [V]$$

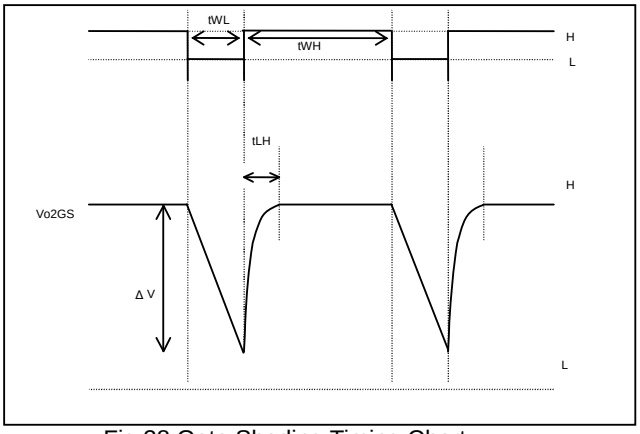


Fig.38 Gate Shading Timing Chart

TIMING STANDARD VALUE

PARAMETER	SYMBOL	LIMIT			UNIT	CONDITION
		MIN	TYP	MAX		
IG " L" Time	tWL	1	2	—	µs	
IG " H" Time	tWH	1	18	—	µs	
Vo2GS"H" to "L" Voltage difference	ΔV		10		V	tWL = 2 us R = 500 Ω*
Vo2GS"L" to "H" Time	tLH		0.1		µs	V = 10 V*

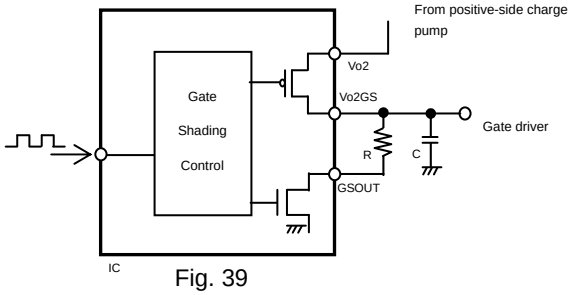


Fig. 39

●I/O Equivalent Circuit Diagram

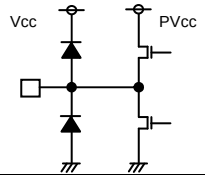
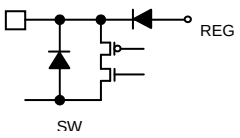
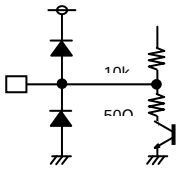
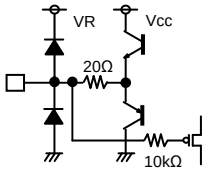
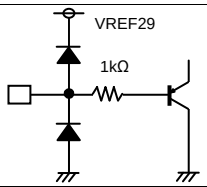
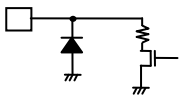
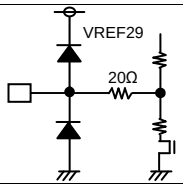
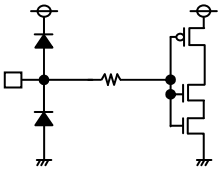
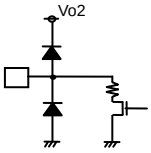
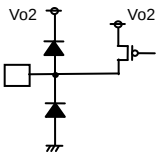
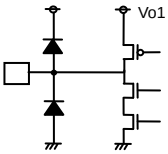
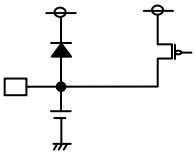
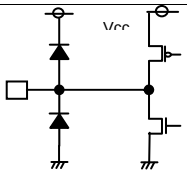
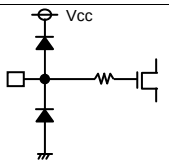
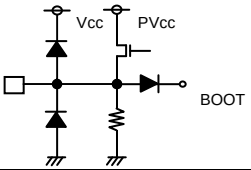
2. SW2 3. SW2 38. SW1 39. SW1	4. BOOT2 37. BOOT1	6. SS2 9. SCP 34. SS1
		
7. COMP2 33. COMP1	8. FB2 12. FB3 25. FB4 32. FB1	11. FOULT
		
13. SS3 30. SS4	14. IG	15. GSOUT
		
16. Vo2GS	18. C1L 19. C2L 24. C3	22. VGH
		
26. COM	27. V- 28. V+	35. VREG
		

Fig. 40

●Notes for use

1) Absolute maximum ratings
Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. A physical safety measure such as a fuse should be implemented when use of the IC in a special mode where the absolute maximum ratings may be exceeded is anticipated.

2) GND potential
Ensure a minimum GND pin potential in all operating conditions.

3) Setting of heat
Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

4) Pin short and mistake fitting
Use caution when orienting and positioning the IC for mounting on printed circuit boards. Improper mounting may result in damage to the IC. Shorts between output pins or between output pins and the power supply and GND pins caused by the presence of a foreign object may result in damage to the IC.

5) Actions in strong magnetic field
Use caution when using the IC in the presence of a strong magnetic field as doing so may cause the IC to malfunction.

6) Testing on application boards
When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Ground the IC during assembly steps as an antistatic measure, and use similar caution when transporting or storing the IC. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process.

7) Ground wiring patterns
When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the application's reference point so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring patterns of any external components.

8) Regarding input pin of the IC
This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P/N junctions are formed at the intersection of these P layers with the N layers of other elements to create a variety of parasitic elements.
For example, when the resistors and transistors are connected to the pins as shown in Fig. 41, a parasitic diode or a transistor operates by inverting the pin voltage and GND voltage.
The formation of parasitic elements as a result of the relationships of the potentials of different pins is an inevitable result of the IC's architecture. The operation of parasitic elements can cause interference with circuit operation as well as IC malfunction and damage. For these reasons, it is necessary to use caution so that the IC is not used in a way that will trigger the operation of parasitic elements such as by the application of voltages lower than the GND (P substrate) voltage to input and output pins.

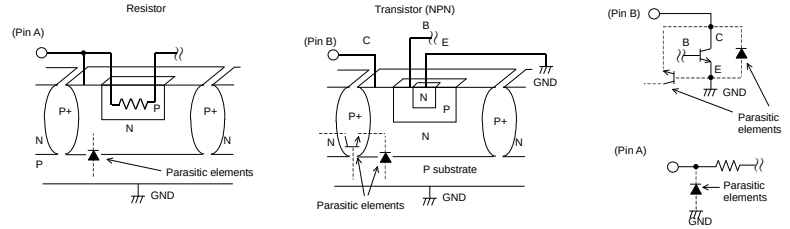


Fig. 41 Example of a Simple Monolithic IC Architecture

9) Overcurrent protection circuits
An overcurrent protection circuit designed according to the output current is incorporated for the prevention of IC damage that may result in the event of load shorting. This protection circuit is effective in preventing damage due to sudden and unexpected accidents. However, the IC should not be used in applications characterized by the continuous operation or transitioning of the protection circuits. At the time of thermal designing, keep in mind that the current capacity has negative characteristics to temperatures.

10) Thermal shutdown circuit (TSD)

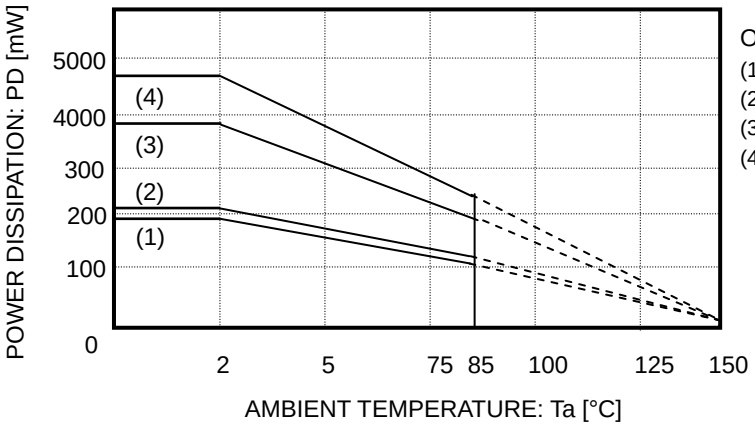
This IC incorporates a built-in TSD circuit for the protection from thermal destruction. The IC should be used within the specified power dissipation range. However, in the event that the IC continues to be operated in excess of its power dissipation limits, the attendant rise in the chip's junction temperature Tj will trigger the TSD circuit to turn off all output power elements. The circuit automatically resets once the junction temperature Tj drops.

Operation of the TSD circuit presumes that the IC's absolute maximum ratings have been exceeded. Application designs should never make use of the TSD circuit.

11) Testing on application boards

At the time of inspection of the installation boards, when the capacitor is connected to the pin with low impedance, be sure to discharge electricity per process because it may load stresses to the IC. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process. Ground the IC during assembly steps as an antistatic measure, and use similar caution when transporting or storing the IC.

●Power Dissipation



On 70 × 70 × 1.6 mm glass epoxy PCB
(1) 1-layer board (Backside copper foil area 0 mm × 0 mm)
(2) 2-layer board (Backside copper foil area 15 mm × 15 mm)
(3) 2-layer board (Backside copper foil area 70 mm × 70 mm)
(4) 4-layer board (Backside copper foil area 70 mm × 70 mm)

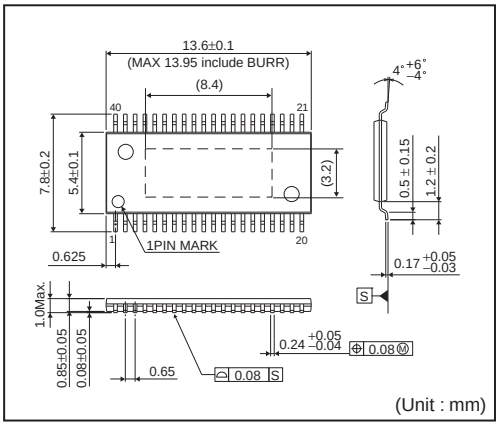
Fig. 42

●Ordering part number

B	D	8	1	6	6	E	F	V	-	E	2

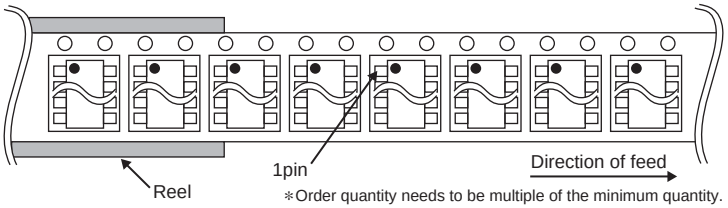
Part No. (BD) | Part No. (8166) | Package: HTSSOP-B40 | Packaging and forming specification: E2: Embossed tape and reel

HTSSOP-B40



<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Notice

Precaution on using ROHM Products

1. Our Products are designed and manufactured for application in ordinary electronic equipments (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are designed and manufactured for use under standard conditions and not under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

QR code printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since our Products might fall under controlled goods prescribed by the applicable foreign exchange and foreign trade act, please consult with ROHM representative in case of export.

Precaution Regarding Intellectual Property Rights

1. All information and data including but not limited to application example contained in this document is for reference only. ROHM does not warrant that foregoing information or data will not infringe any intellectual property rights or any other rights of any third party regarding such information or data. ROHM shall not be in any way responsible or liable for infringement of any intellectual property rights or other damages arising from use of such information or data.:

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Other Precaution

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2. The Products may not be disassembled, converted, modified, reproduced or otherwise changed without prior written consent of ROHM.

3. In no event shall you use in any way whatsoever the Products and the related technical information contained in the Products or this document for any military purposes, including but not limited to, the development of mass-destruction weapons.

4. The proper names of companies or products described in this document are trademarks or registered trademarks of ROHM, its affiliated companies or third parties.

General Precaution

1. Before you use our Products, you are requested to carefully read this document and fully understand its contents. ROHM shall not be in any way responsible or liable for failure, malfunction or accident arising from the use of any ROHM's Products against warning, caution or note contained in this document.

2. All information contained in this document is current as of the issuing date and subject to change without any prior notice. Before purchasing or using ROHM's Products, please confirm the latest information with a ROHM sales representative.

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LifeElectronics
Живое партнерство

ООО «ЛайфЭлектроникс» **“LifeElectronics” LLC**

ИНН 7805602321 КПП 780501001 Р/С 40702810122510004610 ФАКБ "АБСОЛЮТ БАНК" (ЗАО) в г.Санкт-Петербурге К/С 30101810900000000703 БИК 044030703

Компания «Life Electronics» занимается поставками электронных компонентов импортного и отечественного производства от производителей и со складов крупных дистрибьюторов Европы, Америки и Азии.

С конца 2013 года компания активно расширяет линейку поставок компонентов по направлению коаксиальный кабель, кварцевые генераторы и конденсаторы (керамические, пленочные, электролитические), за счёт заключения дистрибьюторских договоров

Мы предлагаем:

- *Конкурентоспособные цены и скидки постоянным клиентам.*
- *Специальные условия для постоянных клиентов.*
- *Подбор аналогов.*
- *Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.*

- *Приемлемые сроки поставки, возможна ускоренная поставка.*
- *Доставку товара в любую точку России и стран СНГ.*
- *Комплексную поставку.*
- *Работу по проектам и поставку образцов.*
- *Формирование склада под заказчика.*

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- *Поставку компонентов, требующих военную и космическую приемку.*
- *Входной контроль качества.*
- *Наличие сертификата ISO.*

В составе нашей компании организован Конструкторский отдел, призванный помогать разработчикам, и инженерам.

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- *Защиту от снятия компонента с производства.*
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- *Изготовление тестовой платы монтаж и пусконаладочные работы.*

Тел: +7 (812) 336 43 04 (многоканальный)
Email: org@lifeelectronics.ru

www.lifeelectronics.ru