

# 74HC175; 74HCT175

Quad D-type flip-flop with reset; positive-edge trigger

Rev. 5 — 29 January 2016

Product data sheet

## 1. General description

The 74HC175; 74HCT175 is a quad positive-edge triggered D-type flip-flop with individual data inputs ( $D_n$ ) and complementary outputs ( $Q_n$  and  $\overline{Q_n}$ ). The common clock (CP) and master reset ( $\overline{MR}$ ) inputs load and reset all flip-flops simultaneously. The D-input that meets the set-up and hold time requirements on the LOW-to-HIGH clock transition will be stored in the flip-flop and appear at the Q output. A LOW on  $\overline{MR}$  causes the flip-flops and outputs to be reset LOW. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of  $V_{CC}$ .

## 2. Features and benefits

- Input levels:
  - ◆ For 74HC175: CMOS level
  - ◆ For 74HCT175: TTL level
- Four edge-triggered D-type flip-flops
- Asynchronous master reset
- Complies with JEDEC standard no. 7A
- ESD protection:
  - ◆ HBM JESD22-A114F exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V.
- Multiple package options
- Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$  and  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$ .

## 3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC175D	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT175D				
74HC175DB	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HCT175DB				
74HC175PW	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HCT175PW				

## 4. Functional diagram

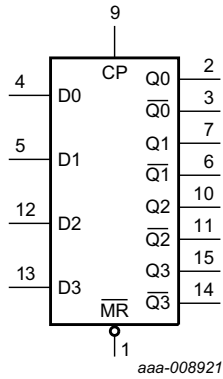


Fig 1. Logic symbol

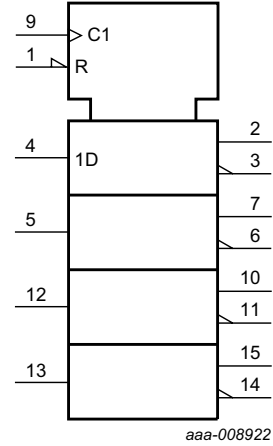


Fig 2. IEC logic symbol

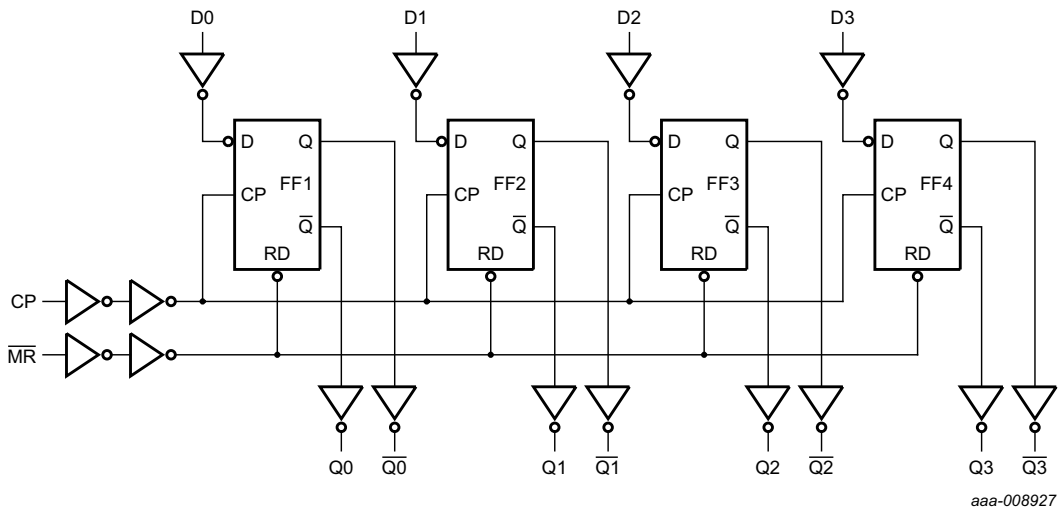


Fig 3. Logic diagram

## 5. Pinning information

### 5.1 Pinning

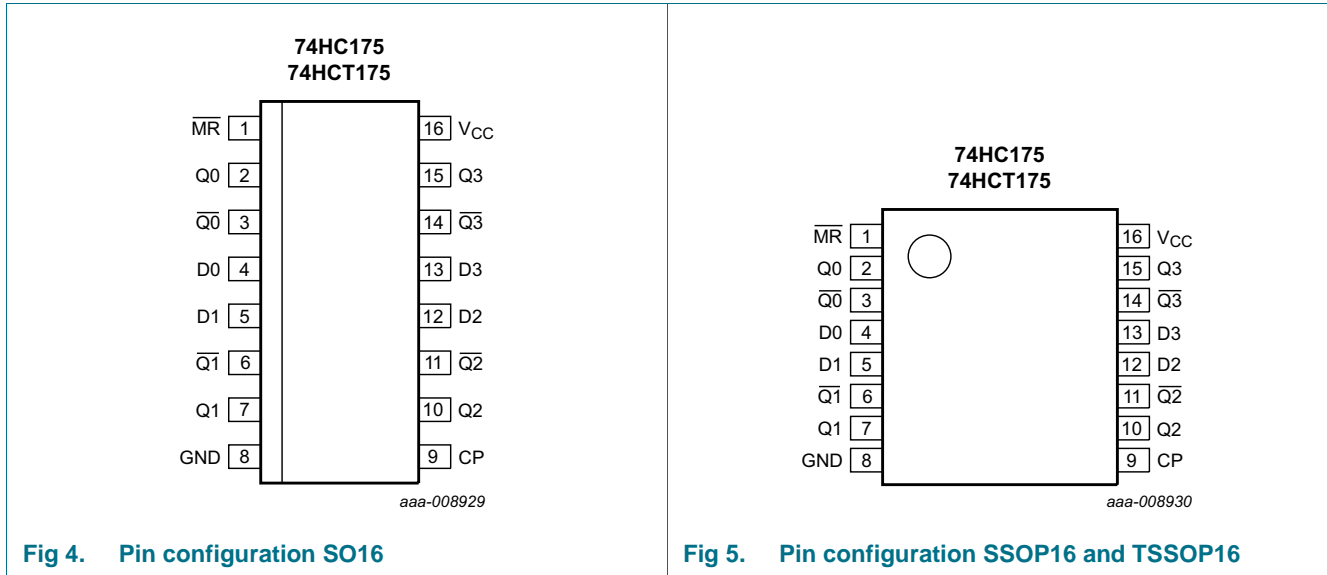


Fig 4. Pin configuration SO16

Fig 5. Pin configuration SSOP16 and TSSOP16

### 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{MR}$	1	asynchronous master reset input (active LOW)
Q0 to Q3	2, 7, 10, 15	flip-flop output
$\overline{Q0}$ to $\overline{Q3}$	3, 6, 11, 14	complementary flip-flop output
D0 to D3	4, 5, 12, 13	data input
GND	8	ground (0 V)
CP	9	clock input (LOW-to-HIGH edge-triggered)
V <sub>CC</sub>	16	positive supply voltage

## 6. Functional description

Table 3. Function table<sup>[1]</sup>

Operating modes	Inputs			Outputs	
	MR	CP	Dn	Qn	$\overline{Qn}$
reset (clear)	L	X	X	L	H
load "1"	H	↑	h	H	L
load "0"	H	↑	l	L	H

- [1] H = HIGH voltage level;
- h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;
- L = LOW voltage level;
- l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;
- X = don't care;
- ↑ = LOW-to-HIGH clock transition.

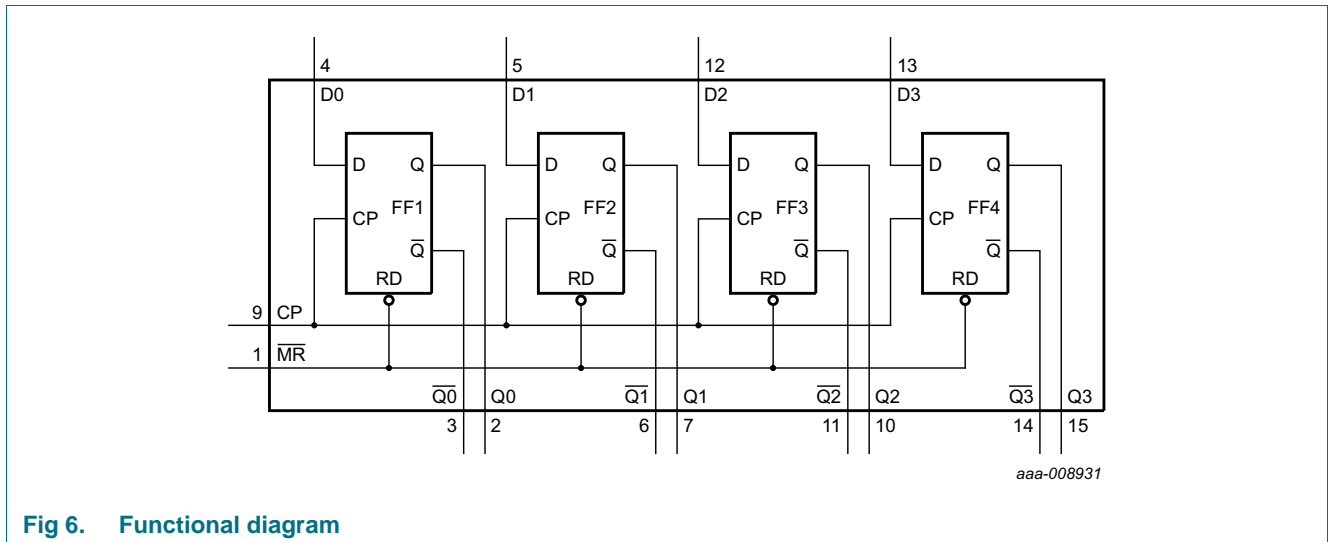


Fig 6. Functional diagram

## 7. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7	V
$I_{IK}$	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	-	$\pm 20$	mA
$I_{OK}$	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$	-	$\pm 20$	mA
$I_O$	output current	$-0.5\text{ V} < V_O < V_{CC} + 0.5\text{ V}$	-	$\pm 25$	mA
$I_{CC}$	supply current		-	50	mA
$I_{GND}$	ground current		-50	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$			
		SO16, SSOP16 and TSSOP16 <a href="#">[1]</a>	-	500	mW

[1] For SO16 package: above 70 °C the value of  $P_{tot}$  derates linearly with 8 mW/K.

For SSOP16 and TSSOP16 packages: above 60 °C the value of  $P_{tot}$  derates linearly with 5.5 mW/K.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC175			74HCT175			Unit
			Min	Typ	Max	Min	Typ	Max	
$V_{CC}$	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
$V_I$	input voltage		0	-	$V_{CC}$	0	-	$V_{CC}$	V
$V_O$	output voltage		0	-	$V_{CC}$	0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	-	+125	-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0\text{ V}$	-	-	625	-	-	-	ns/V
		$V_{CC} = 4.5\text{ V}$	-	1.67	139	-	1.67	139	ns/V
		$V_{CC} = 6.0\text{ V}$	-	-	83	-	-	-	ns/V

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74HC175</b>										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V <sub>CC</sub> = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V <sub>CC</sub> = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V <sub>CC</sub> = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V <sub>CC</sub> = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I <sub>O</sub> = -4.0 mA; V <sub>CC</sub> = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 6.0 V	-	-	±0.1	-	±1	-	±1	μA
		I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 6.0 V	-	-	8.0	-	80	-
C <sub>I</sub>	input capacitance		-	3.5	-	-	-	-	-	pF
<b>74HCT175</b>										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = -20 μA	4.4	4.5	-	4.4	-	4.4	-	V
V <sub>OL</sub>	LOW-level output voltage	I <sub>O</sub> = -4.0 mA	3.98	4.32	-	3.84	-	3.7	-	V
		V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
I <sub>I</sub>	input leakage current	I <sub>O</sub> = 5.2 mA; V <sub>CC</sub> = 5.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5 V	-	-	±0.1	-	±1	-	±1	μA

**Table 6. Static characteristics ...continued**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	8.0	-	80	-	160	μA
ΔI <sub>CC</sub>	additional supply current	per input pin; V <sub>I</sub> = V <sub>CC</sub> - 2.1 V; other inputs at V <sub>CC</sub> or GND; V <sub>CC</sub> = 4.5 V to 5.5 V								
		Dn input	-	40	144	-	180	-	196	μA
		CP input	-	60	216	-	270	-	294	μA
		MR input	-	100	360	-	450	-	490	μA
C <sub>I</sub>	input capacitance		-	3.5	-	-	-	-	-	pF

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**GND (ground = 0 V); C<sub>L</sub> = 50 pF unless otherwise specified; for test circuit, see [Figure 10](#)

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74HC175</b>										
t <sub>pd</sub>	propagation delay	CP to Qn, $\overline{Qn}$ ; see <a href="#">Figure 7</a> <a href="#">[1]</a>								
		V <sub>CC</sub> = 2.0 V	-	55	175	-	220	-	265	ns
		V <sub>CC</sub> = 4.5 V	-	20	35	-	44	-	53	ns
		V <sub>CC</sub> = 5 V; C <sub>L</sub> = 15 pF	-	17	-	-	-	-	-	ns
		V <sub>CC</sub> = 6.0 V	-	16	30	-	37	-	45	ns
t <sub>PHL</sub>	HIGH to LOW propagation delay	MR to Qn, $\overline{Qn}$ ; see <a href="#">Figure 9</a>								
		V <sub>CC</sub> = 2.0 V	-	50	150	-	190	-	225	ns
		V <sub>CC</sub> = 4.5 V	-	18	30	-	38	-	45	ns
		V <sub>CC</sub> = 5 V; C <sub>L</sub> = 15 pF	-	15	-	-	-	-	-	ns
		V <sub>CC</sub> = 6.0 V	-	14	26	-	33	-	38	ns
t <sub>t</sub>	transition time	Qn output; see <a href="#">Figure 7</a> <a href="#">[2]</a>								
		V <sub>CC</sub> = 2.0 V	-	19	75	-	95	-	110	ns
		V <sub>CC</sub> = 4.5 V	-	7	15	-	19	-	22	ns
		V <sub>CC</sub> = 6.0 V	-	6	13	-	16	-	19	ns

**Table 7. Dynamic characteristics ...continued**GND (ground = 0 V);  $C_L = 50$  pF unless otherwise specified; for test circuit, see [Figure 10](#)

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit	
			Min	Typ	Max	Min	Max	Min	Max		
$t_{w}$	pulse width	CP input HIGH or LOW; see <a href="#">Figure 7</a>									
		$V_{CC} = 2.0$ V	80	22	-	100	-	120	-	ns	
		$V_{CC} = 4.5$ V	16	8	-	20	-	24	-	ns	
			$V_{CC} = 6.0$ V	14	6	-	17	-	20	-	ns
	MR input LOW; see <a href="#">Figure 9</a>	$V_{CC} = 2.0$ V	80	19	-	100	-	120	-	ns	
		$V_{CC} = 4.5$ V	16	7	-	20	-	24	-	ns	
		$V_{CC} = 6.0$ V	14	6	-	17	-	20	-	ns	
$t_{rec}$	recovery time	MR to CP; see <a href="#">Figure 9</a>									
		$V_{CC} = 2.0$ V	5	−33	-	5	-	5	-	ns	
		$V_{CC} = 4.5$ V	5	−12	-	5	-	5	-	ns	
		$V_{CC} = 6.0$ V	5	−10	-	5	-	5	-	ns	
$t_{su}$	set-up time	Dn to CP; see <a href="#">Figure 7</a>									
		$V_{CC} = 2.0$ V	80	3	-	100	-	120	-	ns	
		$V_{CC} = 4.5$ V	16	1	-	20	-	24	-	ns	
		$V_{CC} = 6.0$ V	14	1	-	17	-	20	-	ns	
$t_h$	hold time	Dn to CP; see <a href="#">Figure 7</a>									
		$V_{CC} = 2.0$ V	25	2	-	30	-	40	-	ns	
		$V_{CC} = 4.5$ V	5	0	-	6	-	8	-	ns	
		$V_{CC} = 6.0$ V	4	0	-	5	-	7	-	ns	
$f_{max}$	maximum frequency	CP input; see <a href="#">Figure 7</a>									
		$V_{CC} = 2.0$ V	6	25	-	4.8	-	4	-	MHz	
		$V_{CC} = 4.5$ V	30	75	-	24	-	20	-	MHz	
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	83	-	-	-	-	-	MHz	
		$V_{CC} = 6.0$ V	35	89	-	28	-	24	-	MHz	
$C_{PD}$	power dissipation capacitance	per package; $V_I = \text{GND to } V_{CC}$	<sup>3)</sup>	-	32	-	-	-	-	pF	



**Table 7. Dynamic characteristics ...continued**GND (ground = 0 V);  $C_L = 50$  pF unless otherwise specified; for test circuit, see [Figure 10](#)

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74HCT175</b>										
$t_{pd}$	propagation delay	CP to $Q_n, \bar{Q}_n$ ; see <a href="#">Figure 7</a> <sup>[1]</sup>								
		$V_{CC} = 4.5$ V	-	19	33	-	41	-	50	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	16	-	-	-	-	-	ns
$t_{PHL}$	HIGH to LOW propagation delay	$\overline{MR}$ to $Q_n$ ; see <a href="#">Figure 9</a>								
		$V_{CC} = 4.5$ V	-	22	38	-	48	-	57	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	19	-	-	-	-	-	ns
		$\overline{MR}$ to $\bar{Q}_n$ ; see <a href="#">Figure 9</a>								
		$V_{CC} = 4.5$ V	-	19	35	-	44	-	53	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	16	-	-	-	-	-	ns
$t_t$	transition time	$Q_n$ output; see <a href="#">Figure 7</a> <sup>[2]</sup>								
		$V_{CC} = 4.5$ V	-	7	15	-	19	-	22	ns
$t_W$	pulse width	CP input; see <a href="#">Figure 7</a>								
		$V_{CC} = 4.5$ V	20	12	-	25	-	30	-	ns
		$\overline{MR}$ input LOW; see <a href="#">Figure 9</a>								
$t_{rec}$	recovery time	$\overline{MR}$ to CP; see <a href="#">Figure 9</a>								
		$V_{CC} = 4.5$ V	5	-10	-	5	-	5	-	ns
$t_{su}$	set-up time	$D_n$ to CP; see <a href="#">Figure 7</a>								
		$V_{CC} = 4.5$ V	16	5	-	20	-	24	-	ns
$t_h$	hold time	$D_n$ to CP; see <a href="#">Figure 7</a>								
		$V_{CC} = 4.5$ V	5	0	-	5	-	5	-	ns
$f_{max}$	maximum frequency	CP input; see <a href="#">Figure 7</a>								
		$V_{CC} = 4.5$ V	25	49	-	20	-	17	-	MHz
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	54	-	-	-	-	-	MHz
$C_{PD}$	power dissipation capacitance	per package; $V_I = GND$ to $V_{CC} - 1.5$ V <sup>[3]</sup>	-	34	-	-	-	-	-	pF

[1]  $t_{pd}$  is the same as  $t_{PHL}$  and  $t_{PLH}$ .

[2]  $t_t$  is the same as  $t_{THL}$  and  $t_{TLH}$ .

[3]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu$ W).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;

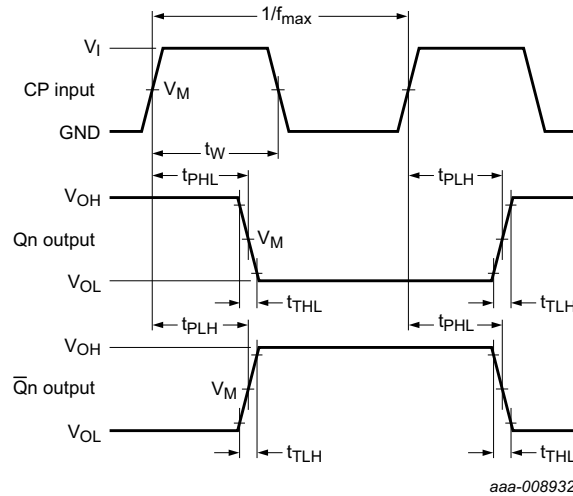
$f_o$  = output frequency in MHz;

$\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs;

$C_L$  = output load capacitance in pF;

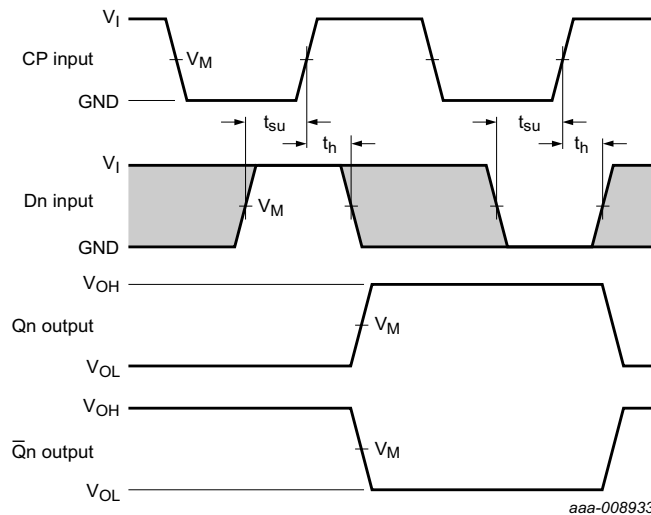
$V_{CC}$  = supply voltage in V.

## 11. Waveforms



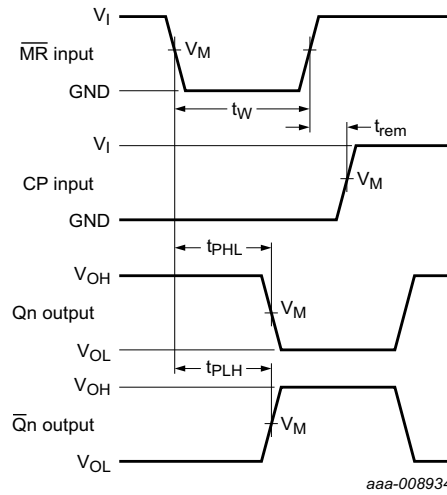
Measurement points are given in [Table 8](#).

**Fig 7. Input to output propagation delay, output transition time, clock input pulse width and maximum frequency**



Measurement points are given in [Table 8](#).

**Fig 8. Data set-up and hold times for data input**

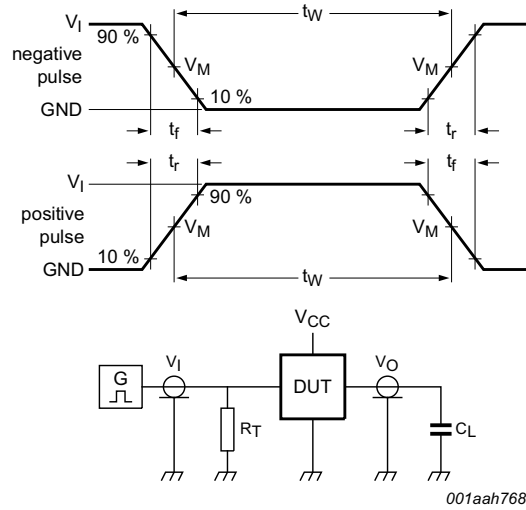


Measurement points are given in [Table 8](#).

**Fig 9. Master reset to output propagation delays, master reset pulse width and master reset to clock recovery time**

**Table 8. Measurement points**

Type	Input		Output
	$V_I$	$V_M$	$V_M$
74HC175	$V_{CC}$	$0.5V_{CC}$	$0.5V_{CC}$
74HCT175	3 V	1.3 V	1.3 V



Test data is given in [Table 9](#).

Definitions for test circuit:

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_L$  = Load resistance.

**Fig 10. Test circuit for measuring switching times**

**Table 9. Test data**

Type	Input		Load		Test
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	
74HC175	$V_{CC}$	6 ns	15 pF, 50 pF	1 k $\Omega$	$t_{PLH}, t_{PHL}$
74HCT175	3 V	6 ns	15 pF, 50 pF	1 k $\Omega$	$t_{PLH}, t_{PHL}$

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

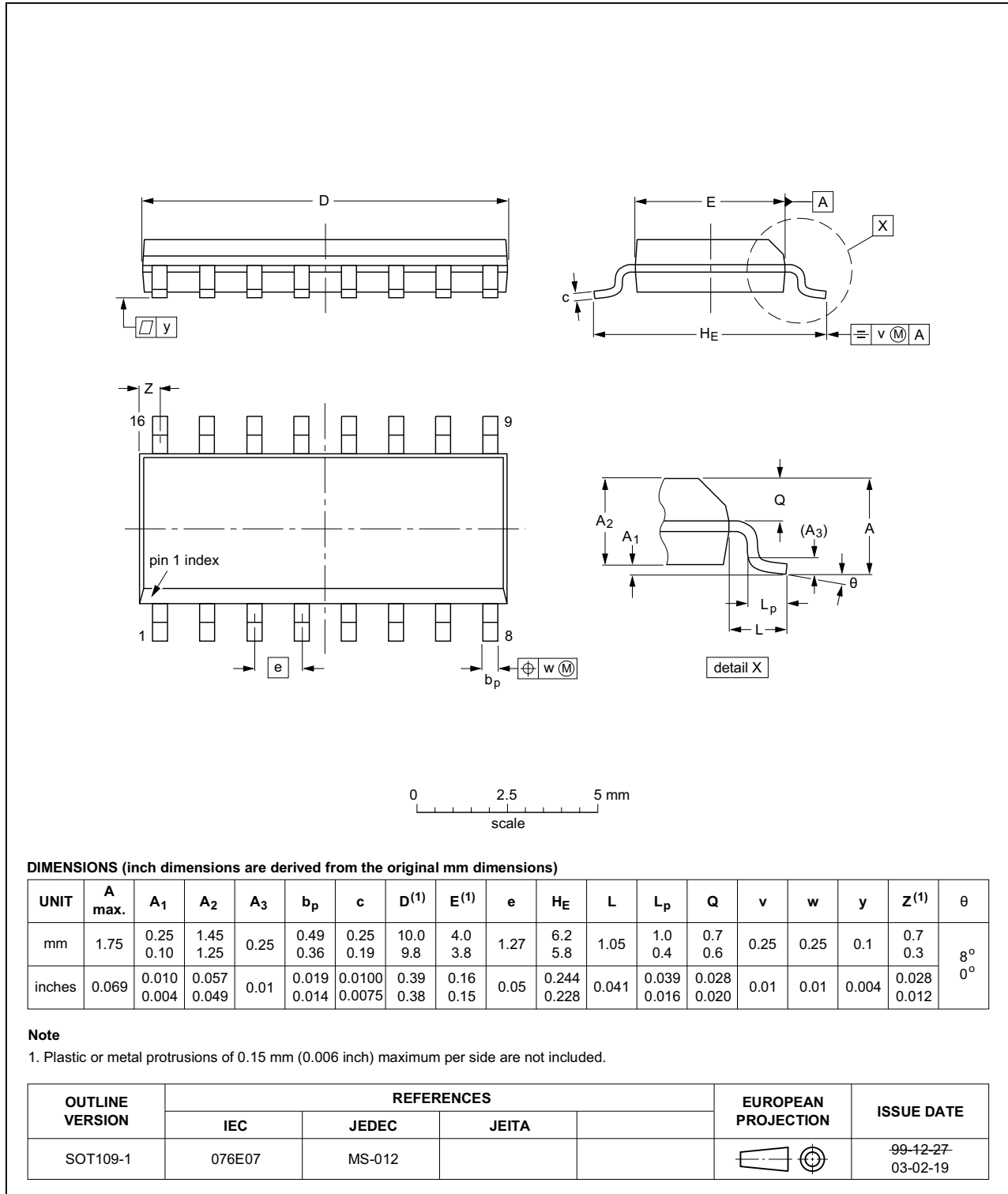


Fig 11. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

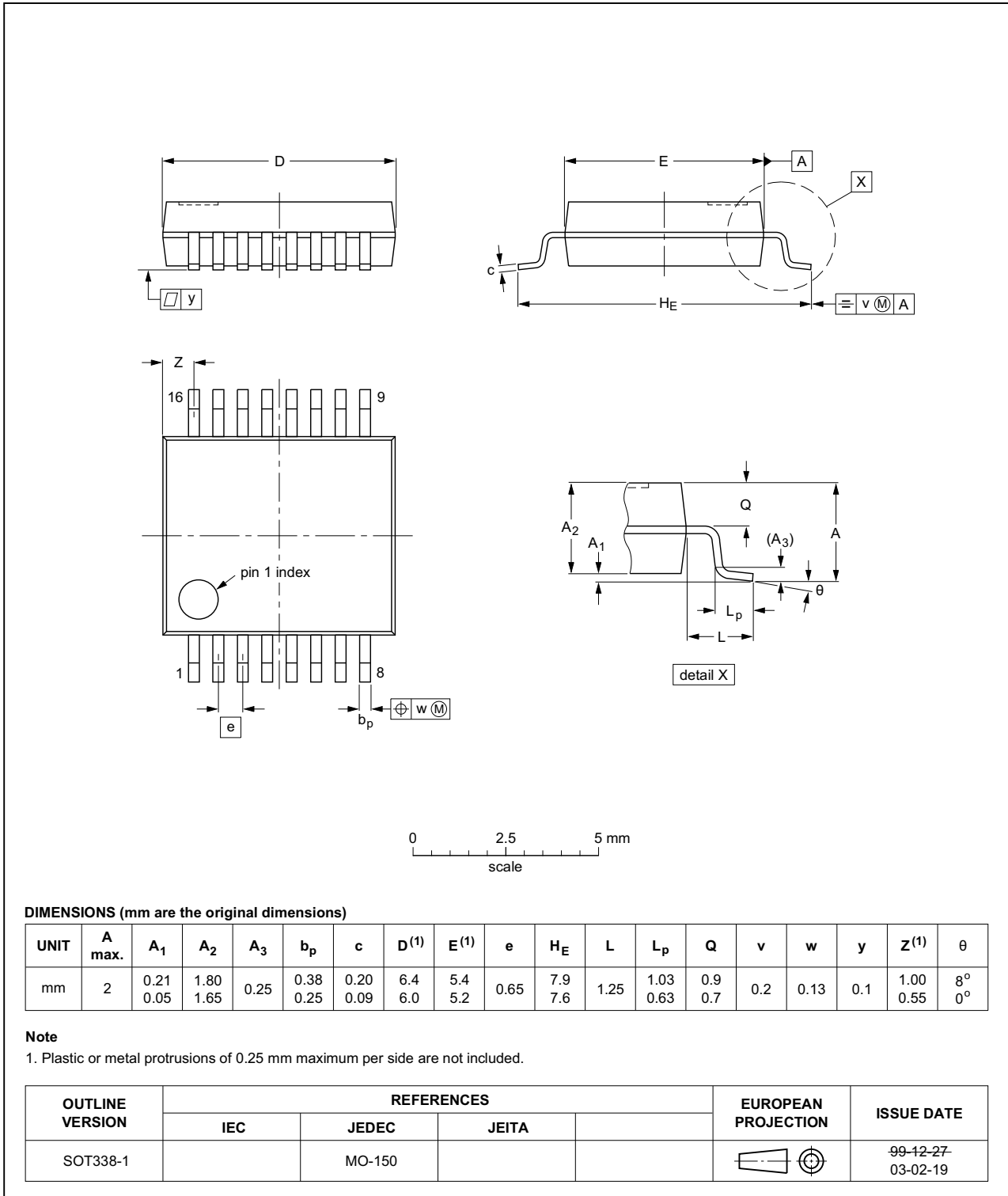


Fig 12. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

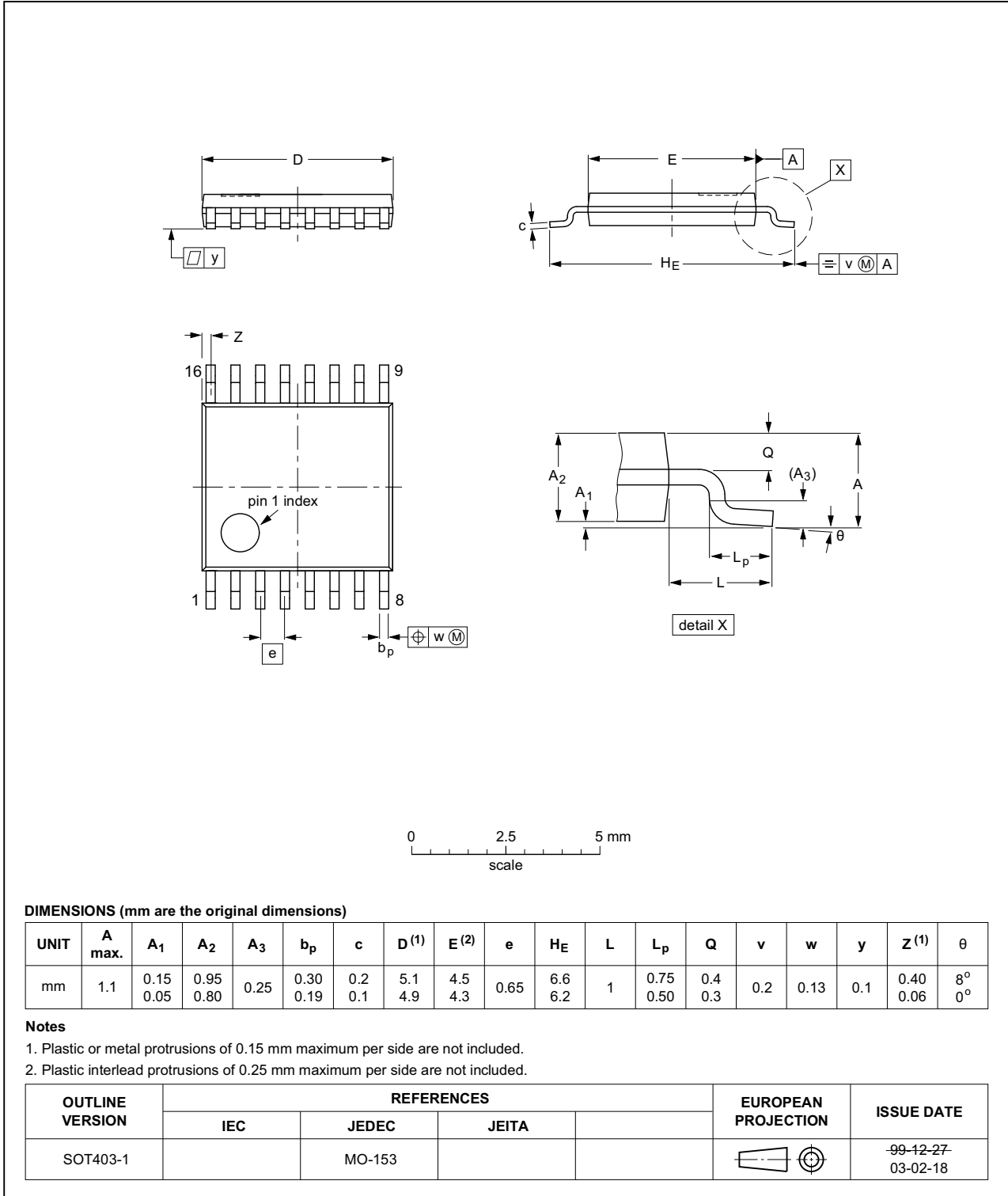


Fig 13. Package outline SOT403-1 (TSSOP16)

## 13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT175 v.5	20160129	Product data sheet	-	74HC_HCT175 v.4
Modifications:	<ul style="list-style-type: none"> <li>Type numbers 74HC175N and 74HCT175N (SOT38-4) removed.</li> </ul>			
74HC_HCT175 v.4	20140408	Product data sheet	-	74HC_HCT175 v.3
Modifications:	<ul style="list-style-type: none"> <li>General description corrected (errata).</li> </ul>			
74HC_HCT175 v.3	20140331	Product data sheet	-	74HC_HCT175_CNV_2
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> </ul>			
74HC_HCT175_CNV_2	19980708	Product specification	-	-



## 15. Legal information

### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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