

NOIL1SN3000A

LUPA3000: 3 MegaPixel High Speed CMOS Sensor



ON Semiconductor®

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Features

- 1696 x 1710 Active Pixels
- 8 μm x 8 μm Square Pixels
- 1.2 inch Optical Format
- Monochrome or Color Digital Output
- 485 Frames per Second (fps) Frame Rate
- 64 On-Chip 8-Bit ADCs
- 32 Low-Voltage Digital Signaling (LVDS) Serial Outputs
- Random Programmable Region of Interest (ROI) Readout
- Pipelined and Triggered Global Shutter
- Serial Peripheral Interface (SPI)
- Dynamic Range Extended by Double Slope
- Limited Supplies: Nominal 2.5 V and 3.3 V
- 0°C to 60°C Operational Temperature Range
- 369-Pin μPGA Package
- 1.1 W Power Dissipation
- These Devices are Pb-Free and are RoHS Compliant

Applications

- High Speed Machine Vision
- Holographic Data Storage
- Motion Analysis
- Intelligent Traffic System
- Medical Imaging
- Industrial Imaging

Description

The LUPA3000 is a high-speed CMOS image sensor with an image resolution of 1696 by 1710 pixels. The pixels are 8 μm x 8 μm in size and consist of high sensitivity 6T pipelined global shutter capability where integration during readout is possible. The LUPA3000 delivers 8-bit color or monochrome digital images with a 3 Megapixels resolution at 485 fps that makes this product ideal for high-speed vision machine, intelligent traffic system, and holographic data storage. The LUPA3000 captures complex high-speed events for traditional machine vision applications and various high-speed imaging applications.

The LUPA3000 production package is housed in a 369-pin ceramic μPGA package and is available in a monochrome version or Bayer (RGB) patterned color filter array with micro lens. Contact your local ON Semiconductor representative for more information.

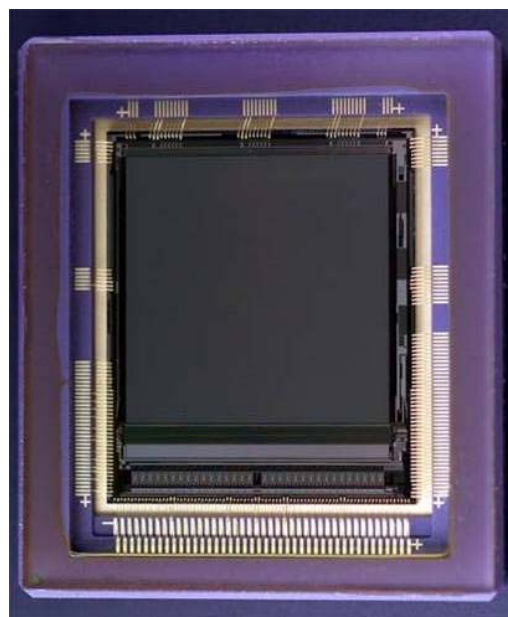


Figure 1. LUPA3000 Package Photo

ORDERING INFORMATION

| Marketing Part Number | Mono / Color | Package |
|-----------------------|-----------------------------|-------------------------|
| NOIL1SN3000A-GDC | Mono micro lens with glass | 369-pin μPGA |
| NOIL1SE3000A-GDC | Color micro lens with glass | |

NOTE: Refer to Ordering Code Definition on page 54 for more information.

NOIL1SN3000A

CONTENTS

| | | | |
|-----------------------------------|----------|---|-----------|
| Features | 1 | Operating Modes | 32 |
| Applications | 1 | Image Sensor Timing and Readout | 34 |
| Description | 1 | Additional Features | 41 |
| Ordering Information | 1 | Package Information | 44 |
| Contents | 2 | Specifications and Useful References | 54 |
| Specifications | 3 | Acronyms | 55 |
| Overview | 6 | Glossary | 56 |
| Sensor Architecture | 8 | | |

NOIL1SN3000A

SPECIFICATIONS

Key Specifications

Table 1. GENERAL SPECIFICATIONS

| Parameter | Specifications |
|------------------------|--|
| Active pixels | 1696 (H) x 1710 (V) |
| Pixel size | 8 μm x 8 μm |
| Pixel type | 6T pixel architecture |
| Data rate | 412 Mbps (32 serial LVDS outputs) |
| Shutter type | Pipelined and Triggered Global Shutter |
| Frame rate | 485 fps at full frame |
| Master clock | 206 MHz |
| Windowing (ROI) | Randomly programmable ROI read out. Implemented as scanning of lines or columns from an uploaded position. |
| ADC resolution | 8-bit, on-chip |
| Extended dynamic range | Double slope (up to 80 dB optical dynamic range) |

Table 2. ELECTRO-OPTICAL SPECIFICATIONS

| Parameter | Specifications |
|--|--|
| Conversion gain | 39.2 $\mu\text{V}/e^-$ |
| Full well charge | 27000 e^- |
| Responsivity | 1270 $\text{V}\cdot\text{m}^2/\text{W}\cdot\text{s}$ at 550 nm with micro lens |
| Parasitic light sensitivity | < 1/5000 |
| Dark noise | 21 e^- |
| Quantum efficiency (QE) x Fill-factor (FF) | 37% at 680 nm with micro lens |
| Fixed pattern noise (FPN) | 2% of V_{sweepRMS} |
| Photo response non-uniformity (PRNU) | 2.2% of V_{signal} |
| Dark signal | 277 mV/s at 25°C |
| Power dissipation | 1.1 W at 485 fps |

Table 3. RECOMMENDED OPERATING RATINGS

| T_J (Note 2) | Operating temperature range | 0 | 60 | °C |
|----------------|-----------------------------|---|----|----|
| | | | | |

Table 4. ABSOLUTE MAXIMUM RATINGS (Note 1)

| Symbol | Description | Min | Max | Units |
|---|-----------------------------------|------------------------------------|------|-------|
| ABS (2.5 V supply group) | ABS rating for 2.5 V supply group | -0.5 | 3.0 | V |
| ABS (3.3 V supply group) | ABS rating for 3.3 V supply group | -0.5 | 4.3 | V |
| T_S (Notes 3 and 4) | ABS Storage temperature range | -40 | +150 | °C |
| | ABS Storage humidity range | 5 | 90 | %RH |
| Electrostatic Discharge (ESD) (Note 3) | Human Body Model (HBM) | 2000 | | V |
| | Charged Device Model (CDM) | 500 | | V |
| LU | Latch-up | LUPA3000 is not rated for latch-up | | mA |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Absolute maximum ratings are limits beyond which damage may occur.
2. Operating ratings are conditions in which operation of the device is intended to be functional.
3. ON Semiconductor recommends that customers become familiar with, and follow the procedures in JEDEC Standard JESD625-A. Refer to Application Note AN52561. Long term exposure toward the maximum storage temperature will accelerate color filter degradation.
4. Caution needs to be taken to avoid dried stains on the underside of the glass due to condensation. The glass lid glue is permeable and can absorb moisture if the sensor is placed in a high % RH environment.

NOIL1SN3000A

Electrical Specifications

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 5. POWER SUPPLY RATINGS (Notes 1, 2 and 3)

Limits in bold apply for $T_A = T_{MIN}$ to T_{MAX} , all other limits $T_A = +25^\circ\text{C}$. System speed = 50 MHz, Sensor clock = 200 MHz

| Symbol | Power Supply | Parameter | Condition | Min | Typ | Max | Units |
|----------------------------------|-------------------------------------|-------------------------|--|-------------|------|-------------|-------|
| V_{ANA} , GND_{ANA} | Analog Supply | Operating Voltage | | -5% | 2.5 | +5% | V |
| | | Dynamic Current | Clock enabled, lux = 0 | | 35 | | mA |
| | | Peak Current | Row overhead time (ROT) | | 100 | | mA |
| V_{DD} , GND_{DD} | Digital Supply | Operating Voltage | | -5% | 2.5 | +5% | V |
| | | Dynamic Current | Clock enabled, lux = 0 | | 1 | | mA |
| | | Peak Current | Frame overhead time (FOT) | | 80 | | mA |
| V_{DD_HS} , GND_{DD_HS} | Digital Supply high speed | Operating Voltage | | -5% | 2.5 | +5% | V |
| | | Dynamic Current | Clock enabled, lux = 0 | | 100 | | mA |
| | | Peak Current | FOT | | 60 | | mA |
| V_{PIX} , GND_{PIX} | Pixel Supply | Operating Voltage | | -5% | 2.5 | +5% | V |
| | | Peak Current during FOT | Transient duration = 2 μs | | 210 | | mA |
| | | Peak Current during ROT | Transient duration = 0.5 μs | | 100 | | mA |
| V_{LVDS} , GND_{LVDS} | LVDS Supply | Operating Voltage | | -5% | 2.5 | +5% | V |
| | | Dynamic Current | Clock enabled, lux = 0 | | 170 | | mA |
| | | Peak Current | ROT | | 80 | | mA |
| V_{ADC} , GND_{ADC} | ADC Supply | Operating Voltage | | -5% | 2.5 | +5% | V |
| | | Dynamic Current | Clock enabled, lux = 0 | | 150 | | mA |
| | | Peak Current | Clock enabled, lux = 0 | | 275 | | mA |
| V_{RES} | Reset Supply | Operating Voltage | | -5% | 3.3 | +5% | V |
| | | Peak current during FOT | Transient duration: 200 ns | | 1000 | | mA |
| V_{RES_DS} | Reset dual slope supply | Operating Voltage | | 1.8 | 2.5 | 3.5 | V |
| V_{MEM_L} (Note 4) | Memory Element low level supply | Operating Voltage | | -5% | 2.5 | +5% | V |
| | | Peak current during FOT | Clock enabled, bright | | 180 | | mA |
| V_{MEM_H} | Memory Element high level supply | Operating Voltage | | -5% | 3.3 | +5% | V |
| | | Peak current during FOT | | | 90 | | mA |
| $V_{PRECHARGE}$ | Pre_charge Driver Supply | Operating Voltage | | -10% | 0.4 | +10% | V |
| | | Peak Current during FOT | Transient duration: 50 ns | | 10 | | mA |
| V_{CM} | Common mode voltage | Operating Voltage | (Refer to Table 44 on page 29) | | 0.9 | | V |

1. All parameters are characterized for DC conditions after thermal equilibrium is established.
2. Peak currents are measured without the load capacitor from the LDO (Low Dropout Regulator). The 100 nF capacitor bank is connected to the pin in question.
3. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, take normal precautions to avoid application of any voltages higher than the maximum rated voltages to this high impedance circuit.
4. The V_{MEM_L} power supply should have a sourcing and sinking current capability.

Table 6. POWER DISSIPATION (Note 1)

Power supply specifications according to Table 5.

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---------------|------------------------------|-------------------------|-----|-----|-----|-------|
| Dynamic Power | Average power dissipation | lux = 0, clock = 50 MHz | 0.8 | 1.1 | 1.4 | W |
| Standby Power | Power dissipation in standby | lux = 0, No clock | | 180 | | mW |

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Table 7. AC ELECTRICAL CHARACTERISTICS (Note 1)

The following specifications apply for VDD = 2.5 V

| Symbol | Parameter | Condition | Typ | Max | Units |
|------------------|-----------------------|---------------------|-----|-----|-------|
| F _{CLK} | Input clock frequency | fps = 485 | | 206 | MHz |
| fps | Frame rate | Maximum clock speed | | 485 | fps |

1. All parameters are characterized for DC conditions after thermal equilibrium is established.

Combining Power Supplies

Every module in the image sensor has its own power supply and ground. The grounds can be combined externally, but not all power supply inputs may be combined. Some power supplies must be isolated to reduce electrical crosstalk and improve shielding, dynamic range, and output swing. Internal to the image sensor, the ground lines of each module are kept separate to improve shielding and electrical crosstalk between them.

The LUPA3000 contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, take normal precautions to avoid voltages higher than the maximum rated voltages in this high-impedance circuit. All power supply pins should be decoupled to ground with a 100 nF capacitor. The V_{pix} and V_{res_ds} power are the most sensitive to power supply noise.

The recommended combinations of supplies are:

- Analog group of +2.5 V supply: V_{RES_DS}, V_{ADC}, V_{pix}, V_{ANA}
- Digital Group of +2.5 V supply: V_{DD}, V_{D_HS}, V_{LVDS}
- The V_{MEM_L} and V_{PRECHARGE} supplies should have sinking and sourcing capability

Biasing

The sensor requires three biasing resistors. Refer to Table 8 for more information.

For low frame rates (< 2000 fps), the PRECHARGE_BIAS_1 pins are connected directly with the V_{PRECHARGE} pins. The DC level on the PRECHARGE_BIAS_1 pins acts as a power supply and must be decoupled.

For higher frame rates, the duty cycle on V_{PRECHARGE} is too high and the voltage drops. This causes the black level to shift compared to the low frame rate case. In higher frame rates, the voltage on PRECHARGE_BIAS_1 is buffered on the PCB and the buffered voltage is taken for V_{PRECHARGE}. A second possibility is to make the biasing resistor larger until the correct DC level is reached.

PRECHARGE_BIAS_2 must be left floating, because it is intended for testing purposes.

Table 8. BIASING RESISTORS

| Signal | Comment | Related Module | DC level |
|------------------|---|-------------------|-----------------|
| Current_Ref_1 | Connect with 20 kΩ (1% prec.) to V _{AA} . Decouple to GND _{AA} | Column amplifiers | 769 mV at 86 μA |
| Current_Ref_2 | Connect with 50 kΩ (1% prec.) to GND _{ADC} . No decoupling | ADCs | 25 μA to gnd |
| Precharge_Bias_1 | Connect with 90 kΩ (1% prec.) to V _{PIX} . Decouple to V _{pix} with 100 nF. | Pixel array | 0.45 V at 23 μA |
| Precharge_Bias_2 | Leave floating | | |

OVERVIEW

The datasheet describes the interfaces of the LUPA3000. The CMOS image sensor features synchronous shutter with a maximum frame rate of 485 fps at full resolution.

The sensor contains 64 on-chip 8-bit ADCs operating at 25.75 Msamples/s each, resulting in an aggregate pixel rate of 1.4 Gigapix/s. The outputs of the 64 ADCs are multiplexed onto 32 LVDS serial links operating at 412 Mbit/s each resulting in an aggregate data rate of 13.2 Gbits. The 32 data channel LVDS interface allows a high data rate with limited number of pins. Each channel runs at 51.5 MSPS pixel rate, which results in 485 fps frame rate at full resolution. Higher frame rates are achieved by windowing, which is programmable over the SPI interface.

All required clocks, control, and bias signals are generated on-chip. The incoming high speed clock is divided to generate the different low speed clocks required for sensor operation. The sensor generates all its bias signals from an internal bandgap reference. An on-chip sequencer generates all the required control signals for the image core, the ADCs, and the on-chip digital data processing path. The sequencer settings are stored in registers that can be programmed through the serial command interface. The sequencer supports windowed readout at frame rates up to 10000 fps.

Color Filter Array

The color version of LUPA3000 is available in Bayer (RGB) patterned color filter array. The orientation of RGB and active pixel array [0,0] is shown in Figure 2.

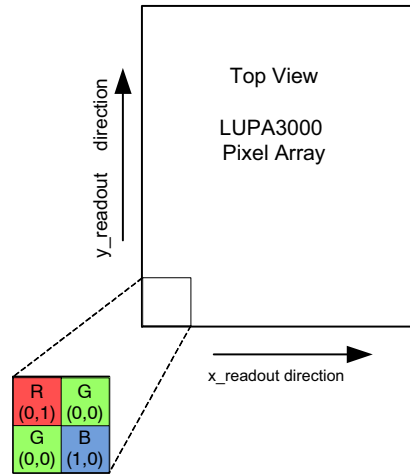


Figure 2. RGB Bayer

Spectral Response

Figure 3 shows the spectral response of the mono and color versions of the LUPA3000. Figure 4 and Figure 5 on page 7 depict the micro lens behaviour for mono and color devices for mid range wavelengths.

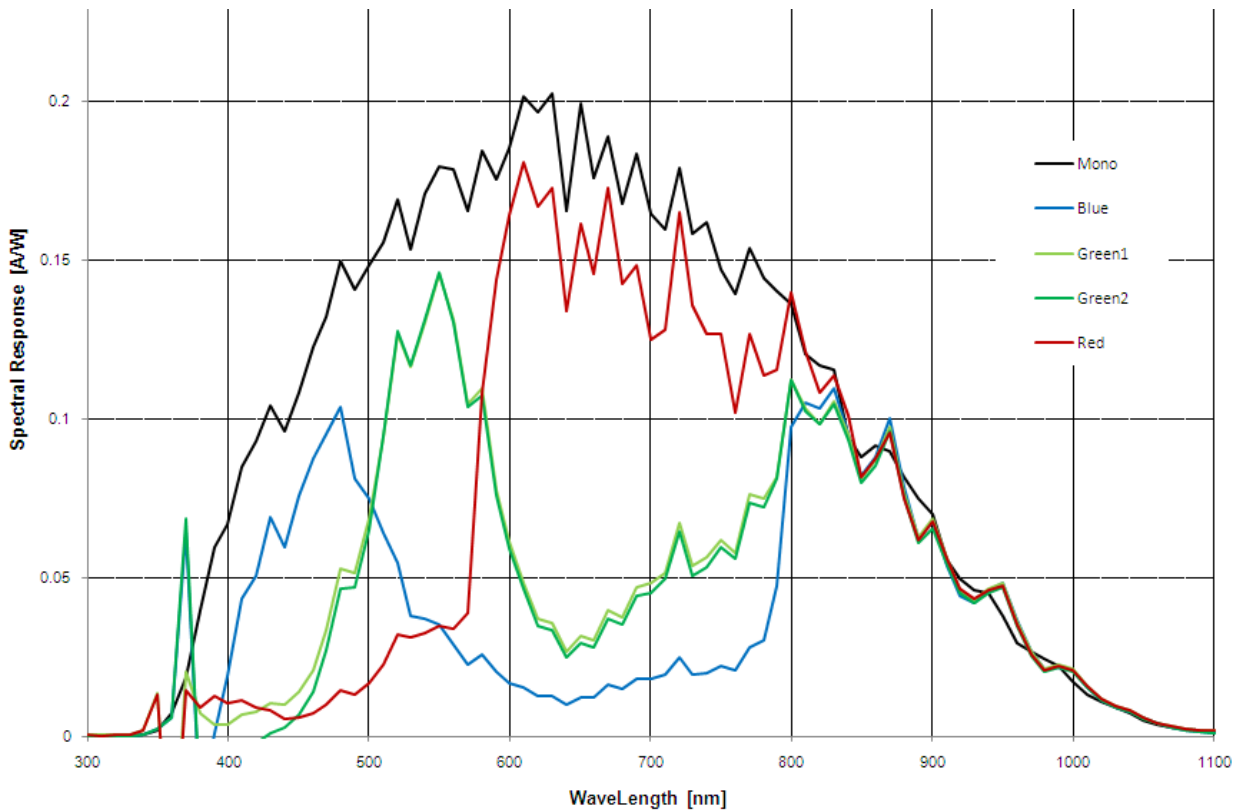


Figure 3. Mono and Color Spectral Response

NOIL1SN3000A

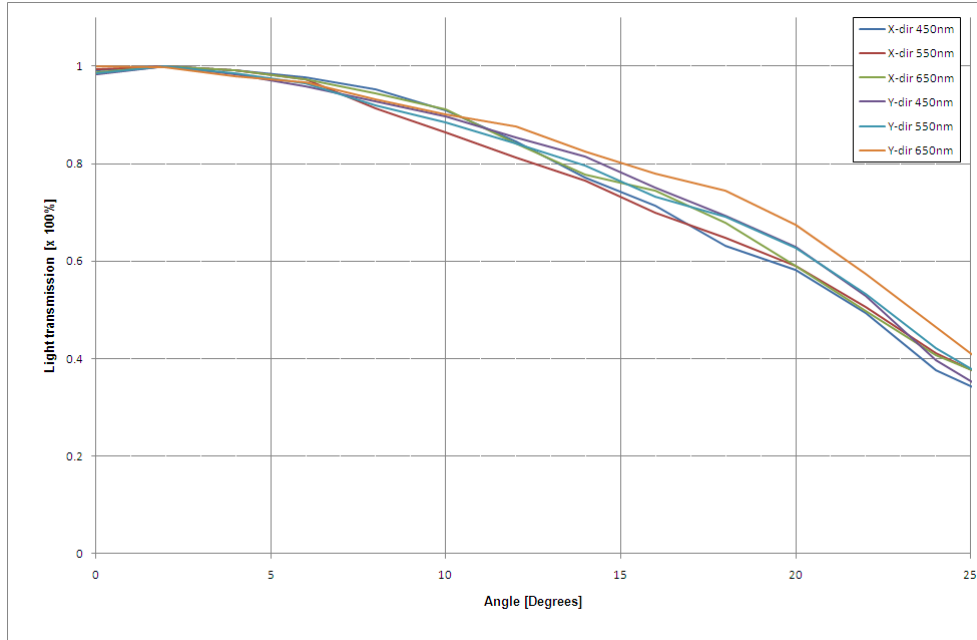


Figure 4. Micro Lens Behavior for Mono

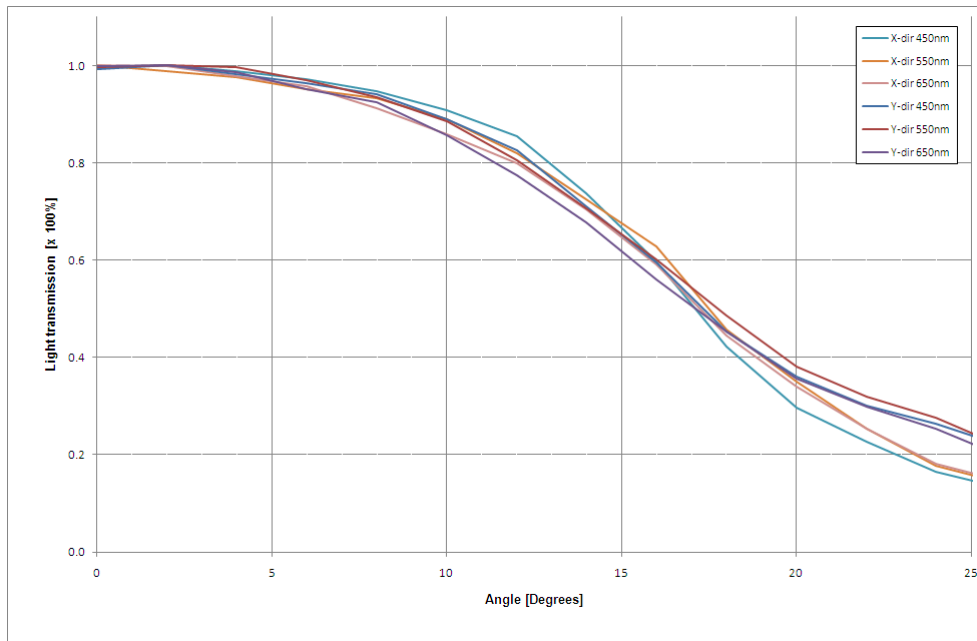


Figure 5. Micro Lens Behavior for Color

SENSOR ARCHITECTURE

Image Sensor Core

The LUPA3000 floor plan is shown in Figure 6. The sensor consists of the pixel array, column amplifiers, analog front end (AFE) consisting of programmable gain amplifier and ADCs, data block (not shown), sequencer, and LVDS transmitter and receivers. The image sensor of 1696 x 1710 active pixels is read out in progressive scan.

The architecture enables programmable addressing in the x-direction in steps of 32 pixels, and in the y-direction in

steps of one line. The starting point of the address can be uploaded by the SPI.

The AFE prepares the signal for the digital data block when the data is multiplexed and prepared for the LVDS interface.

NOTE: In Figure 7 on page 9, 32 pixels (1 kernel) are read out, where the most significant bit (MSB) is the first bit out.

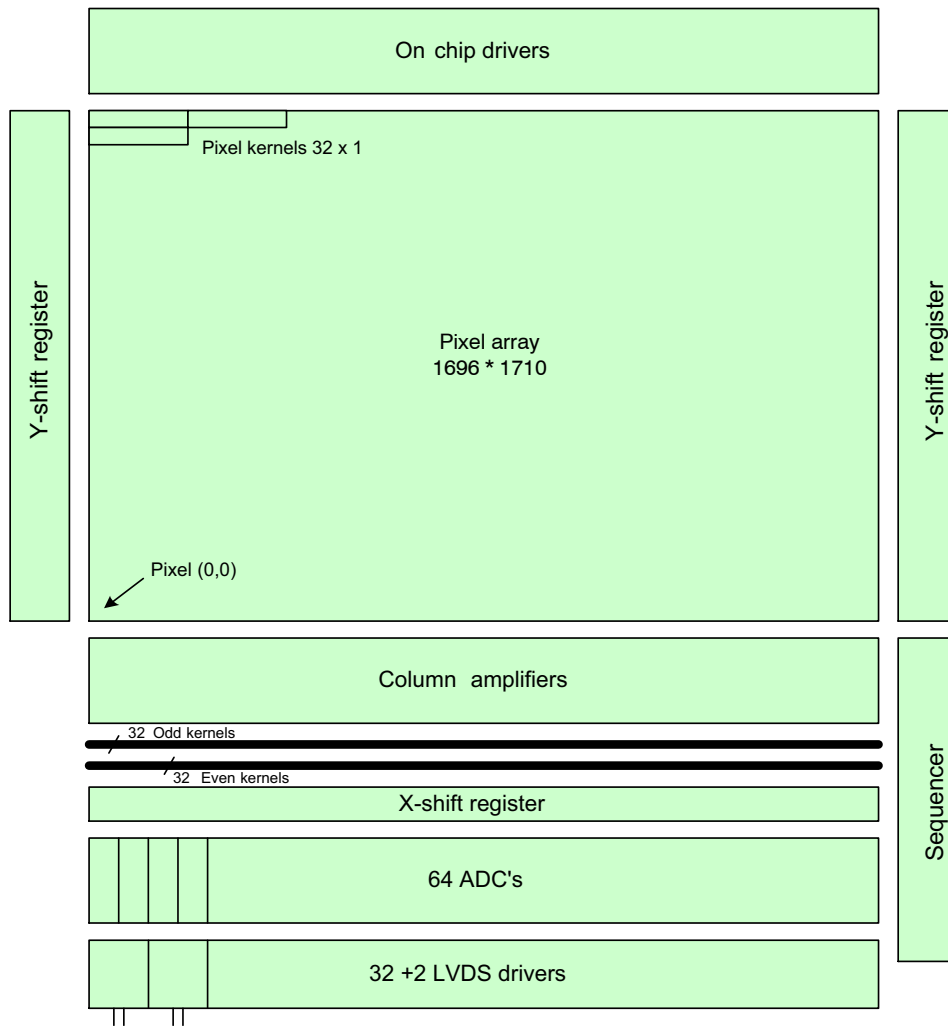


Figure 6. Sensor Floor Plan

NOIL1SN3000A

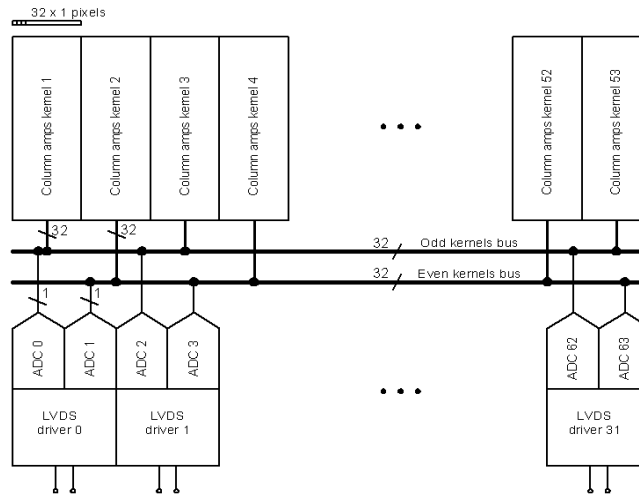


Figure 7. Column Multiplexing Scheme

6T Pixel Architecture

The pixel architecture shown in Figure 8 features the global shutter combined with a high sensitivity and good parasitic light sensitivity (PLS). This pixel architecture is designed in an $8\ \mu\text{m} \times 8\ \mu\text{m}$ pixel pitch and designed with a large fill factor to meet the electro-optical specifications as shown in Table 2 on page 3.

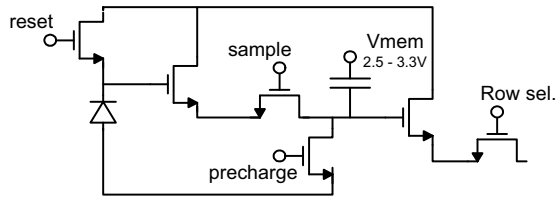


Figure 8. Pixel Schematic

Figure 9 displays the electro-optical response of the LUPA3000 6T pixels at $V_{DD} = 2.5\ \text{V}$.

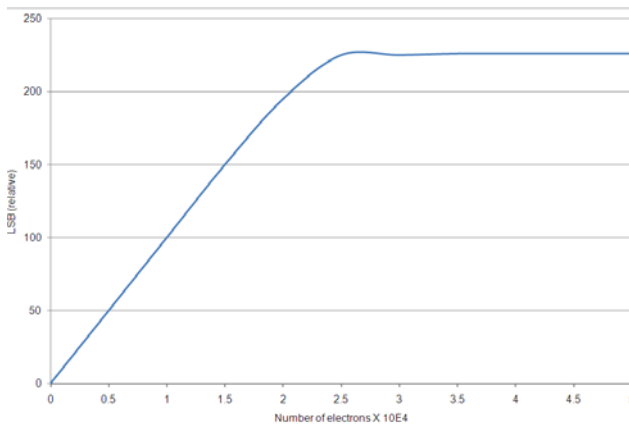


Figure 9. Electro-optical Response of LUPA3000 Pixel

Analog Front End

Programmable Gain Amplifiers(PGA)

LUPA3000 includes analog PGA (before each of the 64 ADCs) to maximize sensor array signal levels to the ADC dynamic range. Six gain settings are available through the SPI register interface to allow 1x, 1.5x, 2x, 2.25x, 3x, or 4x gain.

The entire AFE signal processing and ADC concept for the LUPA3000 chip is shown in Figure 10.

The analog signal processing frontend circuits provide programmable gain level. They also convert the single ended pixel voltage from each column (as referenced to the user programmable black or dark reference level) to a unipolar differential signal for the PGA stages. This is followed by a conversion to a bipolar differential signal to maximize the ADC dynamic range and noise immunity.

NOIL1SN3000A

Overview: HD11 Analog Front-end (Signal Conditioning + Gain) and ADC Concept

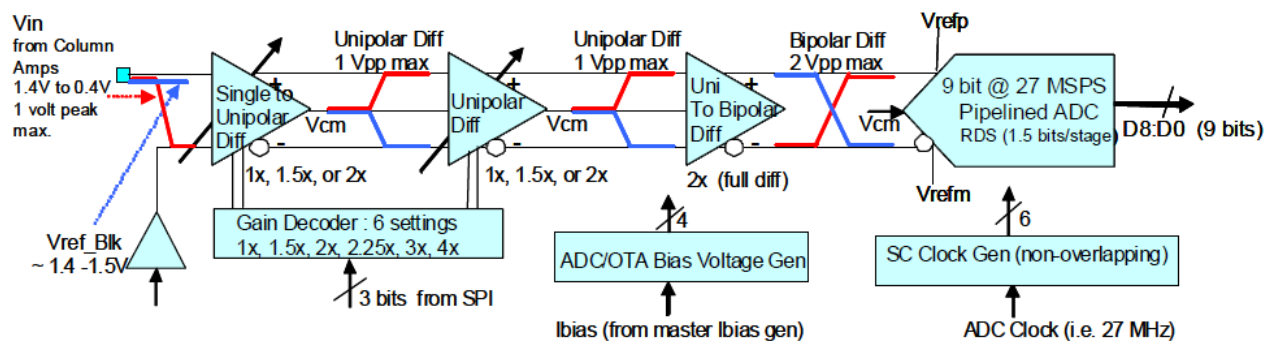


Figure 10. Analog Frontend and ADC Concept

Table 9. PROGRAMMABLE AMPLIFIERS GAIN SETTINGS

| Register Address d73 | | | Gain Level | Comments |
|----------------------|-------|-------|------------|-----------------------------------|
| Bit 2 | Bit 1 | Bit 0 | | |
| 0 | 0 | 0 | 1x | POR default value |
| 0 | 0 | 1 | 1.5x | |
| 0 | 1 | 0 | 2.0x | |
| 0 | 1 | 1 | 2.25x | |
| 1 | 0 | 0 | 3.0x | |
| 1 | 0 | 1 | 4.0x | |
| 1 | 1 | x | 3.0x | Do not use (Redundant gain codes) |

The gain is set through bits 2:0 in register 73 (decimal).

The gain register controls the gain setting globally for all 64 PGA and ADC channels.

A latency (delay) is incurred for the analog signal processing, PGA, and ADC stages. The total latency is 44 high-speed input clock delays. The output synchronization signals from the LVDS sync channel factor in this latency.

Programmable Dark Level

An SPI-controlled DAC provides the PGA with a dark level. This analog voltage corresponds with the all-zero output of the ADC. This dark level is tuned to optimally use the ADC range.

The dark level coming from the pixels follow a Gaussian distribution. This distribution is visible in a dark image as the FPN. The spread on the distribution is influenced by the dark current and temperature. Typically the spread is 100 mV peak-to-peak.

The average dark level of this distribution depends on several parameters:

- The processing corner
- Tolerances on the pixel power supplies (V_{pix} , V_{reset} , V_{mem_l} , and V_{mem_h})
- Pixel timing

The combination of these parameters adds an offset to the dark level. The offset is in the order of magnitude of 200 mV.

To allow off-chip FPN calibration, the full spread on the dark level is mapped inside the range of the ADC. To optimally use the input range of the ADC, the spread on the dark level is mapped as close as possible to the high level of the ADC's input range.

The default startup value of the dark level coming from the DAC is 1.5 V. This ensures that the spread on the dark level is completely mapped in the ADC range. The startup DAC dark level is not optimal. By taking a dark image after startup, the offset on the dark image histogram is measured. The offset from the optimal case is subtracted from the dark level coming from the DAC. This places the dark level distribution optimally inside the range of the ADC. Follow this procedure after every change in operation condition such as temperature, FOT timing, and ROT.

Analog-to-Digital Converters

LUPA3000 includes 64 pipelined 9-bit ADCs operating at approximately 25.75 mega samples per second (MSPS). Two ADCs are combined to provide digitized data to one of the 32 LVDS serialization channels. One of the ADC pair converts data from an 'odd kernel' of the LUPA3000 pixel array, the other from an 'even kernel'. LUPA3000 only processes the eight MSBs of the converter to realize an improved noise performance 8-bit converter.

The ADCs are designed using fully differential circuits to improve performance and noise immunity. In addition, a redundant signed digit (RSD) 1.5 bit per stage architecture with digital error correction is used to improve differential nonlinearity (DNL) and ensure that no codes are missing. Interstage ADC gain errors are addressed using commutation techniques for capacitor matching. Auto-zeroing and other calibration methods are implemented to remove offsets.

References and Programmable Trimming

Bits 6:4 of SPI register 64 (decimal) allow adjustment of the Vrefp-Vrefm differential ADC reference level. Eight settings are provided to enable trimming of the dynamic range. Reduced dynamic range is used to optimize signals in low light intensity, where reduced pixel levels require further gain. Table 10 provides the permitted trim settings.

Table 10. PROGRAMMABLE ADC REFERENCE LEVEL

| Register Address 64 (dec) | | | Vrefp-Vrefm Gain Level (typ) | Comments |
|---------------------------|-------|-------|------------------------------|-------------------------------------|
| Bit 6 | Bit 5 | Bit 4 | | |
| 0 | 0 | 0 | 0.5x | Maximum effective gain +6.0 dB (2x) |
| 0 | 0 | 1 | 0.67x | |
| 0 | 1 | 0 | 0.71x | |
| 0 | 1 | 1 | 0.77x | |
| 1 | 0 | 0 | 0.83x | |
| 1 | 0 | 1 | 0.91x | Available setting to ensure 0 code |
| 1 | 1 | 0 | 0.95x | Available setting to ensure 0 code |
| 1 | 1 | 1 | 1.0 x | POR (startup) default level |

The black voltage level from the pixel array is more positive than the user set Vdark or “black” reference level. This results in a nonzero differential voltage in the PGAs and other AFE stages. This condition prevents obtaining a desired 0 code out of the ADCs. The 0.95x and 0.91x trim settings are specifically supplied to allow minor adjustment to the ADC differential reference (Vrefp-Vrefm) to ensure a zero level code in these conditions.

The additional trim settings are provided as dynamic range adjustments in low light intensities to act as effective global gain settings. The absolute level of gain (from the typical values) is not guaranteed. However, the gain increases are monotonic. Using this method, you can obtain a maximum gain of approximately 2x (+6.0 dB). As a result, the combined gain of both PGAs and the ADC reference trimming available is 8x maximum.

Some reference voltages are overdriven after the on-chip control logic is powered down (refer section On-Chip BandGap Reference and Current Biasing on page 17). Overdriving, a feature intended for testing and debugging, is not recommended for normal operation. The reference voltages that are overdriven are:

- Vrefp - Vrefm (can be overdriven as a pair)
- Vcm
- Vdark
- Internal bandgap voltage

Table 11 summarizes the ADC and AFE (signal processing) parameters.

Each pair of odd and even kernel AFE + ADC channels are individually powered down with its associated LVDS serialization channel. This is controlled through bits in SPI registers 66–70 (decimal). Logic 1 is the power down state. The POR defaults are logic 0 for all channels powered on.

Table 11. AFE AND ADC PARAMETERS

| Parameter | Parameter Value (typical) | Comment |
|---|--|---|
| Input range (single to differential converter; S2D) | 1.5 V to 0.3 V (SE to unipolar differential) | S2D performs inversion. Referenced from Vblack |
| Vblack | 1.2 V to 1.5 V (typical) | Dark or black level reference from SPI programmable DAC. 0.01 μF to gnd |
| Analog PGA gain and settings | 1x to 4x (6 gain settings) | 3-bit SPI programmable. 1x, 1.5x, 2x, 2.25x, 3x, 4x |
| Input range (ADC) | 0.75 V to 1.75 V | 1 V maximum Vrefp-Vrefm (2 Vp-p maximum) |
| ADC type | Pipelined (four ADC clock latency) | With digital error correction (no missing codes) |
| ADC resolution | 8 bits | |
| Sampling rate per ADC | 26.5 MSPS | Maximum 30 MSPS |
| ENOB | 7.5 bits | Effective number of bits |
| Differential nonlinearity (DNL) | ±0.5 LSB | No missing codes |
| Integral nonlinearity (INL) | ±1.0 LSB | |
| Power supply | 2.5 V ±0.25 V | |

Table 11. AFE AND ADC PARAMETERS

| Parameter | Parameter Value (typical) | Comment |
|---|---------------------------|------------------------------------|
| Total AFE + ADC latency | 44 master clocks | 5.5 ADC clocks = 1/8 of master clk |
| Total AFE + ADC power (32 channels = 64 AFE + ADC) | 400 mW (at 2.5 V) | 160 mA |

Protocol Layer

Digital data from the ADCs is reorganized in the protocol layer before it is transferred to the LVDS drivers. Perform these operations in the protocol layer:

- Multiplexing of two ADCs to one output data channel.
- Adding the cyclical redundancy check (CRC) checksum to the data stream. This operation is done row by row. A new CRC checksum is calculated for every new row that is readout.
- Switching readout mode. The LUPA3000 sensor is programmed to operate in two other readout modes: training and test image modes. These modes synchronize the readout circuitry of the end user with the sensor.
- Assembling the data stream of the synchronization channel.

CRC

LUPA3000 implements a CRC for each row (line) of processed data to detect errors during the high speed transmission. CRC provides error detection capability at low cost and overhead.

The CRC polynomial implemented for LUPA3000 is: $x^8+x^6+x^3+x^2+1$.

The CRC result is transmitted with the original data. When the data is received (or recovered), the CRC algorithm is reapplied and the latest result compared to the original result. If a transmission error occurs, a different CRC result is obtained. The system then chooses to operate on the detected error or has the frame resent.

The CRC shift register is initialized with logic 1s at reset to improve bit error detection efficiency.

Referring to Figure 11, the CRC value is calculated for each row and inserted into the serial data stream. Bit 0 of SPI register 71 (decimal) is an enable bit to insert the CRC checksum. CRC is enabled when a logic 1 is written to this bit. This is the default (POR) value. Bit 1 of this register allows calculation and insertion of a CRC checksum to the “synchronization” channel. No checksum is attached by default.

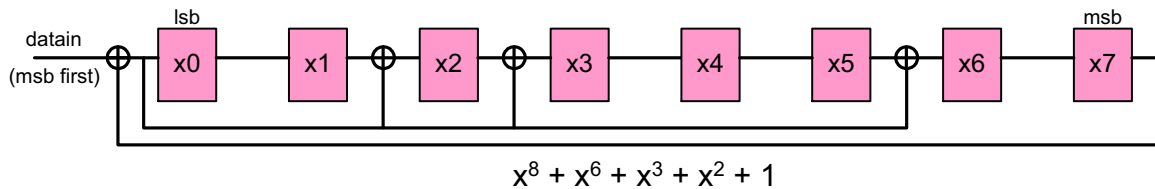


Figure 11. Equivalent Polynomial Representation in Serial Format

Data Block

The data block is positioned in between the AFE (output stage + ADCs) and the LVDS interface. It multiplexes the outputs of two ADCs to one LVDS block and performs some minor data handling:

- Calculate and insert CRC
- Generate training and test pattern

It also contains a huge part of the functionality for black level calibration.

A number of data blocks are placed in parallel to serve all data output channels. One additional channel generates the synchronization protocol. A high level overview is illustrated in Figure 12.

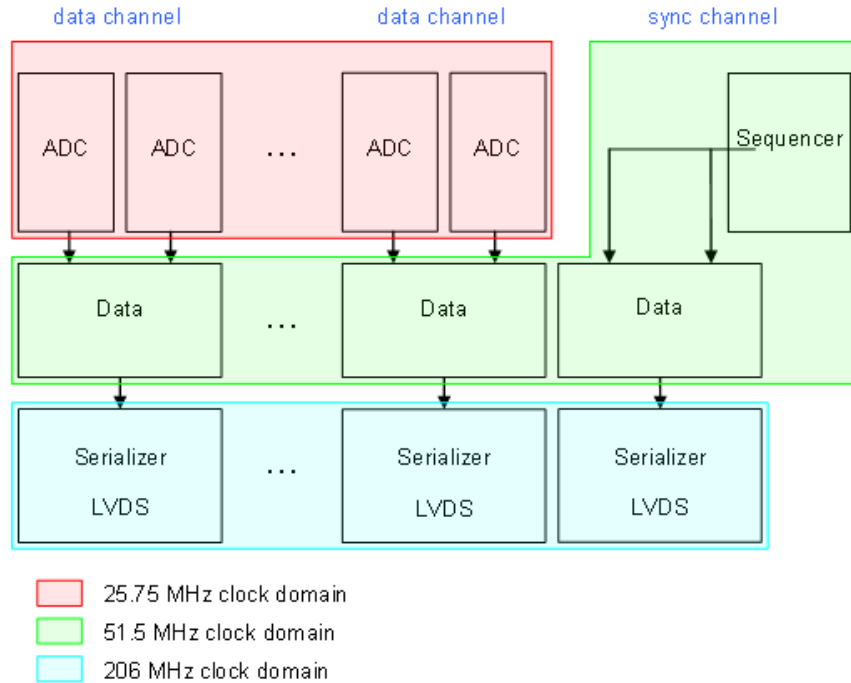


Figure 12. Interaction of the Data Block with ADC and LVDS

LVDS

LUPA3000 uses LVDS I/O. LVDS offers low power and low noise coupling. It also offers low EMI emissions that are essential for the high data readout rates that are required by the LUPA3000 image sensor. LVDS voltage swings range from 250 mV to 450 mV with a typical of 350 mV. Because of the low voltage swings, rise and fall times are reduced, enabling higher operating speeds than CMOS, TTL, or other drivers operating at the same slew rate. It uses a common mode voltage ~1.2 V to 1.25 V above ground, and as a result is more independent of the power supply level and less susceptible to noise. Differential transmission also reduces EMI levels. The 2-pin differential output drives a cable with approximately 100 Ω characteristic impedance, which is ‘far-end’ terminated with 100 Ω.

LVDS Data Channels

LUPA3000 has 32 LVDS data output channels operating at a double data rate (DDR) of 412 Mb per second (typical) using a 206-MHz input clock. The LVDS data channels have a high speed parallel to the serial converter logic function (serializer) that serializes the 52 MSPS 8-bit parallel data from a time multiplexed odd and even kernel ADC pair. The high-speed serial bit stream drives a LVDS output driver.

The LVDS driver must deliver positive or negative current through a 2-pin differential output to represent a logical 1 and logical 0 state respectively. The driver is designed in compliance with the ANSI/TIA/EIA-644-A-2001 standard. The circuit consists of a programmable current sink that defines the drive current, a dynamically controlled current source, a 4-transistor bridge that steers these currents to the differential outputs, and a common mode feedback circuit to balance the sink and source currents.

The LVDS standard defines the drive current between 2.5 mA to 4.5 mA. The termination resistance is specified from 90 Ω to 132 Ω. To allow flexibility in power consumption, the output drive current is programmed through the SPI register interface. Settings are available for operation outside the specified ANSI standard to allow custom settings for power and speed enhancements. These settings may require the use of nonstandard termination resistance. Current drive programming is accomplished using bits 3:0 of SPI register 72 (decimal – LVDS trim). Figure 13 on page 14 defines the programmable LVDS output current settings.

NOIL1SN3000A

| REG 72 <3:0> | IOUT [mA] | RT[Ω] | VOUT [mV] | Comments |
|--------------|-----------|-------|-----------|--------------------------|
| 0000 | 1.26 | 100 | 126 | |
| 0001 | 1.68 | 100 | 168 | Low power range |
| 0010 | 2.1 | 100 | 210 | |
| 0011 | 2.52 | 100 | 252 | |
| 0100 | 2.94 | 100 | 294 | Standard range |
| 0101 | 3.36 | 100 | 336 | |
| 0110 | 3.78 | 100 | 378 | |
| 0111 | 4.2 | 100 | 420 | |
| 1000 | 4.62 | 72.97 | 337 | |
| 1001 | 5.04 | 68.75 | 347 | Extra drive current |
| 1010 | 5.46 | 68.75 | 375 | to accommodate high |
| 1011 | 5.88 | 68.75 | 404 | interconnect capacitance |
| 1100 | 6.3 | 50 | 315 | |
| 1101 | 6.72 | 50 | 336 | |
| 1110 | 7.14 | 50 | 357 | |
| 1111 | 7.56 | 50 | 378 | |

Figure 13. LVDS Driver Programmable Drive Current Settings

LVDS Sync Channel

LUPA3000 includes a LVDS output channel to encode sensor synchronization control words such as start of frame (SOF), start of line (SOL), end of line (EOL), idle words (IdleA and IdleB), and the sensor line address.

This channel includes a serializer logic section, but receives its input directly from the image core sequencer. An additional synchronization control logic block ensures proper data alignment of the synchronization codes to account for the latency incurred in the other 32 data channels (due to AFE and ADC signal processing). The LVDS output driver is similar to that used in other data channel outputs.

LVDS Clk (Clock) Output

The LUPA3000 provides a LVDS clock output channel. This channel provides an output clock that is in phase and aligned with the data bit stream of the 32 data channels. It is required for clock and data recovery by the system processing circuits.

A serializer logic section is connected to accept the differential CMOS serializer clock, after processing through the clock distribution buffer network that provides clocks to all LUPA3000 data channels. The group delay of the output clock and data channels is ~2.5 ns relative to the incoming master clock. The LVDS output driver is similar to that used in other data channel outputs.

LVDS CLK (Clock) Input

LUPA3000 includes a differential LVDS receiver for the master input clock. The input clock rate is typically 206 MHz and also complies with the ANSI LVDS receiver standards. The input clock drives the internal clock generator circuit that produces the required internal clocks for image core and sequencer, AFE and ADCs, CRC insertion logic, and serializers. LUPA3000 requires the

following internal clock domains (all internal clock domains are 2.5 V CMOS levels):

- Serializer clock = 1x differential version of the input clock (206 MHz typical)
- CRC clock = 1/4x the input clock (51.5 MHz typical)
- Load pulse = 1/4 (the input clock) at 12.5% duty cycle version of the input clock: for load and handshake between CRC parallel data to serializer
- ADC and AFE clock = 1/8x the input clock (25.75 MHz typical)
- Sensor clock = 1/4x the input clock (51.5 MHz typical) with programmable delay
- ADC clock = 1/8x the input clock (25.75 MHz typical) with programmable delay

All clock domains are designed with identical clock buffer networks to ensure equal group delays and maintain less than 100 ps maximum channel to channel clock variation.

Programmable delay adjustment is provided for the clock domains of image sensor core and sequencer. This adjustment optimizes the data acquisition handshaking between the image sensor core and the digitization and serialization channels. SPI register 65 (decimal) controls delay (or advance) adjustments for these two clocks. For each of these two imager clocks, 15 adjustments settings are provided. Each setting allows adjustment for 1/(2x master clock) adjustment. For example, if the master input clock runs at 206 MHz, 1/412 MHz = 2.41 ns adjustment resolution is possible. Refer to Sensor Clock Edge Adjust Register (b1000001 / d65) on page 26 for programming details.

ON Semiconductor provides default settings for the programmable delay. These settings allow correct

NOIL1SN3000A

operation; there is no need to change these settings (unless for testing).

LVDS Specifications

The LUPA3000 features a 33 channel LVDS data interface, which enables high data rates at a limited pin count with low power and noise. The LUPA3000 guarantees

412 Mbps transmission over all channels accumulating to an aggregate guaranteed data rate of 13.6 Gbps. The transmission medium can be PCB traces, backplanes, or cables with a characteristic impedance of approximately 100 Ω .

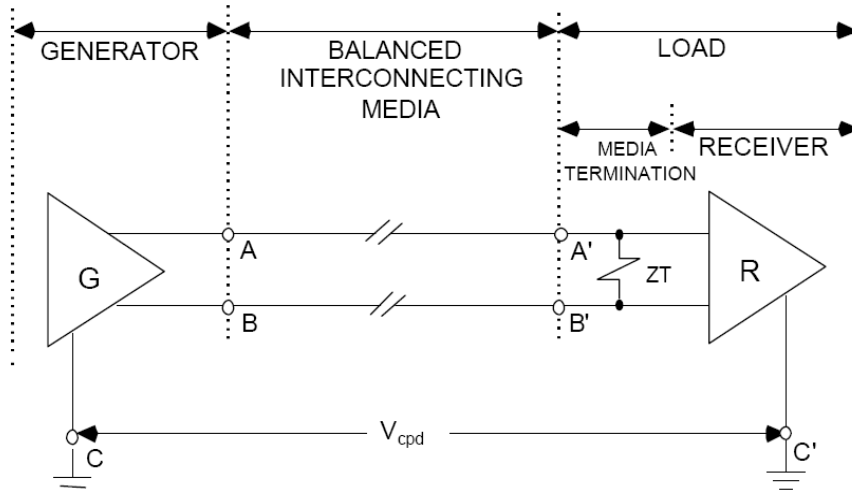


Figure 14. Overview of LVDS Setup

The LUPA3000 accepts an LVDS input clock to generate and synchronize the serial data stream. The clock used to synchronize all the data channels is transmitted over the thirty-fourth channel. This clock signal recovers the data on the receive end without the need for clock recovery. The receiver must feature per channel skew correction to account for on-chip mismatches and intrinsic delays, and also for interconnect medium mismatches.

The LVDS outputs comply to the ANSI/TIA/EIA-644 and IEEE 1596.3 standards. The main specifications are described in the standard. Following the measurement conditions of the standard, the LUPA3000 LVDS drivers feature the specifications listed in Table 12 on page 16.

NOIL1SN3000A

Table 12. LVDS DRIVER SPECIFICATIONS

| Parameter | Description | Specification (guaranteed by design) | | | Units |
|-------------------------|---|--------------------------------------|------|-----------------|------------------|
| | | Min | Typ | Max | |
| $ V_T $ (Note 1) | Differential logic voltage | 247 | 350 | 454 | mV |
| $ V_T(1) - V_T(0) $ | Delta differential voltage | – | – | 50 | mV |
| V_{OS} | Common mode offset | 1.125 | 1.25 | 1.375 | V |
| $d V_{OS} $ | Difference in common mode voltage for logic 1 and 0 | – | – | 50 | mV |
| I_{SA}/I_{SB} | Output currents in short to ground condition | – | – | 24 | mA |
| I_{SAB} | Output current in differential short condition | – | – | 12 | mA |
| t_r, t_f | Differential rise and fall time | 400 | – | 250 | ps |
| $ V_{ring} $ | Differential over and undershoot | – | – | $0.2 \cdot V_T$ | V |
| $d V_{OS} $ | Dynamic common mode offset | – | – | 150 | mV _{PP} |
| Z _T | Termination resistance | 90 | 100 | 132 | Ω |
| ZC(f) | Characteristic impedance of the interconnect | 90 | – | 132 | Ω |
| I_{OFF} | Offstate current | – | – | 10 | μ A |
| t_{SKD1} | Differential skew | – | – | 0.25 | ns |
| t_{SKD2} | Differential channel to channel skew | – | – | 0.5 | ns |
| t_{SKCD1} | Differential clock out to data skew | – | – | 1 | ns |
| t_{SKCD2} | Differential clock in to data skew | – | – | 3 | ns |
| t_{jit_rms} (Note 2) | Random jitter | – | – | 50 | ps |
| t_{jit_det} (Note 3) | Deterministic jitter | – | – | 500 | ps |
| f_{MAX} | Maximum operating frequency | – | – | 206 | MHz |
| f_{MIN} (Note 4) | Minimum operating frequency | 1 | – | – | MHz |

1. The V_{MEM_L} power supply should have a sourcing and sinking current capability.
2. The driver output swing is tuned through the LVDS driver bias current settings in the SPI register. This feature is also used to reduce power consumption. Alternatively, decrease the termination resistor to boost the speed and keep the swing identical by increasing the bias current.
3. Jitter with reference to LUPA3000 input clock
4. This is from LVDS point of view, from sensor point of view f_{MIN} is 4 MHz (about 10 fps). At lower speeds dark current and storage node leakage starts influencing the image quality.

Output trace characteristics affect the performance of the LUPA3000 interface. Use controlled impedance traces to match trace impedance to the transmission medium. The best practice regarding noise coupling and reflections is to run the differential pairs close together. Limit skew due to

receiver end limitations and for reasons of EMI reduction. Matching the differential traces is very important. Common mode and interconnect media specifications are identical to LVDS receiver specifications.

Table 13. LVDS RECEIVER SPECIFICATIONS

| Parameter | Description | Specification (guaranteed by design) | | | Units |
|-----------------------|--------------------------------------|--------------------------------------|-----|-----|----------|
| | | Min | Typ | Max | |
| I_{IA}, I_{IB} | Input current | – | – | 20 | μ A |
| $I_{IA} - I_{IB}$ | Input current unbalance | – | – | 6 | μ A |
| Z _T | Required external termination | 90 | 100 | 132 | Ω |
| $ V_{ID} $ | Differential input | 100 | – | 600 | mV |
| V_{IH}, V_{IL} | Minimum and maximum input voltages | 0 | – | 2.4 | V |
| T _{JIT_TOT} | Total jitter at LUPA3000 clock input | – | – | 500 | ps |

On-Chip BandGap Reference and Current Biasing

For current biasing and voltage reference requirements for the AFEs, ADCs, and LVDS I/O, LUPA3000 includes a bandgap voltage reference that is typically 1.25 V. This reference is used to generate the differential V_{refp} – V_{refm} ADC reference and an analog voltage reference for the LVDS driver I/O.

The bandgap reference voltage also forms a stable current reference for the LVDS drivers and bias currents for all of the analog amplifiers. A Current-Ref_2 pin is included on the package to allow connection of an ~50 K resistor ($\pm 1\%$) to gnd to realize a desired 25 μ A current sourced from the LUPA3000 device. A buffered version of the internal bandgap reference is monitored at this pin.

An optional mode is available to enable an external bandgap regulator. Control bits in SPI register 74 (decimal) allow this feature. Bit 2 is a power-down control bit for the internal bandgap. Setting this bit high along with bit 1 (int_res), and bit 0 (bg_disable), allow driving the Current_Ref_2 pin with an external reference. An internal current reference resistor of 50 K to ground is applied. This mode has reduced current accuracy; $\sim \pm 10\%$ from the external resistor mode ($\pm 1\%$).

Five trimming levels for the internal bandgap voltage are available through bits 2:0 of SPI register 64 (decimal). This

allows minor adjustment in process variations for voltage level and temperature tracking. A POR value is preset so that user adjustment is not required. Each setting adjusts an internal resistor value used to adjust the PTAT (proportional to absolute temperature) “K” factor ratio. Each of the five settings affect the “K” trimming factor by $\sim 1.2\%$. Minor adjustments are made to tune the reference voltage level and temperature tracking rate to compensate for IC processing variations.

The reference generation circuits also form the internal analog common mode voltage for the differential analog circuits. The V_{cm} level is available at a package pin for external decoupling and should be driven by a 0.9 V supply (refer to Table 44 on page 29). The V_{dark} or “black” level reference supplied from an on-chip SPI programmable DAC is also buffered and distributed on-chip as input to each of the 64 AFE and ADC channels. This signal is also available at a package pin for external decoupling. Separate power down control bits are available for the differential ADC reference (V_{refp} – V_{refm}), V_{cm} , and V_{dark} . When any of these are powered down, external references are driven on the external package pins. Table 14 overviews primary parameters for the references and biases.

Table 14. REFERENCE AND BIAS PARAMETERS

| Parameter | Parameter Value (Typical) | Comment |
|------------------------------|---|--|
| V_{refp} | 1.7 V to 1.75 V | At $V_{DD} = 2.5$ V. Requires 0.01 μ F to gnd. |
| V_{refm} | 0.8 V to 0.75 V | At $V_{DD} = 2.5$ V. Requires 0.01 μ F to gnd. |
| V_{refp} – V_{refm} | 0.95 V to 1.0 V (difference) | ADC range. 3-bit SPI trim settings 1x, 0.95x, 0.91x, 0.83x, 0.77x, 0.71x, 0.67x, 0.5x. |
| V_{cm} | 0.9 V | External power supply voltage. Requires 10 nF to gnd. Refer to Table 44 on page 29. |
| Current_Ref_2 | 1.25 V \pm 0.1 V at 25 μ A to gnd | Must pull down to gnd with ~ 50 k Ω . |
| Bandgap reference (internal) | 1.25 V \pm 0.05 V at 2.5 V, T = 40°C | Typical < 50 PPM. Level and tracking are 3-bit SPI trimmable. Five settings at $\sim 1.2\%$ adjust per step. |

NOIL1SN3000A

Sequencer and Logic

The sequencer generates the internal timing of the image core based on the SPI settings uploaded. You can control the following settings:

- Window resolution
- FOT and ROT
- Enabling or disabling reduced ROT mode
- Readout modes (training, test image, and normal)

Table 15. DETAILED DESCRIPTION OF SPI REGISTERS

| Address | Bits | Name | Description |
|---------|-------|--------------------|---|
| 0 | <5:0> | SEQUENCER | |
| | <0> | Power down | Power down analog core |
| | <1> | Reset_n_seq | Reset_n of on chip sequencer |
| | <2> | Red_rot | Enable reduced ROT mode |
| | <3> | Ds_en | Enable DS operation |
| | <5:4> | Sel_pre_width | Width of sel_pre pulse |
| 1 | <4:0> | ROT_TIMER | Length of ROT |
| 2 | <7:0> | PRECHARGE_TIMER | Length of pixel precharge in clk/4 |
| 3 | <7:0> | SAMPLE_TIMER | Length of pixel sample in clk/4 |
| 4 | <7:0> | VMEM_TIMER | Length of pixel vmem in clk/4 |
| 5 | <7:0> | FOT_TIMER | Length of FOT in clk/4 |
| 6 | <5:0> | NB_OF_KERNELS | Number of kernels to readout |
| 7 | <7:0> | Y_START <7:0> | Start pointer Y readout |
| 8 | <2:0> | Y_START <10:8> | |
| 9 | <7:0> | Y_END <7:0> | |
| 10 | <2:0> | Y_END <10:8> | End pointer Y readout |
| 11 | <4:0> | X_START | Start pointer X |
| 12 | <1:0> | TRAINING | |
| | <0> | Training_en | 1: Transmit training pattern; 0: transmit test patterns |
| | <1> | Bypass_en | 1: Evaluate TRAINING_EN bit; 0: ignore TRAINING_EN bit, captured image readout. |
| | <2> | Analog_out_en | Enable analog output |
| 13 | <7:0> | BLACK_REF | ADC black reference |
| 14 | <6:0> | BIAS_COL_LOAD | Biasing of column load |
| 15 | <7:0> | BIASING_CORE_1 | Biasing of image core |
| | <3:0> | Bias_col_amp | Biasing of first column amplifier |
| 16 | <7:4> | Bias_col_outputamp | Biasing of the output column amplifier |
| | <7:0> | BIASING_CORE_2 | Biasing of image core |
| 17 | <3:0> | Bias_sel_pre | Biasing for column precharge structure |
| | <7:4> | Bias_analog_out | Biasing for analog output amplifier |
| 30 | <7:0> | BIASING_CORE_3 | Biasing of image core |
| | <3:0> | Bias_decoder_y | Biasing of y decoder |
| 31 | <7:4> | Bias_decoder_x | Biasing of x decoder |
| | <7:0> | FIXED | Fixed, read only register |
| 31 | <7:0> | CHIP_REV_NB | Chip revision number |

NOIL1SN3000A

Table 15. DETAILED DESCRIPTION OF SPI REGISTERS

| Address | Bits | Name | Description |
|---------|-------|--------------------------|---------------------------------------|
| 32 | <7:0> | SOF | Start of frame keyword |
| 33 | <7:0> | SOL | Start of line keyword |
| 34 | <7:0> | EOL | End of line keyword |
| 35 | <7:0> | IDLE_A | Idle_A keyword |
| 36 | <7:0> | IDLE_B | Idle_B keyword |
| 64 | <6:0> | Voltage reference adjust | |
| | <2:0> | bg_trim | Bandgap voltage adjust |
| | <3> | | Unused reads 0 |
| | <6:4> | vref_trim | Voltage reference adjust |
| 65 | <7:0> | Clock edge delay | |
| | <3:0> | dly_sen | clk/4 edge placement for sequencer |
| | <7:4> | dly_seq | clk/8 edge placement for sequencer |
| 66 | <7:0> | pwd_chan<7:0> | Channel 0-7 power down |
| 67 | <7:0> | pwd_chan<15:8> | Channel 8-15 power down |
| 68 | <7:0> | pwd_chan<23:16> | Channel 16-23 power down |
| 69 | <7:0> | pwd_chan<31:24> | Channel 24-31 power down |
| 70 | <1:0> | pwd_chan<33:32> | Channel clkout and sync power down |
| 71 | <7:0> | Misc1 SuperBlk controls | |
| | <0> | crc_en | Enable CRC for data channels |
| | <1> | crc_sync_en | Enable CRC for sync channel |
| | <2> | pwd_ena | Enable channel power down |
| | <3> | pwd_glob | Global power down (all 32 channels) |
| | <4> | test_en | Serial LVDS test enable |
| | <5> | atst_en | Analog ADC test enable |
| | <6> | sblk_spare1 | Spare |
| | <7> | sblk_spare2 | Spare |
| 72 | <3:0> | LVDS Trim | LVDS output drive adjust |
| 73 | <2:0> | pgagn | Programmable analog gain |
| 74 | <7:0> | Misc2 SuperBlk Controls | |
| | <0> | bg_disable | Disable on-chip bandgap |
| | <1> | int_res | Internal and external resistor select |
| | <2> | pwd_bg | Power down bandgap |
| | <3> | pwd_vdark | Power down dark reference driver |
| | <4> | pwd_vref | Power down voltage references |
| | <5> | pwd_vcm | Power down common mode voltage |
| | <6> | sblk_spare3 | Spare |
| | <7> | sblk_spare4 | Spare |
| 96 | <7:0> | Testpattern 0 | Test pattern for channel 0 |
| 97 | <7:0> | Testpattern 1 | Test pattern for channel 1 |
| 98 | <7:0> | Testpattern 2 | Test pattern for channel 2 |
| 99 | <7:0> | Testpattern 3 | Test pattern for channel 3 |
| 100 | <7:0> | Testpattern 4 | Test pattern for channel 4 |

Table 15. DETAILED DESCRIPTION OF SPI REGISTERS

| Address | Bits | Name | Description |
|---------|-------|----------------|-----------------------------|
| 101 | <7:0> | Testpattern 5 | Test pattern for channel 5 |
| 102 | <7:0> | Testpattern 6 | Test pattern for channel 6 |
| 103 | <7:0> | Testpattern 7 | Test pattern for channel 7 |
| 104 | <7:0> | Testpattern 8 | Test pattern for channel 8 |
| 105 | <7:0> | Testpattern 9 | Test pattern for channel 9 |
| 106 | <7:0> | Testpattern 10 | Test pattern for channel 10 |
| 107 | <7:0> | Testpattern 11 | Test pattern for channel 11 |
| 108 | <7:0> | Testpattern 12 | Test pattern for channel 12 |
| 109 | <7:0> | Testpattern 13 | Test pattern for channel 13 |
| 110 | <7:0> | Testpattern 14 | Test pattern for channel 14 |
| 111 | <7:0> | Testpattern 15 | Test pattern for channel 15 |
| 112 | <7:0> | Testpattern 16 | Test pattern for channel 16 |
| 113 | <7:0> | Testpattern 17 | Test pattern for channel 17 |
| 114 | <7:0> | Testpattern 18 | Test pattern for channel 18 |
| 115 | <7:0> | Testpattern 19 | Test pattern for channel 19 |
| 116 | <7:0> | Testpattern 20 | Test pattern for channel 20 |
| 117 | <7:0> | Testpattern 21 | Test pattern for channel 21 |
| 118 | <7:0> | Testpattern 22 | Test pattern for channel 22 |
| 119 | <7:0> | Testpattern 23 | Test pattern for channel 23 |
| 120 | <7:0> | Testpattern 24 | Test pattern for channel 24 |
| 121 | <7:0> | Testpattern 25 | Test pattern for channel 25 |
| 122 | <7:0> | Testpattern 26 | Test pattern for channel 26 |
| 123 | <7:0> | Testpattern 27 | Test pattern for channel 27 |
| 124 | <7:0> | Testpattern 28 | Test pattern for channel 28 |
| 125 | <7:0> | Testpattern 29 | Test pattern for channel 29 |
| 126 | <7:0> | Testpattern 30 | Test pattern for channel 30 |
| 127 | <7:0> | Testpattern 31 | Test pattern for channel 31 |

Detailed Description of Internal Registers

All registers are reset to their default value when RESET_N is low. When the chip is not in reset, all registers are written and read through the SPI. The registers are written when the on-chip sequencer is in reset (RESET_N_SEQ bit is low). Resetting the sequencer has no influence on the SPI registers.

Registers are written during normal operation. However, this influences image characteristics such as black level or interrupts readout. To avoid this, change registers at the appropriate moment during operation.

Registers that control the readout and reference voltages are changed during the FOT (when FOT pin is high). Registers that are used for pixel timing are changed outside the FOT (when FOT pin is low). Change SPI registers when the RESET_N_SEQ bit is low.

SPI Registers

Sequencer Register (b0000000 / d0)

The sequencer register controls the power down of the analog core and the different modes of the sequencer. Bits <7:6> are ignored. The sequencer register contains several sub registers.

- **Powerdown, bit <0>**. Setting this bit high brings the image core in power down mode. It shuts down all analog amplifiers.
- **Reset_n_seq, bit <1>**. Bringing this bit low resets the on-chip sequencer. This allows interruption of light integration and readout. Bringing the bit high triggers a new readout and integration cycle in the sequencer.
- **Red_ROT, bit <2>**. Setting this bit activates the reduced ROT mode. This mode allows increasing the frame rate at a possibly reduced dynamic range. The reduction in dynamic range depends on the length of

NOIL1SN3000A

the ROT. See ROT_timer (b0000001 / d1) on page 21. The default timing is in reduced ROT mode, so there is no reduction in dynamic range.

- **Ds_en, bit<3>**. Bit to enable dual slope operation. Enabling this mode allows to enlarge optical dynamic range.

- **Sel_pre_width, bit<5:4>**. Setting these two bits allows changing the width of the sel_pre pulse that is used to precharge all column lines at the start of every ROT. Changing these bits does not change the total ROT length.

Table 16. SEQUENCER REGISTER

| Value | Effect |
|--------------------------------------|---|
| Powerdown, bit <0> | |
| 0 | Normal operation |
| 1 | Image core in power down |
| On startup | 0 |
| Reset_n_seq, bit<1> | |
| 0 | Sequencer kept in reset |
| 1 | Normal operation |
| On startup | 1 |
| Red_ROT, bit<2> | |
| 0 | Long ROT mode |
| 1 | Reduced ROT mode |
| On startup | 1 |
| Ds_en, bit<3> | |
| 0 | Disable dual slope operation |
| 1 | Enable dual slope operation |
| On startup | 0 |
| Sel_pre_width, bit<5:4> | |
| 00 | Sel_pre is 1 sensor clock period long (4 master clocks) |
| 01 | Sel_pre is 2 sensor clock periods long (8 master clocks) |
| 10 | Sel_pre is 3 sensor clock periods long (12 master clocks) |
| 11 | Same effect as '10' setting |
| On startup | 00 |

ROT_timer (b0000001 / d1)

The ROT_timer register controls the length of the ROT. The ROT length, in number of sensor clock periods, is expressed by the formula: ROT length = ROT_timer + 2.

The relation between the row overhead time and the ROT pin is described in the section ROT Pin on page 39. Bits <7:5> are ignored.

Table 17. ROT TIMER REGISTER

| Value Bit<4:0> | Effect |
|----------------|---|
| 00000 | ROT length is 35 sensor clocks, 140 master clocks. |
| xxxxx | ROT length is <N+2> sensor clocks (<N+2>*4 master clocks) where N is the register value |
| On startup | 00111 (9 sensor clocks) |

Precharge_timer (b0000010 / d2)

The precharge_timer register controls the length of the pixel precharge pulse as described in Frame Overhead Time on page 38. The pixel precharge length is expressed in the number of sensor clock periods by the following formula:

$$\text{Pixel precharge length} = \text{precharge_timer} \times 4$$

Table 18. PRECHARGE TIMER REGISTER

| Value | Effect |
|------------|--|
| 00000000 | Pixel precharge length is 1 sensor clock |
| xxxxxxx | Pixel precharge length is <N x 4> sensor clocks (<N x 4> x 4 master clocks), where N is the register value |
| On startup | 00010011 |

Sample_timer (b0000011 / d3)

The sample_timer register controls the length of the pixel sample pulse as described in Frame Overhead Time on page 38. The length of the pixel sample is expressed in the number of sensor clock periods by the following formula:

$$\text{Pixel sample length} = \text{sample_timer} \times 4$$

Sample_timer must be equal to or larger than precharge_timer.

Table 19. SAMPLE TIMER REGISTER

| Value | Effect |
|------------|---|
| 00000000 | Pixel sample length is two sensor clock |
| xxxxxxx | Pixel sample length is <N x 4> sensor clocks (<N x 4> x 4 master clocks), where N is the register value |
| On startup | 00011111 |

Vmem_timer (b0000100 / d4)

The vmem_timer register controls the length of the pixel vmem pulse as described in Frame Overhead Time on page 38. The length of the pixel vmem is expressed in the number of sensor clock periods by the following formula:

$$\text{Pixel vmem length} = \text{vmem_timer} \times 4$$

Vmem_timer must be equal to or larger than sample_timer.

Table 20. VMEM TIMER REGISTER

| Value | Effect |
|------------|---|
| 00000000 | Pixel vmem length is four sensor clock. |
| xxxxxxx | Pixel vmem length is <N x 4> sensor clocks (<N x 4> x 4 master clocks), where N is the register value |
| On startup | 00100010 |

Fot_timer (b0000101 / d5)

The fot_timer register controls the length of the FOT as described in Frame Overhead Time on page 38. The length of the FOT is expressed in the number of sensor clock periods by the following formula:

$$\text{FOT length} = \text{fot_timer} \times 4 + 2$$

The relation between the frame overhead time and the FOT pin is described in FOT Pin on page 39. Fot_timer must be larger than vmem_timer.

Table 21. FOT_TIMER REGISTER

| Value | Effect |
|------------|--|
| 00000000 | Invalid setting |
| xxxxxxx | FOT length is <N x 4 + 2> sensor clocks (<N x 4 + 2> x 4 master clocks), where N is the register value |
| On startup | 00101000 |

Nb_of_kernels (b0000110 / d6)

This register controls the window size in X. The value of the register determines the number of pixel kernels that is readout every line. The maximum number of kernels to readout is 53. The minimum number of kernels to readout is four.

Bits <7:6> are ignored.

Table 22. NB_OF_KERNELS REGISTER

| Value Bit<5:0> | Effect |
|----------------|--------------------------------|
| 000100 | Window size in X is 4 kernels |
| 000101 | Window size in X is 5 kernels |
| ... | |
| 110101 | Window size in X is 53 kernels |
| On startup | 110101 |

Y_start (b0000111 / d7 and b0001000 / d8)

The Y_start register contains the row address of the Y start pointer. Because a row address is 11-bit wide, the Y_start address is split over two registers: Y_start<10:8> and Y_start<7:0>. Y_start<10:8> contains 3 MSBs of the 11-bit address, and Y_start<7:0> contains 8 LSBs of the address. Y_start<10:0> must not be larger than 1709.

Table 23. Y_START REGISTER

| Value Bit<2:0> | Effect |
|---|----------|
| Y_start<7:0> (b0000111 / d7) | |
| On startup | 00000000 |
| Y_start<10:8> (b0001000 / d8): Bits<7:3> are ignored | |
| On startup | 00000000 |

NOI1SN3000A

Y_end (b0001001 / d9 and b0001010 / d10)

The *Y_end* register contains the row address of the last row to readout. Because a row address is 11-bit wide, the *Y_end* address is split over two registers: *Y_end*<10:8> and *Y_end*<7:0>. *Y_end*<10:8> contains 3 MSBs of the 11-bit address, and *Y_end*<7:0> contains 8 LSBs of the address. *Y_end*<10:0> must be larger than *Y_start*<10:0> and not larger than 1709.

Table 24. Y_END REGISTER

| Value Bit<2:0> | Effect |
|--|----------|
| Y_end<7:0> (b0001001 / d9) | |
| On startup | 10101101 |
| Y_end<10:8> (b0001010 / d10): Bits<7:3> are ignored | |
| On startup | 00000110 |

X_start (b0001011 / d11)

The *X_start* register contains the start position for the X readout. Readout in X starts only at odd kernel positions. As a result, possible start positions are 64 columns (2 kernels) separated from each other.

Bits <7:5> are ignored.

Table 25. X_START REGISTER

| Value Bit<4:0> | Effect |
|----------------|--|
| 00000 | X readout starts with the first kernel (column 0) |
| 00001 | X readout starts with the third kernel (column 64) |
| 11010 | X readout starts with the fifty third kernel (column 1664) |
| On startup | 00000 |

Training (b0001100 / d12)

This register allows switching between different readout modes. Bits <7:2> are ignored.

- **Training_en, bit<0>**. In bypass mode, this bit is evaluated and determines if the training pattern or test image is transmitted.
- **Bypass_mode, bit<1>**. This bit allows the sensor to switch between normal readout of an image and readout for testing or training purposes.
- **Analog_out_en, bit<2>**. This bit activates the analog output of the sensor. The analog value of column<1696> is brought to the output.

Table 26. TRAINING REGISTER

| Value | Effect |
|------------------------------------|--|
| Training_en, bit<0> | |
| 1 | In bypass mode, the training pattern is transmitted |
| 0 | In bypass mode, the test image is transmitted |
| On startup | 0 |
| Bypass_mode, bit<1> | |
| 0 | Normal readout of captured images |
| 1 | Bypass mode readout. The content of register TRAINING_EN is evaluated. |
| On startup | 0 |
| Analog_out_en, bit<2> | |
| 0 | Analog output disabled |
| 1 | Analog output enabled |
| On startup | 0 |

Black_ref (b0001101 / d13)

This register controls the DAC that sets the dark level for the ADC. The analog output of the DAC corresponds with the all zero code of the ADC. The DAC has an 8-bit resolution and outputs between VAA2V5 and 0 V. This means that the step size corresponds with about 9.8 mV. The DAC itself outputs between VAA2V5 and 0 V, but the buffering circuit that follows after the DAC clips the voltage close to ground and supply.

Table 27. BLACK_REF REGISTER

| Value | Effect |
|------------|--------------------------------|
| 00000000 | Output of DAC is VAA2V5 |
| 00000001 | Output of DAC is VAA2V5–9.8 mV |
| ... | |
| 11111111 | Output of DAC is 0 V |
| On startup | 01100110 |

NOIL1SN3000A

Bias_col_load (b0001110 / d14)

This register controls the biasing current of the column load. A higher biasing current has the following effects:

- Faster settling on the pixel columns
- Increased power consumption from V_{pix} .
- Lower dark level

Bias current changes 1.56 μA per LSB. Bits <7:6> are ignored.

Table 28. BIAS_COL_LOAD REGISTER

| Value (Bit<5:0>) | Effect |
|------------------|------------------------------|
| 000000 | Bias current is 0 A |
| ... | |
| 111111 | Maximum bias current |
| On startup | 001000 (13.6 μA) |

Biasing_1 (b0001111 / d15)

- **Bias_col_amp, bits<3:0>**. This register controls the biasing current of the first column amplifier. The register value must not be changed.
- **Bias_col_outputamp, bits<7:4>**. This register controls the biasing current of the output column amplifier. The register value must not be changed.

Table 29. BIASING_1 REGISTER

| Value | Effect |
|--|---------------------------|
| Bias_col_amp, bits<3:0> | |
| 0000 | Bias current is 0 A |
| ... | |
| 1111 | Maximum bias current |
| On startup | 0111 (0.4 μA) |
| Bias_col_outputamp, bits<7:4> | |
| 0000 | Bias current is 0 A |
| ... | |
| 1111 | Maximum bias current |
| On startup | 0111 (6.5 μA) |

Biasing_2 (b0010000 / d16)

- **Bias_sel_pre, bits<3:0>**. This register controls the biasing current of the column precharge structure. The register value must not be changed. Bias current changes 57 μA per LSB.
- **Bias_analog_out, bits<7:4>**. This register controls the biasing current of the last stage of the analog amplifier. The register value must not be changed.

Table 30. BIASING_2 REGISTER

| Value | Effect |
|---|-----------------------------|
| Bias_sel_pre, bits<3:0> | |
| 0000 | Bias current is 0 A |
| ... | |
| 1111 | Maximum bias current |
| On startup | 0111 (~ 500 μA) |
| Bias_analog_out, bits<7:4> | |
| 0000 | Bias current is 0 A |
| ... | |
| 1111 | Maximum bias current |
| On startup | 0111 |

Biasing_3 (b0010001 / d17)

- **Bias_decoder_y, bits<3:0>**. This register controls the biasing current of the y decoder. The register value must not be changed.
- **Bias_decoder_x, bits<7:4>**. This register controls the biasing current of the last stage of the analog amplifier. The register value must not be changed.

Table 31. BIASING_3 REGISTER

| Value | Effect |
|--|----------------------|
| Bias_decoder_y, bits<3:0> | |
| 0000 | Bias current is 0 A |
| ... | |
| 1111 | Maximum bias current |
| On startup | 0111 |
| Bias_decoder_x, bits<7:4> | |
| 0000 | Bias current is 0 A |
| ... | |
| 1111 | Maximum bias current |
| On startup | 0111 |

NOIL1SN3000A

Fixed (b0011110 / d30)

This register is read only and always returns 11000100.

Table 32. FIXED REGISTER

| Value | Effect |
|------------|----------|
| On startup | 11000100 |

Chip_rev_nb (b0011111 / d31)

This register contains the revision number of the chip. It is a read only register and a write operation does not have any effect.

The revision number is not guaranteed to represent all mask changes. Some mask changes do not allow to change the revision number.

Table 33. CHIP_REV_NB REGISTER

| Value | Effect |
|------------|-------------------------|
| 00000001 | Rev. A |
| 00000010 | Rev. B |
| ... | |
| On startup | Current revision number |

SOF (b0100000 / d32)

This register contains the SOF keyword.

Table 34. SOF REGISTER

| Value | Effect |
|------------|----------|
| On startup | 00100000 |

SOL (b0100001 / d33)

This register contains the SOL keyword.

Table 35. SOL REGISTER

| Value | Effect |
|------------|----------|
| On startup | 00100010 |

EOL (b0100010 / d34)

This register contains the EOL keyword.

Table 36. EOL REGISTER

| Value | Effect |
|------------|----------|
| On startup | 00100011 |

Idle_A (b0100011 / d35)

This register contains the idle A keyword.

Table 37. IDLE_A REGISTER

| Value | Effect |
|------------|----------|
| On startup | 11101011 |

Idle_B (b0100100 / d36)

This register contains the idle B keyword.

Table 38. IDLE_B REGISTER

| Value | Effect |
|------------|----------|
| On startup | 11101011 |

Reference Voltage Adjust Register (b1000000 / d64)

The reference voltage adjust register allows trimming of the bandgap and vref levels. Bits <7> and <3> are ignored.

- **bg_trim**, bits <2:0>: Setting these bits adjusts the bandgap voltage by selecting the value for the on-chip resistor R2. This resistor trims the PTAT “K” factor. See On-Chip BandGap Reference and Current Biasing on page 17
- **vref_trim**, bits <6:4>: Setting these bits adjusts the reference voltage range (vrefp-vrefm) for the ADCs.

Table 39. REFERENCE VOLTAGE ADJUST REGISTER

| Value | Effect |
|------------------------------------|--------------------------------|
| bg_trim, bits <2:0> | |
| 000 | R2= 82.5K |
| 001 | R2= 83.5K |
| 010 | R2= 84.5K Vbg 1.25 Vnominal |
| 011 | R2= 85.5K |
| 1xx | R2= 86.5K |
| On startup | 010 |
| vref_trim, bits <6:4> | |
| 000 | 0.50x |
| 001 | 0.67x |
| 010 | 0.71x |
| 011 | 0.77x |
| 100 | 0.83x |
| 101 | 0.91x |
| 110 | 0.95x |
| 111 | 1.00x nominal |
| On startup | 111 |

NOIL1SN3000A

Sensor Clock Edge Adjust Register (b1000001 / d65)

The sensor clock edge adjust register allows programmable delay between the column readout and the ADC capture clock edges. The relationship is programmed to align to ± 7 edges of the input high-speed clock (input lvds

clock or CLK_SER). Figure 15 shows this relationship between the input clock and all the derived on-chip clocks. Some examples of programmed delay values for both CLK_SEN and CLK_SEQ are also shown.

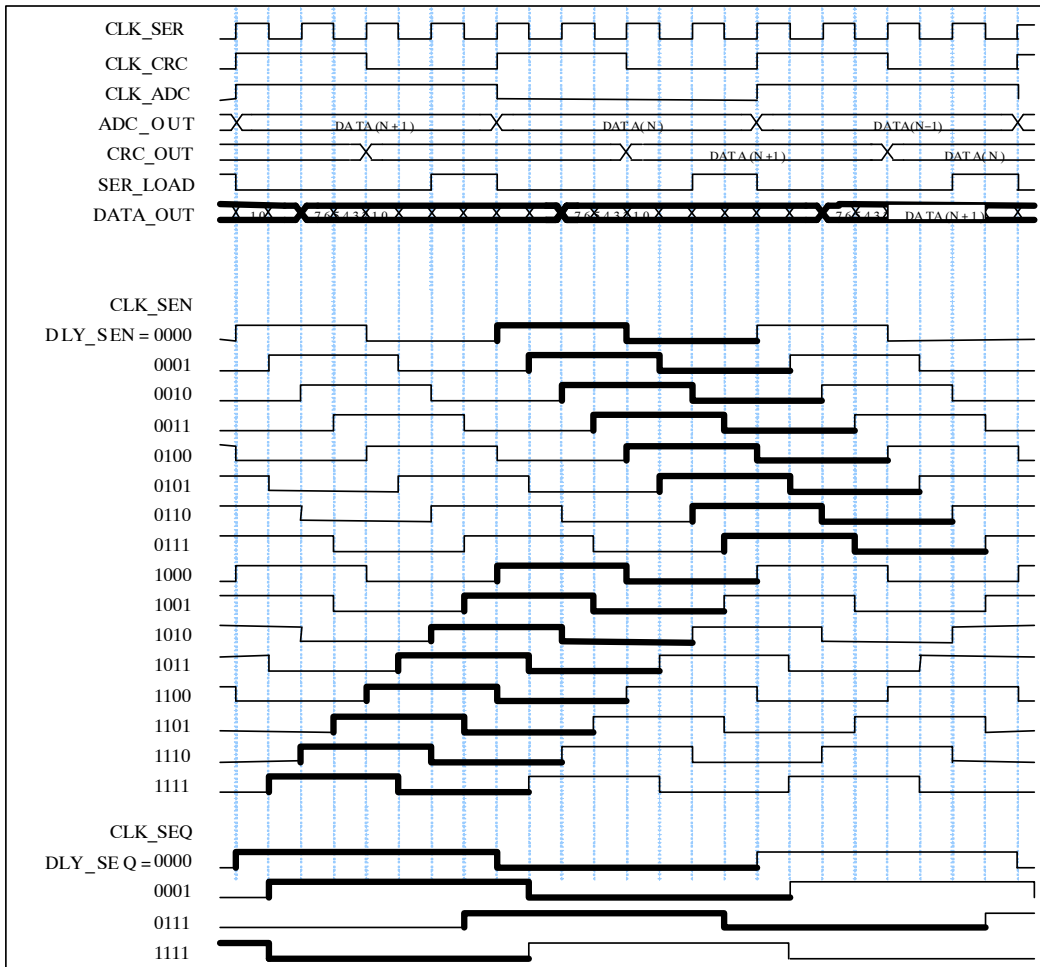


Figure 15. LUPA3000 Internal Clocking

NOIL1SN3000A

dly_sen, bits <3:0>

These bits allow adjusting the rising edge of the sensor clock (CLK_SEN, clk/4) position, with respect to the high speed input clock (clk) and the falling edge of the ADC sample clock (ADC_CLK, clk/8).

Table 40. DLY_SEN BITS

| Value | Effect |
|------------|--|
| 0000 | Rising edge of CLK_SEN coincident with falling edge of CLK_ADC |
| 0001 | CLK_SEN is +1 clk edge after falling edge of CLK_ADC |
| 0010 | +2 |
| 0011 | +3 |
| 0100 | +4 |
| 0101 | +5 |
| 0110 | +6 |
| 0111 | +7 |
| 1000 | Same as code 0000 |
| 1001 | CLK_SEN is -1 clk edge before falling edge of CLK_ADC same as 0111 |
| 1010 | -2 same as 0110 |
| 1011 | -3 same as 1010 |
| 1100 | -4 same as 0100 |
| 1101 | -5 same as 0011 |
| 1110 | -6 same as 0010 |
| 1111 | -7 same as 0001 |
| On startup | 0000 |

dly_seq, bits <7:4>

These bits allow adjusting the falling edge of the sensor odd/even select (CLK_SEQ, clk/8) position, with respect to the high speed input clock (clk) and the falling edge of the ADC sample clock (ADC_CLK, clk/8).

Table 41. DLY_SEQ BITS

| Value | Effect |
|------------|---|
| 0000 | Falling edge of CLK_SEQ coincident with falling edge of CLK_ADC |
| 0001 | CLK_SEQ is +1 clk edge after falling edge of CLK_ADC |
| 0010 | +2 |
| 0011 | +3 |
| 0100 | +4 |
| 0101 | +5 |
| 0110 | +6 |
| 0111 | +7 |
| 1000 | Same as code 0000 |
| 1001 | CLK_SEQ is -1 clk edge before falling edge of CLK_ADC |
| 1010 | -2 |
| 1011 | -3 |
| 1100 | -4 |
| 1101 | -5 |
| 1110 | -6 |
| 1111 | -7 |
| On startup | 1100 |

ADC and LVDS Channel Powerdown Registers (b1000010-1000110 / d66-70)

Each of the 32 data channels, sync, and clock out LVDS channels are individually powered down by setting the appropriate bits of these registers. Powering down a channel stops the clock for the odd and even ADCs and LVDS serializer, and turns off the LVDS output driver. Note that the enable `pwd_ena` in register d71 is set for these bits to take affect. Bits 31:0 are used for data channels 31:0 respectively. Setting bit 33 powers down the output clock channel; bit 32 powers down the sync channel. Setting a particular bit high brings the selected channel to its power down mode.

Table 42. PWD_CHAN<33:0>

| Value bit<x> | Effect |
|--------------|----------------------|
| 0 | Normal operation |
| 1 | Channel powered down |
| On startup | 0 |

Misc1 SuperBlk Control Register (b1000111 / d71)

The misc1 superblk control register contains several control and test enable bits. The superblk refers to the AFE, ADC, CRC, Serialization, and LVDS channels and supporting controls.

- **crc_en, bit <0>**. This bit enables inserting CRC words into the data channels at the end of a row of image data. Protocol Layer on page 12 contains more details on this protocol.
- **crc_sync_en, bit<1>**: This bit enables inserting CRC words into the sync channel. This is generally not desired.
- **pwd_ena, bit<2>**. This bit provides the ability to power down individual channels through the `pwd_chan` registers.
- **pwd_glob, bit<3>**. This bit, when set, globally powers down all 32 data channels, the sync channel, and the clock out channel. This overrides the per channel power down controls.
- **test_en, bit<4>**. This bit is provided to test the serial LVDS output drivers. When set, the LVDS output clock is routed to all output data channels. This is intended for debug and testing only.
- **atst_en, bit<5>**. This bit enables driving an external analog input voltage to the 64 ADCs for testing. When set, the external pin `Analog_in` and `Vdark` reference are sent to all ADCs.
- **sblk_spare1, bit<6>**. This bit is a spare control bit. It is set to 0 at POR.
- **sblk_spare2, bit<7>**:. This bit is a spare control bit. It is set to 1 at POR.

Table 43. MISC1 SUPERBLK CONTROL REGISTER

| Value | Effect |
|----------------------------------|---|
| crc_en, bit <0> | |
| 0 | No CRC words inserted |
| 1 | CRC words inserted into the data stream Normal operation |
| On startup | 1 |
| crc_sync_en, bit<1> | |
| 0 | No CRC words inserted Normal operation |
| 1 | Crc words inserted into the sync channel |
| On startup | 0 |
| pwd_ena, bit<2> | |
| 0 | Per channel power down disabled Normal operation |
| 1 | Enable per channel power down |
| On startup | 0 |
| pwd_glob, bit<3> | |
| 0 | Normal operation |
| 1 | Power down all channels |
| On startup | 0 |
| test_en, bit<4> | |
| 0 | Normal operation |
| 1 | Test Mode |
| On startup | 0 |
| atst_en, bit<5> | |
| 0 | Normal operation |
| 1 | ADC analog test mode |
| On startup | 0 |
| sblk_spare1, bit<6> | |
| 0 | Normal operation |
| 1 | |
| On startup | 0 |
| sblk_spare2, bit<7> | |
| 0 | |
| 1 | Normal operation |
| On startup | 1 |

LVDS Output Current Adjust Register (b1001000 / d72)

The LVDS output drive current is adjusted with this control register. The startup value is b0110 that represents 3.76 mA, reflecting the typical LVDS operating point. There are 16 programmable values available. For more information, see the section LVDS Data Channels on page 13.

Programmable Gain Register (b1001001 / d73)

The amount of analog gain (in the AFE) is adjusted from 1x–4x in eight steps. This is used with the vref_trim register to match the ADC dynamic range to the pixel voltage range. The startup value for this register is b000, which corresponds to a unity gain (1x). See Programmable Gain Amplifiers (PGA) on page 9 for information on the control bit to gain setting table relationship.

Misc2 SuperBlk Control Register (b1001010 / d74)

The misc2 superblk control register contains additional analog bias and reference controls. The bits are defined in this section.

- **bg_disable, bit <0>**: This bit is provided if the on-chip bandgap needs to be disabled.
- **int_res, bit<1>**: This bit controls whether an on-chip or external resistor is used in setting the bandgap voltage.
- **pwd_bg, bit<2>**: This bit is provided to power down the bandgap. It is intended for test and debug only.
- **pwd_vdark, bit<3>**: This bit is provided to power down the driver for the dark reference voltage. It is intended for test and debug only.
- **pwd_vref, bit<4>**: This bit is provided to power down the voltage references, vrefp and vrefm. It is intended for test and debug only.
- **pwd_vcm, bit<5>**: This bit is fixed to ‘1’. See Table 44.
- **sblk_spare3, bit<6>**: This bit is a spare control bit. It is set to ‘0’ at POR.
- **sblk_spare4, bit<7>**: This bit is a spare control bit. It is set to ‘1’ at POR.

Table 44. MISC2 SUPERBLK CONTROL REGISTER

| Value | Effect |
|----------------------------------|--|
| bg_disable, bit <0> | |
| 0 | On-chip bandgap enabled Normal operation |
| 1 | On-chip bandgap disabled |
| On startup | 0 |
| int_res, bit<1> | |
| 0 | External resistor used in Normal operation |
| 1 | On-chip resistor used |
| On startup | 0 |
| pwd_bg, bit<2> | |
| 0 | Normal operation |
| 1 | Bandgap powered down |
| On startup | 0 |
| pwd_vdark, bit<3> | |
| 0 | Normal operation |
| 1 | Power down vdark buffer |
| On startup | 0 |
| pwd_vref, bit<4> | |
| 0 | Normal operation |
| 1 | Power down vrefp/vrefm references |
| On startup | 0 |
| pwd_vcm, bit<5> | |
| 1 | Disable on-chip VCM generation. Apply 0.9 V to Vcm pin 87 and decouple to ground with 10 nF capacitor. |
| On startup | 1 |
| sblk_spare3, bit<6> | |
| 0 | Normal operation |
| 1 | |
| On startup | 0 |
| sblk_spare4, bit<7> | |
| 0 | |
| 1 | Normal operation |
| On startup | 1 |

NOIL1SN3000A

Testpattern 0-31 Registers (b1100000- 1111111 / d96-127)

A register is provided for each of the 32 data channels for LVDS data recovery calibration, alignment, and testing. A unique test pattern is programmed for each data channel and

routed to the LVDS outputs by bypassing the ADCs and disabling the training mode (setting `bypass_en` and clearing `training_en`, both contained in register d11).

Table 45. TEST PATTERN REGISTERS

| Register | Startup Value |
|---------------|---------------|
| Testpattern0 | b00000001 |
| Testpattern1 | b00000001 |
| Testpattern2 | b00000010 |
| Testpattern3 | b00000010 |
| Testpattern4 | b00000100 |
| Testpattern5 | b00000100 |
| Testpattern6 | b00001000 |
| Testpattern7 | b00001000 |
| Testpattern8 | b00010000 |
| Testpattern9 | b00010000 |
| Testpattern10 | b00100000 |
| Testpattern11 | b00100000 |
| Testpattern12 | b01000000 |
| Testpattern13 | b01000000 |
| Testpattern14 | b10000000 |
| Testpattern15 | b10000000 |
| Testpattern16 | b10000000 |
| Testpattern17 | b10000000 |
| Testpattern18 | b01000000 |
| Testpattern19 | b01000000 |
| Testpattern20 | b00100000 |
| Testpattern21 | b00100000 |
| Testpattern22 | b00010000 |
| Testpattern23 | b00010000 |
| Testpattern24 | b00001000 |
| Testpattern25 | b00001000 |
| Testpattern26 | b00000100 |
| Testpattern27 | b00000100 |
| Testpattern28 | b00000010 |
| Testpattern29 | b00000010 |
| Testpattern30 | b00000000 |
| Testpattern31 | b00000000 |

Serial Peripheral Interface (SPI)

The SPI registers have an address space of 7 bits, $a<6>-a<0>$, and 8 data bits, $d<7>-d<0>$. A single instruction bit chooses between a read or write instruction.

The SPI is used only after the clock has started and the chip is not in reset. Otherwise, the SPI register is kept in reset. SPI registers are reset to their default value by bringing RESET_N low. The SPI bit RESET_N_SEQ has no effect on the SPI bits.

Setup and hold requirements of interface signals relative to SPI_CLK are for both requirements 2.5 ns. Output delay is 1.5 ns after falling edge of SPI_CLK. Rise time (10% to 90%) is 9 ns assuming a 18 pF load. To upload SPI, follow this sequence:

Disable sequencer → Upload through SPI → Enable sequencer

Read Sequence, C=0

The part is selected by pulling CS low. The 1-bit instruction (READ) is transmitted to the image sensor, followed by the 7-bit address (A6 through A0). The instruction and address bits are clocked in on the rising edge of the clock. After the correct READ instruction and address are sent, the data stored in the memory at the selected address is shifted out on the MISO pin. The data bits are shifted out on the first falling edge after the last address bit is clocked. The read operation is terminated by raising the CS pin. The maximum operating frequency is 10 MHz.

NOTE: SPI settings cannot be uploaded during readout.

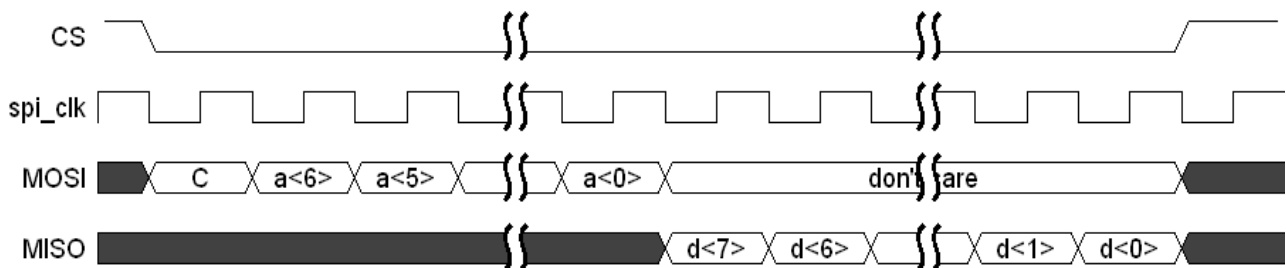


Figure 16. SPI Read Timing

Write Sequence, C=1

The image sensor is selected by pulling CS low. The WRITE instruction is issued, followed by the 7-bit address, and then the 8-bit data. All data is clocked in on the rising edge of the clock.

To write the data to the array, the CS is brought high after the least significant bit (D0) of the data byte is clocked in. If CS is brought high at any other time, the write operation is not completed. Maximum operating frequency is 10 MHz.

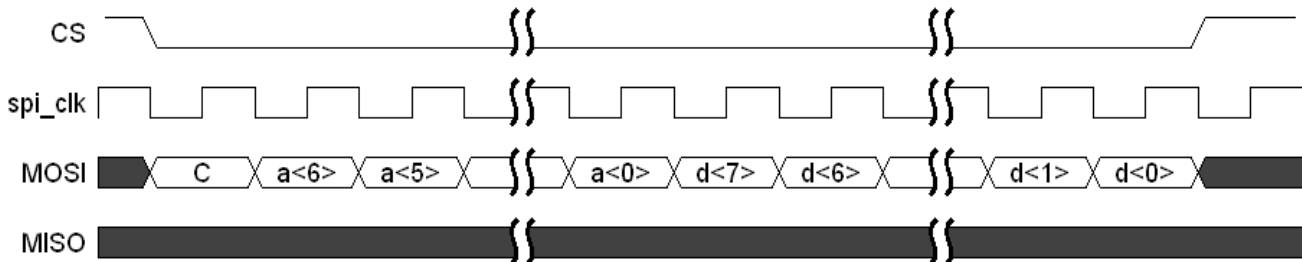


Figure 17. SPI Write Timing

OPERATING MODES

This sensor supports multiple operation modes. The following list provides an overview.

- Global shutter mode
 - ◆ Pipelined global shutter mode
 - Master mode
 - Slave mode
 - ◆ Triggered global shutter mode
 - Master mode
 - Slave mode

Global Shutter Mode

In a global shutter mode, light integration takes place on all pixels in sync, although subsequent readout is sequential as shown in Figure 18. Figure 19 shows the integration and readout sequence for the global shutter. All pixels are light sensitive at the same time. The whole pixel core is reset simultaneously and after the integration time, all pixel values are sampled together on the storage node inside each pixel. The pixel core is read out line by line after integration. Note that the integration and readout can occur in parallel or sequentially. The integration starts at a certain period, relative to the frame start.

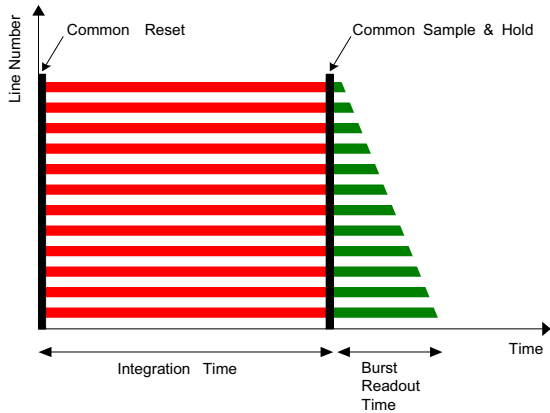


Figure 18. Global Shutter Operation

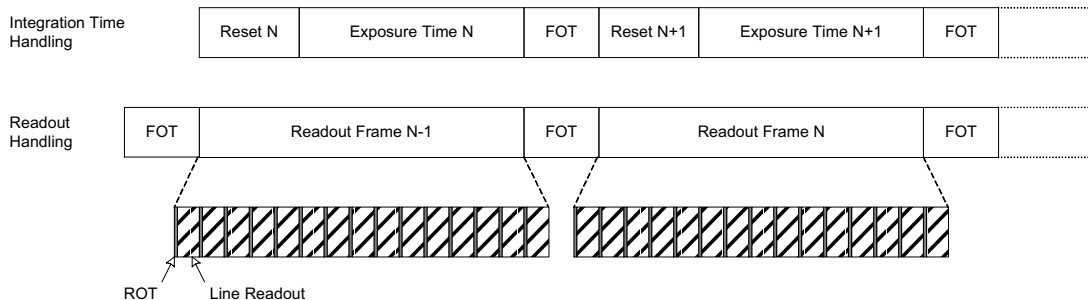


Figure 19. Integration and Readout for Pipelined Shutter

Pipelined Global Shutter Mode

In pipelined shutter mode, the integration and readout are done in parallel. Images are continuously read and integration of frame N is ongoing during readout of the previous frame N-1. The readout of every frame starts with a FOT, during which the analog value on the pixel diode is transferred to the pixel memory element. After the FOT, the sensor is read out line by line and the readout of each line is preceded by the ROT.

Master Mode

In this operation mode, the integration time is set through the register interface and the sensor integrates and reads out the images autonomously. The sensor acquires images without any user interaction.

Slave Mode

The slave mode adds more manual control to the sensor. The integration time registers are ignored in this mode and the integration time is instead controlled by an external pin. As soon as the control pin is asserted, the pixel array goes out of reset and integration starts. The integration continues until the user/system deasserts the external pin. Then the image is sampled and the readout starts.

NOIL1SN3000A

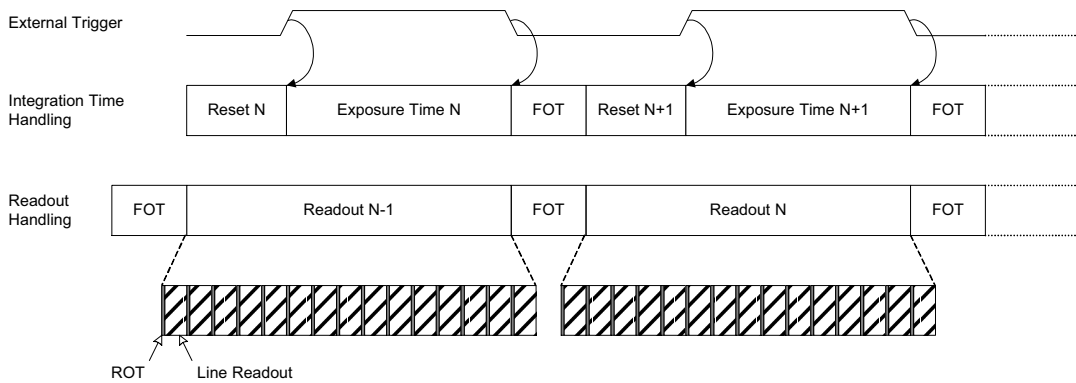


Figure 20. Pipelined Shutter Operated in Slave Mode

Triggered Global Shutter

In this mode, manual intervention is required to control both the integration time and the start of readout. After the integration time, indicated by a user controlled pin, the image core is read out. After this sequence, the sensor goes to an idle mode until a new user action is detected.

The three main differences from the pipelined shutter mode are:

- Upon user action, one single image is read.
- Normally, integration and readout are done sequentially. However, you can control the sensor in such a way that two consecutive batches are overlapping, that is, having concurrent integration and readout.
- You can control integration and readout through an external pin.

This mode requires manual intervention for every frame. The pixel array is kept in reset state until requested.

The triggered global mode can also be controlled in a master or in a slave mode.

Master Mode

As shown in Figure 21, in the master mode, a rising edge on the synchronization pin is used to trigger the start of integration and readout. The integration time is defined by a register setting. The sensor autonomously integrates during this predefined time, after which the FOT starts and the image array is read out sequentially. A falling edge on the synchronization pin does not have any impact on the readout or integration and subsequent frames are started again for each rising edge.

Slave Mode

Integration time control is identical to the pipelined shutter slave mode where both integration time and readout requests are controlled by an external trigger. An external synchronization pin controls the start of integration. The moment it is deasserted, the FOT starts. At this time the analog value on the pixel diode is transferred to the pixel memory element and the image readout can start. A request for a new frame is started when the synchronization pin is asserted again.

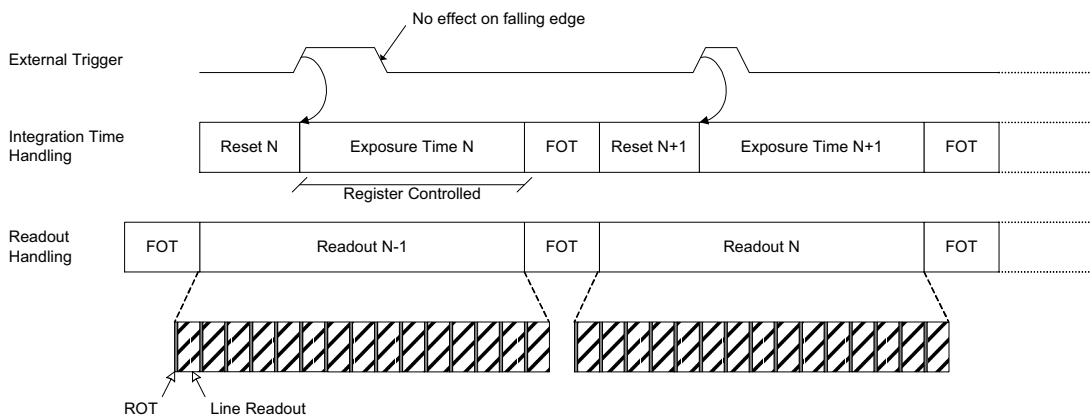


Figure 21. Triggered Shutter Operated in Master Mode

IMAGE SENSOR TIMING AND READOUT

Pixel Timing

After every exposure cycle, the value on the pixel diode is transferred to the pixel storage capacitor. This is controlled by Vmem, precharge, and sample signals. The duration of this operation is the FOT. At the beginning of the FOT, Vmem is brought low, and precharge and sample are brought high. The precharge pulse ensures that the old information on the storage node is destroyed. This ensures there is no image lag. After the falling edge of the precharge pulse, the sampling operation on the storage node is completed during the high level of sample.

After the falling edge of sample, Vmem is brought high. The rise in Vmem compensates for the voltage loss in the last source follower in the pixel. The readout begins after this. The pulse length is controlled by the user. The registers that control this are listed in the following section.

Considerations in Pixel Timing

The length of the FOT_TIMER, PRECHARGE_TIMER, and SAMPLE_TIMER influences the final image quality.

- Precharge pulse: The pixel precharge prevents image lag. A very short pulse results in image lag.
- Sample pulse: A shorter sample results in a reduced dark level.
- FOT_TIMER register: The vmem signal must charge all pixel storage capacitors simultaneously. This is a large combined capacitance (96 nF) and Vmem takes some time to stabilize. Readout must start only after Vmem is stable.

The length of pixel_reset influences image lag. The pixel must be reset for at least 3 μs.

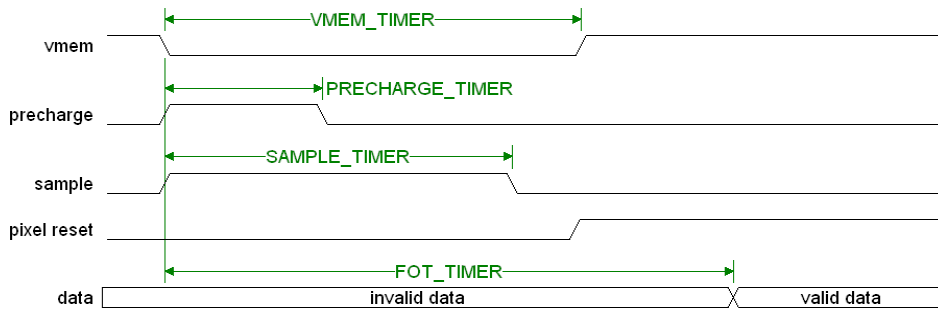


Figure 22. Pixel Timing

Frame Rate and Windowing

Frame Rate

The frame rate depends on the input clock, FOT, and ROT. The frame period is calculated as follows:

1 kernel = 32 pixels

1 granularity clock = 4 clock periods

Frame period = FOT + Nr. lines x (ROT + Nr. pixels/4 x data period)

Or

Frame period = FOT + Nr. lines x (ROT + Nr. kernels * granularity clock cycles)

Example

Readout time for full resolution at nominal speed of 206 MHz (4.854 ns) is given by

Frame period = 3.2 μs + (1710 x (176 ns + 1696/4 x 2.427 ns)) = 2.063 ms

Or

Frame period = 3.2 μs + (1710 x (176 ns + 53 x 19.4174 ns)) = 2.063 ms

Frame Rate = 485 fps

Alternatively, frame rate can also be expressed in terms of reset length and integration time rather than readout time.

Table 46. CLARIFICATION OF FRAME RATE PARAMETERS

| Parameter | Comment | Clarification |
|-------------|--|---|
| FOT | Frame overhead time | The FOT does a frame transfer from pixel diode to pixel storage node. During this transfer, the sensor is not read out. The FOT length is programmable. The default length is 3.2 μs. |
| ROT | Row overhead time | The ROT transfers the pixel output to the column amplifiers. Default ROT is 176 ns. |
| Nr. lines | Number of lines read out in each frame | Default is 1710 lines. |
| Nr. pixels | Number of pixels read out in each line | Default is 1696 pixels. |
| Data period | 0.5 x clock period = 2.427 ns | Because the outputs operate at DDR, the data period is half the clock period (206 MHz clk). |

NOIL1SN3000A

The sequence of events shown in Figure 23 occurs during integration and readout in pipelined global shutter mode.

$$\text{Frame period} = \text{FOT} + \text{Reset length} + \text{Integration time} = t_1 + t_2 + t_3$$

To receive the frames without any overlap, the sum of reset time and integration time should always be greater than the readout time.

$$(\text{Reset time} + \text{Integration time}) > \text{Readout time}$$

In global shutter mode, the whole pixel array is integrated simultaneously. For more information, see ON Semiconductor application note AN57864, *Frame Rate Based on Integration Time*.

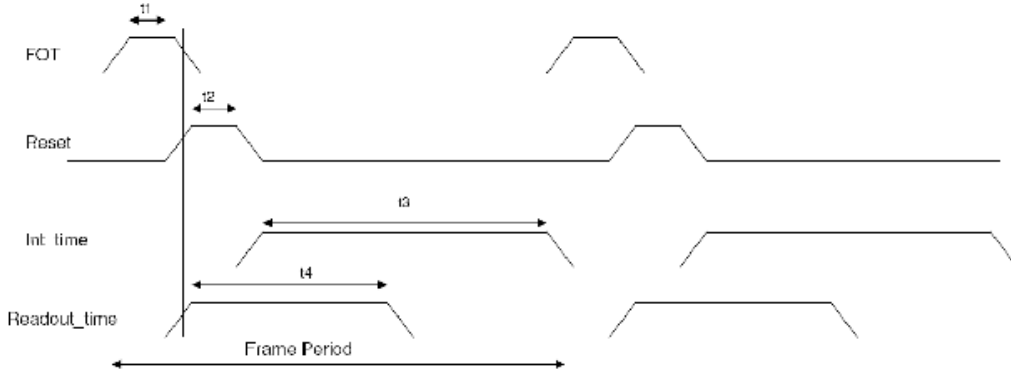


Figure 23. Timing Diagram

Windowing

Windowing is easily achieved by SPI. The starting point of the x and y address and the window size can be uploaded. The minimum step size in the x-direction is 32 pixels (choose only multiples of 32 as a start or stop addresses). The minimum step in the y-direction is 1 line (every line can be addressed in the normal mode).

Table 47. TYPICAL FRAME RATES AT 206 MHz

| Image Resolution (x * y) | Frame Rate (fps) | Frame Period (ms) |
|--------------------------|------------------|-------------------|
| 1696 x 1710 | 485 | 2.065 |
| 1600 x 1200 | 712 | 1.404 |
| 1280 x 1024 | 1001 | 1.000 |
| 640 x 480 | 2653 | 0.377 |
| 512 x 512 | 3808 | 0.263 |
| 256 x 256 | 10704 | 0.093 |
| 128 x 128 | 26178 | 0.038 |

Digital Signals

LUPA3000 can operate in slave mode. To do so, the pixel array of the image sensor requires different digital control signals. The function of each signal is listed in Table 48.

Table 48. OVERVIEW OF DIGITAL SIGNALS

| Signal Name | I/O | Comments |
|-------------|--------|-------------------------------------|
| FOT | Output | Output pin for FOT |
| ROT | Output | Output pin for ROT |
| Exposure_2 | Input | Integration pin dual slope |
| Exposure_1 | Input | Integration pin first slope |
| RESET_N | Input | Sequencer reset, active LOW |
| CLK | Input | System clock (206 MHz) |
| SPI_CS | Input | SPI chip select |
| SPI_CLK | Input | SPI clock |
| SPI_MOSI | Input | Data line of the SPI, serial input |
| SPI_MISO | Output | Data line of the SPI, serial output |

Image Format and Readout Protocol

The active area read out by the sequencer in full frame mode is shown in Figure 24. Pixels are always read in multiples of 32.

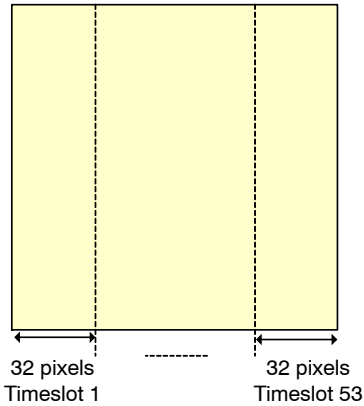


Figure 24. Sensor Read Out Format

Sensor Timing and Readout

High Level Timing

The LUPA3000 sensor is a pipelined synchronous shutter. This indicates that light integration and readout occur in parallel, achieving the high frame rate and data throughput.

The maximum frame rate of the sensor is determined by the time needed to readout a full frame. This frame time is separated in the FOT and the time to readout all lines. The readout of a line is separated in a ROT and the readout of all kernels.

Integration Timing

The integration time is controlled through the EXPOSURE_1 pin. The rising edge of EXPOSURE_1 determines the start of exposure and the falling edge of EXPOSURE_1 starts the FOT and determines the end of the integration time.

The falling edge of the internal pixel reset pulse causes a visible crosstalk in the image, unless the edge occurs in the beginning of the ROT during readout. As a result, the EXPOSURE pulse is internally delayed until the next ROT. The duration of this delay depends on the length of the line being readout. If the EXPOSURE_1 is after Lx is finished, then integration starts immediately. There is no need to wait for ROT.

The internal timing of the FOT is controlled by the sequencer. The length of the FOT is set by the SPI registers PRECHARGE_TIMER, SAMPLE_TIMER, VMEM_TIMER, and FOT_TIMER.

Ensure that pixel_reset is high for at least 3 μs.

FOT Starts After Readout

This is the normal situation where a full window is readout. A full window refers to the resolution set by the Y_START, Y_END, and NB_OF_KERNELS register. This may be the full resolution or a partial window. Figure 26 shows a high level timing; 'Lx' refers to 'line x'.

When EXPOSURE_1 goes low, the FOT begins immediately. Integration time continues until the falling edge of pix_sample. The falling edge of pix_sample is a fixed amount of time after the falling edge of EXPOSURE_1. This time is set SAMPLE_TIMER (see Frame Overhead Time).

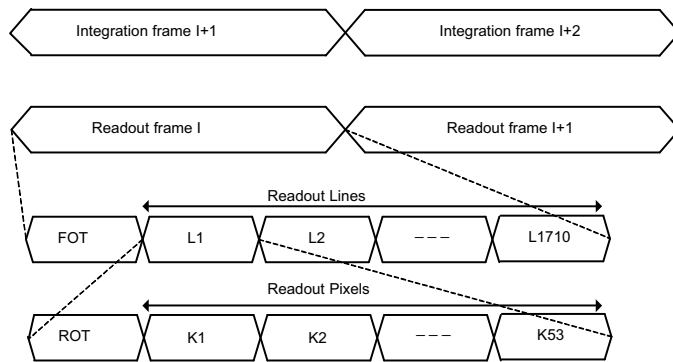


Figure 25. Pipelined Operation

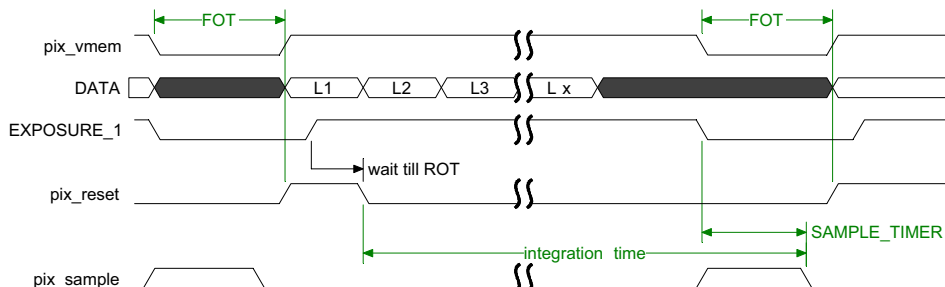


Figure 26. High Level Readout Timing

NOIL1SN3000A

.FOT starts before readout. When the EXPOSURE_1 signal goes low before the window readout has finished, the readout is interrupted after the completion of the current line's readout (line x in Figure 27).

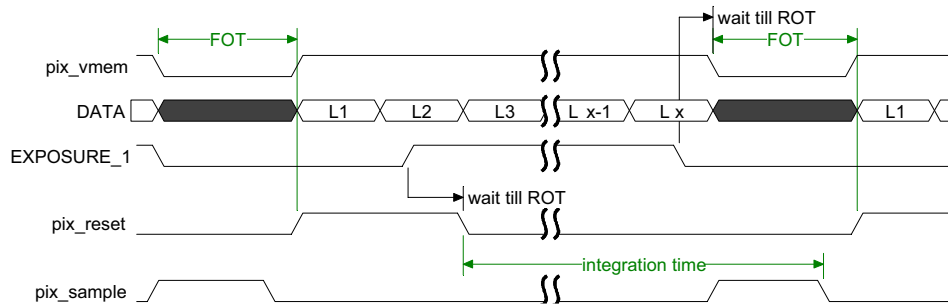


Figure 27. High Level Readout Timing

Dual Slope Integration Timing

If the dual slope enable bit is set high, dual slope integration is controlled through the EXPOSURE_2 pin. If the dual slope enable bit is set low, the dual slope integration is disabled. Figure 28 shows the timing. The pix_reset signal is controlled by the EXPOSURE_1 pin. When pix_reset goes low, the dual slope reset of the pixel array is activated. Bringing the EXPOSURE_2 pin high starts the dual slope integration. The start of FOT is controlled by the falling edge

of the EXPOSURE_1 pin. The EXPOSURE_2 pin must be brought low during FOT to be ready for the next cycle.

Setup and Hold Requirements

EXPOSURE_1 and EXPOSURE_2 are deglitched using two chained flipflops that clock on the sensor clock. As a result, there is no setup requirement for both signals relative to LVDS_CLKIN. The hold requirement is 15 clock periods of LVDS_CLKIN.

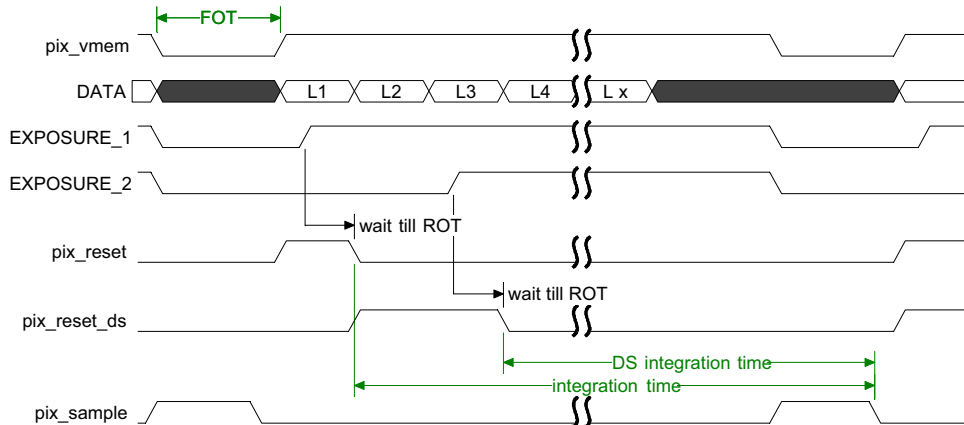


Figure 28. Dual Slope Integration Timing

Readout Modes

The sensor is configured to operate in three readout modes: training, test image readout, and normal readout. These modes enable correct communication between the sensor and the customer system.

Readout of Training Sequence

By setting the TRAINING_EN and BYPASS_MODE bit, all data channels and the sync channel transmit alternating the Idle_A and Idle_B word. Rotating the received Idle_A and Idle_B words in the receiver allows correcting for skew between the LVDS outputs and the receiver clock. You can program the Idle_A and Idle_B words.

Readout of Test Image

By setting the BYPASS_MODE bit high and the TRAINING_EN bit low, the sensor is configured to output a programmable test pattern.

The sync channel operates as in normal readout and enables frame and line synchronization. Every data channel transmits a fixed, programmable word to replace normal data words coming from the ADC. In this mode, the sensor behaves as in normal readout. The sync channel transmits programmable keywords to allow frame and line synchronization. When not transmitting data from the ADC, the data channels transmit the toggling Idle_A and Idle_B words. As a result, the data stream from the sensor has a fixed format.

Data Stream

Figure 29 represents the data stream of the data and control channels. Data channel “i” outputs the data from column “i” of every kernel. All control words in Table 49 can be uploaded through the SPI.

A SOF word is followed by an EOL word, as shown in Figure 29. This misplaced EOL word is ignored. The CRC is valid during transmission of the test image.

Normal Readout Mode

In normal readout mode, the data channels transmit data coming from the ADCs. The sync channel operates as described in the section Readout of Test Image on page 37. The data stream shown in Figure 29 is still valid.

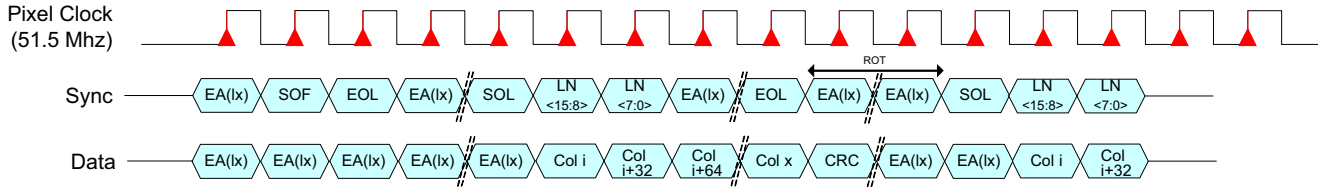


Figure 29. Timing of Data Stream

Table 49. CONTROL WORDS TRANSMITTED OVER SYNC CHANNEL

| Keyword | Description |
|---------|---|
| la | Idle word A |
| lb | Idle word B |
| lx | Idle word A or idle word B |
| SOF | Start of frame |
| SOL | Start of line |
| EOL | End of line |
| a<15:8> | Address of line being readout, a<15> is the MSB |
| a<7:0> | Address of line being readout |

Frame Overhead Time

The FOT is controlled by the PRECHARGE_TIMER, SAMPLE_TIMER, VMEM_TIMER, and FOT_TIMER SPI registers. Typical values are:

- PRECHARGE_TIMER: 1.5 μs
- SAMPLE_TIMER: 2.5 μs
- VMEM_TIMER: 2.7 μs
- FOT_TIMER: 3.2 μs

FOT_TIMER provides the moment when the signal sampled in the pixel is stable and ready for readout. FOT_TIMER arrives typically 500 ns after VMEM_TIMER. The rising edge of pixel_reset coincides with the rising edge of pixel_vmem.

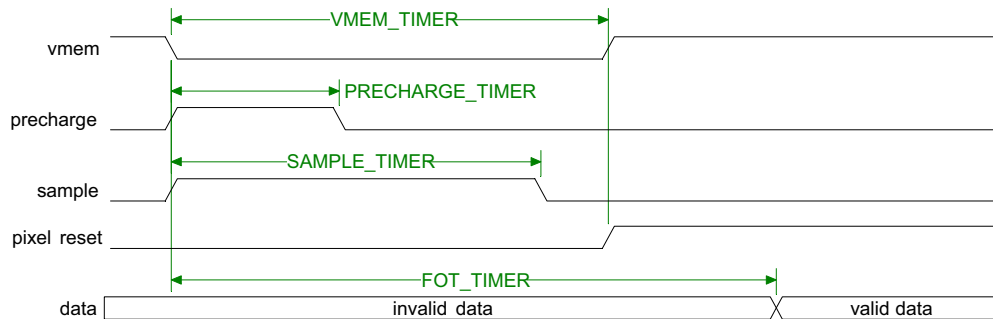


Figure 30. FOT Timing

Reduced ROT Readout Mode

When a row is selected, each pixel sees a large capacitive load.

This comes from two sections - 1) metal line connecting the pixel output to the column amplifier and parasitic caps of the 1695 pixels connected to it. 2) The column amplifier current source transistors. In normal ROT mode, both the structures are on and to transfer the charge from the pixel to the column amplifiers, each column amplifier must draw a larger current.

In the reduced ROT mode, the column amplifier current source is turned off/disabled. The capacitance of the column itself acts like the sampling capacitor and the capacitance seen by the pixel is reduced. As a result, the transfer of the charge is faster and a reduced ROT can be used. In reduced ROT mode, the dynamic range of the pixel is lesser than in normal ROT mode but the power consumption is also reduced.

The sensor operates in reduced ROT by default, with a ROT of nine sensor clock periods (175 ns).

FOT and ROT Pin Timing

The chip has two pins (FOT and ROT) that indicate internal FOT and ROT periods.

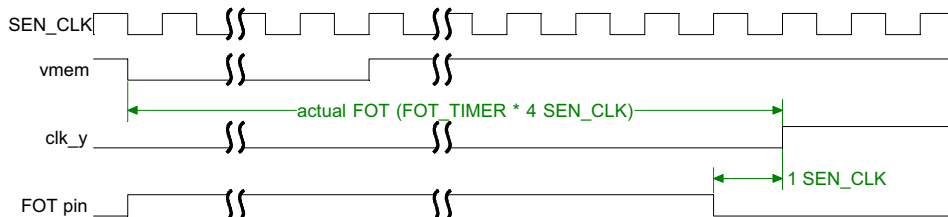


Figure 31. FOT Pin Timing

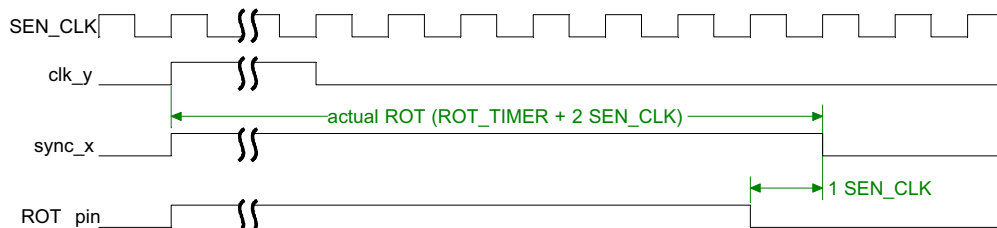


Figure 32. ROT Pin Timing

Asynchronous Reset

The sensor has a reset pin, RESET_N, and a reset SPI register, RESET_N_SEQ. Both are active low.

RESET_N is the chip reset. All components on the chip are reset when this pin is low. This includes the sequencer, the SPI register, and X and Y shift registers. The reset is asynchronous.

RESET_N_SEQ is the sequencer reset. Bringing this bit low only resets the sequencer. This is used to restart the sequencer with the current SPI settings.

Reset on Startup

When the sensor starts up, RESET_N is kept low until all supply voltages are stable. After the rising edge of

FOT Pin

The actual FOT goes from the falling edge of the internal VMEM signal to the rising edge of the first internal CLK_Y. After this rising edge of CLK_Y, the first ROT starts. The FOT pin goes high at the same moment VMEM goes low and remains high until one sensor clock period (CLKIN/4) before the end of the actual FOT. This is shown in Figure 31.

ROT Pin

The actual ROT goes from the rising edge of the internal CLK_Y signal to the falling edge of the internal SYNC_X signal. The ROT pin goes high at the rising edge of CLK_Y and remains high until one sensor clock (CLKIN/4) before the end of the actual ROT.

Table 50. FOT AND ROT PIN TIMING

| Pin | Delay vs. Sensor Clock | Rise and Fall Times (20 pF Load) |
|-----|------------------------|----------------------------------|
| FOT | 2.5 ns | 6 ns |
| ROT | 2.5 ns | 6 ns |

RESET_N, RESET_N_SEQ is kept low for an additional 0.5 μs.

During the chip reset the data on the LVDS outputs (data channels and sync channel) is invalid. When the chip comes out of reset, but the sequencer is kept in reset, the LVDS outputs toggle between the idle words.

If RESET_N_SEQ is only low for a short period of time (100 ns), the pixel array is not completely reset. Information from the previous integration cycle is still present on the photodiode. Ensure that the pixels are in reset for at least 3 μs by keeping RESET_N_SEQ low for a long time, or by not starting exposure before 3 μs after RESET_N_SEQ.

NOIL1SN3000A

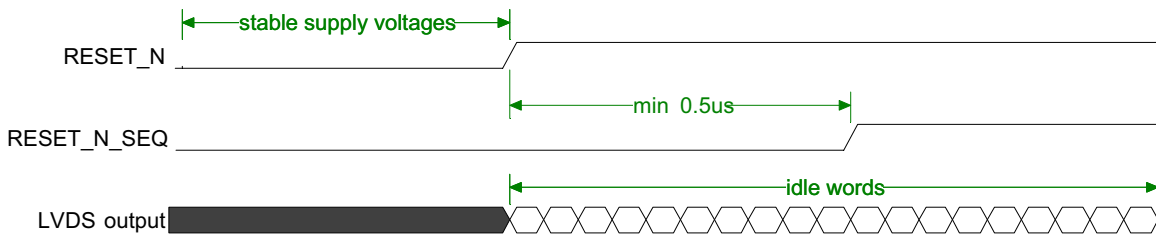


Figure 33. Reset on Startup

Sequencer Reset

The sequencer is reset separately by bringing the RESET_N_SEQ register low. This causes an asynchronous reset of the sequencer. The reset must have a length of at least 20 clock cycles (five words). Resetting the sequencer corrupts the analog voltages stored in the pixel array.

Therefore, a new readout sequence must start with an exposure first. After the reset, a readout sequence is reinitiated by using EXPOSURE_1 pin. Ensure the reset of the pixel array is long enough ($\geq 3 \mu\text{s}$).

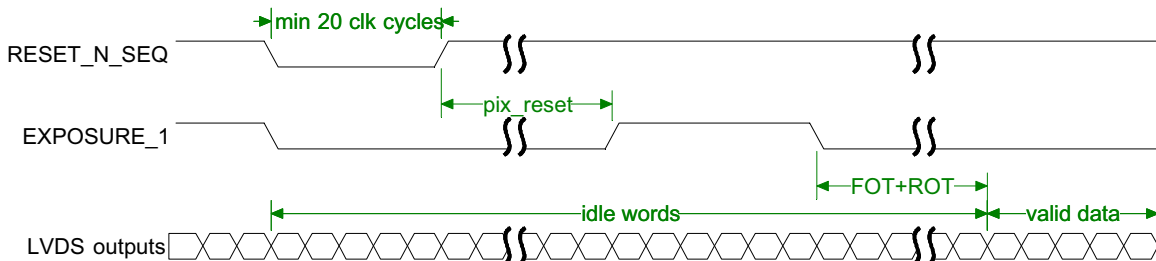


Figure 34. Sequencer Reset

Startup Sequence

To guarantee the correct startup of all the sensor modules, perform the following startup sequence:

1. All supplies are powered on simultaneous, but the RESET_N pin is kept low. The VAA is not powered on before VDD is powered on.
2. When all supplies are stable, bring RESET_N pin high. The sensor now begins to operate.
3. Set RESET_N_SEQ register bit to zero if other SPI registers need to be uploaded.
4. Set the RESET_N_SEQ bit to 1 if all required SPI registers are changed. LUPA3000 operates only in slave mode; therefore, the sensor is now controlled through the EXPOSURE_1 pin.

ADDITIONAL FEATURES

Windowing

A fully configurable window can be selected for readout. The parameters to configure this window are:

X_START: It is the start position for the X readout. Readout starts only at odd kernel positions. As a result possible start positions are 64 columns (two kernels) separated from each other.

X_kernels: The number of kernels to be read out.

Y_start: The starting line of the readout window.

Y_end: The end line of the readout window, granularity of 1.

For windowing, the effective readout time is smaller than in full frame mode, because only the relevant part of the image array is accessed. As a result, it is possible to achieve higher frame rates.

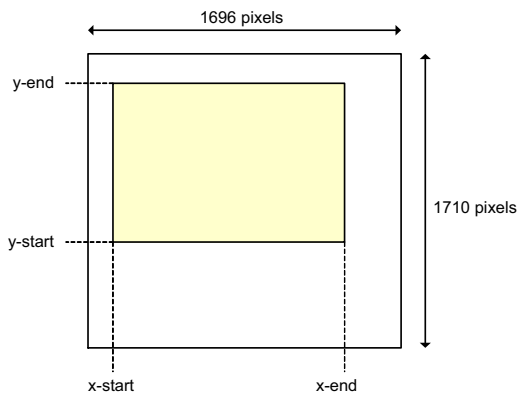


Figure 35. Window Selected for Readout

Restrictions to Windowing

To ensure correct operation of the sensor, the readout of partial windows must be done with some restrictions.

- The minimum window size is 4 kernels (128 pixels) in the x-direction and 1 line in the y-direction.
- In the x-direction, windowing can only start at an odd kernel (kernel1, kernel3, and so on). Then number of kernels to readout is not subject to an odd-even restriction.
- The sum of the ROT_TIMER and the NB_OF_KERNELS spi registers should always be an even number.

This means that for a fixed ROT time, the window size can only change in steps of 64 pixels. If the number of kernels to readout is decreased with one and the ROT is already at the minimum value, then the ROT time should be increased with one (clock cycle) to compensate. The framerate remains unchanged by this, but the data rate drops.

Sub Sampling

Not supported by LUPA3000.

Reverse Scan

Not supported by LUPA3000.

Multiple Windows

Not supported by LUPA3000.

Dual Slopes

Dynamic range can be extended by the dual slope capability of the sensor. The four colored lines in Figure 36 represents analog signals of the photodiode of four pixels, which decreases as a result of exposure. The slope is determined by the amount of light at each pixel (the more light, the steeper the slope). When the pixels reach the saturation level, the analog does not change despite further exposure. Without the dual slope capabilities, the pixels p3 and p4 are saturated before the end of the exposure time, and no signal is received. However, when using dual slopes, the analog signal is reset to a second reset level (lower than the original) before the integration time ends. The analog signal starts decreasing with the same slope as before, and pixels that were saturated before could be nonsaturated at read out time. For pixels that never reach any of the reset levels (for example, p1 and p2), there is no difference between single and multiple slope operation.

By choosing the time stamps of the double slope resets (typical at 90%, configurable by the user), it is possible to have a nonsaturated pixel value even for pixels that receive a huge amount of light.

The reset levels are configured through external (power) pins.

NOIL1SN3000A

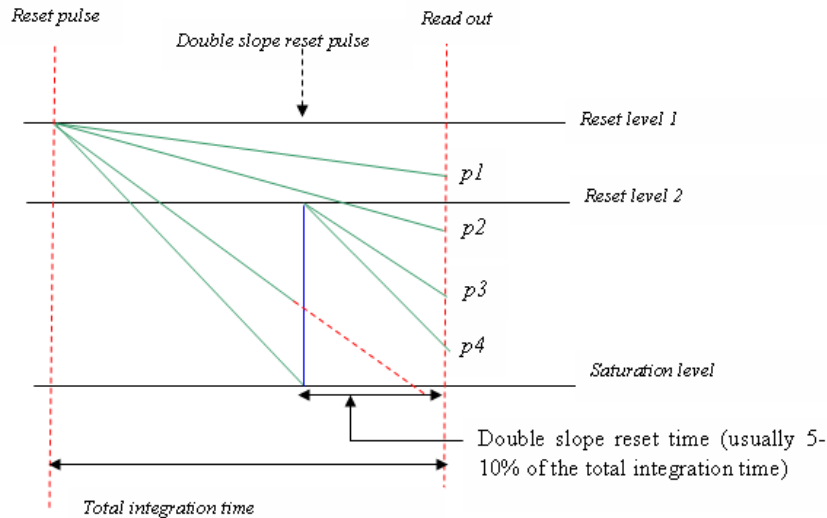


Figure 36. Dynamic Range Extended by Double Slope Capability

In slave mode, you have full control through the pins Exposure 1 and Exposure 2. Configure the multiple slope parameters for the application and interpret the pixel data accordingly.

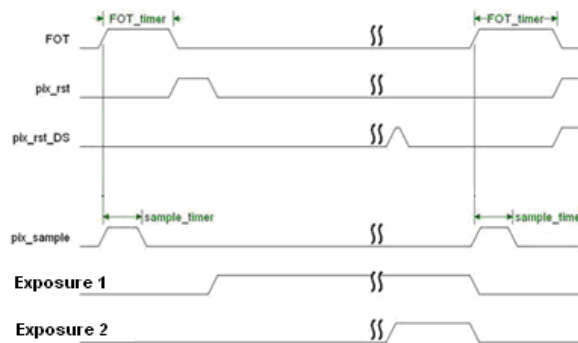


Figure 37. Dual Slope Timing in Slave Mode

Off-Chip FPN Correction

FPN is a kind of spatial noise, a noise that does not change with time. FPN comes from two different sources. The first source involves the variations between individual pixels. Within a CMOS image sensor, the device is designed such that each pixel is identical to all the others.

Although each pixel is similar to all of the others within the array, there are slight variations. These variations arise from variations in threshold voltages and offsets of the amplifier within each pixel. Because these can vary for each pixel within the pixel array; they are referred to as pixel FPN.

The second source of FPN involves the performance variations of the amplifiers shared by each column of the pixel array. The information within the pixel array is read out on a column-by-column basis through these column amplifiers. When one amplifier behaves slightly different from another, the entire column can be affected. When this

happens, it results in what appears to be vertical lines in the image. This is commonly called column FPN. Of the two sources of FPN, column FPN is more noticeable than pixel FPN.

LUPA3000 has no on-chip FPN correction so it must be corrected off-chip in the software.

FPN can be calibrated off-chip by subtracting a dark image from all captured images. For optimal results two guidelines can be followed:

- Use an averaged dark image to calibrate FPN; this eliminates other noise sources that are present in the dark image.
- Use a different dark image to calibrate for different operation conditions. Different operation conditions can be changes in temperature, FOT and ROT timing, and gain settings.

Software FPN Correction

The procedure is as follows:

1. Adjust the black level with the help of histogram by modifying DAC offset.
2. Store a dark image by closing the lens aperture, but make sure no value is absolute zero.
3. Subtract the dark reference image from all the captured images.

Off-Chip PRNU Correction

Pixel response non-uniformity (PRNU) is also a kind of spatial noise. It refers to the slight variations in response to the same input that each pixel has due to the slight active response variations between the amplifiers within different pixels. Even though every pixel is carefully designed to match one another, slight variations in processing, noise, and other areas can cause these amplifiers to behave differently.

This is corrected with the help of a grey image; the correction is done by equalization of gain.

The procedure is as follows:

1. Capture the grey image under the same condition as the dark image.
2. Open the aperture of the lens to allow light and then capture the grey frame. All the pixels in the grey image should have a grey value of approximately 70% white (histogram should peak at 70% white and the distribution should be uniform around the peak as much as possible).

This grey image is stored.

FPN and PRNU correction formula:

$$V_n = (\text{Avg}(W_n) / [W_n - B_n + 1]) \times (G_n - B_n)$$

V_n - data of a pixel after a calibration

G_n - data of a pixel before carrying out a calibration

B_n - black calibration data of the pixel

W_n - white (gray) calibration data of the pixel

NOIL1SN3000A

PACKAGE INFORMATION

Pin Definitions

The package has 369 pins. Table 51 lists 228 pins. The remaining pins are used as die attach ground pins.

Table 51. PIN LIST

| Finger Number | Pin Number | Function | Description |
|---------------|------------|----------|---------------------------|
| 1 | A3 | GNDd_hs | Ground high speed digital |
| 2 | B3 | Vdd_hs | 2.5-V high speed digital |
| 3 | A2 | Clk_Outp | Output clock P |
| 4 | B2 | CLK_Outn | Output clock N |
| 5 | A1 | Outp 0 | LVDS data output |
| 6 | B1 | Outn 0 | LVDS data output |
| 7 | C4 | Outp 1 | LVDS data output |
| 8 | D4 | Outn 1 | LVDS data output |
| 9 | C3 | Outp 2 | LVDS data output |
| 10 | D3 | Outn 2 | LVDS data output |
| 11 | C2 | Outp 3 | LVDS data output |
| 12 | D2 | Outn 3 | LVDS data output |
| 13 | C1 | Outp 4 | LVDS data output |
| 14 | D1 | Outn 4 | LVDS data output |
| 15 | E5 | Outp 5 | LVDS data output |
| 16 | F5 | Outn 5 | LVDS data output |
| 17 | E4 | Vlvds | 2.5-V LVDS |
| 18 | F4 | GNDlvds | Ground LVDS |
| 19 | E3 | Outp 6 | LVDS data output |
| 20 | F3 | Outn 6 | LVDS data output |
| 21 | E2 | Outp 7 | LVDS data output |
| 22 | F2 | Outn 7 | LVDS data output |
| 23 | E1 | Outp 8 | LVDS data output |
| 24 | F1 | Outn 8 | LVDS data output |
| 25 | G5 | Outp 9 | LVDS data output |
| 26 | H5 | Outn 9 | LVDS data output |
| 27 | G4 | Outp 10 | LVDS data output |
| 28 | H4 | Outn 10 | LVDS data output |
| 29 | G3 | Outp 11 | LVDS data output |
| 30 | H3 | Outn 11 | LVDS data output |
| 31 | G2 | Outp 12 | LVDS data output |
| 32 | H2 | Outn 12 | LVDS data output |
| 33 | G1 | Vlvds | 2.5-V LVDS |
| 34 | H1 | GNDlvds | Ground LVDS |
| 35 | J5 | Outp 13 | LVDS data output |
| 36 | K5 | Outn 13 | LVDS data output |
| 37 | J4 | Outp 14 | LVDS data output |
| 38 | K4 | Outn 14 | LVDS data output |
| 39 | J3 | Outp 15 | LVDS data output |

NOIL1SN3000A

Table 51. PIN LIST

| Finger Number | Pin Number | Function | Description |
|---------------|------------|----------|-------------------|
| 40 | K3 | Outn 15 | LVDS data output |
| 41 | J2 | Vadc | 2.5-V ADC |
| 42 | K2 | GNDadc | Ground ADC |
| 43 | J1 | Outp 16 | LVDS data output |
| 44 | K1 | Outn 16 | LVDS data output |
| 45 | L5 | Outp 17 | LVDS data output |
| 46 | M5 | Outn 17 | LVDS data output |
| 47 | L4 | Outp 18 | LVDS data output |
| 48 | M4 | Outn 18 | LVDS data output |
| 49 | L3 | Vlvds | 2.5-V LVDS |
| 50 | M3 | GNDlvds | Ground LVDS |
| 51 | L2 | Outp 19 | LVDS data output |
| 52 | M2 | Outn 19 | LVDS data output |
| 53 | L1 | Outp 20 | LVDS data output |
| 54 | M1 | Outn 20 | LVDS data output |
| 55 | N5 | Outp 21 | LVDS data output |
| 56 | P5 | Outn 21 | LVDS data output |
| 57 | N4 | Outp 22 | LVDS data output |
| 58 | P4 | Outn 22 | LVDS data output |
| 59 | N3 | Outp 23 | LVDS data output |
| 60 | P3 | Outn 23 | LVDS data output |
| 61 | N2 | Outp 24 | LVDS data output |
| 62 | P2 | Outn 24 | LVDS data output |
| 63 | N1 | Outp 25 | LVDS data output |
| 64 | P1 | Outn 25 | LVDS data output |
| 65 | R5 | Vlvds | 2.5-V LVDS |
| 66 | T5 | GNDlvds | Ground LVDS |
| 67 | R4 | Outp 26 | LVDS data output |
| 68 | T4 | Outn 26 | LVDS data output |
| 69 | R3 | Outp 27 | LVDS data output |
| 70 | T3 | Outn 27 | LVDS data output |
| 71 | R2 | Outp 28 | LVDS data output |
| 72 | T2 | Outn 28 | LVDS data output |
| 73 | R1 | Outp 29 | LVDS data output |
| 74 | T1 | Outn 29 | LVDS data output |
| 75 | U4 | Outp 30 | LVDS data output |
| 76 | V4 | Outn 30 | LVDS data output |
| 77 | U3 | Outp 31 | LVDS data output |
| 78 | V3 | Outn 31 | LVDS data output |
| 79 | U2 | Clk_inp | LVDS input clock |
| 80 | V2 | Clk_inn | LVDS input clock |
| 81 | U1 | Syncp | LVDS sync channel |

NOIL1SN3000A

Table 51. PIN LIST

| Finger Number | Pin Number | Function | Description |
|---------------|------------|---------------|-------------------------------------|
| 82 | V1 | Syncn | LVDS sync channel |
| 83 | W1 | Vdd_hs | 2.5-V high speed digital |
| 84 | W2 | GNDd_hs | Ground high speed digital |
| 85 | W3 | GNDd_hs | Ground high speed digital |
| 86 | W4 | Vdd_hs | 2.5-V high speed digital |
| 87 | W5 | Vcm | Decoupling analog reference voltage |
| 88 | W6 | Vdark | Decoupling analog reference voltage |
| 89 | V5 | GNDadc | Ground ADC |
| 90 | U5 | Vadc | 2.5-V ADC |
| 91 | V6 | GNDd | Ground digital |
| 92 | U6 | Vdd | 2.5-V digital |
| 93 | T6 | GNDadc | Ground ADC |
| 94 | T7 | Vadc | 2.5-V ADC |
| 95 | V7 | GNDadc | Ground ADC |
| 96 | U7 | Vadc | 2.5-V ADC |
| 97 | W7 | GNDd | Ground digital |
| 98 | W8 | Vdd | 2.5-V digital |
| 99 | V8 | GNDaa | Ground analog |
| 100 | U8 | GNDaa | Ground analog |
| 101 | T8 | GNDaa | Ground analog |
| 102 | W9 | Vaa | 2.5-V analog |
| 103 | V9 | Vaa | 2.5-V analog |
| 104 | U9 | GNDaa | Ground analog |
| 105 | T9 | GNDaa | Ground analog |
| 106 | W10 | Vaa | 2.5-V analog |
| 107 | V10 | Vaa | 2.5-V analog |
| 108 | U10 | GNDaa | Ground analog |
| 109 | T10 | Vaa | 2.5-V analog |
| 110 | W11 | Vpix | Vpix (typically 2.5 V) |
| 111 | V11 | GNDd | Ground digital |
| 112 | U11 | Vdd | 2.5-V digital |
| 113 | T11 | Not Assigned | Not assigned |
| 114 | T12 | Not Assigned | Not assigned |
| 115 | U12 | Reset_n | Digital input |
| 116 | V12 | Exposure 1 | Digital input |
| 117 | W12 | Exposure 2 | Digital input |
| 118 | W13 | ROT | Digital output |
| 119 | V13 | FOT | Digital output |
| 120 | U13 | Not Assigned | Not assigned |
| 121 | T13 | Current_Ref_1 | Current reference resistor |
| 122 | T14 | Not Assigned | Not assigned |
| 123 | U14 | Analog_Out | Analog output (leave floating) |

NOIL1SN3000A

Table 51. PIN LIST

| Finger Number | Pin Number | Function | Description |
|---------------|------------|------------------|--|
| 124 | V14 | Not Assigned | Not assigned |
| 125 | W14 | Not Assigned | Not assigned |
| 126 | W15 | EOS_x | End of Scan in x-direction. For test purpose only. Leave floating. |
| 127 | V15 | SPI_MISO | Digital output |
| 128 | U15 | SPI_MOSI | Digital input |
| 129 | T15 | SPI_CLK | Digital input |
| 130 | T16 | SPI_CS | Digital input |
| 131 | U16 | GNDd | Ground digital |
| 132 | V16 | Vdd | 2.5-V digital |
| 133 | W16 | Vpix | Vpix (typically 2.5 V) |
| 134 | W17 | GNDdesd | Ground for ESD |
| 135 | V17 | Not Assigned | Not assigned |
| 136 | U17 | Not Assigned | Not assigned |
| 137 | T17 | Test_Array | Not assigned |
| 138 | T18 | Full_Diode | Not assigned |
| 139 | U18 | Not Assigned | Not assigned |
| 140 | V18 | Not Assigned | Not assigned |
| 141 | W18 | EOSy_right | End of Scan in y-direction. For test purpose only. Leave floating. |
| 142 | V19 | GNDd | Ground digital |
| 143 | U19 | Vdd | 2.5-V digital |
| 144 | W19 | Vpix | Vpix (typically 2.5 V) |
| 145 | W20 | Precharge_Bias_2 | Leave floating |
| 146 | V20 | GNDdesd | Ground for ESD |
| 147 | U20 | Not Assigned | Not assigned |
| 148 | W21 | GNDdrivers | Ground array drivers |
| 149 | V21 | Vres_ds | Reset DS supply (typically 2.5 V) |
| 150 | U21 | Vres | Reset supply (typically 3.3 V) |
| 151 | T21 | Vmem_l | Vmem low supply (typically 2.5 V) |
| 152 | T20 | Vmem_h | Vmem high supply (typically 3.3 V) |
| 153 | R20 | Vprecharge | Pix precharge supply |
| 154 | R21 | D/A Ground | Die attach ground |
| 155 | P21 | Vdd | 2.5-V digital |
| 156 | P20 | Not Assigned | Not assigned |
| 157 | N20 | GNDdrivers | Ground array drivers |
| 158 | N21 | Vres_ds | Reset DS supply (typically 2.5 V) |
| 159 | M21 | Vres | Reset supply (typically 3.3 V) |
| 160 | L21 | Vmem_l | Vmem low supply (typically 2.5 V) |
| 161 | K21 | Vmem_h | Vmem high supply (typically 3.3 V) |
| 162 | J21 | Vprecharge | Pix precharge supply |
| 163 | H21 | D/A Ground | Die attach ground |

NOIL1SN3000A

Table 51. PIN LIST

| Finger Number | Pin Number | Function | Description |
|---------------|------------|------------------|--|
| 164 | G21 | Vdd | 2.5-V digital |
| 165 | F21 | Not Assigned | Not assigned |
| 166 | E21 | GNDdrivers | Ground array drivers |
| 167 | D21 | Vres_ds | Reset DS supply (typically 2.5 V) |
| 168 | D20 | Vres | Reset supply (typically 3.3 V) |
| 169 | C20 | Vmem_l | Vmem low supply (typically 2.5 V) |
| 170 | C21 | Vmem_h | Vmem high supply (typically 3.3 V) |
| 171 | B21 | Vprecharge | Pix precharge supply |
| 172 | A21 | D/A Ground | Die attach ground |
| 173 | B20 | Vdd | 2.5-V digital |
| 174 | A20 | Not Assigned | Not assigned |
| 175 | A19 | No Pin | No pin |
| 176 | B19 | GND_esd | Ground for ESD |
| 177 | B18 | Precharge_Bias_1 | Pix precharge supply |
| 178 | A18 | Vpix | Vpix (typically 2.5 V) |
| 179 | B17 | Vdd | 2.5-V digital |
| 180 | A17 | GNDd | Ground digital |
| 181 | A16 | EOSy_left | End of Scan in y-direction. For test purpose only. Leave floating. |
| 182 | B16 | Not Assigned | Not assigned |
| 183 | B15 | Not Assigned | Not assigned |
| 184 | A15 | Not Assigned | Not assigned |
| 185 | A14 | Not Assigned | Not assigned |
| 186 | B14 | GNDesd | Ground for ESD |
| 187 | A13 | Vpix | Vpix (typically 2.5 V) |
| 188 | B13 | Vdd | 2.5-V digital |
| 189 | C13 | GNDd | Ground digital |
| 190 | D13 | Not Assigned | Not assigned |
| 191 | D12 | Not Assigned | Not assigned |
| 192 | C12 | Not Assigned | Not assigned |
| 193 | B12 | Analog_In | Analog Input of ADC |
| 194 | A12 | Current_Ref_2 | Current Reference Resistor |
| 195 | D11 | Not Assigned | Not assigned |
| 196 | C11 | Not Assigned | Not assigned |
| 197 | B11 | Vdd | 2.5-V digital |
| 198 | A11 | GNDd | Ground digital |
| 199 | A10 | Vpix | Vpix (typically 2.5 V) |
| 200 | C10 | Vaa | 2.5-V analog |
| 201 | B10 | GNDa | Ground analog |
| 202 | D10 | Vaa | 2.5-V analog |
| 203 | D9 | Vaa | 2.5-V analog |
| 204 | A9 | GNDa | Ground analog |

NOIL1SN3000A

Table 51. PIN LIST

| Finger Number | Pin Number | Function | Description |
|---------------|------------|------------|-------------------------------------|
| 205 | B9 | GNDa | Ground analog |
| 206 | C9 | Vaa | 2.5-V analog |
| 207 | C8 | Vaa | 2.5-V analog |
| 208 | B8 | GNDa | Ground analog |
| 209 | A8 | GNDa | Ground analog |
| 210 | A7 | GNDa | Ground analog |
| 211 | D8 | Vdd | 2.5-V digital |
| 212 | D7 | GNDd | Ground digital |
| 213 | C7 | Vadc | 2.5-V ADC |
| 214 | B7 | GNDadc | Ground ADC |
| 215 | C6 | Vadc | 2.5-V ADC |
| 216 | B6 | GNDadc | Ground ADC |
| 217 | D6 | Vdd | 2.5-V digital |
| 218 | D5 | GNDd | Ground digital |
| 219 | C5 | Vadc | 2.5-V ADC |
| 220 | B5 | GNDadc | Ground ADC |
| 221 | A6 | Vrefp | Decoupling analog reference voltage |
| 222 | A5 | Vrefm | Decoupling analog reference voltage |
| 223 | B4 | Vdd_hs | 2.5-V high speed digital |
| 224 | A4 | GNDd_hs | Ground high speed digital |
| 225 | F6 | D/A Ground | Die attach ground |
| 226 | R6 | D/A Ground | Die attach ground |
| 227 | T19 | D/A Ground | Die attach ground |
| 228 | E20 | D/A Ground | Die attach ground |

Pin Assignment

Die Attach Ground Pins

The pins listed as die attach pins should be connected to the PCB ground plane or to an active cooling device.

Non Assigned Pins

Pins that are marked “not assigned” in the pin list must be left floating. ON Semiconductor uses some of them for debugging.

NOIL1SN3000A

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | | | |
|---|----|----|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| A | 5 | 3 | 1 | 224 | 222 | 221 | 210 | 209 | 204 | 199 | 198 | 194 | 187 | 185 | 184 | 181 | 180 | 178 | 175 | 174 | 172 | | | |
| B | 6 | 4 | 2 | 223 | 220 | 216 | 214 | 208 | 205 | 201 | 197 | 193 | 188 | 186 | 183 | 182 | 179 | 177 | 176 | 173 | 171 | | | |
| C | 13 | 11 | 9 | 7 | 219 | 215 | 213 | 207 | 206 | 200 | 196 | 192 | 189 | | | | | | | | 169 | 170 | | |
| D | 14 | 12 | 10 | 8 | 218 | 217 | 212 | 211 | 203 | 202 | 195 | 191 | 190 | | | | | | | | | 168 | 167 | |
| E | 23 | 21 | 19 | 17 | 15 | 225 | | | | | | | | | | | | | | | | 228 | 166 | |
| F | 24 | 22 | 20 | 18 | 16 | | | | | | | | | | | | | | | | | | 165 | |
| G | 33 | 31 | 29 | 27 | 25 | | | | | | | | | | | | | | | | | | 164 | |
| H | 34 | 32 | 30 | 28 | 26 | | | | | | | | | | | | | | | | | | 163 | |
| J | 43 | 41 | 39 | 37 | 35 | | | | | | | | | | | | | | | | | | 162 | |
| K | 44 | 42 | 40 | 38 | 36 | | | | | | | | | | | | | | | | | | 161 | |
| L | 53 | 51 | 49 | 47 | 45 | | | | | | | | | | | | | | | | | | 160 | |
| M | 54 | 52 | 50 | 48 | 46 | | | | | | | | | | | | | | | | | | 159 | |
| N | 63 | 61 | 59 | 57 | 55 | | | | | | | | | | | | | | | | | | 157 | 158 |
| P | 64 | 62 | 60 | 58 | 56 | | | | | | | | | | | | | | | | | | 156 | 155 |
| R | 73 | 71 | 69 | 67 | 65 | 226 | | | | | | | | | | | | | | | | | 153 | 154 |
| T | 74 | 72 | 70 | 68 | 66 | 93 | 94 | 101 | 105 | 109 | 113 | 114 | 121 | 122 | 129 | 130 | 137 | 138 | 227 | 152 | 151 | | | |
| U | 81 | 79 | 77 | 75 | 90 | 92 | 96 | 100 | 104 | 108 | 112 | 115 | 120 | 123 | 128 | 131 | 136 | 139 | 143 | 147 | 150 | | | |
| V | 82 | 80 | 78 | 76 | 89 | 91 | 95 | 99 | 103 | 107 | 111 | 116 | 119 | 124 | 127 | 132 | 135 | 140 | 142 | 146 | 149 | | | |
| W | 83 | 84 | 85 | 86 | 87 | 88 | 97 | 98 | 102 | 106 | 110 | 117 | 118 | 125 | 126 | 133 | 134 | 141 | 144 | 145 | 148 | | | |

Signal Groups

| | |
|--|-------------------------------------|
| | LVDS Data Output |
| | Not Assigned |
| | Die Attach Ground |
| | Supply LVDS |
| | Supply ADC |
| | Supply Digital |
| | Supply Analog |
| | Supply Pixel |
| | High Speed Digital Supply |
| | Decoupling Analog Reference Voltage |
| | Digital IO |
| | Current Reference & Precharge Bias |
| | Test Pin |
| | Supply Array Signals |
| | Ground for ESD |
| | No Pin connection |

Figure 38. Visualization of Pin Assignment (Top View)

NOIL1SN3000A

Mechanical Specifications

Table 52. MECHANICAL SPECIFICATIONS

| | Mechanical Specifications | Min | Typ | Max | Units |
|---|---|--|-------------|------|-------|
| Die (Referenced to Pin 1 being bottom left in Figure 39 on page 52) | Die thickness | – | 750 | – | μm |
| | Die center, X offset to the center of package | – | 0 | – | μm |
| | Die center, Y offset to the center of the package | – | 0 | – | μm |
| | Die position, X tilt | –1 | 0 | 1 | deg |
| | Die position, Y tilt | –1 | 0 | 1 | deg |
| | Die placement accuracy in package | –50 | 0 | 50 | um |
| | Die rotation accuracy | –1 | 0 | 1 | deg |
| | Optical center referenced from the package center. | – | –230 | – | μm |
| | Optical center referenced from the package center. | – | 1450 | – | μm |
| | Distance from PCB plane to top of the die surface | – | 2 | – | mm |
| | Distance from top of the die surface to top of the glass lid | – | 2 | – | mm |
| Glass lid specification | X x Y size | – | 28.2 x 19.5 | – | mm |
| | Thickness | – | 1 | – | mm |
| | Spectral range for optical coating of window | 400 | – | 1100 | nm |
| | Reflection coefficient for window | – | – | <0.8 | % |
| Mechanical shock | JESD22-B104C; Condition G | – | 2000 | – | G |
| Vibration | JESD22-B103B; Condition 1 | 20 | – | 2000 | Hz |
| Mounting profile | Lead-free wave soldering profile for pin grid array package if no socket is used | | | | |
| Recommended socket manufacturer | Andon Electronics (http://www.andonelectronics.com) | BGA socket: 10-21-06-369-414T4-R27-L14 | | | |
| | | Thru hole: 10-21-06-369-400T4-R27-L14 | | | |

NOIL1SN3000A

Package Diagram

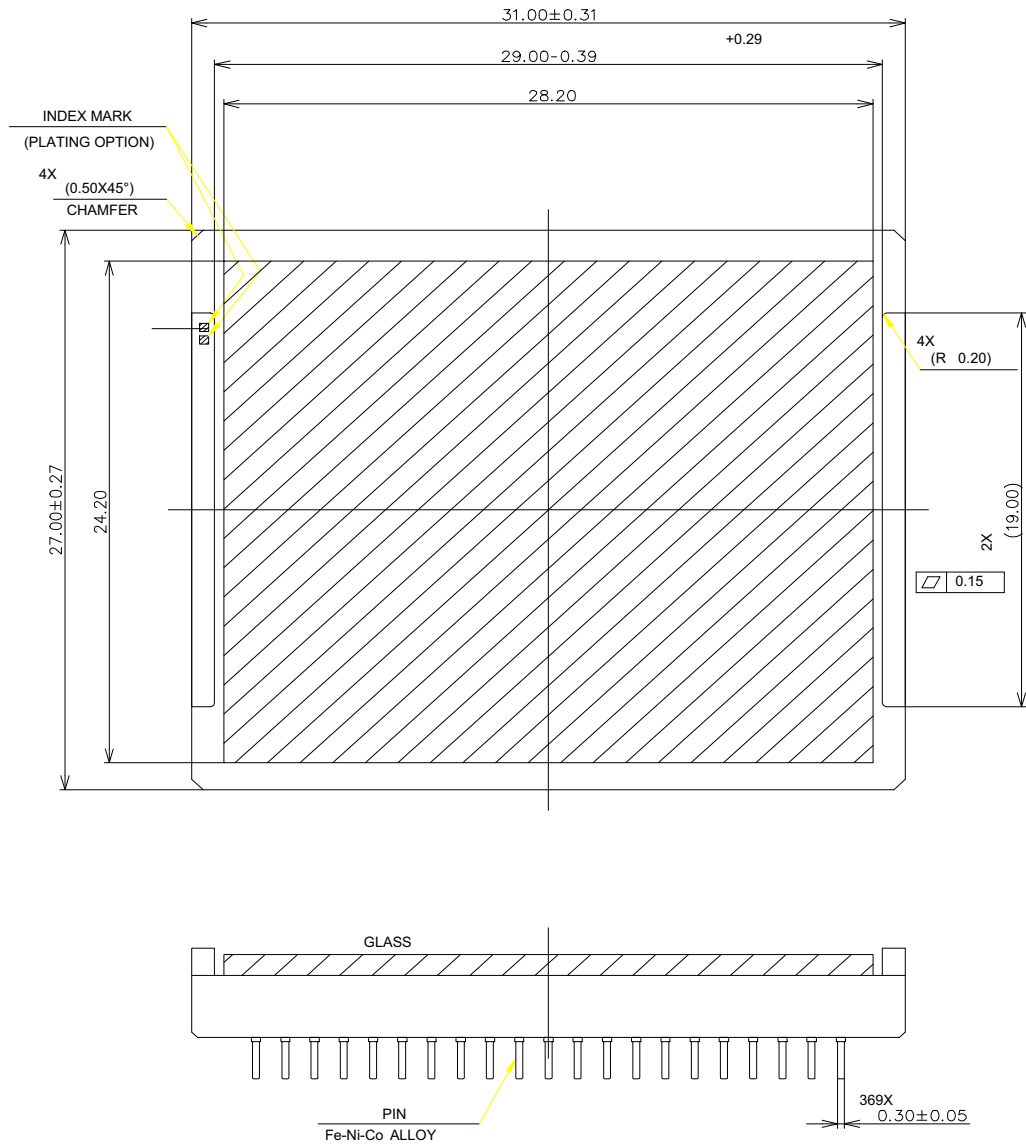


Figure 39. LUPA3000 μPGA Package Diagram (Top View)

NOIL1SN3000A

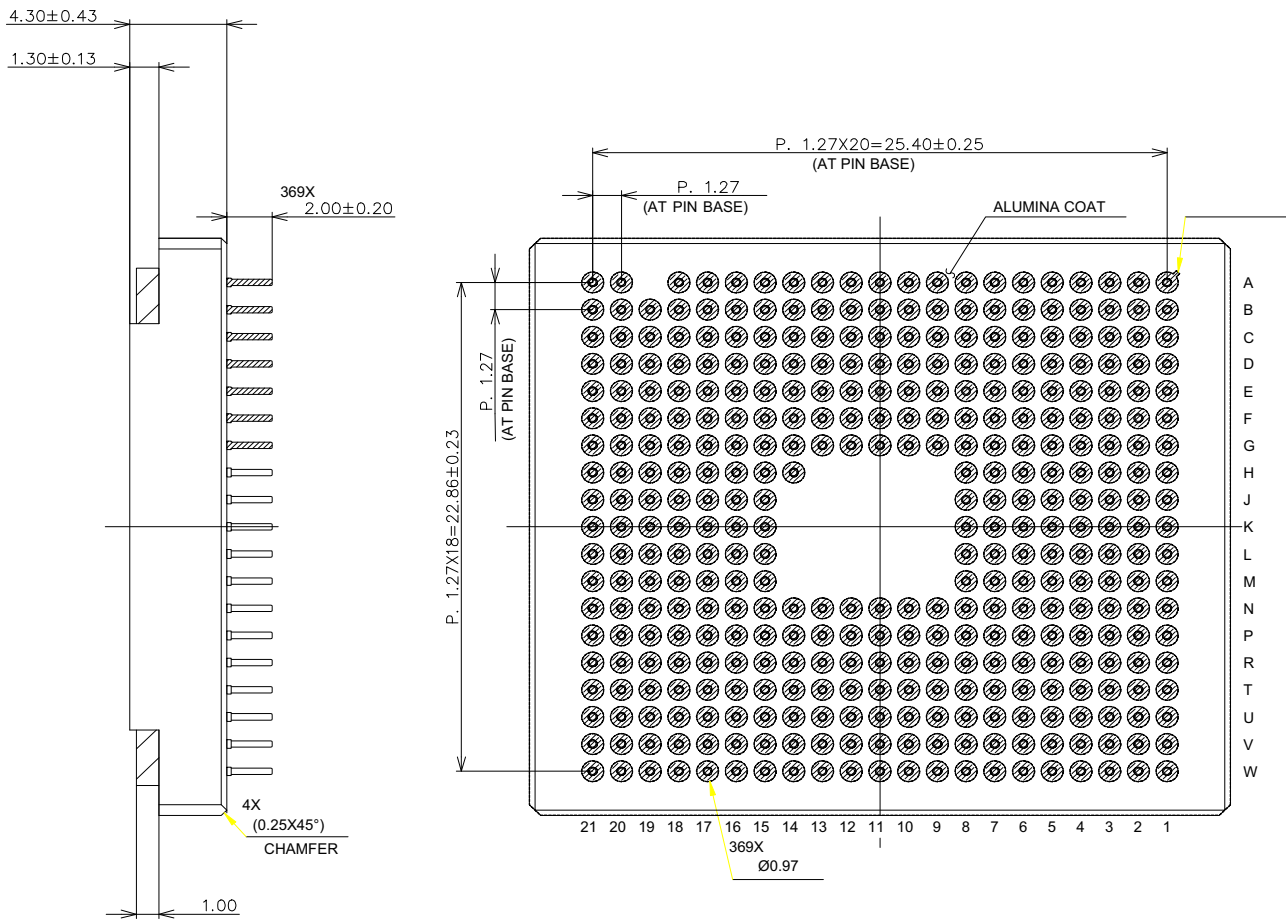


Figure 40. LUPA3000 μPGA Package Diagram (Bottom View)

Glass Lid

The LUPA3000 image sensor uses a glass lid without any coatings. Figure 41 shows the transmission characteristics of the glass lid.

As seen in Figure 41, the sensor does not use infrared attenuating color filter glass. You must provide a filter in the optical path when using color devices.

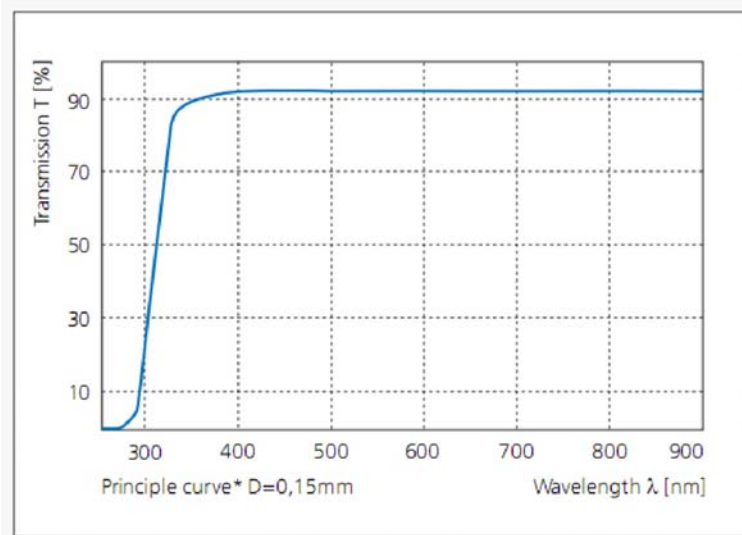


Figure 41. Transmission Characteristics of Glass Lid

ADDITIONAL REFERENCES AND RESOURCES

Application Notes and other resources can be found linked to the product web page at www.onsemi.com. Additional information on this device may also be available in the [Image Sensor Portal](#), accessible within the MyON section of www.onsemi.com. A signed NDA is required to access the Image Sensor Portal – please see your ON Semiconductor sales representative for more information.

For information on ESD and cover glass care and cleanliness, please download the Application Note *Image Sensor Handling and Best Practices* (AN52561/D) from www.onsemi.com.

For quality and reliability information, please download the *Quality & Reliability Handbook* (HBD851/D) from www.onsemi.com.

For information on Standard terms and Conditions of Sale, please download [Terms and Conditions](#) document from www.onsemi.com.

For information on Return Material Authorization procedures, please refer to the [RMA Policy Procedure](#) document from www.onsemi.com.

The Product Acceptance Criteria document, which lists criteria to which this device is tested prior to shipment, is available upon request.

NOIL1SN3000A

ACRONYMS

| Acronym | Description |
|---------|---|
| ADC | analog-to-digital converter |
| AFE | analog front end |
| ANSI | American National Standards Institute |
| BGA | ball grid array |
| BL | black pixel data |
| CDM | Charged Device Model |
| CDS | correlated double sampling |
| CIS | CMOS image sensor |
| CMOS | complementary metal oxide semiconductor |
| CMY | cyan magenta yellow |
| CRC | cyclic redundancy check |
| DAC | digital-to-analog converter |
| DDR | double data rate |
| DFT | design for test |
| DNL | differential nonlinearity |
| DSNU | dark signal nonuniformity |
| EIA | Electronic Industries Alliance |
| EOL | end of line |
| ESD | electrostatic discharge |
| FE | frame end |
| FF | fill factor |
| FOT | frame overhead time |
| FPN | fixed pattern noise |
| FPS | frames per second |
| FS | frame start |
| HBM | Human Body Model |
| HMUX | horizontal multiplexer |
| I2C | inter-integrated circuit |
| IEEE | Institute of Electrical and Electronics Engineers |
| IMG | regular pixel data |

| Acronym | Description |
|---------|---|
| INL | integral nonlinearity |
| IP | intellectual property |
| JTAG | Joint Test Action Group |
| LE | line end |
| LS | line start |
| LSB | least significant bit |
| LVDS | low-voltage differential signaling |
| MBS | mixed boundary scan |
| MSB | most significant bit |
| MTF | modulation transfer function |
| NIR | near infrared |
| PGA | programmable gain amplifier |
| PLS | parasitic light sensitivity |
| PRBS | pseudo-random binary sequence |
| PRNU | pixel random nonuniformity |
| QE | quantum efficiency |
| RGB | red green blue |
| RMS | root mean square |
| ROI | region of interest |
| ROT | row overhead time |
| S/H | sample and hold |
| SNR | signal-to-noise ratio |
| SOF | start of frame |
| SOL | start of line |
| SPI | serial peripheral interface |
| TAP | test access port |
| TBD | to be determined |
| TIA | Telecommunications Industry Association |
| TR | training pattern |
| uPGA | micro pin grid array |


NOIL1SN3000A

GLOSSARY

| | |
|-----------------------|--|
| blooming | The leakage of charge from a saturated pixel into neighboring pixels. |
| camera gain constant | A constant that converts the number of electrons collected by a pixel into digital output (in DN). It can be extracted from photon transfer curves. |
| column noise | Variation of column mean signal strengths. The human eye is sensitive to line patterns so this noise is analyzed separately. |
| conversion gain | A constant that converts the number of electrons collected by a pixel into the voltage swing of the pixel. Conversion gain = q/C where q is the charge of an electron ($1.602E-19$ Coulomb) and C is the capacitance of the photodiode or sense node. |
| CDS | Correlated double sampling. This is a method for sampling a pixel where the pixel voltage after reset is sampled and subtracted from the voltage after exposure to light. |
| CFA | Color filter array. The materials deposited on top of pixels that selectively transmit color. |
| color crosstalk | The leakage of signal from one color channel into another when the imager is NOT saturated. The signal can leak through either optical means, in which a photon enters a pixel of the <u>wrong</u> color, or electrical means, in which a charge carrier generated within one pixel diffuses into a neighboring pixel. |
| CRA | Chief ray angle. Oblique rays that pass through the center of a lens system aperture stop. Color filter array, metal, and micro lens shifts are determined by the chief ray angle of the optical system. In general, optical systems with smaller CRA are desired to minimize color artifacts |
| DN | Digital number. The number of bits (8, 12, 14, ...) should also be specified. |
| DNL | Differential nonlinearity (for ADCs) |
| DSNU | Dark signal nonuniformity. This parameter characterizes the degree of nonuniformity in dark leakage currents, which can be a major source of fixed pattern noise. |
| fill-factor | A parameter that characterizes the optically active percentage of a pixel. In theory, it is the ratio of the actual QE of a pixel divided by the QE of a photodiode of equal area. In practice, it is never measured. |
| grating monochromator | An instrument that produces a monochromatic beam of light. It typically consists of a broadband light source such as a tungsten lamp and a diffraction grating for selecting a particular wavelength. |
| INL | Integral nonlinearity (for ADCs) |
| luminance | Light flux per unit area in photometric units (lux) |
| IR | Infrared. IR light has wavelengths in the approximate range 750 nm to 1 mm. |
| irradiance | Light flux per unit area in radiometric units (W/m^2) |
| Lag | The persistence of signal after pixel reset when the irradiance changes from high to low values. In a video stream, lag appears as 'ghost' images that persist for one or more frames. |
| Lux | Photometric unit of luminance (at 550 nm, $1 \text{ lux} = 1 \text{ lumen}/m^2 = 1/683 \text{ W}/m^2$) |
| NIR | Near Infrared. NIR is part of the infrared portion of the spectrum and has wavelengths in the approximate range 750 nm to 1400 nm. |
| pixel noise | Variation of pixel signals within a region of interest (ROI). The ROI typically is a rectangular portion of the pixel array and may be limited to a single color plane. |
| photometric units | Units for light measurement that take into account human physiology. |
| photon transfer | Measurement in which a bare imager (no external lens) is irradiated with uniform light from dark to saturation levels. Typically the source is collimated, monochromatic 550 nm light. Chapter 2 of J. Janesick's book, <i>Scientific Charge Coupled Devices</i> , describes the technique in detail. |
| PLS | Parasitic light sensitivity. Parasitic discharge of sampled information in pixels that have storage nodes. |
| PRNU | Photo-response nonuniformity. This parameter characterizes the spread in response of pixels, which is a source of FPN under illumination. |
| QE | Quantum efficiency. This parameter characterizes the effectiveness of a pixel in capturing photons and converting them into electrons. It is photon wavelength and pixel color dependent. |
| radiometric units | Units for light measurement based on physics. |
| read noise | Noise associated with all circuitry that measures and converts the voltage on a sense node or photodiode into an output signal. |
| reset | The process by which a pixel photodiode or sense node is cleared of electrons. Soft reset occurs when the reset transistor is operated below the threshold. Hard reset occurs when the reset transistor is operated above threshold. |

NOIL1SN3000A

| | |
|--------------------|--|
| reset noise | Noise due to variation in the reset level of a pixel. In 3T pixel designs, this noise has a component (in units of volts) proportionality constant depending on how the pixel is reset (such as hard and soft). In 4T pixel designs, reset noise can be removed with CDS. |
| responsivity | The standard measure of photodiode performance (regardless of whether it is in an imager or not). Units are typically A/W and are dependent on the incident light wavelength. Note that responsivity and sensitivity are used interchangeably in image sensor characterization literature so it is best to check the units. |
| reverse saturation | Phenomenon in which the signal level decreases with increasing light intensity. It typically occurs at irradiance levels much higher than saturation, such as an image taken of the sun. |
| ROI | Region of interest. The area within a pixel array chosen to characterize noise, signal, crosstalk, and so on. The ROI can be the entire array or a small subsection; it can be confined to a single color plane. |
| row noise | Variation of row mean signal strengths. The human eye is sensitive to line patterns, so this noise is analyzed separately. |
| sense node | In 4T pixel designs, a capacitor used to convert charge into voltage. In 3T pixel designs it is the photodiode itself. |
| sensitivity | A measure of pixel performance that characterizes the rise of the photodiode or sense node signal in Volts upon illumination with light. Units are typically V/(W/m ²)/sec and are dependent on the incident light wavelength. Sensitivity measurements are often taken with 550 nm incident light. At this wavelength, 1 683 lux = 1 W/m ² ; the units of sensitivity are quoted in V/lux/sec. Note that responsivity and sensitivity are used interchangeably in image sensor characterization literature so it is best to check the units. |
| shot noise | Noise that arises from measurements of discretised quanta (electrons or photons). It follows a Poisson distribution with the strength of the noise increasing as the square root of the signal. |
| spectral response | The photon wavelength dependence of sensitivity or responsivity. |
| SNR | Signal-to-noise ratio. This number characterizes the ratio of the fundamental signal to the noise spectrum up to half the Nyquist frequency. |
| temporal noise | Noise that varies from frame to frame. In a video stream, temporal noise is visible as twinkling pixels. |
| tint | Integration time. |

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