0.2 µV/°C Offset Drift, 105 MHz Low Power, Low Noise, Rail-to-Rail Amplifiers

Data Sheet

ADA4805-1/ADA4805-2

FEATURES

- Low input offset voltage: 125 µV (maximum)
- Low input offset voltage drift
  - 0.2 µV/°C (typical)
  - 1.5 µV/°C (maximum)
- Ultralow supply current: 500 µA per amplifier
- Fully specified at V_S = 3 V, 5 V, ±5 V
- High speed performance
  - −3 dB bandwidth: 105 MHz
  - Slew rate: 160 V/µs
  - Settling time to 0.1%: 35 ns
- Rail-to-rail outputs
- Input common-mode range: $-V_S$ − 0.1 V to $+V_S$ − 1 V
- Low noise: 5.9 nV/√Hz at 100 kHz; 0.6 pA/√Hz at 100 kHz
- Low distortion: −102 dBc/−126 dBc HD2/HD3 at 100 kHz
- Low input bias current: 470 nA (typical)
- Dynamic power scaling
  - Turn-on time: 3 µs (maximum) fully settled
- Small packaging
  - 6-lead SC70, 6-lead SOT-23, and 8-lead MSOP

APPLICATIONS

- High resolution, high precision analog-to-digital converter (ADC) drivers
- Battery-powered instrumentation
- Micropower active filters
- Portable point of sales terminals
- Active RFID readers
- Photo multipliers
- ADC reference buffers

GENERAL DESCRIPTION

The ADA4805-1/ADA4805-2 are high speed voltage feedback, rail-to-rail output amplifiers with an exceptionally low quiescent current of 500 µA, making them ideal for low power, high resolution data conversion systems. Despite being low power, these amplifiers provide excellent overall performance. They offer a high bandwidth of 105 MHz at a gain of +1, a high slew rate of 160 V/µs, and a low input offset voltage of 125 µV (maximum).

A shutdown pin allows further reduction of the quiescent supply current to 2.9 µA. For power sensitive applications, the shutdown mode offers a very fast turn-on time of 3 µs. This allows the user to dynamically manage the power of the amplifier by turning the amplifier off between ADC samples.

TYPICAL APPLICATIONS CIRCUIT

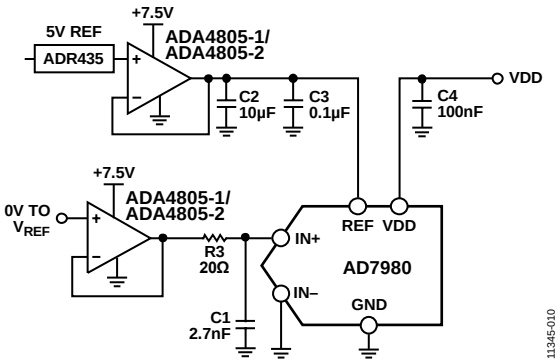

Figure 1. Driving the AD7980 with the ADA4805-1/ADA4805-2

The Analog Devices, Inc., proprietary extra fast complementary bipolar (XFCB) process allows both low voltage and low current noise (5.9 nV/√Hz, 0.6 pA/√Hz). The ADA4805-1/ADA4805-2 operate over a wide range of supply voltages from ±1.5 V to ±5 V, as well as single 3 V and 5 V supplies, making them ideal for high speed, low power instruments.

The ADA4805-1 is available in a 6-lead SOT-23 and a 6-lead SC70 package. The ADA4805-2 is available in an 8-lead MSOP and a 10-lead LFCSP package. These amplifiers are rated to work over the industrial temperature range of −40°C to +125°C.

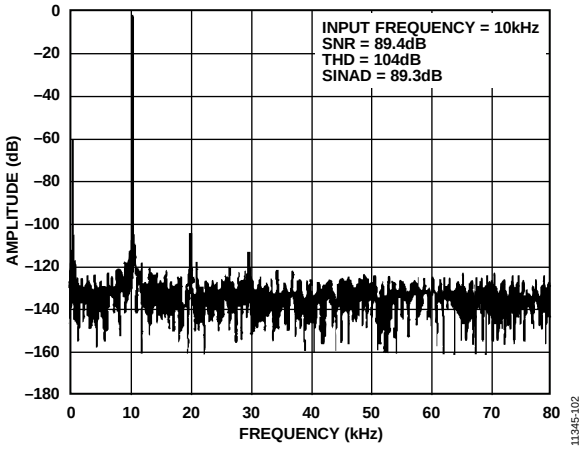

Figure 2. FFT Plot for the Circuit Configuration in Figure 1

Table 1. Complementary ADCs to the ADA4805-1/ADA4805-2

Product	ADC Power (mW)	Throughput (MSPS)	Resolution (Bits)	SNR (dB)
AD7982	7.0	1	18	98
AD7984	10.5	1.33	18	98.5
AD7980	4.0	1	16	91
AD7685	10	0.25	16	88

Rev. B
Document Feedback

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TABLE OF CONTENTS

REVISION HISTORY

12/14—Rev. A to Rev. B

Added 10-Lead LFCSP ... Universal
Changes to $\overline{\text{SHUTDOWN}}$ Current Parameter, Table 2 ... 3
Changes to $\overline{\text{SHUTDOWN}}$ Current Parameter, Table 3 ... 5
Changes to $\overline{\text{SHUTDOWN}}$ Current Parameter, Table 4 ... 6
Changes to Table 6 and Figure 3 ... 7
Changes to Table 8 ... 9
Added Figure 6, Renumbered Sequentially ... 9
Added Figure 42 ... 16
Changed Layout ... 16
Changes to Shutdown Operation Section ... 18
Changes to Dynamic Power Scaling Section and Figure 61 ... 21
Changes to Figure 62 and Figure 63 ... 22
Updated Outline Dimensions ... 25
Changes to Ordering Guide ... 25

9/14—Rev. 0 to Rev. A

Added ADA4805-2 ... Universal
Changes to Features Section, General Description Section, and Table 1 ... 1
Changes to Table 2 ... 3
Changes to Table 3 ... 4
Changes to Table 4 ... 5
Changes to Table 6 and Figure 3 ... 7
Added Figure 6; Renumbered Sequentially; and Table 8; Renumbered Sequentially ... 8
Changes to Figure 7 Caption, Figure 8 Caption, Figure 9 Caption, Figure 10 Caption, and Figure 11 Caption ... 9
Changes to Figure 13 Caption, Figure 14, Figure 17, and Figure 18 ... 10
Change to Figure 29 ... 12
Moved Figure 41 ... 15
Changes to Figure 42 ... 15
Added Figure 43 ... 15
Changes to Figure 47 and Figure 48 ... 16
Changes to Amplifier Description Section, Input Protection Section, Shutdown Operation Section, and Figure 51 ... 17
Changes to Noise Considerations Section and Figure 52 ... 18
Changes to Effect of Feedback Resistor on Frequency Response Section, Compensating Peaking in Large Signal Frequency Response Section, Figure 57, and Driving Low Power, High Resolution Successive Approximation Register (SAR) ADC Section ... 19
Changes to Figure 58, Dynamic Power Scaling Section, Figure 59, and Table 10 ... 20
Change to Figure 60 ... 21
Changes to Single-Ended to Differential Conversion Section, Table 11, and Figure 62 ... 22
Updated Outline Dimensions, Figure 65 ... 24
Changes to Ordering Guide ... 24

7/14—Revision 0: Initial Version

SPECIFICATIONS

±5 V SUPPLY

V_S = ±5 V at T_A = 25°C; R_F = 0 Ω for G = +1; otherwise, R_F = 1 kΩ; R_L = 2 kΩ to ground; unless otherwise noted. All specifications are per amplifier.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	G = +1, V_{OUT} = 0.02 V p-p		120		MHz
	G = +1, V_{OUT} = 2 V p-p		40		MHz
Bandwidth for 0.1 dB Flatness	G = +1, V_{OUT} = 0.02 V p-p		18		MHz
Slew Rate	G = +1, V_{OUT} = 2 V step		190		V/µs
	G = +2, V_{OUT} = 4 V step		250		V/µs
Settling Time to 0.1%	G = +1, V_{OUT} = 2 V step		35		ns
	G = +2, V_{OUT} = 4 V step		78		ns
NOISE/DISTORTION PERFORMANCE					
Harmonic Distortion, HD2/HD3[1]	f_C = 20 kHz, V_{OUT} = 2 V p-p		−114/−140		dBc
	f_C = 100 kHz, V_{OUT} = 2 V p-p		−102/−128		dBc
	f_C = 20 kHz, V_{OUT} = 4 V p-p, G = +1		−109/−143		dBc
	f_C = 100 kHz, V_{OUT} = 4 V p-p, G = +1		−93/−130		dBc
	f_C = 20 kHz, V_{OUT} = 4 V p-p, G = +2		−113/−142		dBc
	f_C = 100 kHz, V_{OUT} = 4 V p-p, G = +2		−96/−130		dBc
Input Voltage Noise	f = 100 kHz		5.2		nV/√Hz
Input Voltage Noise 1/f Corner Frequency			8		Hz
0.1 Hz to 10 Hz Voltage Noise			44		nV rms
Input Current Noise	f = 100 kHz		0.7		pA/√Hz
DC PERFORMANCE					
Input Offset Voltage			13	125	µV
Input Offset Voltage Drift[2]	T_{MIN} to T_{MAX}, 4 σ		0.2	1.5	µV/°C
Input Bias Current			550	800	nA
Input Offset Current			2.1	25	nA
Open-Loop Gain	V_{OUT} = −4.0 V to +4.0 V	107	111		dB
INPUT CHARACTERISTICS					
Input Resistance					
Common Mode			50		MΩ
Differential Mode			260		kΩ
Input Capacitance			1		pF
Input Common-Mode Voltage Range		−5.1		+4	V
Common-Mode Rejection Ratio	$V_{IN, CM}$ = −4.0 V to +4.0 V	103	130		dB
$\overline{\text{SHUTDOWN}}$ PIN					
$\overline{\text{SHUTDOWN}}$ Voltage					
Low	Powered down		<−1.3		V
High	Enabled		>−0.9		V
$\overline{\text{SHUTDOWN}}$ Current					
Low	Powered down	−1.0	0.2		µA
High	Enabled		0.02	1.0	µA
Turn-Off Time	50% of $\overline{\text{SHUTDOWN}}$ to <10% of enabled quiescent current		1.25	2.75	µs
Turn-On Time	50% of $\overline{\text{SHUTDOWN}}$ to >90% of final V_{OUT}		2	3	µs
OUTPUT CHARACTERISTICS					
Output Overdrive Recovery Time (Rising/Falling Edge)	V_{IN} = +6 V to −6 V, G = +2		95/100		ns
Output Voltage Swing	R_L = 2 kΩ	−4.98		+4.98	V

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Short-Circuit Current	Sinking/sourcing		85/73		mA
Linear Output Current	<1% THD at 100 kHz, V_{OUT} = 2 V p-p		±58		mA
Off Isolation	V_{IN} = 0.5 V p-p, f = 1 MHz, $\overline{SHUTDOWN}$ = $-V_S$		41		dB
Capacitive Load Drive	30% overshoot		15		pF
POWER SUPPLY					
Operating Range		2.7		10	V
Quiescent Current per Amplifier	Enabled		570	625	µA
	$\overline{SHUTDOWN}$ = $-V_S$		7.4	12	µA
Power Supply Rejection Ratio					
Positive	$+V_S$ = 3 V to 5 V, $-V_S$ = −5 V	100	119		dB
Negative	$+V_S$ = 5 V, $-V_S$ = −3 V to −5 V	100	122		dB

[1] f_C is the fundamental frequency.
[2] Guaranteed, but not tested.

5 V SUPPLY

V_S = 5 V at T_A = 25°C; R_F = 0 Ω for G = +1; otherwise, R_F = 1 kΩ; R_L = 2 kΩ to midsupply; unless otherwise noted. All specifications are per amplifier.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	G = +1, V_{OUT} = 0.02 V p-p		105		MHz
	G = +1, V_{OUT} = 2 V p-p		35		MHz
Bandwidth for 0.1 dB Flatness	G = +1, V_{OUT} = 0.02 V p-p		20		MHz
Slew Rate	G = +1, V_{OUT} = 2 V step		160		V/µs
	G = +2, V_{OUT} = 4 V step		220		V/µs
Settling Time to 0.1%	G = +1, V_{OUT} = 2 V step		35		ns
	G = +2, V_{OUT} = 4 V step		82		ns
NOISE/DISTORTION PERFORMANCE					
Harmonic Distortion, HD2/HD3[1]	f_C = 20 kHz, V_{OUT} = 2 V p-p		−114/−135		dBc
	f_C = 100 kHz, V_{OUT} = 2 V p-p		−102/−126		dBc
	f_C = 20 kHz, G = +2, V_{OUT} = 4 V p-p		−107/−143		dBc
	f_C = 100 kHz, G = +2, V_{OUT} = 4 V p-p		−90/−130		dBc
Input Voltage Noise	f = 100 kHz		5.9		nV/√Hz
Input Voltage Noise 1/f Corner			8		Hz
0.1 Hz to 10 Hz Voltage Noise			54		nV rms
Input Current Noise	f = 100 kHz		0.6		pA/√Hz
DC PERFORMANCE					
Input Offset Voltage			9	125	µV
Input Offset Voltage Drift[2]	T_{MIN} to T_{MAX}, 4 σ		0.2	1.5	µV/°C
Input Bias Current			470	720	nA
Input Offset Current			0.4		nA
Open-Loop Gain	V_{OUT} = 1.25 V to 3.75 V	105	109		dB
INPUT CHARACTERISTICS					
Input Resistance					
Common Mode			50		MΩ
Differential Mode			260		kΩ
Input Capacitance			1		pF
Input Common-Mode Voltage Range		−0.1		+4	V
Common-Mode Rejection Ratio	$V_{IN, CM}$ = 1.25 V to 3.75 V	103	133		dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
$\overline{\text{SHUTDOWN}}$ PIN					
$\overline{\text{SHUTDOWN}}$ Voltage					
Low	Powered down		<1.5		V
High	Enabled		>1.9		V
$\overline{\text{SHUTDOWN}}$ Current					
Low	Powered down	−1.0	0.1		µA
High	Enabled		0.01	1.0	µA
Turn-Off Time	50% of $\overline{\text{SHUTDOWN}}$ to <10% of enabled quiescent current		0.9	1.25	µs
Turn-On Time	50% of $\overline{\text{SHUTDOWN}}$ to >90% of final V_{OUT}		3	4	µs
OUTPUT CHARACTERISTICS					
Overdrive Recovery Time (Rising/Falling Edge)	V_{IN} = −1 V to +6 V, G = +2		130/145		ns
Output Voltage Swing	R_L = 2 kΩ	0.02		4.98	V
Short-Circuit Current	Sinking/sourcing		73/63		mA
Linear Output Current	<1% THD at 100 kHz, V_{OUT} = 2 V p-p		±47		mA
Off Isolation	V_{IN} = 0.5 V p-p, f = 1 MHz, $\overline{\text{SHUTDOWN}}$ = $-V_S$		41		dB
Capacitive Load Drive	30% overshoot		15		pF
POWER SUPPLY					
Operating Range		2.7		10	V
Quiescent Current per Amplifier	Enabled		500	520	µA
	$\overline{\text{SHUTDOWN}}$ = $-V_S$		2.9	4	µA
Power Supply Rejection Ratio					
Positive	$+V_S$ = 1.5 V to 3.5 V, $-V_S$ = −2.5 V	100	120		dB
Negative	$+V_S$ = 2.5 V, $-V_S$ = −1.5 V to −3.5 V	100	126		dB

[1] f_C is the fundamental frequency.
[2] Guaranteed, but not tested.

3 V SUPPLY

V_S = 3 V at T_A = 25°C; R_F = 0 Ω for G = +1; otherwise, R_F = 1 kΩ; R_L = 2 kΩ to midsupply; unless otherwise noted. All specifications are per amplifier.

Table 4.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	G = +1, V_{OUT} = 0.02 V p-p		95		MHz
	G = +1, V_{OUT} = 1 V p-p, $+V_S$ = 2 V, $-V_S$ = −1 V		30		MHz
Bandwidth for 0.1 dB Flatness	G = +1, V_{OUT} = 0.02 V p-p		35		MHz
Slew Rate	G = +1, V_{OUT} = 1 V step, $+V_S$ = 2 V, $-V_S$ = −1 V		85		V/µs
Settling Time to 0.1%	G = +1, V_{OUT} = 1 V step		41		ns
NOISE/DISTORTION PERFORMANCE					
Harmonic Distortion, HD2/HD3[1]	f_C = 20 kHz, V_{OUT} = 1 V p-p, $+V_S$ = 2 V, $-V_S$ = −1 V		−123/−143		dBc
	f_C = 100 kHz, V_{OUT} = 1 V p-p, $+V_S$ = 2 V, $-V_S$ = −1 V		−107/−133		dBc
Input Voltage Noise	f = 100 kHz		6.3		nV/√Hz
Input Voltage Noise 1/f Corner			8		Hz
0.1 Hz to 10 Hz Voltage Noise			55		nV rms
Input Current Noise	f = 100 kHz		0.8		pA/√Hz

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DC PERFORMANCE					
Input Offset Voltage			7	125	μV
Input Offset Voltage Drift[2]	T_{MIN} to T_{MAX}, 4 σ		0.2	1.5	μV/°C
Input Bias Current			440	690	nA
Input Offset Current			0.5		nA
Open-Loop Gain	V_{OUT} = 1.1 V to 1.9 V	100	107		dB
INPUT CHARACTERISTICS					
Input Resistance					
Common Mode			50		MΩ
Differential Mode			260		kΩ
Input Capacitance			1		pF
Input Common-Mode Voltage Range		−0.1		+2	V
Common-Mode Rejection Ratio	$V_{IN, CM}$ = 0.5 V to 2 V	89	117		dB
$\overline{\text{SHUTDOWN}}$ PIN					
$\overline{\text{SHUTDOWN}}$ Voltage					
Low	Powered down		<0.7		V
High	Enabled		>1.1		V
$\overline{\text{SHUTDOWN}}$ Current					
Low	Powered down	−1.0	0.1		μA
High	Enabled		0.01	1.0	μA
Turn-Off Time	50% of $\overline{\text{SHUTDOWN}}$ to <10% of enabled quiescent current		0.9	1.25	μs
Turn-On Time	50% of $\overline{\text{SHUTDOWN}}$ to >90% of final V_{OUT}		7	8	μs
OUTPUT CHARACTERISTICS					
Output Overdrive Recovery Time (Rising/Falling Edge)	V_{IN} = −1 V to +4 V, G = +2		135/175		ns
Output Voltage Swing	R_L = 2 kΩ	0.02		2.98	V
Short-Circuit Current	Sinking/sourcing		65/47		mA
Linear Output Current	<1% THD at 100 kHz, V_{OUT} = 1 V p-p		±40		mA
Off Isolation	V_{IN} = 0.5 V p-p, f = 1 MHz, $\overline{\text{SHUTDOWN}}$ = $-V_S$		41		dB
Capacitive Load Drive	30% overshoot		15		pF
POWER SUPPLY					
Operating Range		2.7		10	V
Quiescent Current per Amplifier	Enabled		470	495	μA
	$\overline{\text{SHUTDOWN}}$ = $-V_S$		1.3	3	μA
Power Supply Rejection Ratio					
Positive	$+V_S$ = 1.5 V to 3.5 V, $-V_S$ = −1.5 V	96	119		dB
Negative	$+V_S$ = 1.5 V, $-V_S$ = −1.5 V to −3.5 V	96	125		dB

[1] f_C is the fundamental frequency.
[2] Guaranteed, but not tested.

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Supply Voltage	11 V
Power Dissipation	See Figure 3
Common-Mode Input Voltage	$-V_S - 0.7$ V to $+V_S + 0.7$ V
Differential Input Voltage	±1 V
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +125°C
Lead Temperature (Soldering, 10 sec)	300°C
Junction Temperature	150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst case conditions, that is, θ_{JA} is specified for a device soldered in a circuit board for surface-mount packages. Table 6 lists the θ_{JA} for the ADA4805-1/ADA4805-2.

Table 6. Thermal Resistance

Package Type	θ_{JA}	Unit
6-Lead SC70	223.6	°C/W
6-Lead SOT-23	209.1	°C/W
8-Lead MSOP	123.8	°C/W
10-Lead LFCSP	51.4	°C/W

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation for the ADA4805-1/ADA4805-2 is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the properties of the plastic change. Even temporarily exceeding this temperature limit may change the stresses that the package exerts on the die, permanently shifting the parametric performance of the ADA4805-1/ADA4805-2. Exceeding a junction temperature of 175°C for an extended period of time can result in changes in silicon devices, potentially causing degradation or loss of functionality.

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the die due to the ADA4805-1/ADA4805-2 output load drive.

The quiescent power dissipation is the voltage between the supply pins (V_S) multiplied by the quiescent current (I_S).

$$P_D = Quiescent\ Power + (Total\ Drive\ Power - Load\ Power)$$

$$P_D = (V_S \times I_S) + \left(\frac{V_S}{2} \times \frac{V_{OUT}}{R_L}\right) - \frac{V_{OUT}^2}{R_L}$$

RMS output voltages must be considered. If R_L is referenced to $-V_S$, as in single-supply operation, the total drive power is $V_S \times I_{OUT}$. If the rms signal levels are indeterminate, consider the worst case, when $V_{OUT} = V_S/4$ for R_L to midsupply.

$$P_D = (V_S \times I_S) + \frac{(V_S/4)^2}{R_L}$$

In single-supply operation with R_L referenced to $-V_S$, worst case is $V_{OUT} = V_S/2$.

Airflow increases heat dissipation, effectively reducing θ_{JA}. Also, more metal directly in contact with the package leads and exposed pad from metal traces, through holes, ground, and power planes reduces θ_{JA}.

Figure 3 shows the maximum safe power dissipation in the package vs. the ambient temperature on a JEDEC standard, 4-layer board. θ_{JA} values are approximations.

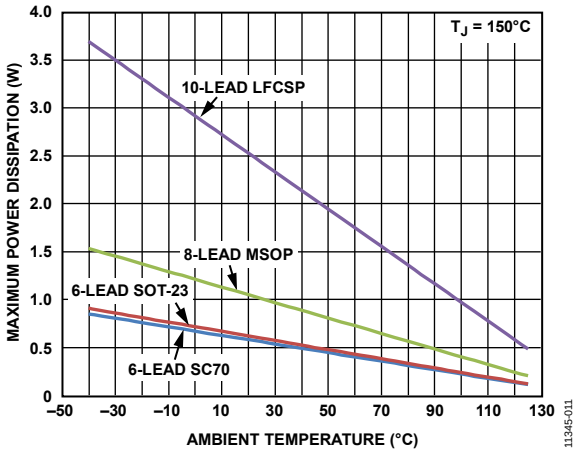


Figure 3. Maximum Power Dissipation vs. Temperature for a 4-Layer Board

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

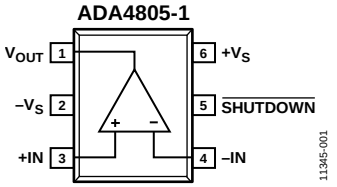


Figure 4. 6-Lead SC70 Pin Configuration

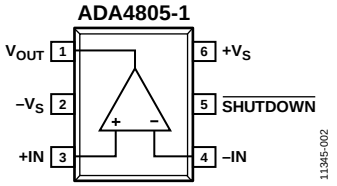


Figure 5. 6-Lead SOT-23 Pin Configuration

Table 7. ADA4805-1 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{OUT}	Output.
2	$-V_S$	Negative Supply.
3	+IN	Noninverting Input.
4	−IN	Inverting Input.
5	$\overline{\text{SHUTDOWN}}$	Active Low Power-Down.
6	$+V_S$	Positive Supply.

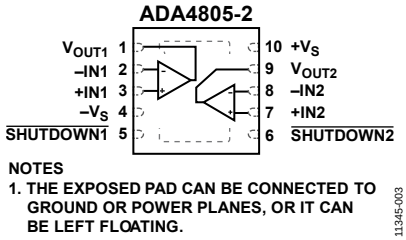


Figure 6. 10-Lead LFCSP Pin Configuration

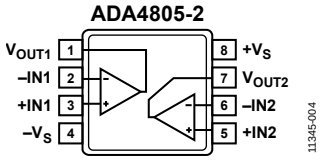


Figure 7. 8-Lead MSOP Pin Configuration

Table 8. ADA4805-2 Pin Function Descriptions

Pin No.			
10-Lead LFCSP	**8-Lead MSOP[1]**	**Mnemonic**	**Description**
1	1	V_{OUT1}	Output 1.
2	2	–IN1	Inverting Input 1.
3	3	+IN1	Noninverting Input 1.
4	4	$-V_S$	Negative Supply.
5	N/A	$\overline{\text{SHUTDOWN1}}$	Active Low Power-Down 1.
6	N/A	$\overline{\text{SHUTDOWN2}}$	Active Low Power-Down 2.
7	5	+IN2	Noninverting Input 2.
8	6	–IN2	Inverting Input 2.
9	7	V_{OUT2}	Output 2.
10	8	$+V_S$	Positive Supply.
	N/A	EPAD	Exposed Pad. For the 10-Lead LFCSP, the EPAD can be connected to ground or power planes, or it can be left floating.

[1] N/A means not applicable.

TYPICAL PERFORMANCE CHARACTERISTICS

R_L = 2 kΩ, unless otherwise noted. When G = +1, R_F = 0 Ω.

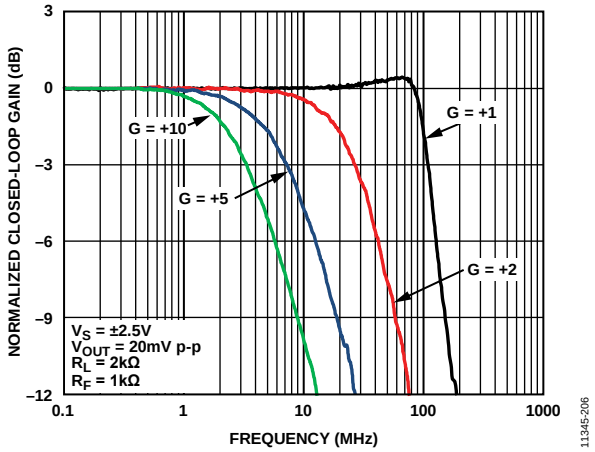


Figure 8. Small Signal Frequency Response for Various Gains

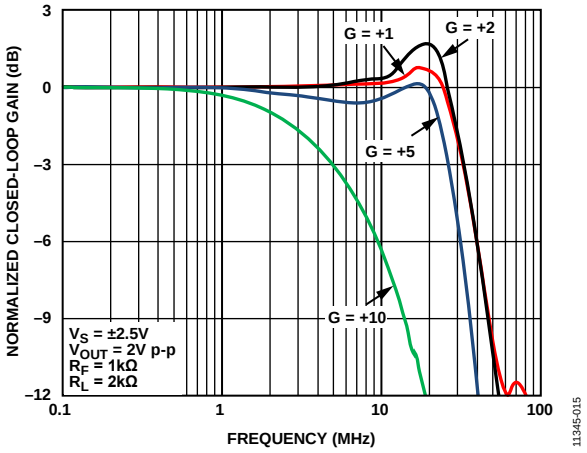


Figure 11. Large Signal Frequency Response for Various Gains

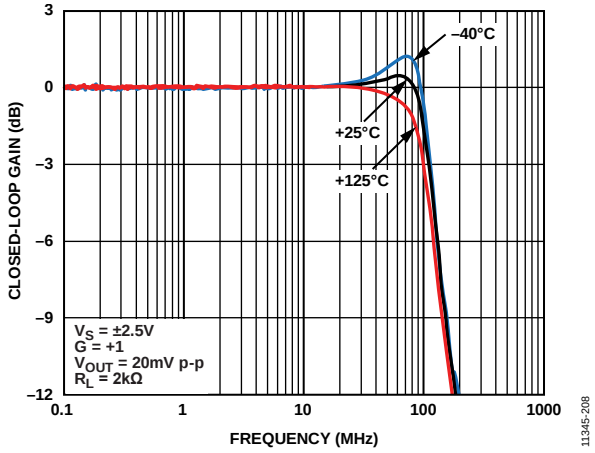


Figure 9. Small Signal Frequency Response for Various Temperatures

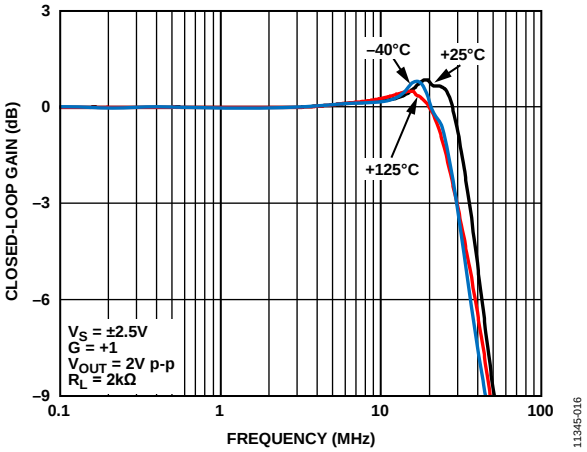


Figure 12. Large Signal Frequency Response for Various Temperatures

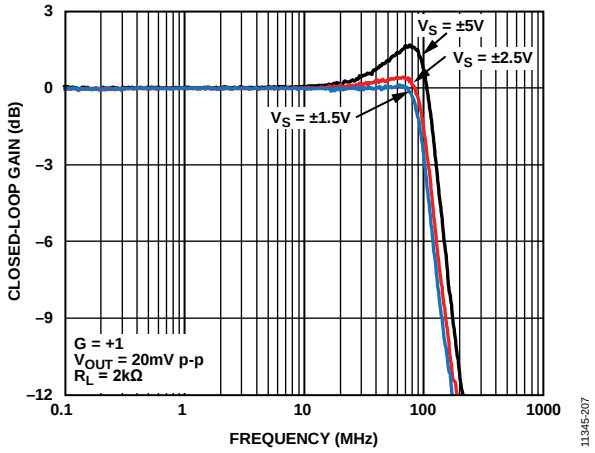


Figure 10. Small Signal Frequency Response for Various Supply Voltages

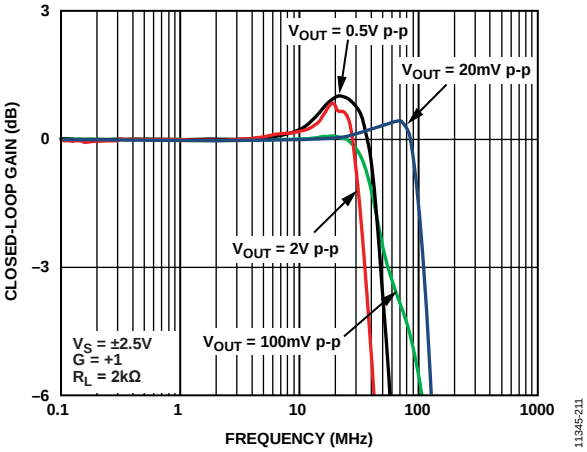


Figure 13. Frequency Response for Various Output Voltages

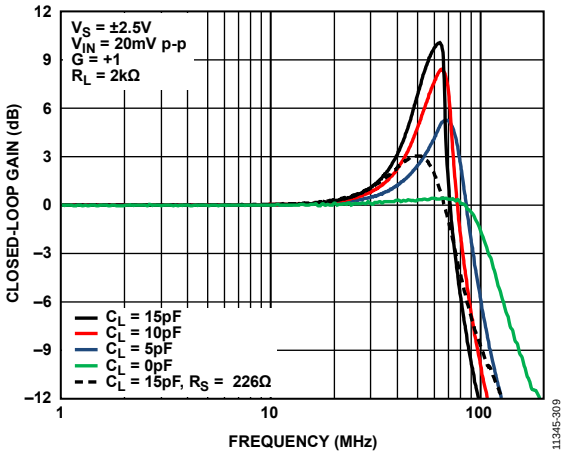


Figure 14. Small Signal Frequency Response for Various Capacitive Loads (See Figure 46)

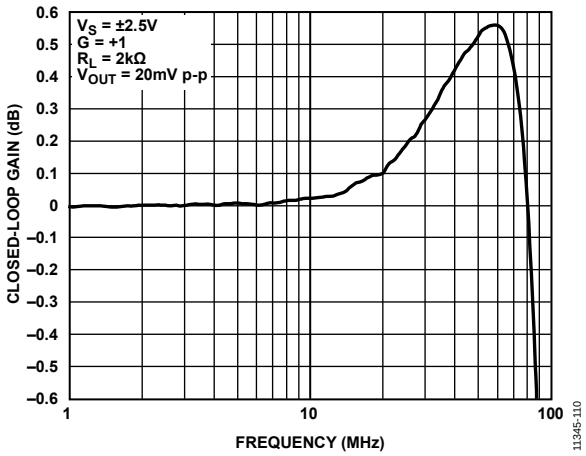


Figure 17. Small Signal 0.1 dB Bandwidth

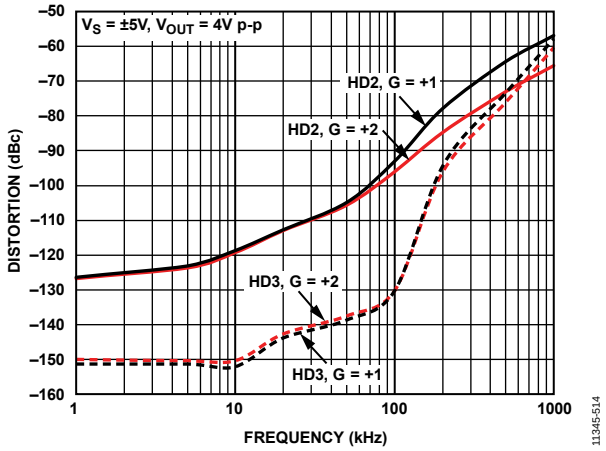


Figure 15. Distortion vs. Frequency for Various Gains

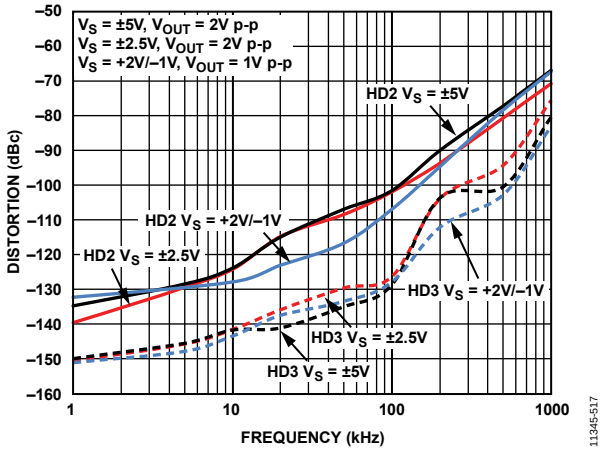


Figure 18. Distortion vs. Frequency for Various Supplies, G = +1

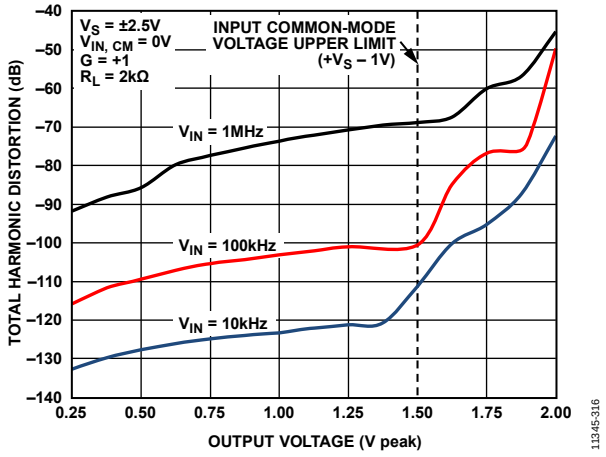


Figure 16. Total Harmonic Distortion vs. Output Voltage For Various Frequencies

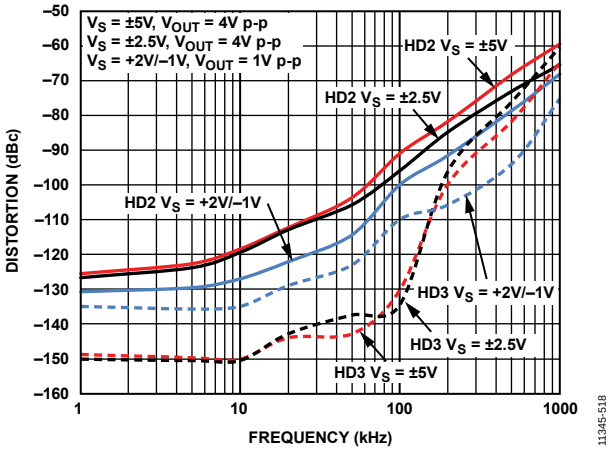


Figure 19. Distortion vs. Frequency, G = +2

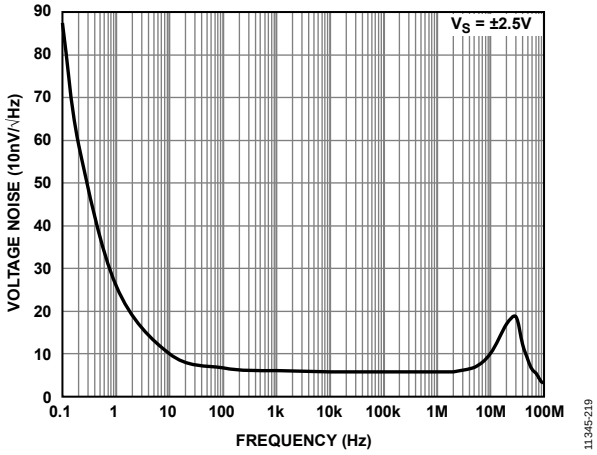


Figure 20. Voltage Noise vs. Frequency

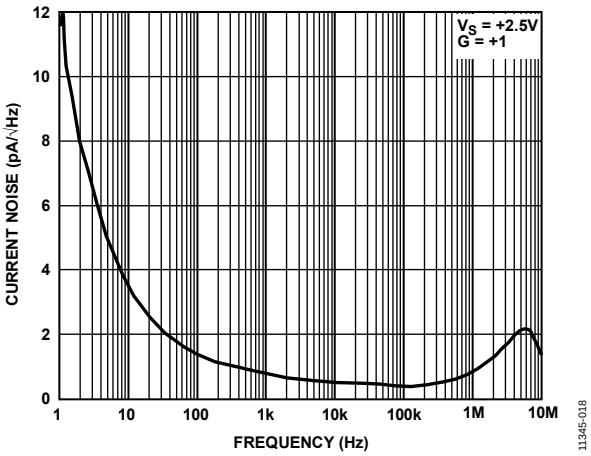


Figure 23. Current Noise vs. Frequency (See Figure 47)

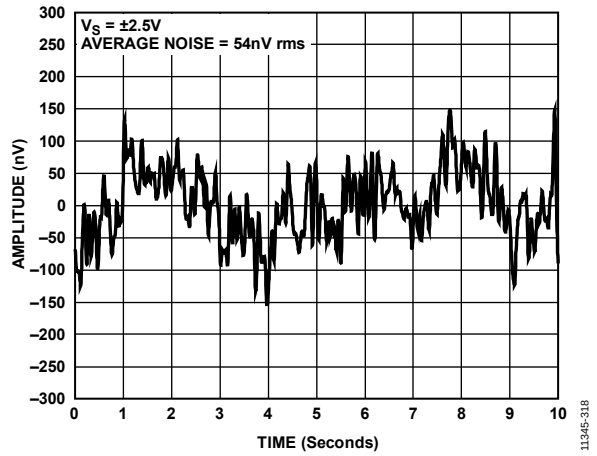


Figure 21. 0.1 Hz to 10 Hz Voltage Noise

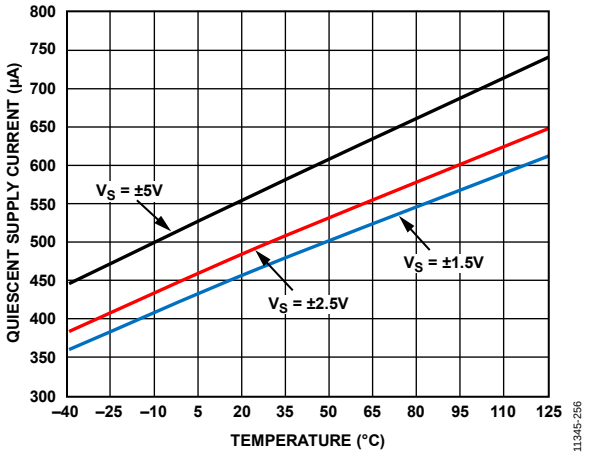


Figure 24. Quiescent Supply Current vs. Temperature for Various Supplies

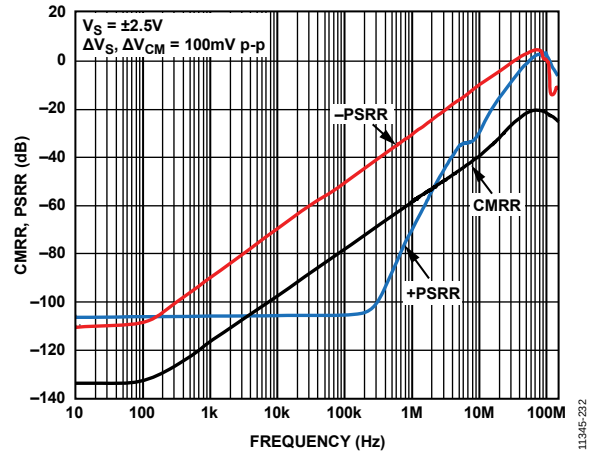


Figure 22. CMRR, PSRR vs. Frequency

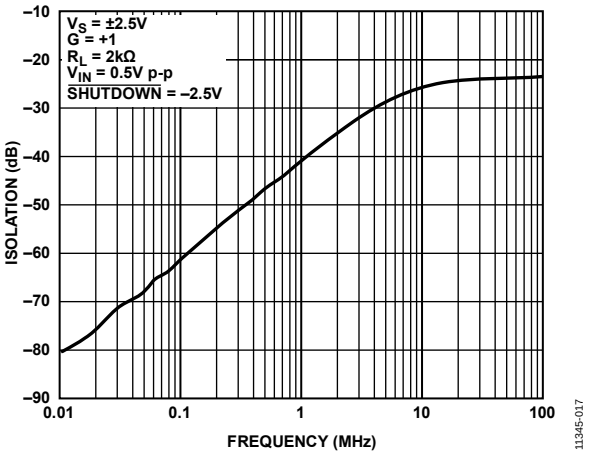


Figure 25. Forward/Off Isolation vs. Frequency

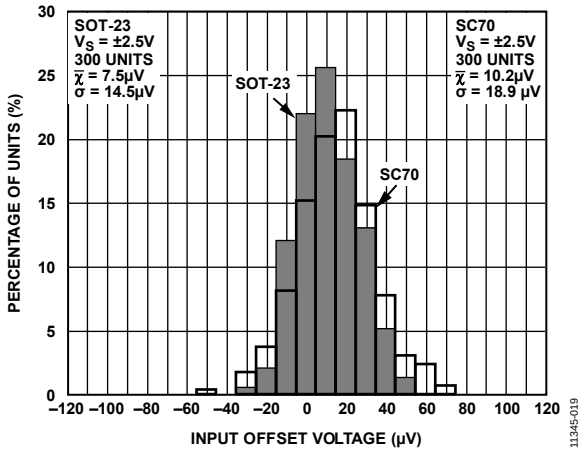


Figure 26. Input Offset Voltage Distribution

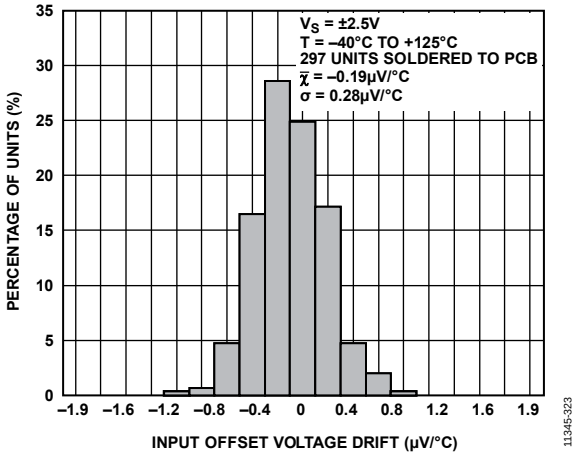


Figure 29. Input Offset Voltage Drift Distribution

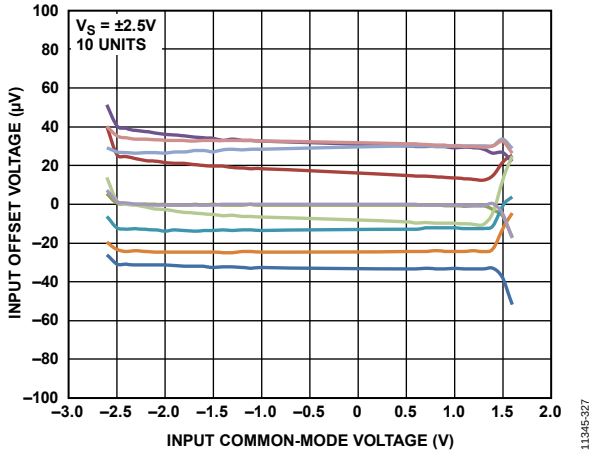


Figure 27. Input Offset Voltage vs. Input Common-Mode Voltage

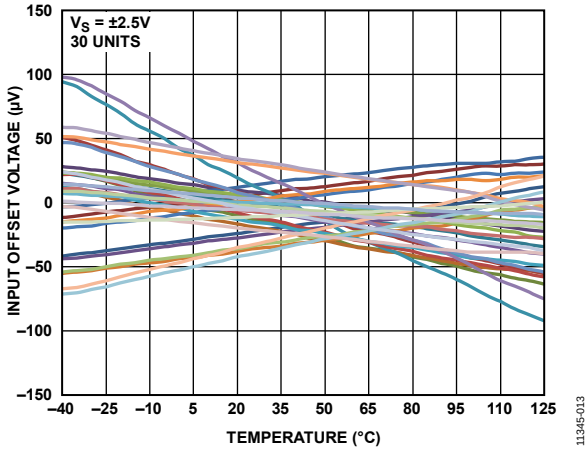


Figure 30. Input Offset Voltage vs. Temperature

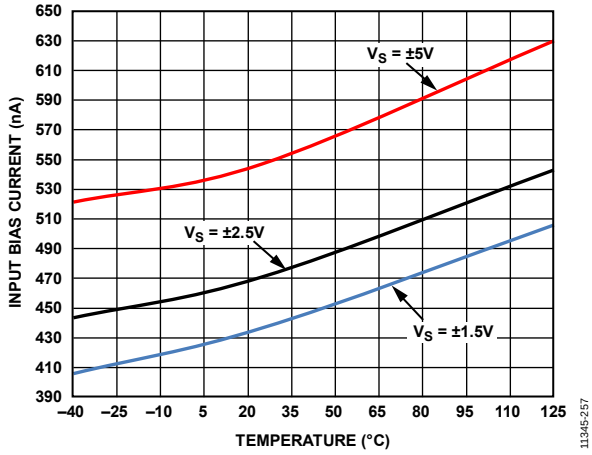


Figure 28. Input Bias Current vs. Temperature for Various Supplies (See Figure 48)

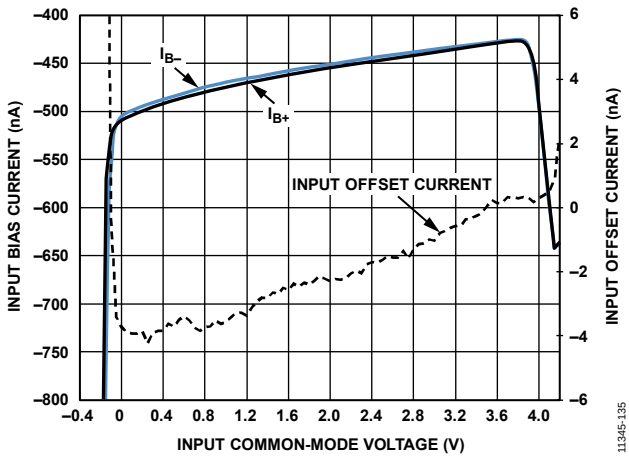


Figure 31. Input Bias Current and Input Offset Current vs. Input Common-Mode Voltage

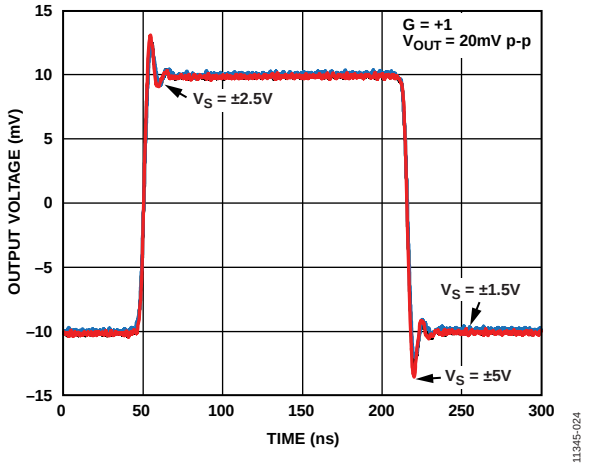


Figure 32. Small Signal Transient Response for Various Supplies, G = +1

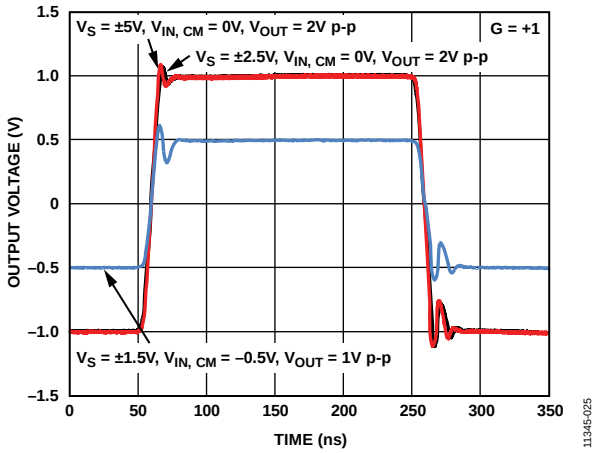


Figure 35. Large Signal Transient Response for Various Supplies, G = +1

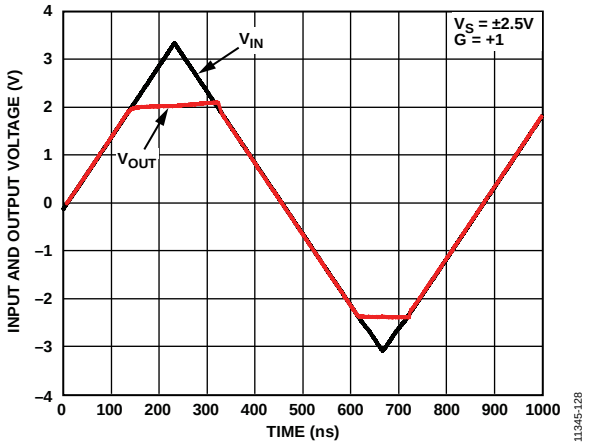


Figure 33. Input Overdrive Recovery Time, G = +1

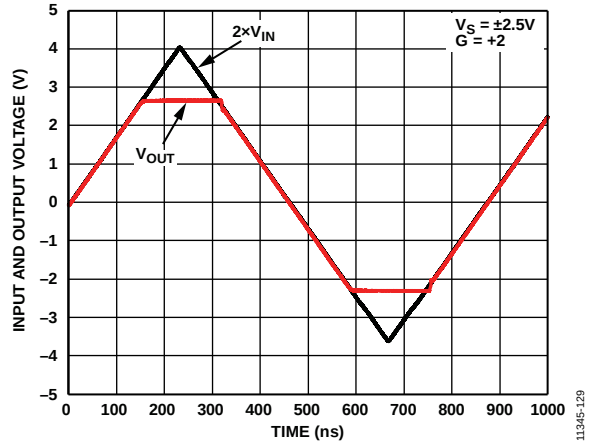


Figure 36. Output Overdrive Recovery Time, G = +2

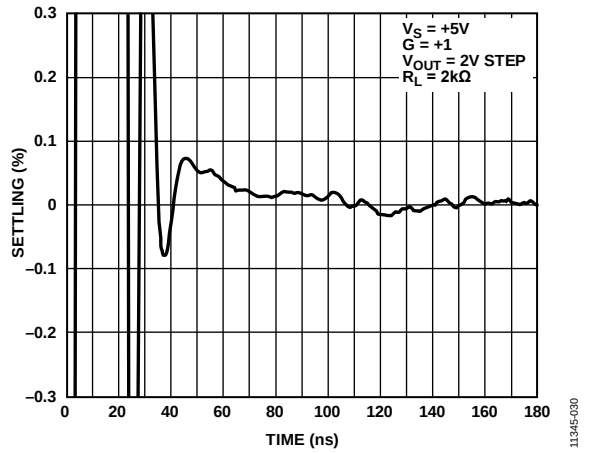


Figure 34. Settling Time to 0.1%

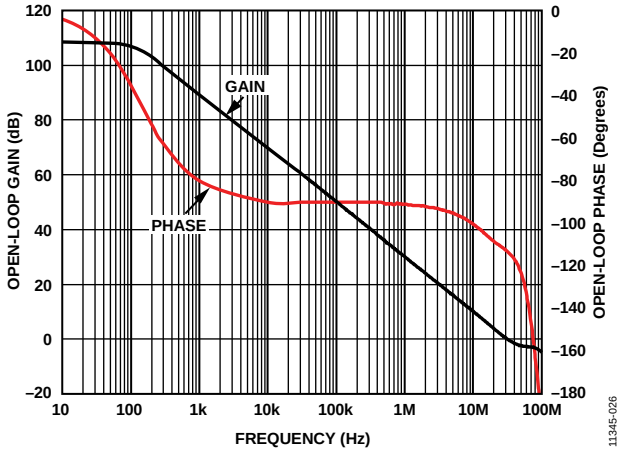


Figure 37. Open-Loop Gain and Phase Margin

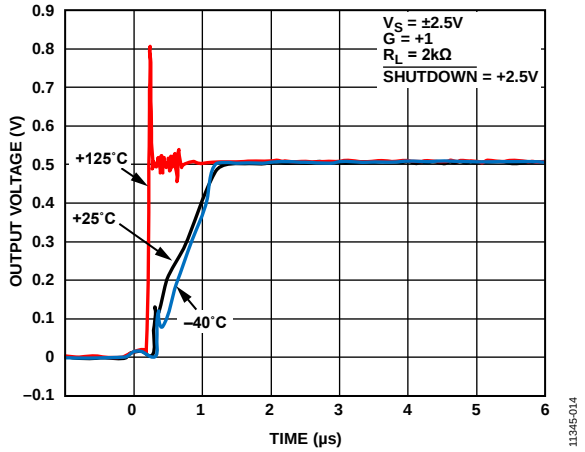


Figure 38. Turn-On Response Time for Various Temperatures (See Figure 49)

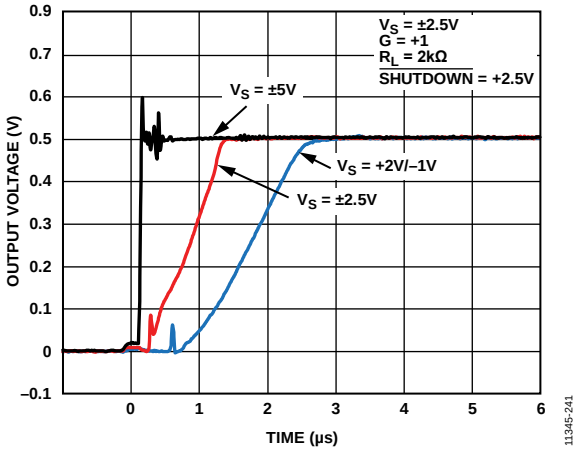


Figure 40. Turn-On Response Time for Various Supplies (See Figure 49)

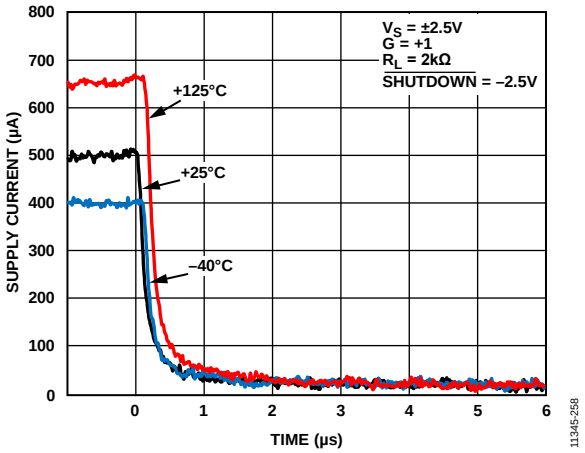


Figure 39. Turn-Off Response Time for Various Temperatures (See Figure 50)

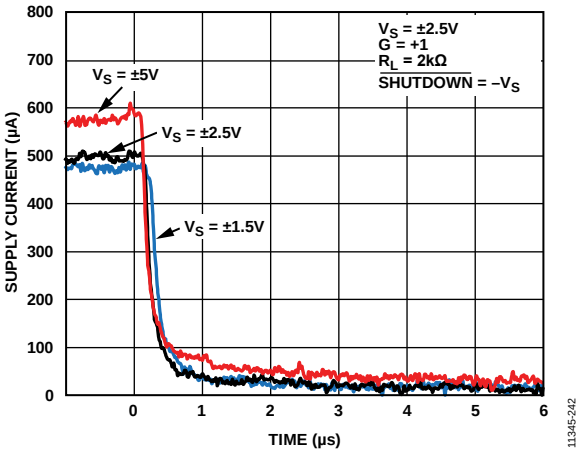


Figure 41. Turn-Off Response Time for Various Supplies (See Figure 50)

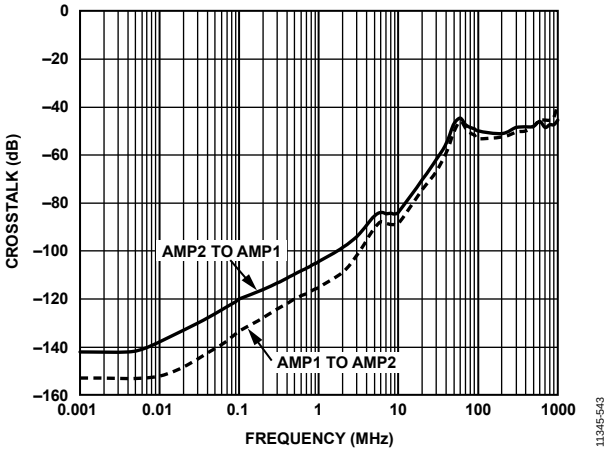


Figure 42. Crosstalk vs. Frequency (LFCSP)

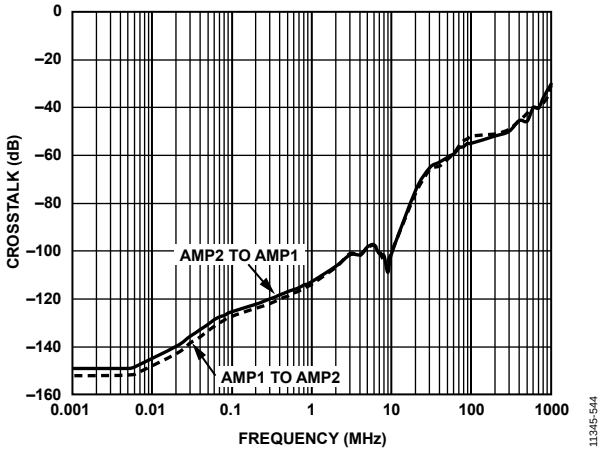


Figure 44. Crosstalk vs. Frequency (MSOP)

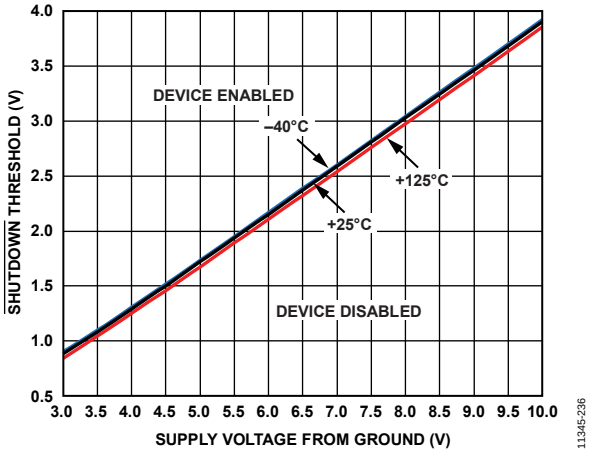


Figure 43. $\overline{SHUTDOWN}$ Threshold vs. Supply Voltage from Ground for Various Temperatures

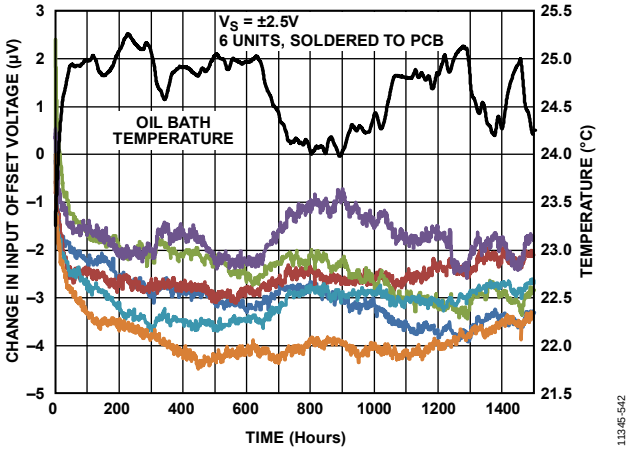


Figure 45. Long-Term V_{OS} Drift

TEST CIRCUITS

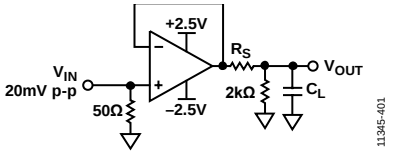


Figure 46. Output Capacitive Load Behavior Test Circuit (See Figure 14)

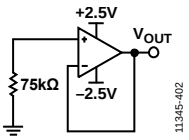


Figure 47. Current Noise Test Circuit (See Figure 23)

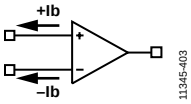


Figure 48. Input Bias Current Temperature Test Circuit (See Figure 28)

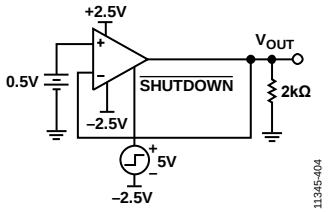


Figure 49. Turn-On Response Test Circuit (See Figure 38 and Figure 40)

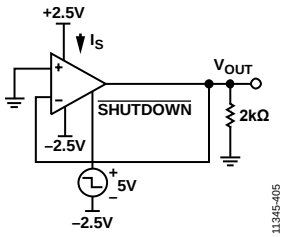


Figure 50. Turn-Off Response Test Circuit (See Figure 39 and Figure 41)

THEORY OF OPERATION

AMPLIFIER DESCRIPTION

The ADA4805-1/ADA4805-2 have a bandwidth of 105 MHz and a slew rate of 160 V/µs. They have an input referred voltage noise of only 5.9 nV/√Hz. The ADA4805-1/ADA4805-2 operate over a supply voltage range of 2.7 V to 10 V and consume only 500 µA of supply current at V_S = 5 V. The low end of the supply range allows for −10% variation of a 3 V supply. The amplifiers are unity-gain stable, and the input structure results in an extremely low input 1/f noise. The ADA4805-1/ADA4805-2 use a slew enhancement architecture, as shown in Figure 51. The slew enhancement circuit detects the absolute difference between the two inputs. It then modulates the tail current, I_{TAIL}, of the input stage to boost the slew rate. The architecture allows higher slew rate and fast settling time with low quiescent current while maintaining low noise.

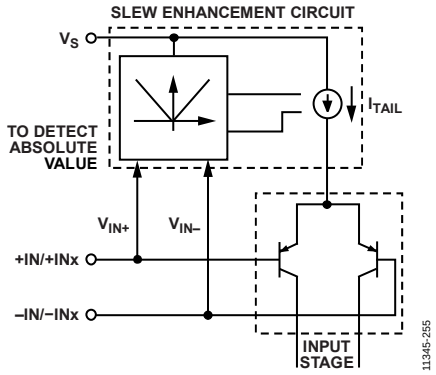


Figure 51. Slew Enhancement Circuit

INPUT PROTECTION

The ADA4805-1/ADA4805-2 are fully protected from ESD events, withstanding human body model ESD events of ±3.5 kV and charged device model events of ±1.25 kV with no measured performance degradation. The precision input is protected with an ESD network between the power supplies and diode clamps across the input device pair, as shown in Figure 52.

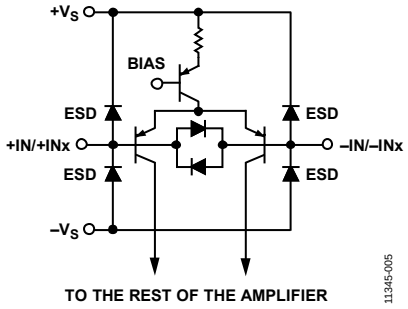


Figure 52. Input Stage and Protection Diodes

For differential voltages above approximately 1.2 V at room temperature, and 0.8 V at 125°C, the diode clamps begin to conduct. If large differential voltages must be sustained across the input terminals, the current through the input clamps must be limited to less than 10 mA. Series input resistors that are sized appropriately for the expected differential overvoltage provide the needed protection.

The ESD clamps begin to conduct for input voltages that are more than 0.7 V above the positive supply and input voltages more than 0.7 V below the negative supply. If an overvoltage condition is expected, the input current must be limited to less than 10 mA.

SHUTDOWN OPERATION

Figure 53 shows the ADA4805-1/ADA4805-2 shutdown circuitry. To maintain very low supply current in shutdown mode, no internal pull-up resistor is supplied; therefore, the $\overline{\text{SHUTDOWN}}$ pin must be driven high or low externally and not be left floating. Pulling the $\overline{\text{SHUTDOWN}}$ pin to ≥1 V below midsupply turns the device off, reducing the supply current to 2.9 µA for a 5 V supply. When the amplifier is powered down, its output enters a high impedance state. The output impedance decreases as frequency increases. In shutdown mode, a forward isolation of −62 dB can be achieved at 100 kHz (see Figure 25).

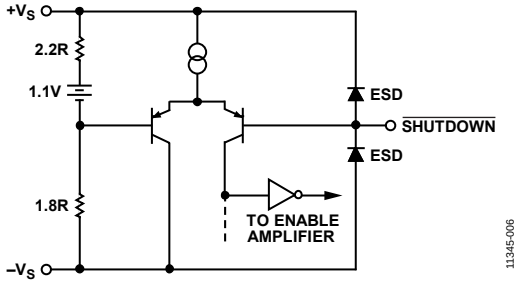


Figure 53. Shutdown Circuit

The $\overline{\text{SHUTDOWN}}$ pin is protected by ESD clamps, as shown in Figure 53. Voltages beyond the power supplies cause these diodes to conduct. To protect the $\overline{\text{SHUTDOWN}}$ pin, ensure that the voltage to this pin does not exceed 0.7 V above the positive supply or 0.7 V below the negative supply. If an overvoltage condition is expected, the input current must be limited to less than 10 mA with a series resistor. Table 9 summarizes the threshold voltages for the powered down and enabled modes for various supplies.

Table 9. Threshold Voltages for Powered Down and Enabled Modes

Mode	+3 V	+5 V	±5 V	+7 V/−2 V
Enabled	>+1.1 V	>+1.9 V	>−0.9 V	>+1.52 V
Powered Down	<+0.7 V	<+1.5 V	<−1.3 V	<+1.52 V

NOISE CONSIDERATIONS

Figure 54 illustrates the primary noise contributors for the typical gain configurations. The total output noise (v_{n_out}) is the root sum square of all the noise contributions.

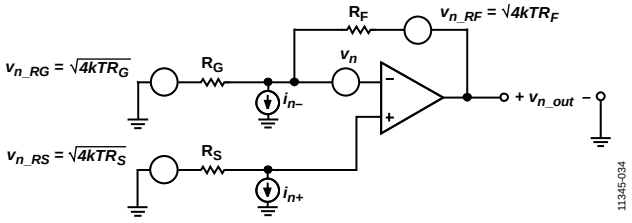


Figure 54. Noise Sources in Typical Connection

The output noise spectral density is calculated by

$$v_{n\_out} = \sqrt{4kTR_F + \left(1+\frac{R_F}{R_G}\right)^2\left[4kTRs + i_{n+}{}^2R_S{}^2 + v_n{}^2\right] + \left(\frac{R_F}{R_G}\right)^2 4kTR_G + i_{n-}{}^2 R_F{}^2}$$

where:

k is Boltzmann's constant.

T is the absolute temperature in degrees Kelvin.

R_F and R_G are the feedback network resistances, as shown in Figure 54.

R_S is the source resistance, as shown in Figure 54.

i_{n+} and i_{n-} represent the amplifier input current noise spectral density in pA/√Hz.

v_n is the amplifier input voltage noise spectral density in nV/√Hz.

Source resistance noise, amplifier input voltage noise (v_n), and the voltage noise from the amplifier input current noise ($i_{n+} \times R_S$) are all subject to the noise gain term ($1 + R_F/R_G$).

Figure 55 shows the total referred to input (RTI) noise due to the amplifier vs. the source resistance. Note that with a 5.9 nV/√Hz input voltage noise and 0.6 pA/√Hz input current noise, the noise contributions of the amplifier are relatively small for source resistances from approximately 2.6 kΩ to 47 kΩ.

The Analog Devices silicon germanium (SiGe) bipolar process makes it possible to achieve a low noise of 5.9 nV/√Hz for the ADA4805-1/ADA4805-2. This noise is much improved compared to similar low power amplifiers with a supply current in the range of hundreds of microamperes.

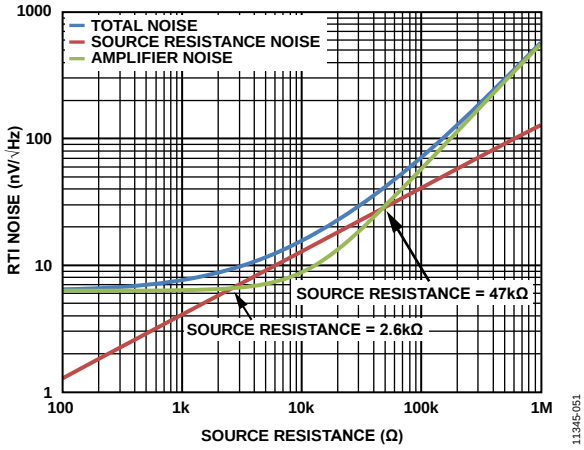


Figure 55. RTI Noise vs. Source Resistance

APPLICATIONS INFORMATION

SLEW ENHANCEMENT

The ADA4805-1/ADA4805-2 have an internal slew enhancement circuit that increases the slew rate as the feedback error voltage increases. This circuit allows the amplifier to settle a large step response faster, as shown in Figure 56. This is useful in ADC applications where multiple input signals are multiplexed. The impact of the slew enhancement can also be seen in the large signal frequency response, where larger input signals cause a slight increase in peaking, as shown in Figure 57.

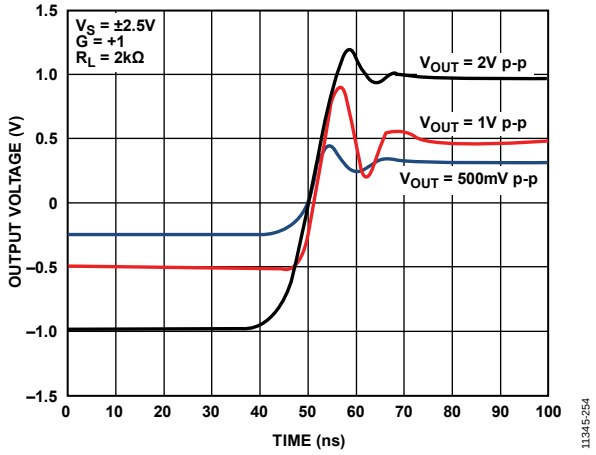


Figure 56. Step Response with Selected Output Steps

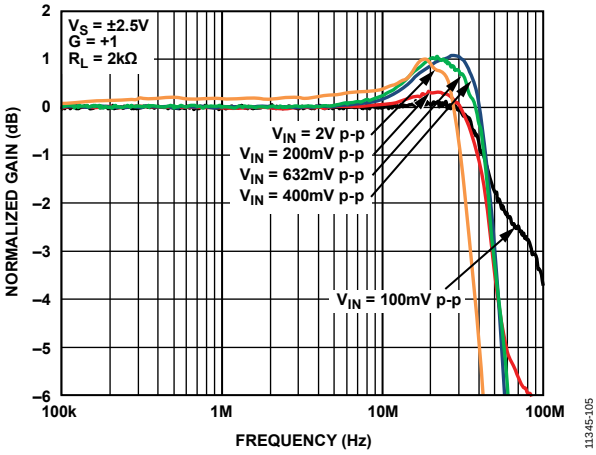


Figure 57. Peaking in Frequency Responses as Signal Level Changes, G = +1

EFFECT OF FEEDBACK RESISTOR ON FREQUENCY RESPONSE

The amplifiers input capacitance and feedback resistor form a pole that, for larger value feedback resistors, can reduce phase margin and contribute to peaking in the frequency response. Figure 58 shows the peaking for selected feedback resistors (R_F) when the amplifier is configured in a gain of +2. Figure 58 also shows how peaking can be mitigated with the addition of a small value capacitor placed across the feedback resistor of the amplifier.

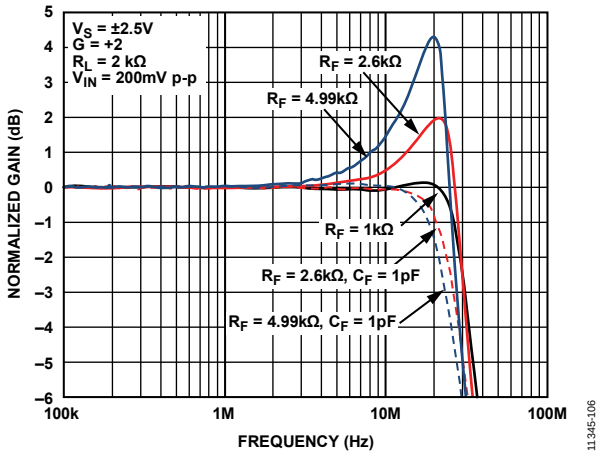


Figure 58. Peaking in Frequency Response at Selected R_F Values

COMPENSATING PEAKING IN LARGE SIGNAL FREQUENCY RESPONSE

At high frequency, the slew enhancement circuit can contribute to peaking in the large signal frequency response. Figure 58 shows the effect of a feedback capacitor on the small signal response, whereas Figure 59 shows that the same technique is effective for reducing peaking in the large signal response.

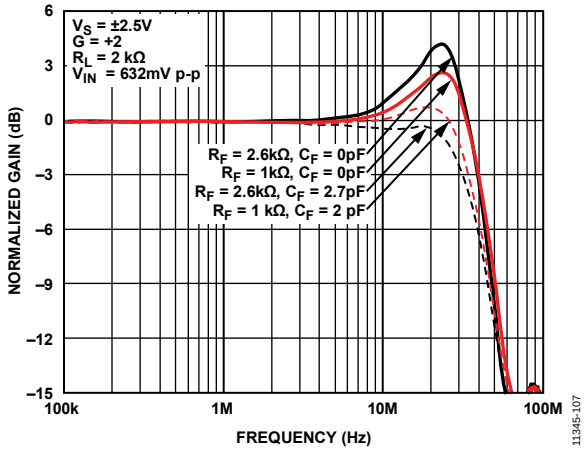


Figure 59. Peaking Mitigation in Large Signal Frequency Response

DRIVING LOW POWER, HIGH RESOLUTION SUCCESSIVE APPROXIMATION REGISTER (SAR) ADCs

The ADA4805-1/ADA4805-2 are ideal for driving low power, high resolution SAR ADCs. The 5.9 nV/√Hz input voltage noise and rail-to-rail output stage of the ADA4805-1/ADA4805-2 help to minimize distortion at large output levels. With its low power of 500 µA, the amplifier consumes power that is compatible with low power SAR ADCs, which are usually in the microwatt (µW) to low milliwatt (mW) range. Furthermore, the ADA4805-1/ADA4805-2 support a single-supply configuration; their input common-mode range extends to 0.1 V below the negative supply, and 1 V below the positive supply.

Figure 60 shows a typical 16-bit, single-supply application. The ADA4805-1/ADA4805-2 drive the AD7980, a 16-bit, 1 MSPS, SAR ADC in a low power configuration. The AD7980 operates on a 2.5 V supply and supports an input from 0 V to V_{REF}. In this case, the ADR435 provides a 5 V reference. The ADA4805-1/ADA4805-2 are used both as a driver for the AD7980 and as a reference buffer for the ADR435.

The low-pass filter formed by R3 and C1 reduces the noise to the input of the ADC (see Figure 60). In lower frequency applications, the designer can reduce the corner frequency of the filter to remove additional noise.

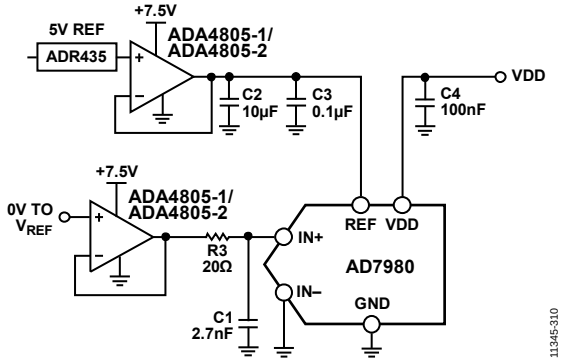


Figure 60. Driving the AD7980 with the ADA4805-1/ADA4805-2

In this configuration, the ADA4805-1/ADA4805-2 consume 7.2 mW of quiescent power. The measured signal-to-noise ratio (SNR), total harmonic distortion (THD), and signal-to-noise-and-distortion ratio (SINAD) of the whole system for a 10 kHz signal are 89.4 dB, 104 dBc, and 89.3 dB, respectively. This translates to an effective number of bits (ENOB) of 14.5 at 10 kHz, which is compatible with the AD7980 performance. Table 10 shows the performance of this setup at selected input frequencies.

DYNAMIC POWER SCALING

One of the merits of a SAR ADC, like the AD7980, is that its power scales with the sampling rate. This power scaling makes SAR ADCs very power efficient, especially when running at a low sampling frequency. However, the ADC driver used with the SAR ADC traditionally consumes constant power regardless of the sampling frequency.

Figure 61 illustrates a method by which the quiescent power of the ADC driver can be dynamically scaled with the sampling rate of the system. By providing properly timed signals to the convert start (CNV) pin of the ADC and the $\overline{\text{SHUTDOWN}}$ pin of the ADA4805-1/ADA4805-2, both devices can be run at optimum efficiency.

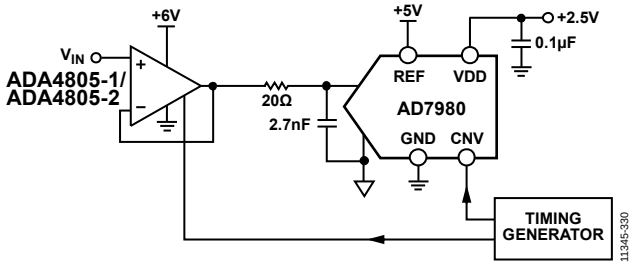


Figure 61. ADA4805-1/ADA4805-2/AD7980 Power Management Circuitry

Figure 62 illustrates the relative signal timing for power scaling the ADA4805-1/ADA4805-2 and the AD7980. To prevent any degradation in the performance of the ADC, the ADA4805-1/ADA4805-2 must have a fully settled output into the ADC before the activation of the CNV pin. In this example, the amplifier is switched to full power mode 3 µs prior to the rising edge of the CNV signal. The $\overline{\text{SHUTDOWN}}$ pin of the ADA4805-1/ADA4805-2 is pulled low when the ADC input is inactive in between samples. The quiescent current of the amplifier typically falls to 10% of the normal operating value within 0.9 µs at V_S = 5 V. While in shutdown mode, the ADA4805-1/ADA4805-2 output impedance is high.

Table 10. System Performance at Selected Input Frequency for Driving the AD7980 Single-Ended

	ADC Driver		Reference Buffer		Results			
Input Frequency (kHz)	Supply (V)	Gain	Supply (V)	Gain	SNR (dB)	THD (dBc)	SINAD (dB)	ENOB
1	7.5	1	7.5	1	89.8	103	89.6	14.6
10	7.5	1	7.5	1	89.4	104	89.3	14.5
20	7.5	1	7.5	1	89.9	103	89.7	14.6
50	7.5	1	7.5	1	88.5	99	88.1	14.3
100	7.5	1	7.5	1	86.3	93.7	85.6	13.9

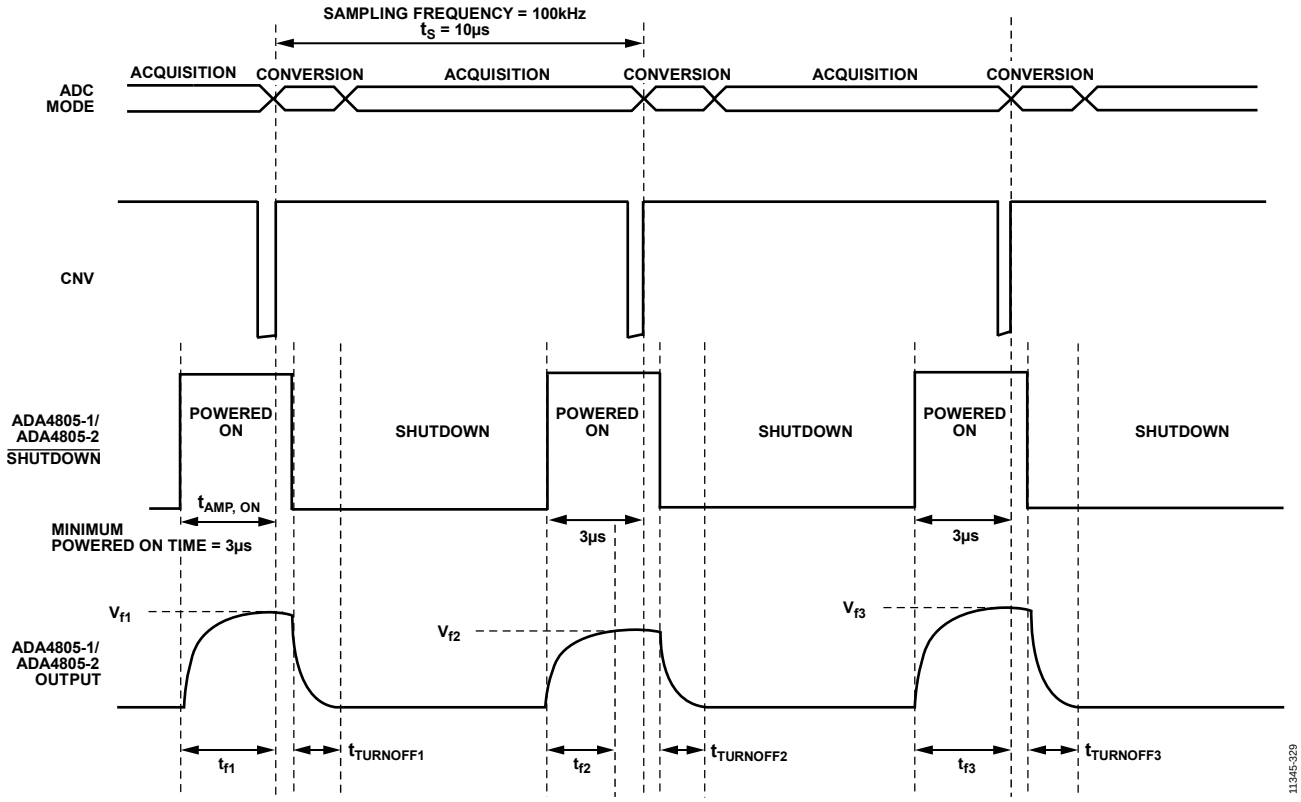


Figure 62. Timing Waveforms

Figure 63 shows the quiescent power of the ADA4805-1/ ADA4805-2 with and without the power scaling. Without power scaling, the ADA4805-1/ADA4805-2 consumes constant power regardless of the sampling frequency, as shown in Equation 1.

$$P_Q = I_Q \times V_S \quad (1)$$

With power scaling, the quiescent power becomes proportional to the ratio between the amplifier on time, $t_{AMP, ON}$, and the sampling time, t_S:

$$P_Q = I_Q \times V_S \times \frac{t_{AMP,ON}}{t_S} \quad (2)$$

Thus, by dynamically switching the ADA4805-1/ADA4805-2 between shutdown and full power modes between consecutive samples, the quiescent power of the driver scales with the sampling rate.

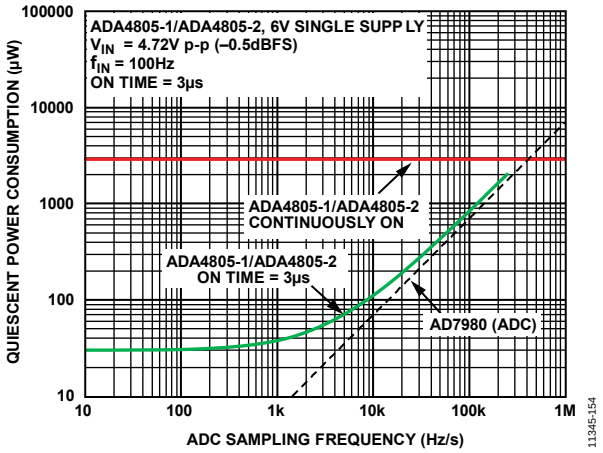


Figure 63. Quiescent Power Consumption of the ADA4805-1/ADA4805-2 vs. ADC Sampling Frequency

SINGLE-ENDED TO DIFFERENTIAL CONVERSION

Most high resolution ADCs have differential inputs to reduce common-mode noise and harmonic distortion. Therefore, it is necessary to use an amplifier to convert a single-ended signal into a differential signal to drive the ADCs.

There are two common ways the user can convert a single-ended signal into a differential signal: either use a differential amplifier, or configure two amplifiers as shown in Figure 64. The use of a differential amplifier yields better performance, whereas the 2-op-amp solution results in lower system cost. The ADA4805-1/ADA4805-2 solve this dilemma of choosing between the two methods by combining the advantages of both. Their low harmonic distortion, low offset voltage, and low bias current mean that they can produce a differential output that is well matched with the performance of the high resolution ADCs.

Figure 64 shows how the ADA4805-1/ADA4805-2 convert a single-ended signal into a differential output. The first amplifier is configured in a gain = +1 with its output then inverted to produce the complementary signal. The differential output then drives the AD7982, an 18-bit, 1 MSPS SAR ADC. To further reduce noise, the user can reduce the values of R1 and R2. However, note that this increases the power consumption. The low-pass filter of the ADC driver limits the noise to the ADC.

The measured SNR, THD, and SINAD of the whole system for a 10 kHz signal are 93 dB, 113 dBc, and 93 dB, respectively. This translates to an ENOB of 15.1 at 10 kHz, which is compatible with the performance of the AD7982. Table 11 shows the performance of this setup at selected input frequencies.

Table 11. System Performance at Selected Input Frequency for Driving the AD7982 Differentially

Input Frequency (kHz)	Results			
	SNR (dB)	THD (dBc)	SINAD (dB)	ENOB
1	93	104	93	15.1
10	93	113	93	15.1
20	93	110	93	15.1
50	92	102	91	14.8
100	89	96	88	14.3

LAYOUT CONSIDERATIONS

To ensure optimal performance, careful and deliberate attention must be paid to the board layout, signal routing, power supply bypassing, and grounding.

Ground Plane

It is important to avoid ground in the areas under and around the input and output of the ADA4805-1/ADA4805-2. Stray capacitance between the ground plane and the input and output pads of a device is detrimental to high speed amplifier performance. Stray capacitance at the inverting input, together with the amplifier input capacitance, lowers the phase margin and can cause instability. Stray capacitance at the output creates a pole in the feedback loop, which can reduce phase margin and cause the circuit to become unstable.

Power Supply Bypassing

Power supply bypassing is a critical aspect in the performance of the ADA4805-1/ADA4805-2. A parallel connection of capacitors from each power supply pin to ground works best. Smaller value ceramic capacitors offer better high frequency response, whereas larger value ceramic capacitors offer better low frequency performance.

Paralleling different values and sizes of capacitors helps to ensure that the power supply pins are provided with a low ac impedance across a wide band of frequencies. This is important for minimizing the coupling of noise into the amplifier—especially when the amplifier PSRR begins to roll off—because the bypass capacitors can help lessen the degradation in PSRR performance.

Place the smallest value capacitor on the same side of the board as the amplifier and as close as possible to the amplifier power supply pins. Connect the ground end of the capacitor directly to the ground plane.

It is recommended that a 0.1 µF ceramic capacitor with a 0508 case size be used. The 0508 case size offers low series inductance and excellent high frequency performance. Place a 10 µF electrolytic capacitor in parallel with the 0.1 µF capacitor. Depending on the circuit parameters, some enhancement to performance can be realized by adding additional capacitors. Each circuit is different and must be analyzed individually for optimal performance.

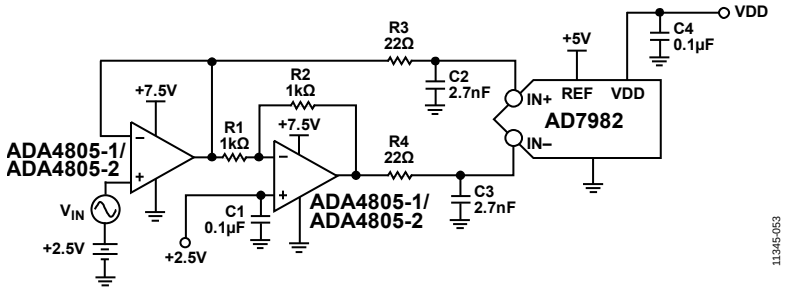
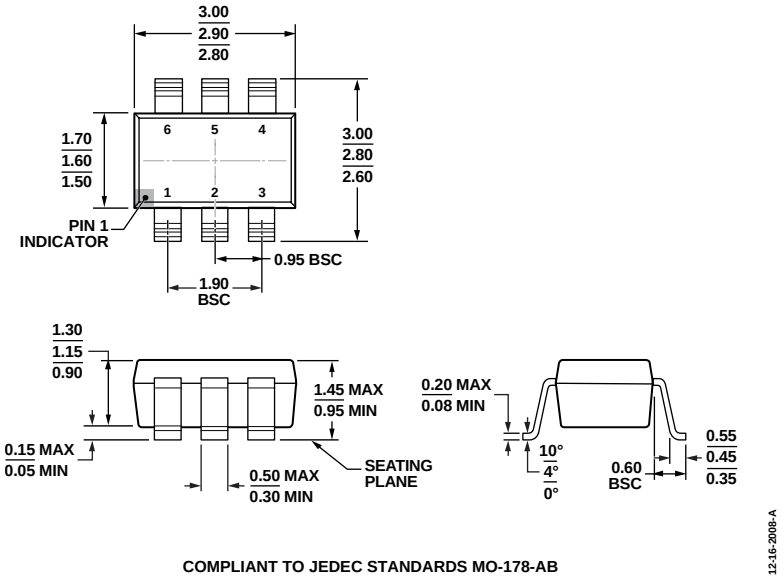


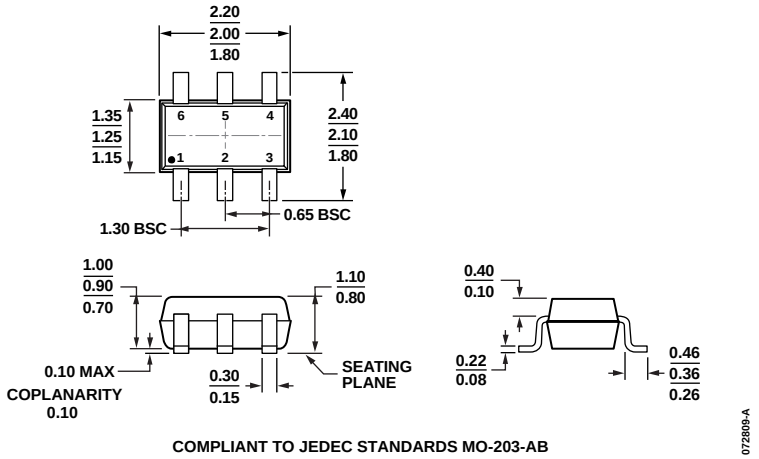
Figure 64. Driving the AD7982 with the ADA4805-1/ADA4805-2

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-178-AB

Figure 65. 6-Lead Small Outline Transistor Package [SOT-23]
(RJ-6)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-203-AB

Figure 66. 6-Lead Plastic Surface-Mount Package [SC70]
(KS-6)
Dimensions shown in millimeters

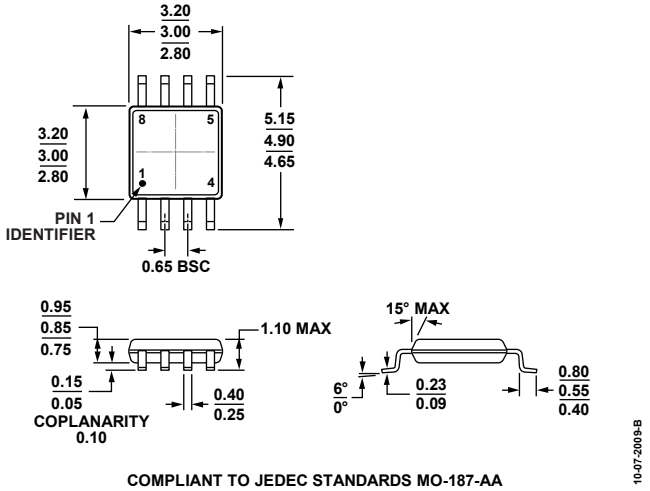


Figure 67. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

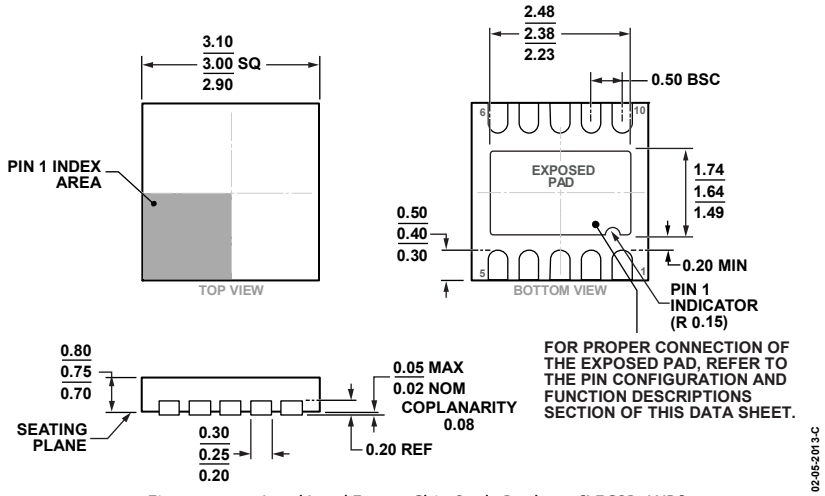


Figure 68. 10-Lead Lead Frame Chip Scale Package [LFCSP_WD]
3 mm × 3 mm Body, Very Very Thin, Dual Lead
(CP-10-9)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
ADA4805-1ARJZ-R2	−40°C to +125°C	6-Lead Small Outline Transistor Package [SOT-23]	RJ-6	H3H
ADA4805-1ARJZ-R7	−40°C to +125°C	6-Lead Small Outline Transistor Package [SOT-23]	RJ-6	H3H
ADA4805-1AKSZ-R2	−40°C to +125°C	6-Lead Plastic Surface-Mount Package [SC70]	KS-6	H3H
ADA4805-1AKSZ-R7	−40°C to +125°C	6-Lead Plastic Surface-Mount Package [SC70]	KS-6	H3H
ADA4805-2ARMZ	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	H3K
ADA4805-2ARMZ-R7	−40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	H3K
ADA4805-2ACPZ-R7	−40°C to +125°C	10-Lead Lead Frame Chip Scale Package [LFCSP_WD]	CP-10-9	H3K
ADA4805-2ACPZ-R2	−40°C to +125°C	10-Lead Lead Frame Chip Scale Package [LFCSP_WD]	CP-10-9	H3K
ADA4805-1ARJZ-EBZ		Evaluation Board for 6-Lead SOT-23		
ADA4805-1AKSZ-EBZ		Evaluation Board for 6-Lead SC70		
ADA4805-2ARMZ-EBZ		Evaluation Board for 8-Lead MSOP		
ADA4805-2ACPZ-EBZ		Evaluation Board for 10-Lead LFCSP		

[1] Z = RoHS Compliant Part.

D11345-0-12/14(B)

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