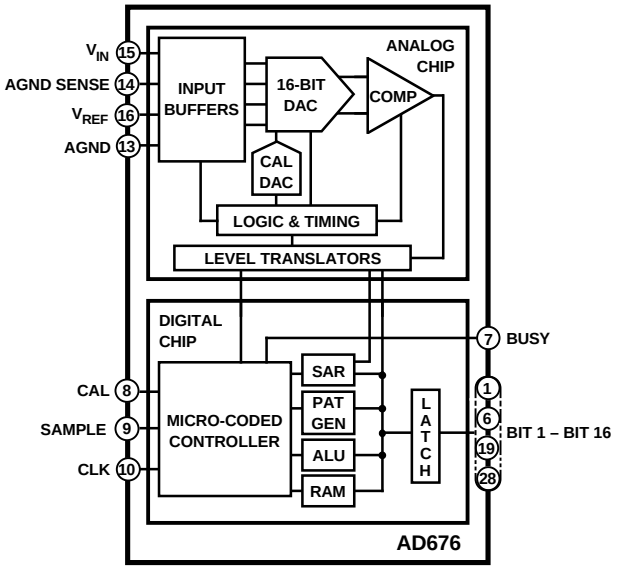
16-Bit 100 kSPS Sampling ADC

AD676

FEATURES
Autocalibrating
On-Chip Sample-Hold Function
Parallel Output Format
16 Bits No Missing Codes
±1 LSB INL
–97 dB THD
90 dB S/(N+D)
1 MHz Full Power Bandwidth

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD676 is a multipurpose 16-bit parallel output analog-to-digital converter which utilizes a switched-capacitor/charge redistribution architecture to achieve a 100 kSPS conversion rate (10 µs total conversion time). Overall performance is optimized by digitally correcting internal nonlinearities through on-chip autocalibration.

The AD676 circuitry is segmented onto two monolithic chips—a digital control chip fabricated on Analog Devices DSP CMOS process and an analog ADC chip fabricated on our BiMOS II process. Both chips are contained in a single package.

The AD676 is specified for ac (or "dynamic") parameters such as S/(N+D) Ratio, THD and IMD which are important in signal processing applications. In addition, dc parameters are specified which are important in measurement applications.

The AD676 operates from +5 V and ±12 V supplies and typically consumes 360 mW during conversion. The digital supply (V_{DD}) is separated from the analog supplies (V_{CC}, V_{EE}) for reduced digital crosstalk. An analog ground sense is provided for the analog input. Separate analog and digital grounds are also provided.

The AD676 is available in a 28-pin plastic DIP or 28-pin side-brazed ceramic package. A serial-output version, the AD677, is available in a 16-pin 300 mil wide ceramic or plastic package.

REV. A

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AD676–SPECIFICATIONS

AC SPECIFICATIONS (T_{MIN} to T_{MAX}, V_{CC} = +12 V ± 5%, V_{EE} = –12 V ± 5%, V_{DD} = +5 V ± 10%)[1]

Parameter	AD676J/A Min	AD676J/A Typ	AD676J/A Max	AD676K/B Min	AD676K/B Typ	AD676K/B Max	Units
Total Harmonic Distortion (THD)[2]							
@ 83 kSPS, T_{MIN} to T_{MAX}		–96	–88		–97	–90	dB
		0.0016	0.004		0.0014	0.003	%
@ 100 kSPS, +25°C		–96			–97		dB
		0.0016			0.0014		%
@ 100 kSPS, T_{MIN} to T_{MAX}		–92			–92		dB
		0.0025			0.0025		%
Signal-to-Noise and Distortion Ratio (S/(N+D))[2, 3]							
@ 83 kSPS, T_{MIN} to T_{MAX}	85	89		87	90		dB
@ 100 kSPS, +25°C		89			90		dB
@ 100 kSPS, T_{MIN} to T_{MAX}		86			86		dB
Peak Spurious or Peak Harmonic Component		–98			–98		dB
Intermodulation Distortion (IMD)[4]							
2nd Order Products		–102			–102		dB
3rd Order Products		–98			–98		dB
Full Power Bandwidth		1			1		MHz
Noise		160			160		µV rms

DIGITAL SPECIFICATIONS (for all grades T_{MIN} to T_{MAX}, V_{CC} = +12 V ± 5%, V_{EE} = –12 V ± 5%, V_{DD} = +5 V ± 10%)

Parameter		Test Conditions	Min	Typ	Max	Units
LOGIC INPUTS						
V_{IH}	High Level Input Voltage		2.4		V_{DD} + 0.3	V
V_{IL}	Low Level Input Voltage		–0.3		0.8	V
I_{IH}	High Level Input Current	$V_{IH} = V_{DD}$	–10		+10	µA
I_{IL}	Low Level Input Current	V_{IL} = 0 V	–10		+10	µA
C_{IN}	Input Capacitance			10		pF
LOGIC OUTPUTS						
V_{OH}	High Level Output Voltage	I_{OH} = 0.1 mA	V_{DD} –1 V			V
		I_{OH} = 0.5 mA	2.4			V
V_{OL}	Low Level Output Voltage	I_{OL} = 1.6 mA			0.4	V

NOTES

[1]V_{REF} = 10.0 V, (Conversion Rate (fs) = 83 kSPS, f_{IN} = 1.0 kHz, V_{IN} = –0.05 dB, Bandwidth = fs/2 unless otherwise indicated. All measurements referred to a 0 dB (20 V p-p) input signal. Values are post-calibration.

[2]For other input amplitudes, refer to Figure 13.

[3]For other input ranges/voltages reference values see Figure 12.

[4]fa = 1008 Hz. fb = 1055 Hz. See Definition of Specifications section and Figure 15.

Specifications subject to change without notice.

DC SPECIFICATIONS (T_{MIN} to T_{MAX}, V_{CC} = +12 V ± 5%, V_{EE} = –12 V ± 5%, V_{DD} = +5 V ± 10%)[1]

Parameter	AD676J/A Min	AD676J/A Typ	AD676J/A Max	AD676K/B Min	AD676K/B Typ	AD676K/B Max	Units
TEMPERATURE RANGE							
J, K Grades	0		+70	0		+70	°C
A, B Grades	–40		+85	–40		+85	°C
ACCURACY							
Resolution	16			16			Bits
Integral Nonlinearity (INL)							
@ 83 kSPS, T_{MIN} to T_{MAX}		±1			±1	±1.5	LSB
@ 100 kSPS, +25°C		±1			±1		LSB
@ 100 kSPS, T_{MIN} to T_{MAX}		±2			±2		LSB
Differential Nonlinearity (DNL)–No Missing Codes		16		16			Bits
Bipolar Zero Error[2] (at Nominal Supplies)		0.005			0.005		% FSR
Gain Error (at Nominal Supplies)							
@ 83 kSPS[2]		0.005			0.005		% FSR
@ 100 kSPS, +25°C		0.005			0.005		% FSR
@ 100 kSPS[2]		0.01			0.01		% FSR
Temperature Drift, Bipolar Zero[3]							% FSR
J, K Grades		0.0015			0.0015		% FSR
A, B Grades		0.003			0.003		% FSR
Temperature Drift, Gain[3]							
J, K Grades		0.0015			0.0015		% FSR
A, B Grades		0.003			0.003		% FSR
VOLTAGE REFERENCE INPUT RANGE[4] (V_{REF})	5		10	5		10	V
ANALOG INPUT[5]							
Input Range (V_{IN})			±V_{REF}			±V_{REF}	V
Input Impedance		*			*		
Input Settling Time		2			2		µs
Input Capacitance During Sample			50*			50*	pF
Aperture Delay		6			6		ns
Aperture Jitter		100			100		ps
POWER SUPPLIES							
Power Supply Rejection							
V_{CC} = +12 V ± 5%		±1			±1		LSB
V_{EE} = –12 V ± 5%		±1			±1		LSB
V_{DD} = +5 V ± 10%		±1			±1		LSB
Operating Current							
I_{CC}		14.5	18		14.5	18	mA
I_{EE}		14.5	18		14.5	18	mA
I_{DD}		2	5		2	5	mA
Power Consumption		360	480		360	480	mW

NOTES
[1]V_{REF} = 5.0 V, Conversion Rate = 83 kSPS unless otherwise noted. Values are post-calibration.
[2]Values shown apply to any temperature from T_{MIN} to T_{MAX} after calibration at that temperature.
[3]Values shown are based upon calibration at +25°C with no additional calibration at temperature. Values shown are the worst case variation from the value at +25°C.
[4]See "APPLICATIONS" section for recommended voltage reference circuit, and Figure 12 for dynamic performance with other reference voltage values.
[5]See "APPLICATIONS" section for recommended input buffer circuit.
*For explanation of input characteristics, see "ANALOG INPUT" section.

Specifications subject to change without notice.

TIMING SPECIFICATIONS (T_{MIN} to T_{MAX} V_{CC} = +12 V ± 5%, V_{EE} = –12 V ± 5%, V_{DD} = +5 V ± 10%, V_{REF} = 10.0 V)[1]

Parameter	Symbol	Min	Typ	Max	Units
Conversion Time[2]	t_C	10		1000	µs
CLK Period[3]	t_{CLK}	480			ns
Calibration Time	t_{CT}			85,530	t_{CLK}
Sampling Time (Included in t_C)	t_S	2			µs
CAL to BUSY Delay	t_{CALB}		75	150	ns
BUSY to SAMPLE Delay	t_{BS}	2			µs
SAMPLE to BUSY Delay	t_{SB}		15	100	ns
CLK HIGH[4]	t_{CH}	50			ns
CLK LOW[4]	t_{CL}	50			ns
SAMPLE LOW to 1st CLK Delay	t_{SC}	50			ns
SAMPLE LOW	t_{SL}	100			ns
Output Delay	t_{OD}		125	200	ns
Status Delay	t_{SD}	50			ns
CAL HIGH Time	t_{CALH}	50			ns

NOTES
[1]See the "CONVERSION CONTROL" and "AUTOCALIBRATION" sections for detailed explanations of the above timing.
[2]Depends upon external clock frequency; includes acquisition time and conversion time. The maximum conversion time is specified to account for the droop of the internal sample/hold function. Longer conversion times may degrade performance. See "General Conversion Guidelines" for additional explanation of maximum conversion time.
[3]580 ns is recommended for optimal accuracy over temperature.
[4]t_{CH} + t_{CL} = t_{CLK} and must be greater than 480 ns.

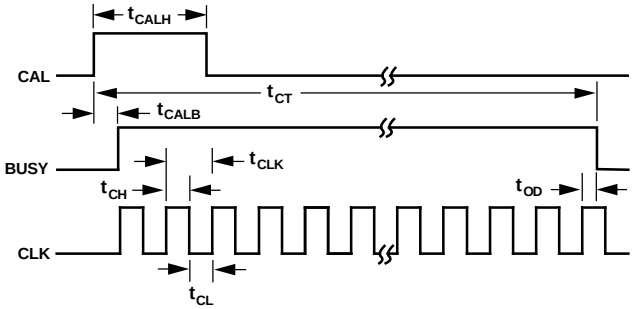


Figure 1. Calibration Timing

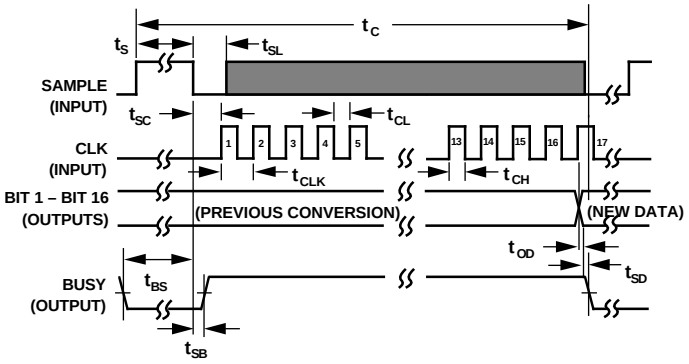


Figure 2a. General Conversion Timing

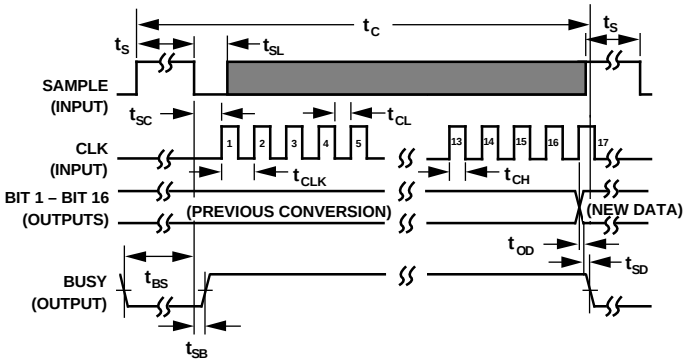


Figure 2b. Continuous Conversion Timing

ORDERING GUIDE

Model	Temperature Range[1]	S/(N+D)	Max INL	Package Description	Package Option[2]
AD676JD	0°C to +70°C	85 dB		Ceramic 28-Pin DIP	D-28
AD676KD	0°C to +70°C	87 dB	±1.5 LSB	Ceramic 28-Pin DIP	D-28
AD676AD	–40°C to +85°C	85 dB		Ceramic 28-Pin DIP	D-28
AD676BD	–40°C to +85°C	87 dB	±1.5 LSB	Ceramic 28-Pin DIP	D-28

NOTES
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the AD676/883 data sheet.
[2]D = Ceramic DIP.

ABSOLUTE MAXIMUM RATINGS*

V_{CC} to V_{EE} . . . . . –0.3 V to +26.4 V
V_{DD} to DGND . . . . . –0.3 V to +7 V
V_{CC} to AGND . . . . . –0.3 V to +18 V
V_{EE} to AGND . . . . . –18 V to +0.3 V
AGND to DGND . . . . . ±0.3 V
Digital Inputs to DGND . . . . . 0 V to +5.5 V
Analog Inputs, V_{REF} to AGND
. . . . . (V_{CC} + 0.3 V) to (V_{EE} – 0.3 V)
Soldering . . . . . +300°C, 10 sec
Storage Temperature . . . . . –65°C to +150°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

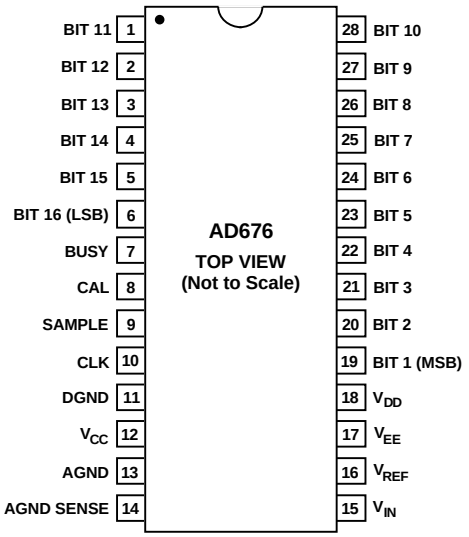
The AD676 features input protection circuitry consisting of large "distributed" diodes and polysilicon series resistors to dissipate both high energy discharges (Human Body Model) and fast, low energy pulses (Charged Device Model). Per Method 3015.2 of MIL-STD-883C, the AD676 has been classified as a Category 1 Device.

Proper ESD precautions are strongly recommended to avoid functional damage or performance degradation. Charges as high as 4000 volts readily accumulate on the human body and test equipment, and discharge without detection. Unused devices must be stored in conductive foam or shunts, and the foam discharged to the destination socket before devices are removed. For further information on ESD Precaution. Refer to Analog Devices' *ESD Prevention Manual.*

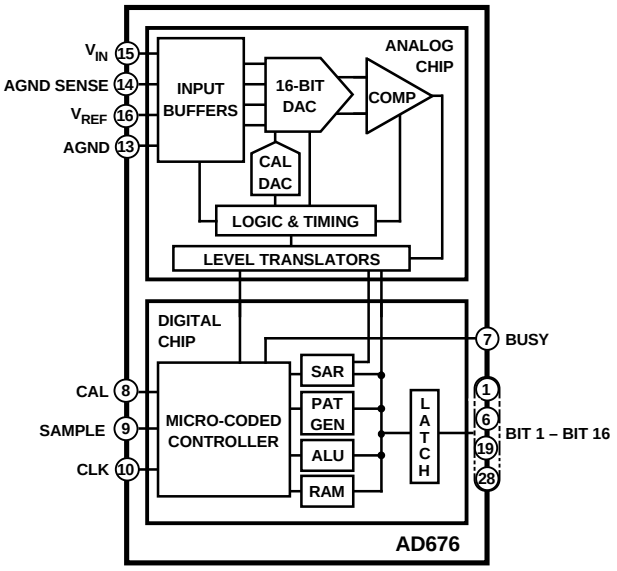
PIN DESCRIPTION

Pin	Name	Type	Description
1–6	BIT 11-BIT 16	DO	BIT 11–BIT 16 represent the six LSBs of data.
7	BUSY	DO	Status Line for Converter. Active HIGH, indicating a conversion or calibration in progress. BUSY should be buffered when capacitively loaded.
8	CAL	DI	Calibration Control Pin (Asynchronous).
9	SAMPLE	DI	V_{IN} Acquisition Control Pin. Active HIGH. During conversion, SAMPLE controls the state of the internal sample-hold amplifier and the falling edge initiates conversion (see "Conversion Control" paragraph). During calibration, SAMPLE should be held LOW. If HIGH during calibration, diagnostic information will appear on the two LSBs (Pins 5 and 6).
10	CLK	DI	Master Clock Input. The AD676 requires 17 clock cycles to execute a conversion.
11	DGND	P	Digital Ground.
12	V_{CC}	P	+12 V Analog Supply Voltage.
13	AGND	P/AI	Analog Ground.
14	AGND SENSE	AI	Analog Ground Sense.
15	V_{IN}	AI	Analog Input Voltage.
16	V_{REF}	AI	External Voltage Reference Input.
17	V_{EE}	P	–12 V Analog Supply Voltage. Note: the lid of the ceramic package is internally connected to V_{EE}.
18	V_{DD}	P	+5 V Logic Supply Voltage.
19–28	BIT 1–BIT 10	DO	BIT 1–BIT 10 represent the ten MSB of data.

Type: AI = Analog Input
DI = Digital Input
DO = Digital Output
P = Power



Package Pinout



Functional Block Diagram

NYQUIST FREQUENCY
An implication of the Nyquist sampling theorem, the "Nyquist frequency" of a converter is that input frequency which is one half the sampling frequency of the converter.

TOTAL HARMONIC DISTORTION
Total harmonic distortion (THD) is the ratio of the rms sum of the harmonic components to the rms value of a full-scale input signal and is expressed in percent (%) or decibels (dB). For input signals or harmonics that are above the Nyquist frequency, the aliased components are used.

SIGNAL-TO-NOISE PLUS DISTORTION RATIO
Signal-to-noise plus distortion is defined to be the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc.

GAIN ERROR
The last transition should occur at an analog value 1.5 LSB below the nominal full scale (4.99977 volts for a ±5 V range). The gain error is the deviation of the actual difference between the first and last code transition from the ideal difference between the first and last code transition.

BIPOLAR ZERO ERROR
Bipolar zero error is the difference between the ideal midscale input voltage (0 V) and the actual voltage producing the midscale output code.

DIFFERENTIAL NONLINEARITY (DNL)
In an ideal ADC, code transitions are one LSB apart. Differential nonlinearity is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

INTEGRAL NONLINEARITY (INL)
The ideal transfer function for an ADC is a straight line bisecting the center of each code drawn between "zero" and "full scale." The point used as "zero" occurs 1/2 LSB before the most negative code transition. "Full scale" is defined as a level 1.5 LSB beyond the most positive code transition. Integral nonlinearity is the worst-case deviation of a code center average from the straight line.

BANDWIDTH
The full-power bandwidth is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3 dB for a full-scale input.

INTERMODULATION DISTORTION (IMD)
With inputs consisting of sine waves at two frequencies, fa and fb, any device with nonlinearities will create distortion products, of order (m+n), at sum and difference frequencies of mfa ± nfb, where m, n = 0, 1, 2, 3. . . . Intermodulation terms are those for which m or n is not equal to zero. For example, the second order terms are (fa + fb) and (fa – fb), and the third order terms are (2 fa + fb), (2 fa – fb), (fa + 2 fb) and (fa – 2 fb). The IMD products are expressed as the decibel ratio of the rms sum of the measured input signals to the rms sum of the distortion terms. The two signals applied to the converter are of equal amplitude, and the peak value of their sum is –0.5 dB from full scale. The IMD products are normalized to a 0 dB input signal.

APERTURE DELAY
Aperture delay is the time required after SAMPLE pin is taken LOW for the internal sample-hold of the AD676 to open, thus holding the value of V_{IN}.

APERTURE JITTER
Aperture jitter is the variation in the aperture delay from sample to sample.

POWER SUPPLY REJECTION
DC variations in the power supply voltage will affect the overall transfer function of the ADC, resulting in zero error and gain error changes. Power supply rejection is the maximum change in either the bipolar zero error or gain error value. Additionally, there is another power supply variation to consider. AC ripple on the power supplies can couple noise into the ADC, resulting in degradation of dynamic performance. This is displayed in Figure 16.

INPUT SETTLING TIME
Settling time is a function of the SHA's ability to track fast slewing signals. This is specified as the maximum time required in track mode after a full-scale step input to guarantee rated conversion accuracy.

FUNCTIONAL DESCRIPTION

The AD676 is a multipurpose 16-bit analog-to-digital converter and includes circuitry which performs an input sample/hold function, ground sense, and autocalibration. These functions are segmented onto two monolithic chips—an analog signal processor and a digital controller. Both chips are contained within the AD676 package.

The AD676 employs a successive-approximation technique to determine the value of the analog input voltage. However, instead of the traditional laser-trimmed resistor-ladder approach, this device uses a capacitor-array, charge redistribution technique. Binary-weighted capacitors subdivide the input sample to perform the actual analog-to-digital conversion. The capacitor array eliminates variation in the linearity of the device due to temperature-induced mismatches of resistor values. Since a capacitor array is used to perform the data conversions, the sample/hold function is included without the need for additional external circuitry.

Initial errors in capacitor matching are eliminated by an autocalibration circuit within the AD676. This circuit employs an on-chip microcontroller and a calibration DAC to measure and compensate capacitor mismatch errors. As each error is determined, its value is stored in on-chip memory (RAM). Subsequent conversions use these RAM values to improve conversion accuracy. The autocalibration routine may be invoked at any time. Autocalibration insures high performance while eliminating the need for any user adjustments and is described in detail below.

The microcontroller controls all of the various functions within the AD676. These include the actual successive approximation algorithm, the autocalibration routine, the sample/hold operation, and the internal output data latch.

AUTOCALIBRATION

The AD676 achieves rated performance without the need for user trims or adjustments. This is accomplished through the use of on-chip autocalibration.

In the autocalibration sequence, sample/hold offset is nulled by internally connecting the input circuit to the ground sense circuit. The resulting offset voltage is measured and stored in RAM for later use. Next, the capacitor representing the most significant bit (MSB) is charged to the reference voltage. This charge is then transferred to a capacitor of equal size (composed of the sum of the remaining lower weight bits). The difference in the voltage that results and the reference voltage represents the amount of capacitor mismatch. A calibration digital-to-analog converter (DAC) adds an appropriate value of error correction voltage to cancel this mismatch. This correction factor is also stored in RAM. This process is repeated for each of the capacitors representing the remaining top eight bits. The accumulated values in RAM are then used during subsequent conversions to adjust conversion results accordingly.

As shown in Figure 1, when CAL is taken HIGH the AD676 internal circuitry is reset, the BUSY pin is driven HIGH, and the ADC prepares for calibration. This is an asynchronous hardware reset and will interrupt any conversion or calibration currently in progress. Actual calibration begins when CAL is taken LOW and completes in 85,530 clock cycles, indicated by BUSY going LOW. During calibration, it is preferable for SAMPLE to be held LOW. If SAMPLE is HIGH, diagnostic data will appear on Pins 5 and 6. This data is of no value to the user.

The AD676 requires one clock cycle after BUSY goes LOW to complete the calibration cycle. If this clock cycle is not provided, it will be taken from the first conversion, likely resulting in first conversion error.

In most applications, it is sufficient to calibrate the AD676 only upon power-up, in which case care should be taken that the power supplies and voltage reference have stabilized first. If not calibrated, the AD676 accuracy may be as low as 10 bits.

CONVERSION CONTROL

The AD676 is controlled by two signals: SAMPLE and CLK, as shown in Figures 2a and 2b. It is assumed that the part has been calibrated and the digital I/O pins have the levels shown at the start of the timing diagram.

A conversion consists of an input acquisition followed by 17 clock pulses which execute the 16-bit internal successive approximation routine. The analog input is acquired by taking the SAMPLE line HIGH for a minimum sampling time of t_S. The actual sample taken is the voltage present on V_{IN} one aperture delay after the SAMPLE line is brought LOW, assuming the previous conversion has completed (signified by BUSY going LOW). Care should he taken to ensure that this negative edge is well defined and jitter free in ac applications to reduce the uncertainty (noise) in signal acquisition. With SAMPLE going LOW, the AD676 commits itself to the conversion—the input at V_{IN} is disconnected from the internal capacitor array, BUSY goes HIGH, and the SAMPLE input will be ignored until the conversion is completed (when BUSY goes LOW). SAMPLE must be held LOW for a minimum period of time t_{SL}. A period of time t_{SC} after bringing SAMPLE LOW, the 17 CLK cycles are applied; CLK pulses that start before this period of time are ignored. BUSY goes HIGH t_{SB} after SAMPLE goes LOW, signifying that a conversion is in process, and remains HIGH until the conversion is completed. BUSY goes LOW during the 17th CLK cycle at the point where the data outputs have changed and are valid. The AD676 will ignore CLK after BUSY has gone LOW and the output data will remain constant until a new conversion is completed. The data can, therefore, be read any time after BUSY goes LOW and before the 17th CLK of the next conversion (see Figures 2a and 2b). The section on Microprocessor Interfacing discusses how the AD676 can be interfaced to a 16-bit databus.

Typically BUSY would be used to latch the AD676 output data into buffers or to interrupt microprocessors or DSPs. It is recommended that the capacitive load on BUSY be minimized by driving no more than a single logic input. Higher capacitive loads such as cables or multiple gates may degrade conversion quality unless BUSY is buffered.

CONTINUOUS CONVERSION

For maximum throughput rate, the AD676 can be operated in a continuous convert mode (see Figure 2b). This is accomplished by utilizing the fact that SAMPLE will no longer be ignored after BUSY goes LOW, so an acquisition may be initiated even during the HIGH time of the 17th CLK pulse for maximum throughput rate while enabling full settling of the sample/hold circuitry. If SAMPLE is already HIGH when BUSY goes LOW at the end of a conversion, then an acquisition is immediately initiated and t_S and t_C start from that time. Data from the previous conversion may be latched up to t_{SD} before BUSY goes LOW or t_{OD} after the rising edge of the 17th clock pulse. However, it is preferred that latching occur on or after the falling edge of BUSY.

Care must he taken to adhere to the minimum/maximum timing requirements in order to preserve conversion accuracy.

GENERAL CONVERSION GUIDELINES

During signal acquisition and conversion, care should be taken with the logic inputs to avoid digital feedthrough noise. It is possible to run CLK continuously, even during the sample period. However, CLK edges during the sampling period, and especially when SAMPLE goes LOW, may inject noise into the sampling process. The AD676 is tested with no CLK cycles during the sampling period. The BUSY signal can be used to prevent the clock from running during acquisition, as illustrated in Figure 3. In this circuit BUSY is used to reset the circuitry which divides the system clock down to provide the AD676 CLK. This serves to interrupt the clock until after the input signal has been acquired, which has occurred when BUSY goes HIGH. When the conversion is completed and BUSY goes LOW, the circuit in Figure 3 truncates the 17th CLK pulse width which is tolerable because only its rising edge is critical.

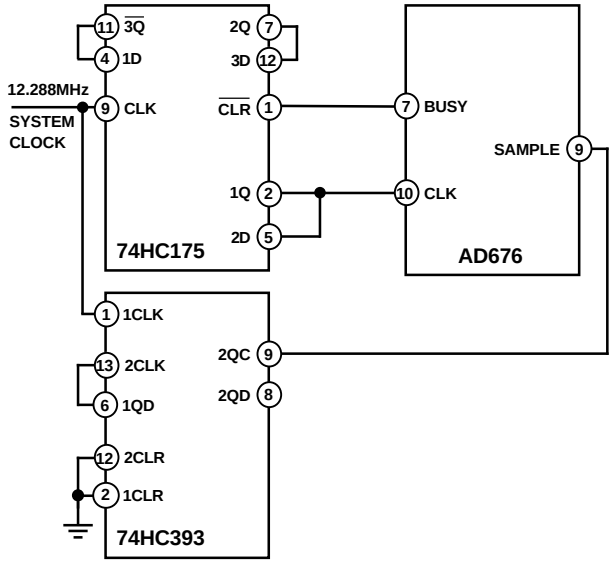


Figure 3.

Figure 3 also illustrates the use of a counter (74HC393) to derive the AD676 SAMPLE command from the system clock when a continuous convert mode is desirable. Pin 9 (2QC) provides a 96 kHz sample rate for the AD676 when used with a 12.288 MHz system clock. Alternately, Pin 8 (2QD) could be used for a 48 kHz rate.

If a continuous clock is used, then the user must avoid CLK edges at the instant of disconnecting V_{IN} which occurs at the falling edge of SAMPLE (see t_{SC} specification). The duty cycle of CLK may vary, but both the HIGH (t_{CH}) and LOW (t_{CL}) phases must conform to those shown in the timing specifications. The internal comparator makes its decisions on the rising edge of CLK. To avoid a negative edge transition disturbing the comparator's settling, t_{CL} should be at least half the value of t_{CLK}. To also avoid transitions disturbing the internal comparator's settling, it is not recommended that the SAMPLE pin change state toward the end of a CLK cycle.

During a conversion, internal dc error terms such as comparator voltage offset are sampled, stored on internal capacitors and used to correct for their corresponding errors when needed. Because these voltages are stored on capacitors, they are subject to leakage decay and so require refreshing. For this reason there is a maximum conversion time t_C (1000 µs). From the time SAMPLE goes HIGH to the completion of the 17th CLK pulse, no more than 1000 µs should elapse for specified performance. However, there is no restriction to the maximum time between conversions.

Output coding for the AD676 is twos complement, as shown in Table I. By inverting the MSB, the coding can be converted to offset binary. The AD676 is designed to limit output coding in the event of out-of-range inputs.

Table I. Output Coding

V_{IN}	Output Code
>Full Scale	011 . . . 11
Full Scale	011 . . . 11
Full Scale – 1 LSB	011 . . . 10
Midscale + 1 LSB	000 . . . 01
Midscale	000 . . . 00
Midscale – 1 LSB	111 . . . 11
–Full Scale + 1 LSB	100 . . . 01
–Full Scale	100 . . . 00
<–Full Scale	100 . . . 00

POWER SUPPLIES AND DECOUPLING

The AD676 has three power supply input pins. V_{CC} and V_{EE} provide the supply voltages to operate the analog portions of the AD676 including the ADC and sample-hold amplifier (SHA). V_{DD} provides the supply voltage which operates the digital portions of the AD676 including the data output buffers and the autocalibration controller.

As with most high performance linear circuits, changes in the power supplies can produce undesired changes in the performance of the circuit. Optimally, well regulated power supplies with less than 1% ripple should be selected. The ac output impedance of a power supply is a complex function of frequency, and in general will increase with frequency. In other words, high frequency switching such as that encountered with digital circuitry requires fast transient currents which most power supplies cannot adequately provide. This results in voltage spikes on the supplies. If these spikes exceed the ±5% tolerance of the ±12 V supplies or the ±10% limits of the +5 V supply, ADC performance will degrade. Additionally, spikes at frequencies higher than 100 kHz will also degrade performance. To compensate for the finite ac output impedance of the supplies, it is necessary to store "reserves" of charge in bypass capacitors. These capacitors can effectively lower the ac impedance presented to the AD676 power inputs which in turn will significantly reduce the magnitude of the voltage spikes. For bypassing to be effective, certain guidelines should be followed. Decoupling capacitors, typically 0.1 µF, should be placed as closely as possible to each power supply pin of the AD676. It is essential that these capacitors be placed physically close to the IC to minimize the inductance of the PCB trace between the capacitor and the supply pin. The logic supply (V_{DD}) should be decoupled to digital common and the analog supplies (Vcc and V_{EE}) to analog common. The reference input is also considered as a power supply pin in this regard and the same decoupling procedures apply. These points are displayed in Figure 4.

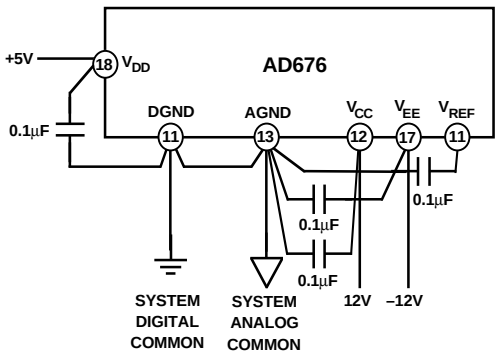


Figure 4. Grounding and Decoupling the AD676

Additionally, it is beneficial to have large capacitors (>47 µF) located at the point where the power connects to the PCB with 10 µF capacitors located in the vicinity of the ADC to further reduce low frequency ripple. In systems that will be subjected to particularly harsh environmental noise, additional decoupling may be necessary. RC-filtering on each power supply combined with dedicated voltage regulation can substantially decrease power supply ripple effects (this is further detailed in Figure 7).

BOARD LAYOUT

Designing with high resolution data converters requires careful attention to board layout. Trace impedance is a significant issue. A 1.22 mA current through a 0.5 Ω trace will develop a voltage drop of 0.6 mV, which is 4 LSBs at the 16-bit level for a 10 V full-scale span. In addition to ground drops, inductive and capacitive coupling need to be considered, especially when high accuracy analog signals share the same board with digital signals.

Analog and digital signals should not share a common return path. Each signal should have an appropriate analog or digital return routed close to it. Using this approach, signal loops enclose a small area, minimizing the inductive coupling of noise. Wide PC tracks, large gauge wire, and ground planes are highly recommended to provide low impedance signal paths. Separate analog and digital ground planes are also desirable, with a single interconnection point at the AD676 to minimize interference between analog and digital circuitry. Analog signals should be routed as far as possible from digital signals and should cross them, if at all, only at right angles. A solid analog ground plane around the AD676 will isolate it from large switching ground currents. For these reasons, the use of wire wrap circuit construction will not provide adequate performance; careful printed circuit board construction is preferred.

GROUNDING

The AD676 has three grounding pins, designated ANALOG GROUND (AGND), DIGITAL GROUND (DGND) and ANALOG GROUND SENSE (AGND SENSE). The analog ground pin is the "high quality" ground reference point for the device, and should be connected to the analog common point in the system.

AGND SENSE is intended to be connected to the input signal ground reference point. This allows for slight differences in level between the analog ground point in the system and the input signal ground point. However no more than 100 mV is recommended between the AGND and the AGND SENSE pins for specified performance.

Using AGND SENSE to remotely sense the ground potential of the signal source can be useful if the signal has to be carried some distance to the A/D converter. Since all IC ground currents have to return to the power supply and no ground leads are free from resistance and inductance, there are always some voltage differences from one ground point in a system to another.

Over distance this voltage difference can easily amount to several LSBs (in a 10 V input span, 16-bit system each LSB is about 0.15 mV). This would directly corrupt the A/D input signal if the A/D measures its input with respect to power ground (AGND) as shown in Figure 5a. To solve this problem the AD676 offers an AGND SENSE pin. Figure 5b shows how the AGND SENSE can be used to eliminate the problem in Figure 5a. Figure 5b also shows how the signal wires should be shielded in a noisy environment to avoid capacitive coupling. If inductive (magnetic) coupling is expected to be dominant such as where motors are present, twisted-pair wires should be used instead.

The digital ground pin is the reference point for all of the digital signals that operate the AD676. This pin should be connected to the digital common point in the system. As Figure 4 illustrated, the analog and digital grounds should be connected together at one point in the system, preferably at the AD676.

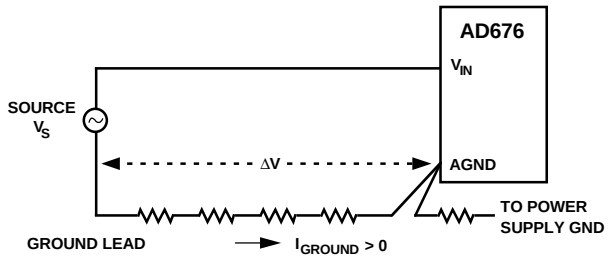


Figure 5a. Input to the A/D Is Corrupted by IR Drop in Ground Leads: $V_{IN} = V_S + \Delta V$

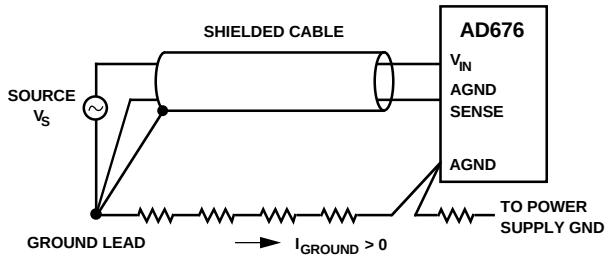


Figure 5b. AGND SENSE Eliminates the Problem in Figure 5a.

VOLTAGE REFERENCE

The AD676 requires the use of an external voltage reference. The input voltage range is determined by the value of the reference voltage; in general, a reference voltage of n volts allows an input range of ±n volts. The AD676 is specified for both 10 V and 5.0 V references. A 10 V reference will typically require support circuitry operated from ±15 V supplies; a 5.0 V reference may be used with ±12 V supplies. Signal-to-noise performance is increased proportionately with input signal range. In the presence of a fixed amount of system noise, increasing the LSB size (which results from increasing the reference voltage) will increase the effective S/(N+D) performance. Figure 12 illustrates S/(N+D) as a function of reference voltage. In contrast, INL will be optimal at lower reference voltage values (such as 5 V) due to capacitor nonlinearity at higher voltage values.

During a conversion, the switched capacitor array of the AD676 presents a dynamically changing current load at the voltage reference as the successive-approximation algorithm cycles through various choices of capacitor weighting. (See the following section "Analog Input" for a detailed discussion of the V_{REF} input characteristics.) The output impedance of the reference circuitry must be low so that the output voltage will remain sufficiently constant as the current drive changes. In some applications, this may require that the output of the voltage reference be buffered by an amplifier with low impedance at relatively high frequencies. In choosing a voltage reference, consideration should be made for selecting one with low noise. A capacitor connected between REF IN and AGND will reduce the demands on the reference by decreasing the magnitude of high frequency components required to be sourced by the reference.

Figures 6 and 7 represent typical design approaches.

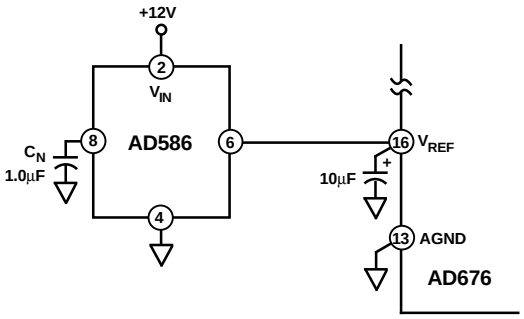


Figure 6.

Figure 6 shows a voltage reference circuit featuring the 5 V output AD586. The AD586 is a low cost reference which utilizes a buried Zener architecture to provide low noise and drift. Over the 0°C to +70°C range, the AD586L grade exhibits less than 2.25 mV output change from its initial value at +25°C. A noise-reduction capacitor, C_N, reduces the broadband noise of the

AD586 output, thereby optimizing the overall performance of the AD676. It is recommended that a 10 µF to 47 µF high quality tantalum capacitor be tied between the V_{REF} input of the AD676 and ground to minimize the impedance on the reference.

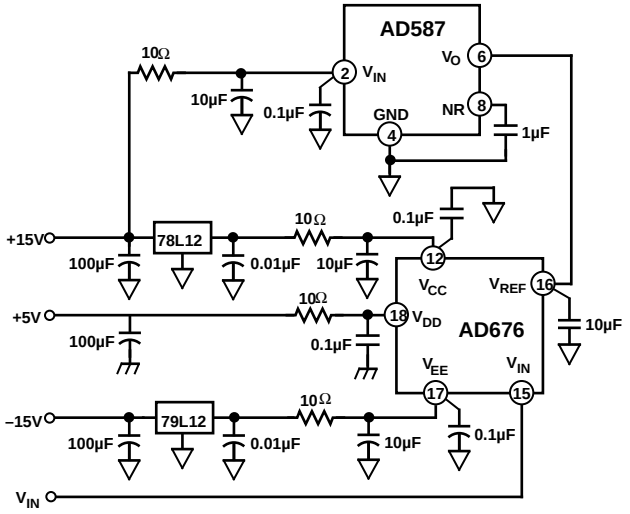


Figure 7.

Using the AD676 with ±10 V input range (V_{REF} = 10 V) typically requires ±15 V supplies to drive op amps and the voltage reference. If ±12 V is not available in the system, regulators such as 78L12 and 79L12 can be used to provide power for the AD676. This is also the recommended approach (for any input range) when the ADC system is subjected to harsh environments such as where the power supplies are noisy and where voltage spikes are present. Figure 7 shows an example of such a system based upon the 10 V AD587 reference, which provides a 300 µV LSB. Circuitry for additional protection against power supply disturbances has been shown. A 100 µF capacitor at each regulator prevents very large voltage spikes from entering the regulators. Any power line noise which the regulators cannot eliminate will be further filtered by an RC filter (10 Ω/10 µF) having a –3 dB point at 1.6 kHz. For best results the regulators should be within a few centimeters of the AD676.

ANALOG INPUT

As previously discussed, the analog input voltage range for the AD676 is $\pm V_{REF}$. For purposes of ground drop and common mode rejection, the V_{IN} and V_{REF} inputs each have their own ground. V_{REF} is referred to the local analog system ground (AGND), and V_{IN} is referred to the analog ground sense pin (AGND SENSE) which allows a remote ground sense for the input signal.

The AD676 analog inputs (V_{IN}, V_{REF} and AGND SENSE) exhibit dynamic characteristics. When a conversion cycle begins, each analog input is connected to an internal, discharged 50 pF capacitor which then charges to the voltage present at the corresponding pin. The capacitor is disconnected when SAMPLE is taken LOW, and the stored charge is used in the subsequent conversion. In order to limit the demands placed on the external source by this high initial charging current, an internal buffer amplifier is employed between the input and this capacitance for a few hundred nanoseconds. During this time the input pin exhibits typically 20 kΩ input resistance, 10 pF input capacitance and ±40 µA bias current. Next, the input is switched directly to the now precharged capacitor and allowed to fully settle. During this time the input sees only a 50 pF capacitor. Once the sample is taken, the input is internally floated so that the external input source sees a very high input resistance and a parasitic input capacitance of typically only 2 pF. As a result, the only dominant input characteristic which must be considered is the high current steps which occur when the internal buffers are switched in and out.

In most cases, these characteristics require the use of an external op amp to drive the input of the AD676. Care should he taken with op amp selection; even with modest loading conditions, most available op amps do not meet the low distortion requirements necessary to match the performance capabilities of the AD676. Figure 8 represents a circuit, based upon the AD845, recommended for low noise, low distortion ac applications.

For applications optimized more for low bias and low offset than speed or bandwidth, the AD845 of Figure 8 may be replaced by the OP27.

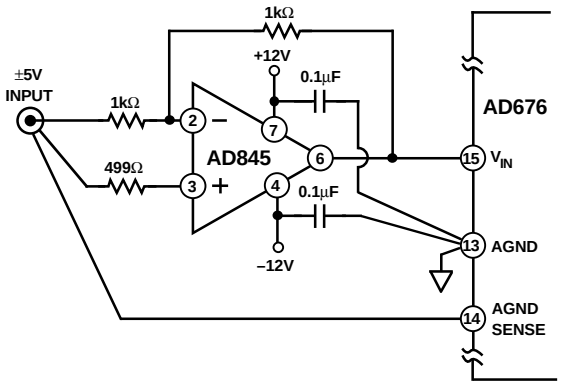


Figure 8.

AC PERFORMANCE

AC parameters, which include S/(N+D), THD, etc., reflect the AD676's effect on the spectral content of the analog input signal. Figures 12 through 16 provide information on the AD676's ac performance under a variety of conditions.

As a general rule, averaging the results from several conversions reduces the effects of noise, and therefore improves such parameters as S/(N+D). AD676 performance may be optimized by operating the device at its maximum sample rate of 100 kSPS and digitally filtering the resulting bit stream to the desired signal bandwidth. This succeeds in distributing noise over a wider frequency range, thus reducing the noise density in the frequency band of interest. This subject is discussed in the following section.

OVERSAMPLING AND NOISE FILTERING

The Nyquist rate for a converter is defined as one-half its sampling rate. This is established by the Nyquist theorem, which requires that a signal he sampled at a rate corresponding to at least twice its highest frequency component of interest in order to preserve the informational content. Oversampling is a conversion technique in which the sampling frequency is more than twice the frequency bandwidth of interest. In audio applications, the AD676 can operate at a $2 \times F_S$ oversampling rate, where F_S = 48 kHz.

In quantized systems, the informational content of the analog input is represented in the frequency spectrum from dc to the Nyquist rate of the converter. Within this same spectrum are higher frequency noise and signal components. Antialias, or low pass, filters are used at the input to the ADC to reduce these noise and signal components so that their aliased components do not corrupt the baseband spectrum. However, wideband noise contributed by the AD676 will not be reduced by the antialias filter. The AD676 quantization noise is evenly distributed from dc to the Nyquist rate, and this fact can be used to minimize its overall affect.

The AD676 quantization noise effects can be reduced by oversampling–sampling at a rate higher than that defined by the Nyquist theorem. This spreads the noise energy over a bandwidth wider than the frequency band of interest. By judicious selection of a digital decimation filter, noise frequencies outside the bandwidth of interest may be eliminated.

The process of analog to digital conversion inherently produces noise, known as quantization noise. The magnitude of this noise is a function of the resolution of the converter, and manifests itself as a limit to the theoretical signal-to-noise ratio achievable. This limit is described by S/(N+D) = (6.02n + 1.76 + 10 log $F_S/2F_A$) dB, where n is the resolution of the converter in bits, F_S is the sampling frequency, and Fa is the signal bandwidth of interest. For audio bandwidth applications, the AD676 is capable of operating at a $2 \times$ oversample rate (96 kSPS), which typically produces an improvement in S/(N+D) of 3 dB compared with operating at the Nyquist conversion rate of 48 kSPS. Oversampling has another advantage as well; the demands on the antialias filter are lessened. In summary, system performance is optimized by running the AD676 at or near its maximum sampling rate of 100 kHz and digitally filtering the resulting spectrum to eliminate undesired frequencies.

DC CODE UNCERTAINTY

Ideally, a fixed dc input should result in the same output code for repetitive conversions. However, as a consequence of system noise and circuit noise, for a given input voltage there is a range of output codes which may occur. Figure 9 is a histogram of the codes resulting from 1000 conversions of a typical input voltage by the AD676 used with a 10 V reference.

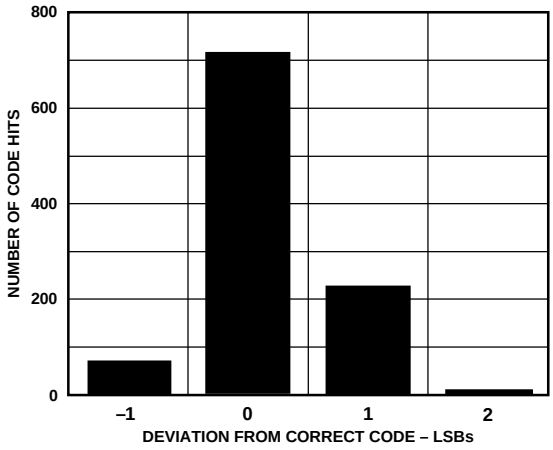


Figure 9. Distribution of Codes from 1000 Conversions, Relative to the Correct Code

The standard deviation of this distribution is approximately 0.5 LSBs. If less uncertainty is desired, averaging multiple conversions will narrow this distribution by the inverse of the square root of the number of samples; i.e., the average of 4 conversions would have a standard deviation of 0.25 LSBs.

MICROPROCESSOR INTERFACE

The AD676 is ideally suited for use in both traditional dc measurement applications supporting a microprocessor, and in ac signal processing applications interfacing to a digital signal processor. The AD676 is designed to interface with a 16-bit data bus, providing all output data bits in a single read cycle. A variety of external buffers, such as 74HC541, can be used with the AD676 to provide 3-state outputs, high driving capability, and to prevent bus noise from coupling into the ADC. The following sections illustrate the use of the AD676 with a representative digital signal processor and microprocessor. These circuits provide general interface practices which are applicable to other processor choices.

ADSP-2101

Figure 10a shows the AD676 interfaced to the ADSP-2101 DSP processor. The AD676 buffers are mapped in the ADSP-2101's memory space, requiring one wait state when using a 12.5 MHz processor clock.

The falling edge of BUSY interrupts the processor, indicating that new data is ready. The ADSP-2101 automatically jumps to the appropriate service routine with minimal overhead. The interrupt routine then instructs the processor to read the new data using a memory read instruction.

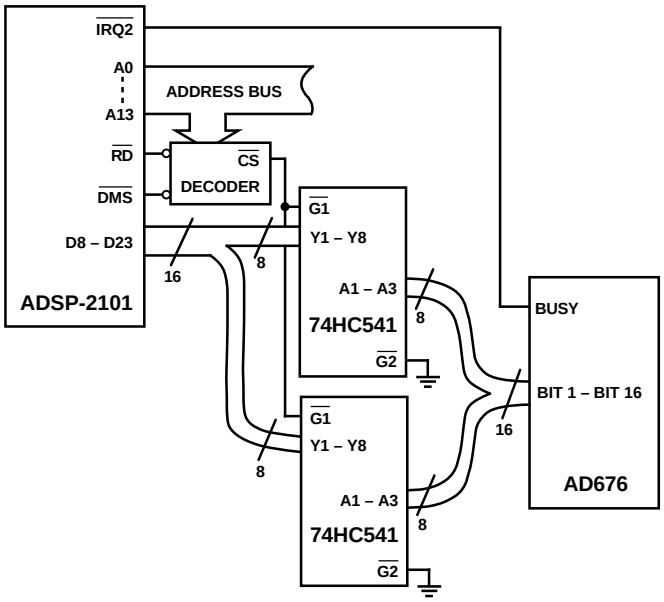


Figure 10a.

Figure 10b shows circuitry which would be included by a typical address decoder for the output buffers. In this case, a data memory access to any address in the range 3000H to 37FFH will result in the output buffers being enabled.

The AD676 CLK and SAMPLE can be generated by dividing down the system clock as described earlier (Figure 3), or if the ADSP-2101 serial port clocks are not being used, they can be programmed to generate CLK and SAMPLE.

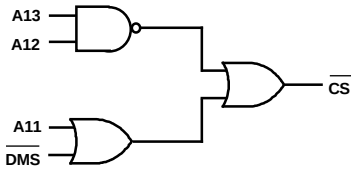


Figure 10b.

80286

The 80286 16-bit microprocessor can be interfaced to a buffered AD676 without any generation of wait states. As seen in Figure 11, BUSY can be used both to control the AD676 clock and to alert the processor when new data is ready. In the system shown, the 80286 should be configured in an edge triggered, direct interrupt mode (integrated controller provides the interrupt vector). Since the 80286 does not latch interrupt signals, the interrupt needs to be internally acknowledged before BUSY goes HIGH again during the next AD676 conversion (BUSY = 0). Depending on whether the AD676 buffers are mapped into memory or 1/0 space, the interrupt service routine will read the data by using either the MOV or the IN instruction. To be able to read all the 16 bits at once, and thereby increase the 80286's efficiency, the buffers should be located at an even address.

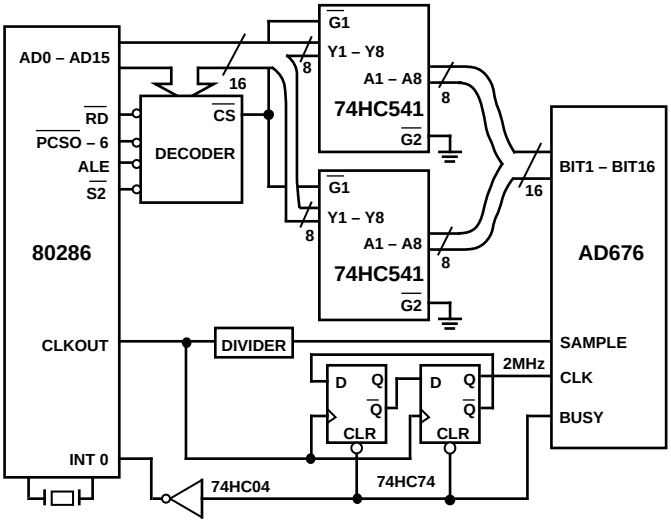


Figure 11.

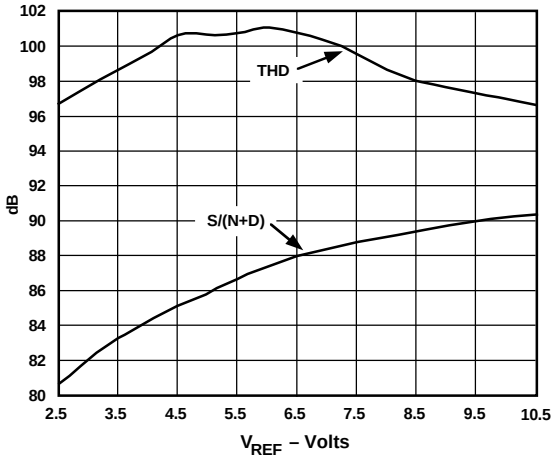


Figure 12. S/(N+D) and THD vs. V_{REF}

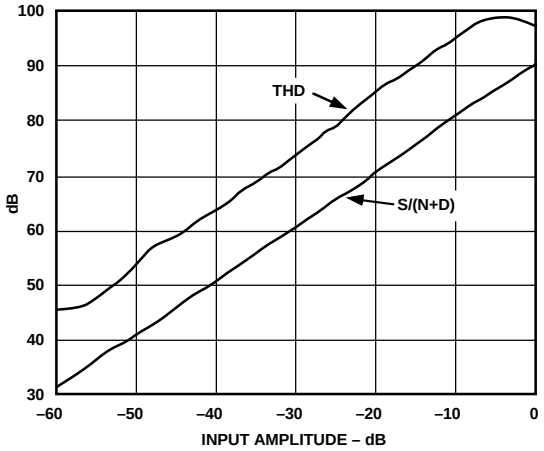


Figure 13. S/(N+D) and THD vs. Input Amplitude

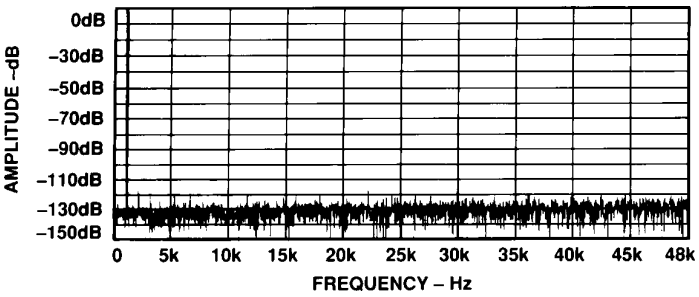


Figure 14. 4096 Point FFT at 96 kSPS, f_{IN} = 1.06 kHz

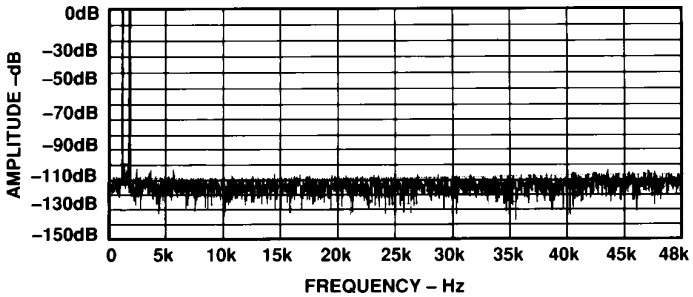


Figure 15. IMD Plot for f_{IN} = 1008 Hz (fa), 1055 Hz (fb) at 96 kSPS

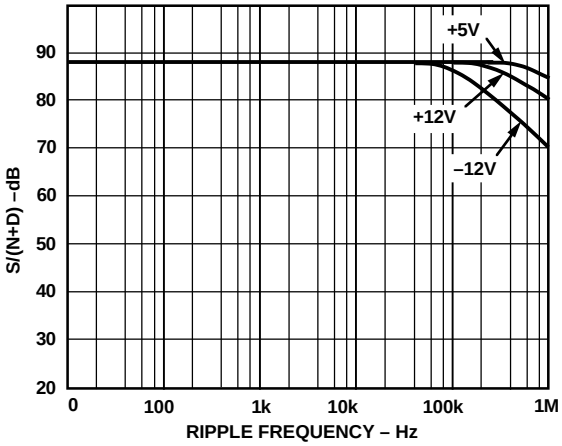
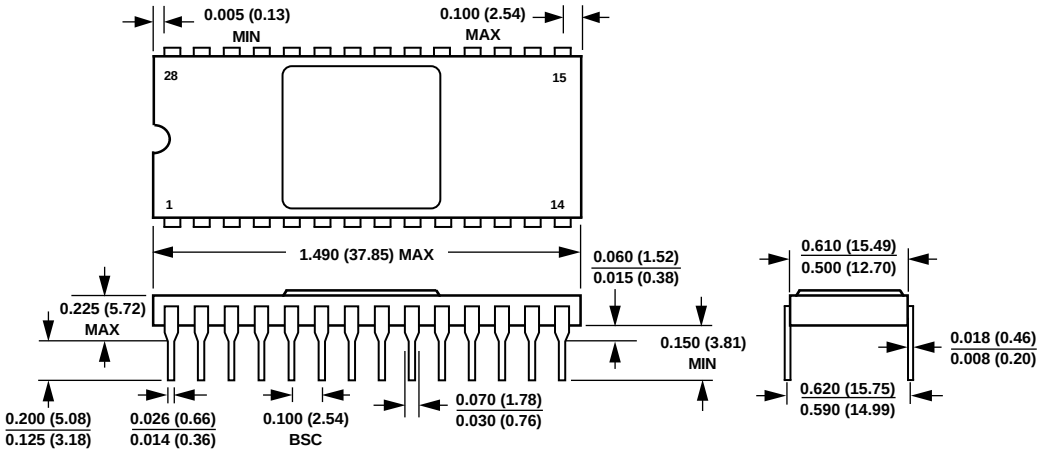


Figure 16. AC Power Supply Rejection (f_{IN} = 1.06 kHz) f_{SAMPLE} = 96 kSPS, V_{RIPPLE} = 0.13 V p-p

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

28-Pin Ceramic DIP Package (D-28)



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