Ordering number : ENA2341

LV25810PEB

ON Semiconductor®

http://onsemi.com

Bi-CMOS LSI

Car DSP Tuner

Overview

LV25810PEB is a DSP tuner LSI which adopts Low-IF. This IC has realized not only the significant reduction of external parts compare to the existing model by integration, but also the reconfiguration of specification according to customers' need by setting and controlling the software of microcontroller, in which constant is programmable. Therefore, this IC curbs the total cost and realizes a tuner which corresponds to on-board type.
This LSI implements serial bus (I^2C) I/F, which realizes reduction of communication line with microcontroller. In mass production, it is effective to prevent troubles related to line layout, and to reduce area of the system main board. In addition to radio basic functions, LV25810PEB integrates a new original CMA circuit to enhance multipath noise rejection feature. Also, LV25810PEB includes an HD Radio decoder interface.

Features

- LOW-IF (AM=57.5/58.33/58.5/58.75/59.75/60.5kHz, FM=300kHz)
- Implementation area is reduced by part reduction.
- Standard AM/FM global tuner [AM (LW, MW, SW), FM (JAPAN, US, EU, E-EU, WB)]
- HD radio ready (I^2S I/O port for external HD Radio decoder)
- The best multipath noise rejection of all the other ICs with new CMA.

Functions

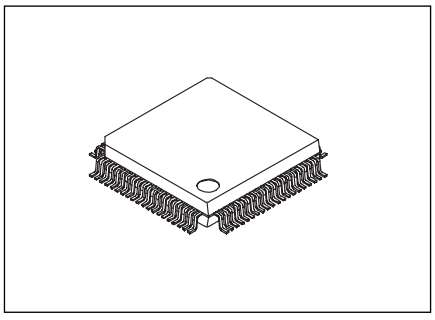
FM/AM FE, PLL, IF, FM/AM detector, FM/AM-noise canceller, FM-multipath noise canceller, FM-MPX, switching diversity, RDS demodulator/decoder, integrated HD Radio interface function (HD blend processing).

Function Overview

1) FM RF-LNA
2) FM IQ mixer
3) FM RF-AGC
4) AM RF-LNA
5) AM IQ mixer
6) AM RF-AGC
7) FM/AM IF-AGC
8) IF ADC
9) Variable IF band filter
10) Image canceller
11) IF block multipath noise rejection (CMA)
12) FM/AM pulse noise canceller
13) FM stereo decoder
14) Audio block multipath noise rejection (MRC)
15) RDS demodulator and decoder
16) IF data output for HD decoder
17) Digital I^2S input for HD blend function
18) Stereo output (analog DAC/ digital I^2S)
19) PLL synthesizer
20) Switching diversity

Package

QFP80 (14×14), 0.65mm pitch
(Required to solder the Exposed-Die-Pad to GND)



QFP80(14X14)

* I^2C Bus is a trademark of Philips Corporation.

ORDERING INFORMATION

See detailed ordering and shipping information on page 28 of this data sheet.

June, 2014

61714NK 20140530-S00001 No.A2341-1/28

Absolute Maximum Ratings at Ta=25°C, VSS=0V

Parameter	Symbol	Pin name	Conditions	Value	unit
Supply voltage	Vcc1 max	VCC (5V)	For FE analog	–0.3 to 5.8	V
Supply voltage	Vcc2 max	VDD33, PLLVDD, XVDD, AVDD33, DACVDD (3.3V)	For FE logic, BE_ADC, and DAC	–0.3 to 3.9	V
Supply voltage	Vcc3 max	VDD15 (1.5V)	BE logic power supply w/ internal regulator and external FET, external power supply is unnecessary.	–0.3 to 1.8	V
Input voltage	VIN1max	*1		VSS–0.3 to VDD+0.3	V
	VIN2max	*2		VSS–0.3 to 5.5	V
Operating temperature	Topr			–40 to +85	°C
Storage temperature	Tstg			–50 to +125	°C

*1) Please refer the "Pin Overview" list of Page5/Page6 for the details of each VDD name and the supply voltage to them.

*2) TEST, RSTB, BL_SEL, BL_LRCK, BL_BCLK, BL_DATA, I2C_SCL, I2C_SDA, TESTI1, TESTI2

Only when the power supplies are On, you can apply voltage to input pin up to 5.5V. When the power is OFF, you can only apply voltage up to 3.6V.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Allowable operating range at Ta=–40 to +85°C, VSS=0V

Parameter	Symbol	Pin name	Conditions	Min.	Typ.	Max.	unit
Supply voltage	Vcc1	VCC_OSC VCC_IF VCC_AM VCC_FM		4.75	5.0	5.25	V
Supply voltage	Vcc21	VDD33, PLLVDD, XVDD		3.15	3.3	3.45	V
Supply voltage	Vcc22	AVDD33, DACVDD		3.15	3.3	3.45	V
Supply voltage	Vcc3	VDD15		1.42	1.5	1.58	V
Input "H" level voltage	VIH	*4		2.0	–	–	V
Input "L" level voltage	VIL	*4		–	–	0.8	V
Allowable power dissipation *3	Pdmax		78mm×106mm×1.7mm PWB (Glass epoxy, Double-sided) Ta=85°C, Exposed-Die-Pad is soldered to GND.	–	–	1250	mW
AM reception frequency			LW MW SW	146k 520k 2.28M	–	281k 1710k 26.1M	Hz
FM reception frequency			E-EU, EU, US, Japan	65	–	108	MHz
WB reception frequency			WB	162.4	–	162.55	MHz
X'tal oscillator frequency		XIN, XOUT	*5	–	62.4	–	MHz

*3) Required more than 90% of Exposed Die-Pad area to be soldered to GND.

*4) TEST, RSTB, MODE, BL_SEL, BL_LRCK, BL_BCLK, BL_DATA, SP_SSB, SP_CLK, SP_DI, SP_DO

*5) X'tal CI value ≤ 40Ω (X'tal oscillator)

In X'tal oscillation circuit, circuit constant fluctuates depends on X'tal oscillator and a pattern of a board. Therefore, it is recommended that a manufactures of the X'tal oscillator performs an evaluation.

Recommended operating supply voltage at Ta=25°C

Parameter	Symbol	Pin name	Min.	Typ.	Max.	unit
Supply voltage	Vcc1	VCC_OSC, VCC_IF, VCC_AM ,VCC_FM	–	5.0	–	V
Supply voltage	Vcc2	VDD33, PLLVDD, XVDD, AVDD33, DACVDD	–	3.3	–	V
Supply voltage	Vcc3	VDD15	–	1.5	–	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Electrical characteristics at Ta=25°C, FM fr=98.1MHz

Parameter	Symbol	Pin name	Conditions	Min.	Typ.	Max.	unit
Current consumption (5V FM)	I5V_FM		No input signal, FM Mode	85	100	115	mA
Current consumption (3.3V FM)	I33V_FM		No input signal, FM Mode	68	80	92	mA
Current consumption (1.5V FM)	I15V_FM		No input signal, FM Mode	153	180	207	mA
Local frequency 3rd spurious rejection ratio	FM_HRR3		Freq. Setting =90MHz, Input Freq. =271.2MHz Reference input level: 90MHz 20dBuV	70	80	–	dB
Input impedance	Zi	FM_IN+ FM_IN-	Impedance between pin 69 and 70	–	300	–	Ω
RF AGC start point	F_RFAGC		RF AGC operation sensitivity @RF_ATT 2→3	67	73	79	dBuV
IF AGC start point	F_IFAGC		IF AGC operation start point @IF_ATT 0→1	53	59	65	dBuV
S-Meter DC 1	SMDC_F1		SMDC Value @30dBuV no-dev input After calibration to SMDC=100	98	100	102	–
S-Meter DC 2	SMDC_F2		SMDC Value @10dBuV no-dev input After calibration to SMDC_F1	43	48	53	–
S-Meter DC 3	SMDC_F3		SMDC Value @50dBuV no-dev input After calibration to SMDC_F1	147	152	157	–
Practical sensitivity (FM)	US	DACLOUT DACROUT	fm=1kHz, 22.5kHz dev. S/N=30dB ANT input level IF BW=60kHz, HCC ON	–	3	6	dBuV
Output level (FM)	VoFM	DACLOUT DACROUT	60dBuV, fm=1kHz, 75kHz dev.		200		mVrms
THD(MONO)	THD_{MONO}	DACLOUT DACROUT	60dBuV, fm=1kHz, 75kHz dev.	–	0.1	0.7	%
S/N(MONO)	S/N MONO	DACLOUT DACROUT	60dBuV, fm=1kHz, 75kHz dev.	66	72	–	dB
THD(STEREO)	THD ST	DACLOUT DACROUT	80dBuV, fm=1kHz, L=R 90% mod., Pilot 10% mod.	–	0.4	1	%
S/N(STEREO)	S/N ST	DACLOUT DACROUT	60dBuV, fm=1kHz, L=R 90% mod., Pilot 10% mod.	61	67	–	dB
AMR	AMR	DACLOUT DACROUT	60dBuV, fm=1kHz, 75kHz dev., fm=1kHz 30%AM, CMA=OFF	60	67	–	dB
Separation	SEP	DACLOUT DACROUT	60dBuV, fm=1kHz, 30%mod, L-ch only	35	45	–	dB
Image rejection rate	IRR	DACLOUT DACROUT	fr=98.7MHz, fm=400Hz, 22.5kHz dev. (after adjustment by IQ correction circuit)	65	80	–	dB
Interference characteristic (Sensitivity reduction)	2SIG	DACLOUT DACROUT	fud=98.5MHz, fm=400Hz, 110dBuV, 22.5kHz dev. fd=98.1MHz, fm= 1kHz, 22.5kHz dev. S/N=30dB ANT input level	–	35	41	dBuV

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AM fr=1MHz, After tuning AM RF Synchronization

Parameter	Symbol	Pin name	Conditions	Min.	Typ.	Max.	unit
Current consumption (5V AM)	I5V_AM		No input signal, AM Mode	72.25	85	97.75	mA
Current consumption (3.3V AM)	I33V_AM		No input signal, AM Mode	68	80	92	mA
Current consumption (1.5V AM)	I15V_AM		No input signal, AM Mode	93.5	110	126.5	mA
Local frequency 3rd and 5th spurious rejection ratio	AM_HRR3 AM_HRR5		Freq. Setting = 1000kHz, AM_HRR3: 3230kHz, with RF input, AM_HRR5: 5230kHz, with RF input	70	80	–	dB
RF AGC start point	RF AGC		RF AGC operation start point @RF_ATT 0→1	78	84	90	dBuV
IF AGC start point	IF AGC		IF AGC operation start point @IF_ATT 0→1	67	73	79	dBuV
S-Meter DC 1	SMDC_A1		SMDC Value @40dBuV no-dev input After calibration to SMDC=140	138	140	142	–
S-Meter DC 2	SMDC_A2		SMDC Value @20dBuV no-dev input After calibration to SMDC_A1	83	88	93	–
S-Meter DC 3	SMDC_A3		SMDC Value @60dBuV no-dev input After calibration to SMDC_A1	187	192	197	–
Practical sensitivity (AM)	US	DACLOUT DACROUT	fm=400Hz 30%, S/N20dB, HCC=ON, Speech enhancer=ON ANT input level	–	22	25	dBuV
Output level(AM)	VoAM	DACLOUT DACROUT)	74dBuV, fm=400Hz30%, det. output level (with LPF)		70		mVrms
S/N(AM)	S/N	DACLOUT DACROUT	74dBuV fm=400Hz 30%mod.	56	62	–	dB
THD(AM)	THD	DACLOUT DACROUT	74dBuV fm=400Hz 80%mod	–	0.1	1.0	%
Image rejection ratio	IRR	DACLOUT DACROUT	fr=1115kHz, fm=400Hz, 30%mod (after adjustment by IQ correction circuit)	70	80	–	dB
Anti-interference feature	CROSS	DACLOUT DACROUT	fud=1.08MHz 100dBuV, fm= 1kHz, 80%mod, fd=1MHz 65dBuV, fm=400Hz, 30%mod.	32	38	–	dB

DC characteristics

Parameter	Symbol	Pin name	Conditions	Min.	Typ.	Max.	unit
Output "H" level Voltage	VOH	*8	IOH=1mA	Vcc2−0.4			V
		*6	IOH=2mA	Vcc2−0.4			V
		*7	IOH=4mA	Vcc2−0.4			V
Output "L" level Voltage	VOL	*8	IOL=1mA			0.4	V
		*6	IOL=2mA			0.4	V
		*7	IOL=4mA			0.4	V
Input leak current	IL	*9		−10		10	μA
Hysteresis voltage	VHYS	*9			0.25		V

*6) ANT1, ANT2, BUSY, SP_ERR, IB_BCLK
*7) I2C_SDA
*8) IB_WS, IB_IDATA, IB_QDATA, RDSC, RDSD, RDSID, AO_BCLK, AO_LRCK, AO_DATA,
*9) TEST, RSTB, BL_SEL, BL_LRCK, BL_BCLK, BL_DATA, I2C_SCL, I2C_SDA, TESTI1, TESTI2

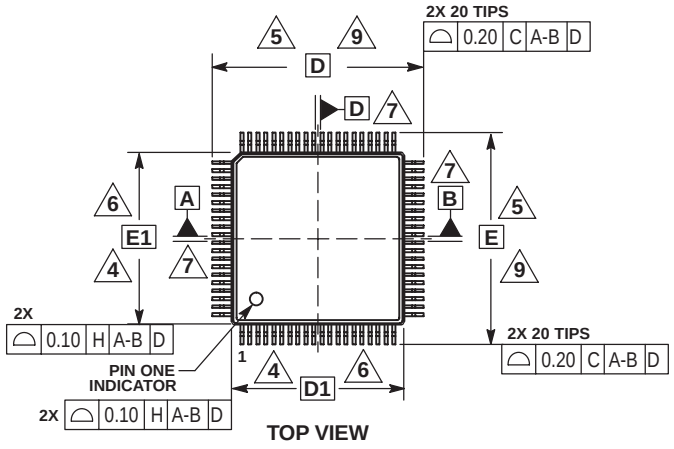
Additional data :

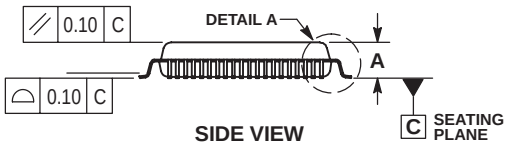
1. Digital audio output (I^2S) Fs=54.167kHz
2. HD decoder output (I^2S) Fs=650kHz
3. DAC output : S/N=87dB typ. (−3dBFS Input)

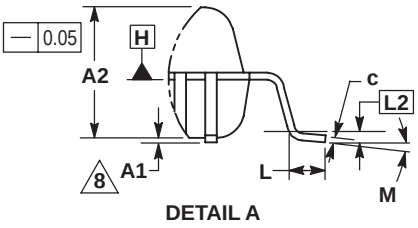
Package Dimensions

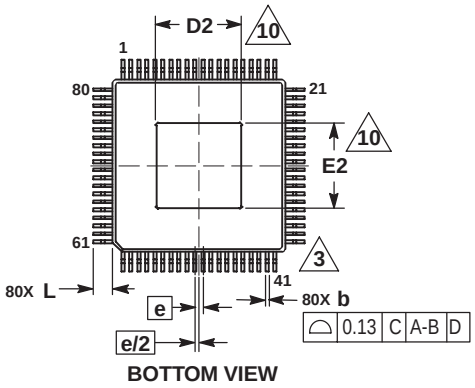
unit : mm

PQFP80 14x14, 0.65P
CASE 122CG
ISSUE O





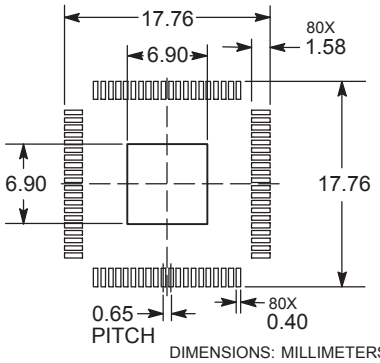




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL BE 0.08 MAX. AT MMC. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07.
4. DIMENSIONS D1 AND E1 DO NO INCLUDE MOLD FLASH, GATE BURRS, OR PROTRUSIONS. MOLD FLASH, GATE BURRS, OR PROTRUSIONS SHALL NOT EXCEED 0.25 PER SIDE. DIMENSIONS D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE INCLUDING MOLD MISMATCH.
5. THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE SIZE BY AS MUCH AS 0.15.
6. DIMENSIONS D1 AND E1 TO BE DETERMINED AT DATUM PLANE H.
7. DATUMS A−B AND D ARE DETERMINED AT DATUM PLANE H.
8. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
9. DIMENSIONS D AND E TO BE DETERMINED AT DATUM PLANE C.
10. EXPOSED PAD TO BE COPLANAR WITH THE BOTTOM OF THE PACKAGE.

	MILLIMETERS	
DIM	MIN	MAX
A	–––	2.95
A1	0.05	0.15
A2	2.70 REF	
b	0.20	0.30
c	0.10	0.30
D	17.20 BSC	
D1	14.00 BSC	
D2	6.70	7.10
E	17.20 BSC	
E1	14.00 BSC	
E2	6.70	7.10
e	0.65 BSC	
L	0.60	1.00
L2	0.25 BSC	
M	0°	10°

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Pin overview

I : Input pin, O : Output Pin, B : Bi-Directional Pin, A : Analogue Pin, P : Power Supply
Output Level1: Initial condition (After finishing reset procedure), Output Level2 : During reset procedure

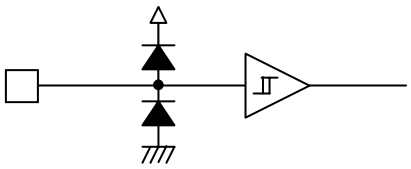
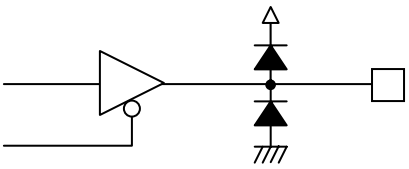
Pin No.	Pin name	I/O	Output Level1	Output Level2	Description	VDD/ VCC	VSS/ GND	Unused connection
1	GND_OSC	P			LoOSC GND			
2	VT_out	A			Tuning voltage output	VCC_OSC	GND_OSC	
3	CP_SW	A			PLL AM/FM time constant switching			
4	VCC_OSC	P			LoOSC power supply (5V)			
5	GND_PLL	P			PLL GND			
6	VDD33_FE	P			FE Digital power supply (3.3V)			
7	VDD33	P			BE Digital power supply (3.3V)			
8	DVSS	P			Digital GND			
9	VDD15	P			Digital power supply (1.5V)			
10	ANT1	O	H	L	Antenna switching 1	VDD33	DVSS	Open
11	ANT2	O	H	L	Antenna switching 2			Open
12	TEST	I			Test pin L: normal operation H: test mode Connect to GND during normal operation			To GND
13	BL_SEL	I			IBOC blend input select			To GND
14	BL_LRCK	I			IBOC blend input LR clock			To GND
15	BL_BCLK	I			IBOC blend input bit clock			To GND
16	BL_DATA	I			IBOC blend input data			To GND
17	IB_WS	O	L	L	IBOC signal output word synchronization			Open
18	IB_BCLK	O	L	L	IBOC signal output bit clock			Open
19	IB_IDATA	O	L	L	IBOC signal output I data			Open
20	IB_QDATA	O	L	L	IBOC signal output Q data			Open
21	RDSC	O	L	L	RDS output clock			Open
22	RDSD	O	L	L	RDS output data			Open
23	RDSID	O	L	L	RDS output data judgment			Open
24	RSTB	I			Reset input			
25	BUSY	O	L	H	CPU interface busy signal output H: busy			
26	SP_ERR	O	L	L	CPU interface error output H : error			
27	I2C_SDA	B	Z	Z	CPU interface I^2C data input / output			
28	TESTI1	I			Test pin (connect to GND)			To GND
29	I2C_SCL	I			CPU interface I^2C clock input			
30	TESTI2	I			Test pin (connect to GND)			To GND
31	AO_BCLK	O	L	L	Audio digital output bit clock			
32	AO_LRCK	O	L	L	Audio digital output LR clock			Open
33	AO_DATA	O	L	L	Audio digital output data			Open
34	VDD33	P			Digital power supply (3.3V)			Open
35	REFV	O			1.5V reference voltage output			
36	DVSS	P			Digital GND	DVDD33	DVSS	Open
37	VDD15	P			Digital power supply (1.5V)			
38	PLLVDD	P			PLL power supply (3.3V)	PLLVDD	PLLVSS	
39	PLLVSS	P			PLL GND			
40	DACVSS	P			Audio DAC GND	DACVDD	DACVSS	
41	DACROUT	A			Audio DAC R channel output			Open
42	DACREF	A			Audio DAC reference voltage			Open
43	DACLOUT	A			Audio DAC L channel output			Open
44	DACVDD	P			Audio DAC power supply (3.3V)			
45	XIN	I			X'tal oscillation amplifier input	XVDD	XVSS	
46	XOUT	O			X'tal oscillation amplifier output			
47	XVDD	P			X'tal oscillation power supply(3.3V)			
48	XVSS	P			X'tal oscillation GND			
49	AVSSVREF	P			IF ADC reference GND	AVDD33	AVSS33	
50	AVREFI	A			IF ADC reference voltage(I)			
51	AVREFQ	A			IF ADC reference voltage(Q)			
52	AVDDVREF	P			IF ADC reference power supply (3.3V)			

Continued on next page

Continued from preceding page.

Pin No.	Pin name	I/O	Output Level1	Output Level2	Description	VDD/ VCC	VSS/ GND	Unused connection
53	TEST-	A	Z	Z	Test pin TEST is normally open.	AVDD33	AVSS33	Open
54	TEST+	A	Z	Z	Test pin TEST is normally open.			Open
55	AVDD33	P			IF ADC power supply (3.3V)			
56	AVSS33	P			GND for IF ADC/ FE-IF			
57	Vref	A			FE reference voltage (3.15V)	VCC_IF	AVSS33	
58	VCC_IF	P			IF power supply (5V)			
59	FE TEST	A			FE TEST pin			Open
60	AM_RF_AGC1	A			Rectifier pin for AM RF AGC	VCC_AM	GND_AM	
61	AM_LNA_IN+	A			AM LNA input+			
62	AM_LNA IN-	A			AM LNA input-			
63	VCC_AM	P			AM power supply (5V)			
64	AM_LNA_out+	A			AM LNA output+	VCC_AM	GND_AM	
65	AM_LNA_out-	A			AM LNA output-			
66	GND_AM	P			AM GND			
67	AM_CB_IN-	A			AM Cap Bank input-	VCC_AM	GND_AM	
68	AM_CB_IN+	A			AM Cap Bank input+			
69	FM_IN+	A			FM LNA input+	VCC_FM	GND_FM	
70	FM_IN-	A			FM LNA input-			
71	VCC_FM	P			FM power supply (5V)			
72	WB_IN+	A			Weather Band LNA input+/ FM ANT buffer output+	VCC_FM	GND_FM	
73	WB_IN-	A			Weather Band LNA input-/ FM ANT buffer output-			
74	GND_FM	P			FM GND			
75	PIN_DIODE	A			Pin diode drive pin	VCC_FM	GND_FM	
76	FM_RF_AGC0	A			Rectifier pin0 for FM RF AGC			
77	FM_RF_AGC1	A			Rectifier pin1 for FM RF AGC			
78	VCO1	A			VCO oscillation pin1	VCC_OSC	GND_OSC	
79	VCO_BIAS	A			VCO bias			
80	VCO2	A			VCO oscillation pin2			

Circuit Stricture

Pin	Function	Equivalent circuit	Remarks
12 13 14 15 16 24 27 28 30	TEST BL_SEL BL_LRCK BL_BCLK, BL_DATA RSTB I2C_SCL, TESTI1 TESTI2		Digital Input (5V tolerant)
10 11 17 18 19 20 21 22 23 25 26 31 32 33	ANT1 ANT2 IB_WS IB_BCLK IB_IDATA IB_QDATA RDSC RDSD RDSID BUSY SP_ERR AO_BCLK AO_LRCK AO_DATA		Digital Output

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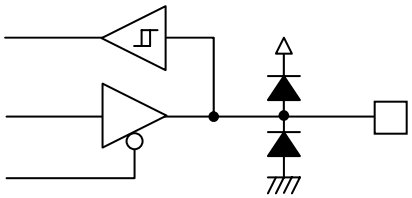
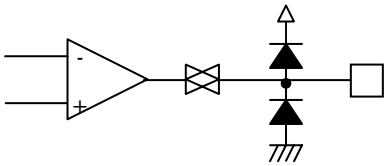
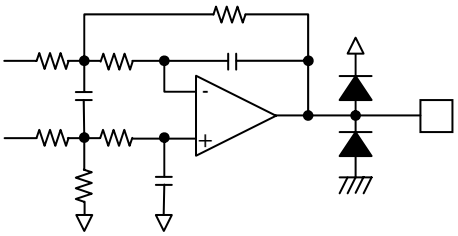
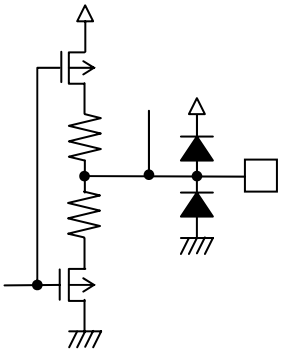
Pin	Function	Equivalent circuit	Remarks
27	I2C_SDA		Digital Input/Output (5V tolerant)
34	VDD33	-	Digital Power Supply (3.3V)
35	REFV		Reference Voltage output
36	DVSS	-	Digital GND
37	VDD15	-	Digital Power Supply (1.5V)
38	PLLVDD	-	PLL Power Supply (3.3V)
39	PLLVSS	-	PLL GND
40	DACVSS	-	GND for Audio DAC
41 43	DACROUT DACLOUT		DAC Output
42	DACREF		Reference Voltage Output for AudioDAC
44	DACVDD	-	VDD for Audio DAC (3.3V)

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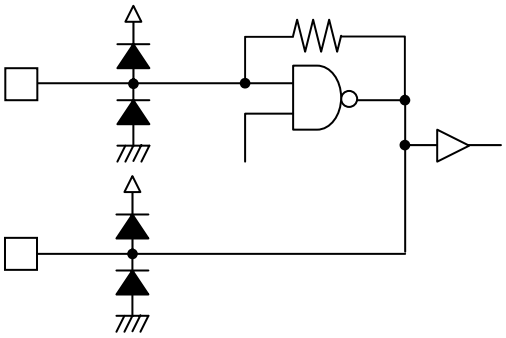
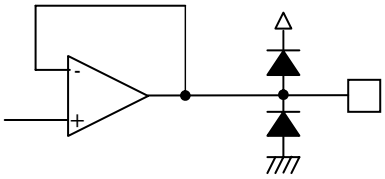
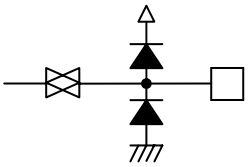
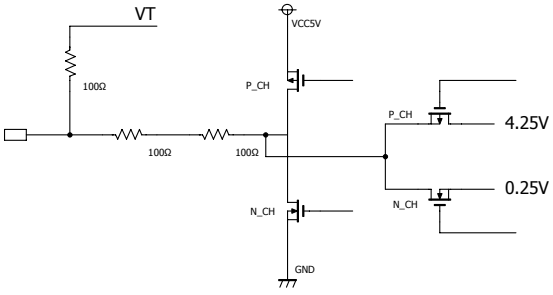
Pin	Function	Equivalent circuit	Remarks
45 46	XIN XOUT		Oscillator circuit
47	XVDD	-	VDD for Crystal OSC (3.3V)
48	XVSS	-	GND for Crystal GND
49	AVSSVREF	-	Reference GND for IF ADC
50 51	AVREFI AVREFQ		ADC REF Output
52	AVDDVREF	-	Reference VDD for IF ADC (3.3V)
53 54	TEST+ TEST-		TEST
1	GND_OSC	-	• GND for LO_OSC
2	VT out		• PLL charge-pump output • Control input for internal varactor Charge-pump output is transferred to DC signal with external LPF.

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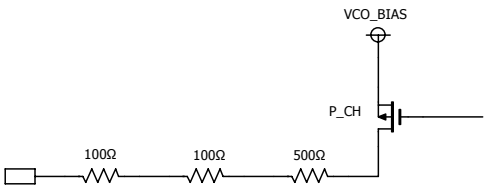
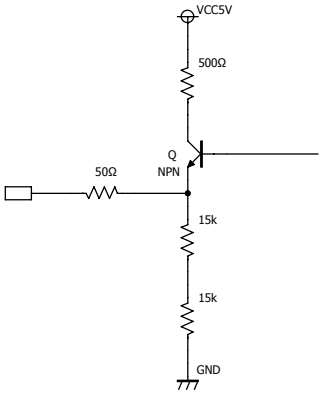
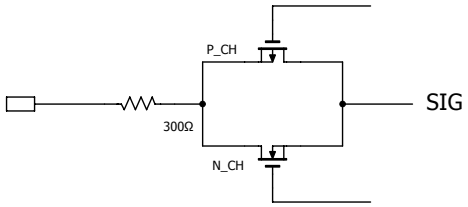
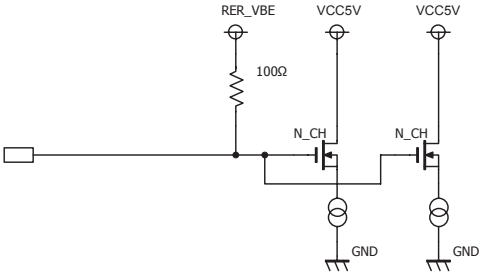
Pin	Function	Equivalent circuit	Remarks
3	CP SW		• Switch the constant value of external LPF.
4	VCC_OSC	-	• 5V supply for LO_OSC
5	GND_PLL	-	• Digital GND for PLL
6	VDD33_FE	-	• 3,3V supply for FE
57	Vref		• Capacitor for internal power supply circuit. This capacitor stabilizes the internal power supply circuit.
58	VCC_IF	-	• 5V supplu for FE IF
59 60	FE_TEST AM RF AGC1		• AM RF AGC output
61 62	AM_IN- AM_IN+		• AM LNA input →Input RF signal.
63	VCC_AM	-	• 5V supply for AM

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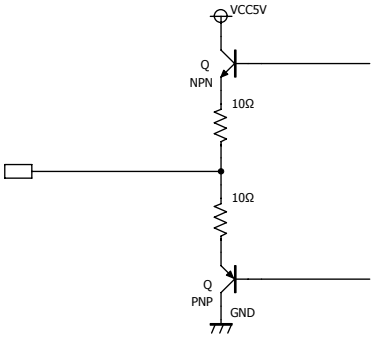
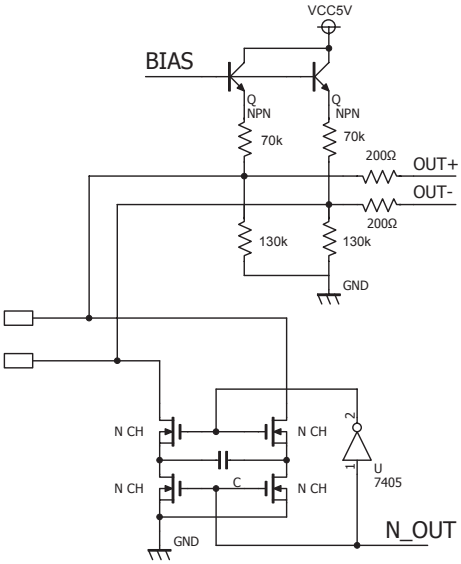
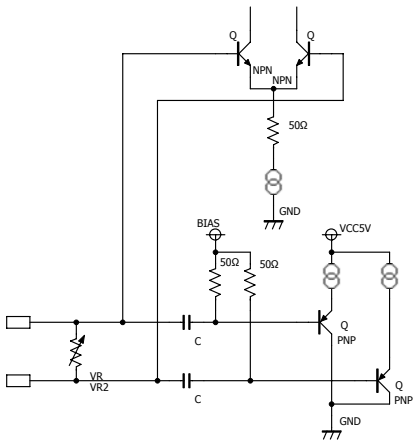
Pin	Function	Equivalent circuit	Remarks
64 65	AM LNA out+ AM LNA out-		• AM LNA output
66	GND_AM	-	• GND for AM
67 68	AM_CB_IN- AM_CB_IN+		• AM capacitor-bank input
69 70	FM_IN+ FM_IN-		• FM LNA input ➔ Input RF signal.
71	VCC_FM	-	• 5V supply for FM

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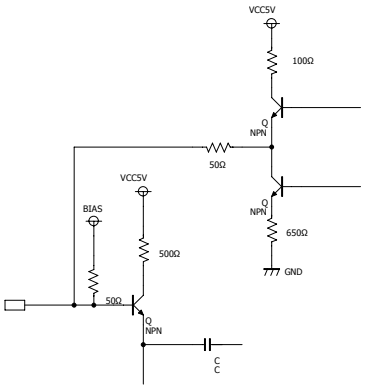
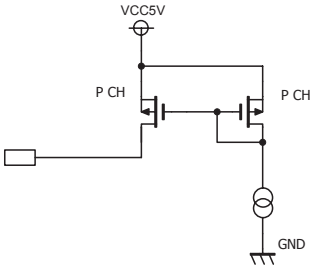
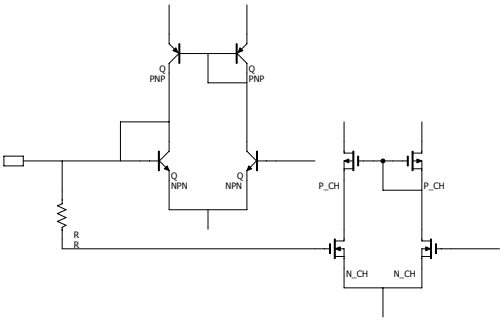
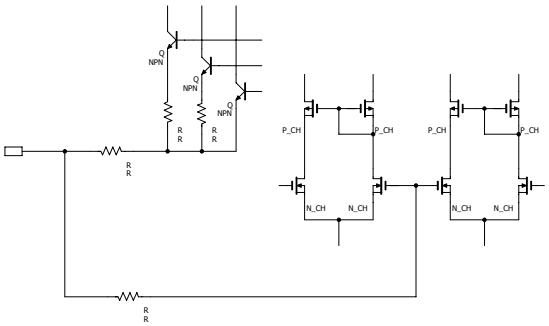
Pin	Function	Equivalent circuit	Remarks
72 73	WB_IN+ WB_IN-		• LNA input for weatherband (WB) • Buffered-Output for sub-tuner ➔ Output RF signal These pins are use for WB input or Buffered-Output for sub-tuner
74	GND_FM	–	• GND for FM
75	PIN_DIODE		• PIN diode driver
76	FM_RF_AGC0		• Rectifier for FM RFAGC0
77	FM_RF_AGC1		• Rectifier for FM RFAGC1

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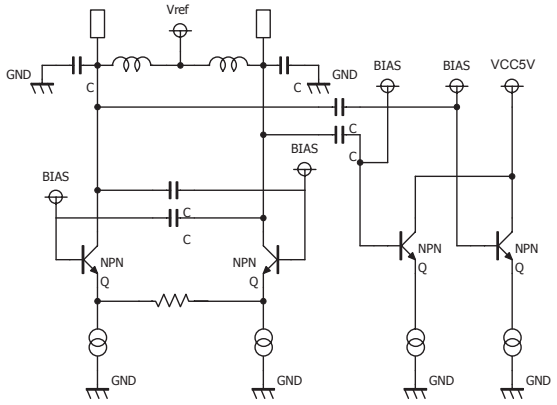
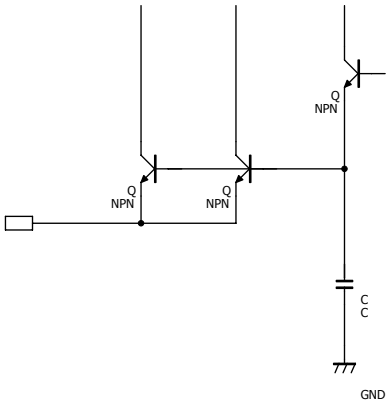
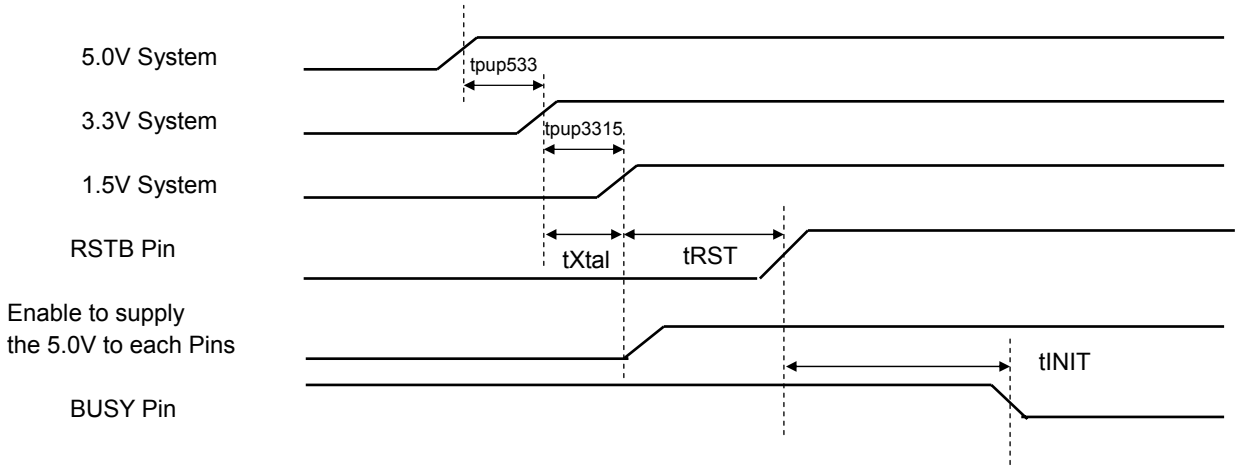
Pin	Function	Equivalent circuit	Remarks
78 80	VCO1 VCO2		• VCO oscillation ➔ Do not connect any other circuit.
79	VCO_BIAS		• VCO BIAS pin ➔ For the stabilization of the VCO bias voltage level with external capacitor .

The Power Supply / Shut Down Procedure

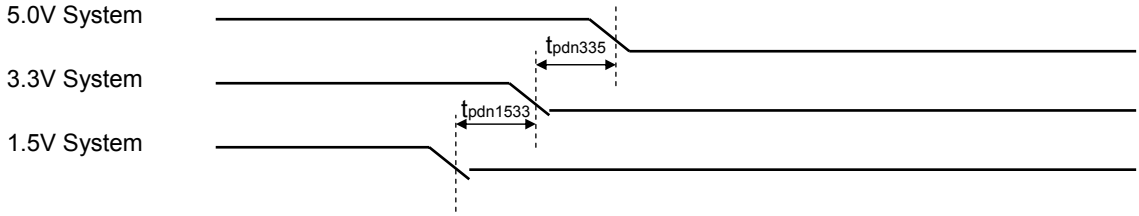
The power supply / shutdown order to each Power pins and the specified pins are as follows.
These order and timings must be kept absolutely.

1) To start the system



RSTB pin must be kept the "L" level during 5ms after latter either the 1.5V System is activated or the waiting time of the OSC being stable.

2) To Shut Down the System



Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Waiting Time (5.0V →3.3V)	tpup533		0		100	ms
Power Supply Waiting Time (3.3V → 1.5V)	tpup3315		0		100	
Waiting time of the OSC being stable	tXtal		5			
Reset Pulse Width	tRST		5			
LSI Initialization time *1	tINIT			9		
Shut Down Waiting Time (1.5V → 3.3V)	tpdn1533		0		100	
Shut Down Waiting Time (3.3V → 5.0V)	tpdn335		0		100	

*) In Digital Input pins (5V-Tolerant system), do not supply the "H (=5V)" level until all of power supply voltage level does not reach a defined value.
*) The input / output direction of each I/O pins are not defined until the 1.5V system is activated.

The order of the power supplies to 5V, 3V, and 1.5V system must be adhered closely to the following order.
5V → 3.3V → 1.5V
If this order is met and the total elapsed time of "tput533" and "tpup3315" is less than 100ms, the order that each power supply reaches the operation voltage can be ignored.

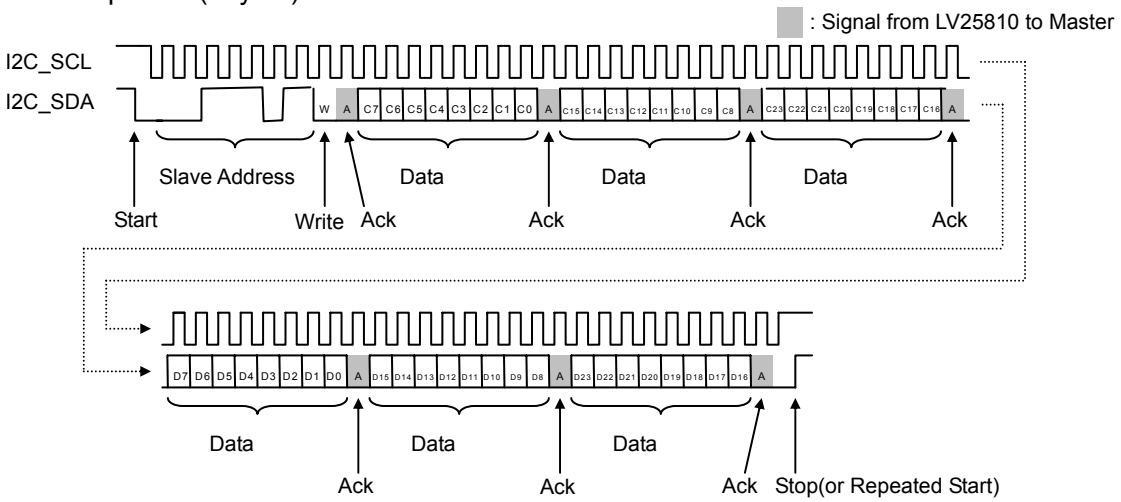
Host I/F

I²C I/F

The I²C interface supports 100kbs Standard mode and 400kbps High-Speed mode, and the unit of data transfer is 8 bits. The details of data read and data write are written in software control manual.
I2C slave address is 0x1D.

Data Write

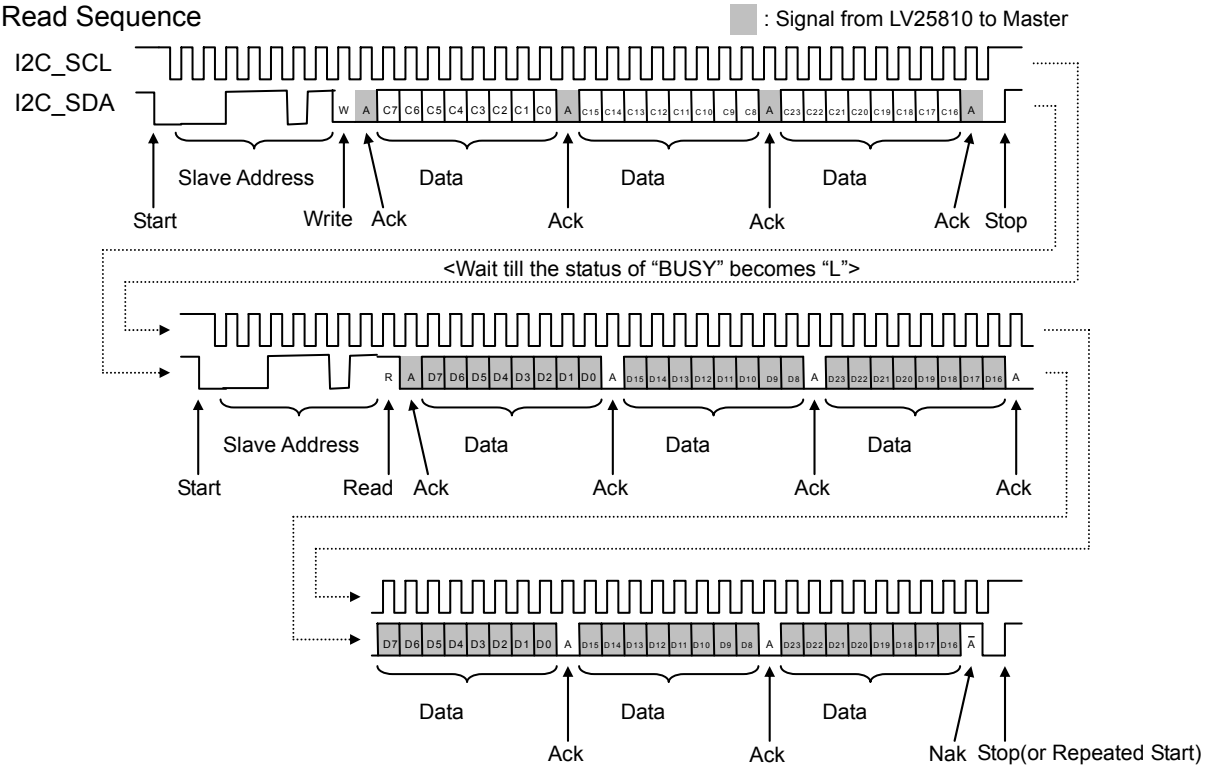
Data Write Sequence (6bytes)



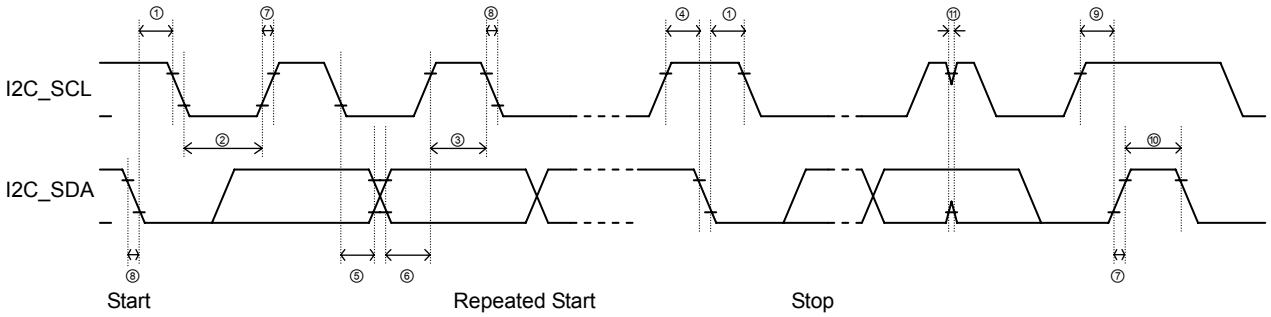
Data write can be accepted during the status of "BUSY" output level is "L". The command and data during the status of "BUSY" output level is "H" cannot be acceptable.

Data Read

Data Read Sequence



Timing Specifications



		Standard Mode (100kbps)		High-Speed Mode (400kbps)		
	Timing Parameters	Min.	Max.	Min.	Max.	Unit
①	Hold time of Start (Repeated-Start) condition	4000		600		ns
②	SCL “L” Level Pulse Width	4700		1300		ns
③	SCL “H” Level Pulse Width	4000		600		ns
④	Setup time of Start (Repeated-Start) condition	4700		600		ns
⑤	SDA Hold Time	0	3450	0	900	ns
⑥	SDA Setup Time	250		100		ns
⑦	SCL, SDA rise time		1000	20 + 0.1Cb	300	ns
⑧	SCL, SDA fall time		300	20 + 0.1Cb	300	ns
⑨	Setup time of Stop conditrion	4000		600		ns
⑩	Bus acceptable time	4700		1300		ns
⑪	Allowed Spike pulse width			0		ns

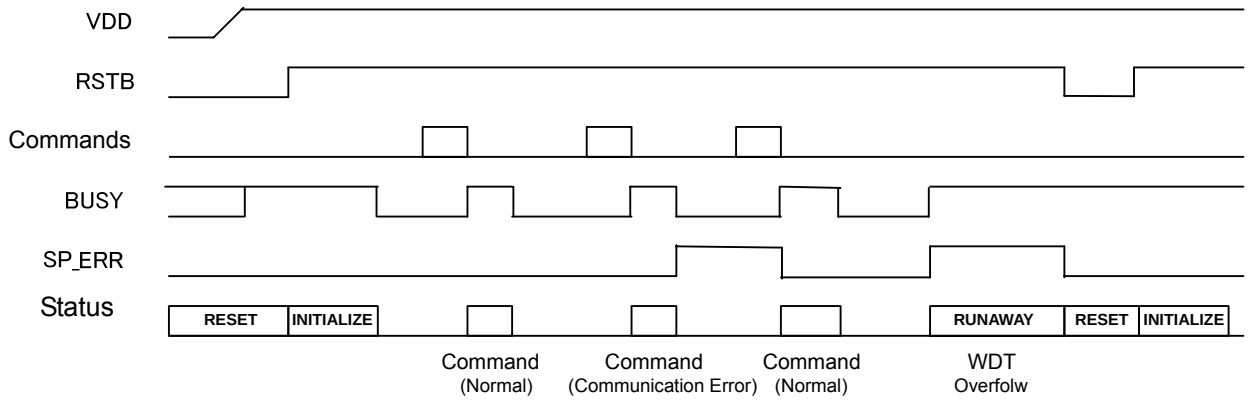
“Cb” in ⑦ and ⑧ means the total capacity of the bus line both I2C_SCL and I2C_SDA.
Details of each command are written in the “Software Control Manual.

WatchDog Timer

To detect the runaway of internal DSP, LV25810 has the WatchDog Timer (WDT) output pin.
When the DSP runaway, the WDT overflows and the DSP status can be confirmed by the output of BUSY and SP_ERR pin

Pin		Status
BUSY	SP_ERR	
0	0	Command Waiting
1	0	Commanad transfer finished
0	1	Communication Error
1	1	DSP Runaway (WDT Overflow)

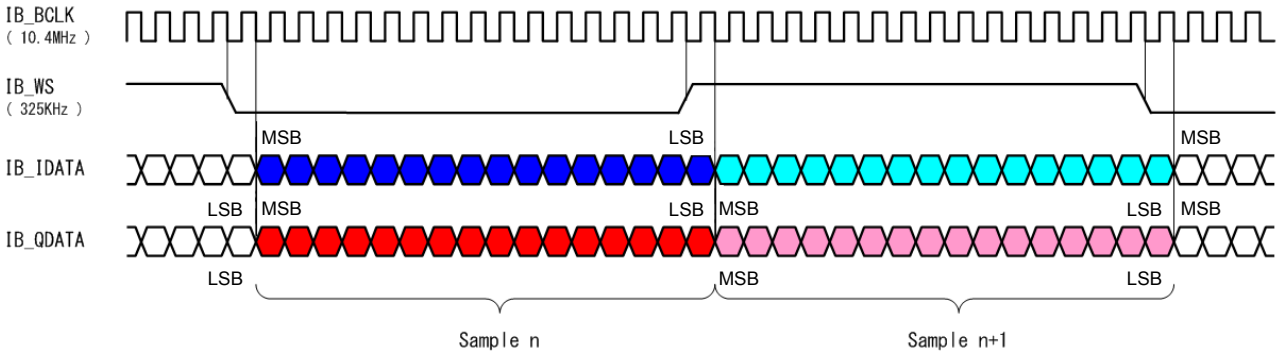
When both of BUSY and SP_ERR output level are “H”, the operation state of the DSP is abnormal.
If this occurs, the host CPU must reset and reboot the LV25810.



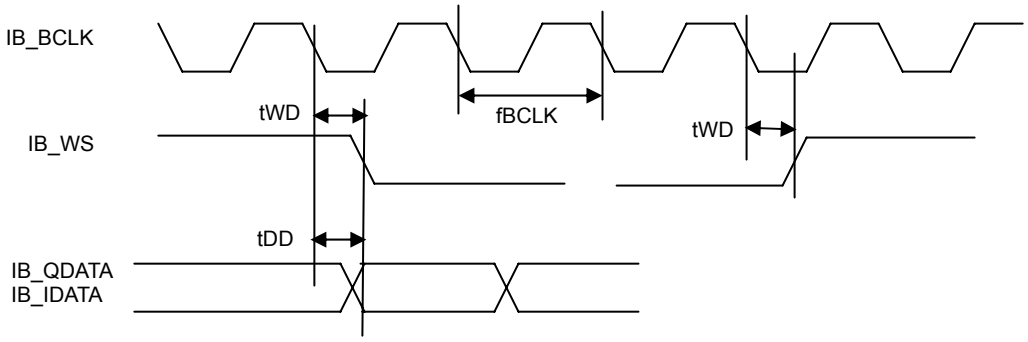
IBOC I/F

IBOC Decoder output is ready.
Fs : 650kHz
BCLK : 10.4MHz
Data Length : 16 bits

IBOC I/F Timing Chart



Timing Specifications

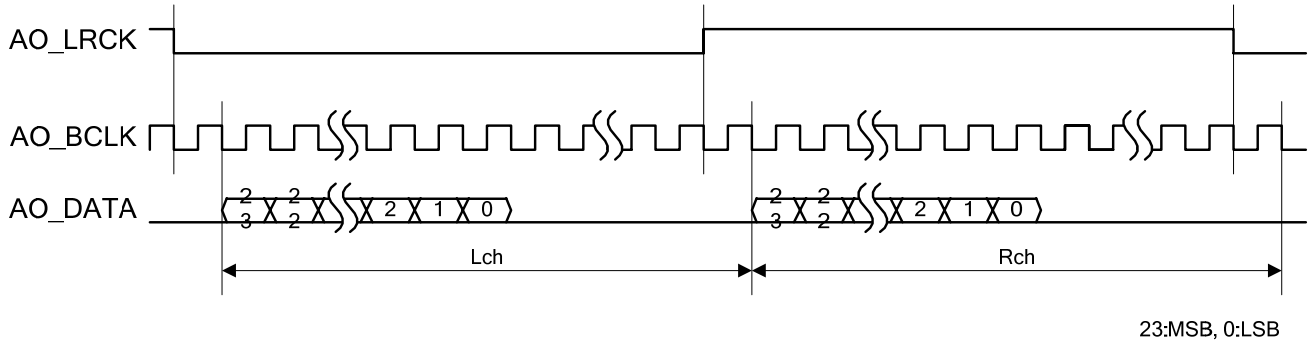


Parameter	Symbol	Min.	Typ.	Max.	Unit
IB_BCLK frequency	fBCLK		10.4		MHz
IB_WS Output Delay Time	tWD	0		10	ns
IB_QDATA, IB_IDATA Output Delay time	tDD	0		15	ns

Audio Output

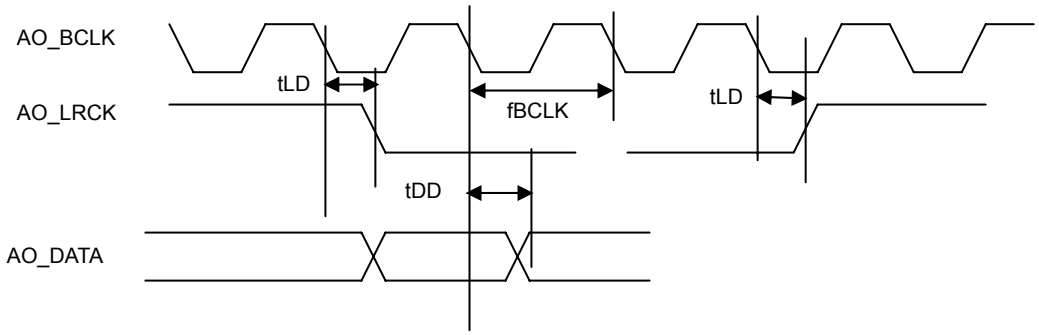
Audio output (I2S format) is available.
fs : 54.167kHz
BCLK : 64fs
Data Length : 24 bits

Audio Output Timing Chart



23:MSB, 0:LSB

Timing Specifications

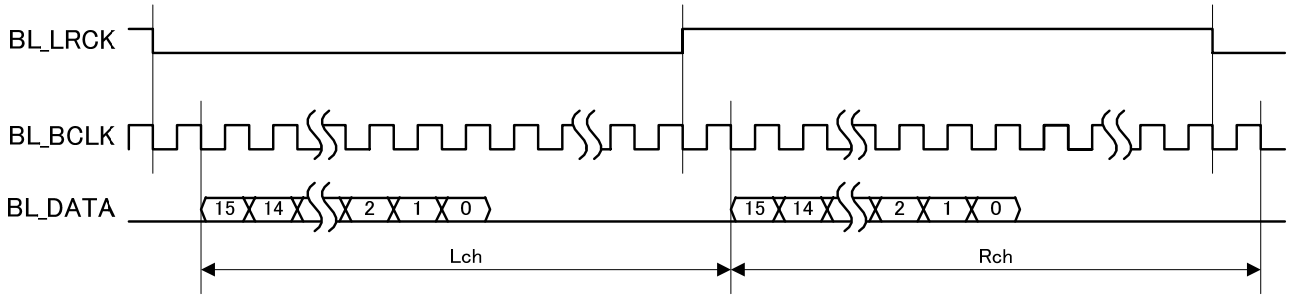


Parameter	Symbol	Min.	Typ.	Max.	Unit
AO_BCLK frequency	fBCLK		3.467		MHz
AO_LRCK Output Delay Time	tLD	-1		10	ns
AO_DATA Output Delay Time	tDD	0		50	ns

IBOC BLEND Input

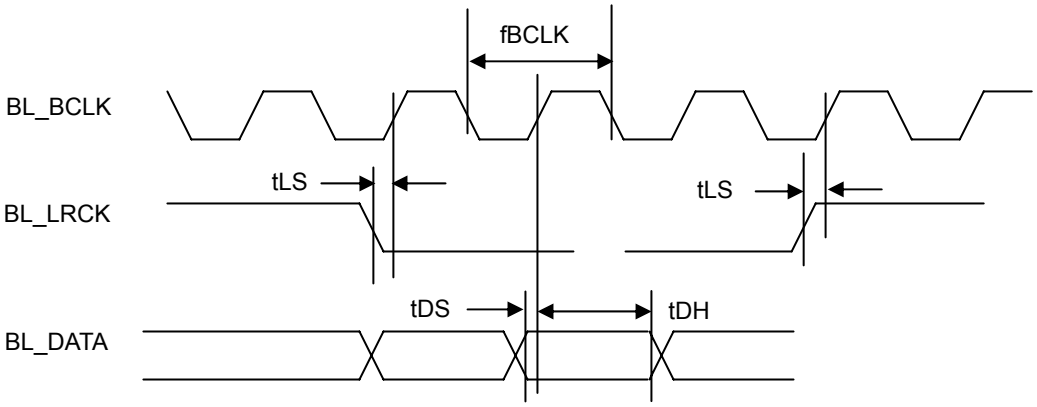
Audio Input (I^2S format) for IBOC BLEND is available.
fs : 44.1kHz
BCLK : 32fs to 64fs
Data Length : 16 bits

Timing Chart



15:MSB, 0:LSB

Timing Specifications



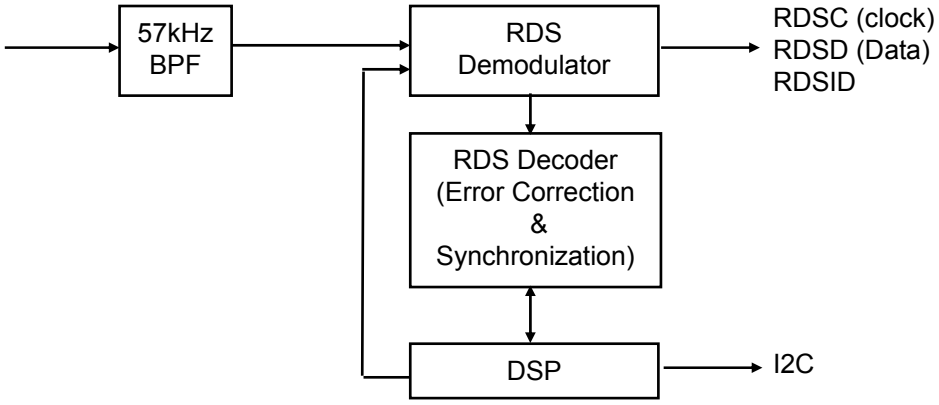
Parameter	Symbol	Min.	Typ.	Max.	Unit
BL_BCLK frequency	fBCLK	1411.2		2822.4	kHz
BL_LRCK Setup Time	tLS	10		100	ns
BL_DATA Setup Time	tDS	10			ns
BL_DATA Hold Time	tDH	100			ns

RDS Demodulation Function

The RDS (Radio Data System) for EBU (Europe Broadcasting Union) and the RBDS (Radio Broadcast Data System) for NSRC (National Radio System Committee (US)) demodulator system is available.
This system includes both the RDS demodulator, which outputs the RDS data directly to the RDSC, RDSD, RDSID pin and the RDS decoder, which contains the error corrector function and data transfer function to the main microcontroller.
The setting method is written in the software control manual.

(1) Block Diagram of RDS demodulation function

RDS demodulation function has following 4 blocks.
57kHZ BPF for RDS carrier signal,
RDS demodulator for by-phase demodulation,
RDS decoder for the error correction and data synchronization,
DSP for whole RDS system control
The block diagram is as follows.



a) 57kHz BPF block

This block contains the band-path filter to get the 57kHz signal, which is the 3rd harmonics of RDS sub-carrier signal (19kHz). The sufficient characteristics of the RDS demodulation is provided with the digital filter.

b) RDS Demodulator block

To demodulate the RDS signal, this block contains the comparator block, by-phase clock regeneration block, and the criterion circuit for data reliability.

The comparator block has the zero cross linear complement function and zero cross detection function.
This block lets the most suitable comparison position for the carrier signal from BPF block with doing the linear complementation.

The bi-phase clock regeneration block has digital PLL, DATA module, and ARI detector. The PLL regenerates the carrier signal and ARI detector detects the ARI signal. The data latch timing is defined depending on the state of the ARI and the RDS data is decoded in DATA module.

The DATA module generates the RDS clock (RDSC) , RDS output data (RDSD), and RDS output data judgement (RDSID) signals.

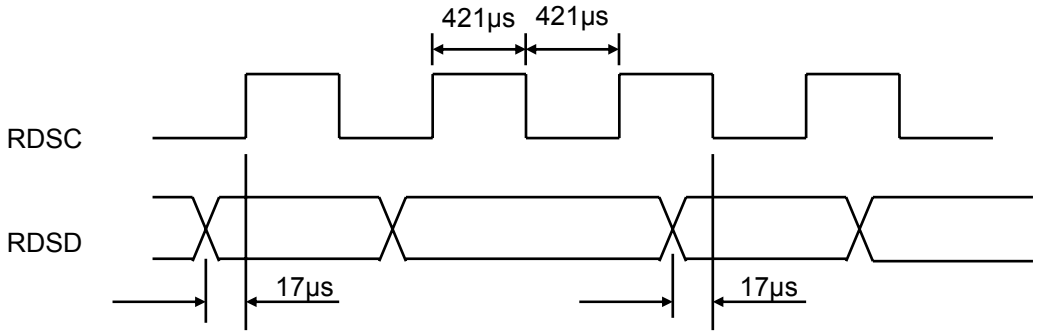
c) RDS Decoder Block (Error correction block)

RDS decoder block has the syndrome-register, the offset word detection function, the synchronism detection function, and the error detection function. The RDS data is processed the syndrome-register, and the offset word is detected with the offset detector by the output signal from the syndrome-register. The synchronization pull-in process is executed in synchronism detection function depending on the content of the off-set word. The selection of whether RDS or RDIS is controlled from DSP.
The intersymbol distance about the RDS data which may be wrong is measured and the soft-detection error correction is executed.

d) DSP

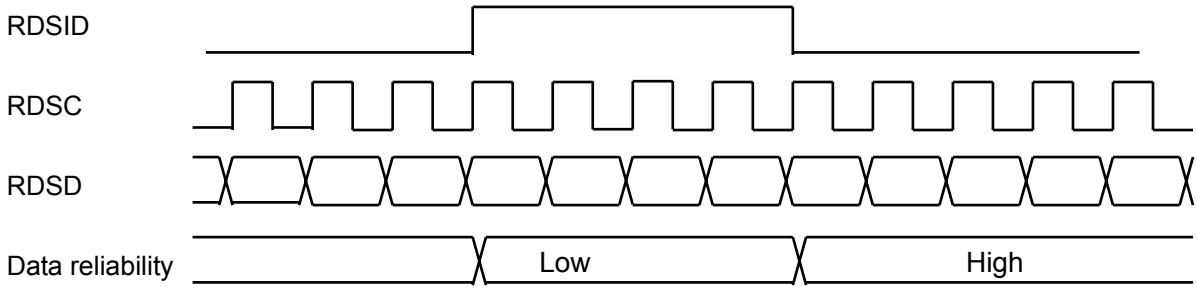
This DSP controls all of the RDS functions by the instructions from the main microcontroller.
The demodulation data and the error collection data is transferred to the main microcontroller via DSP.

(2) RDSC, RDSD output timing



(3) RDSID output timing

RDSID output indicates the reliability of the RDS data.
When the RDS data is reliable, the RDIS output level becomes “L”.

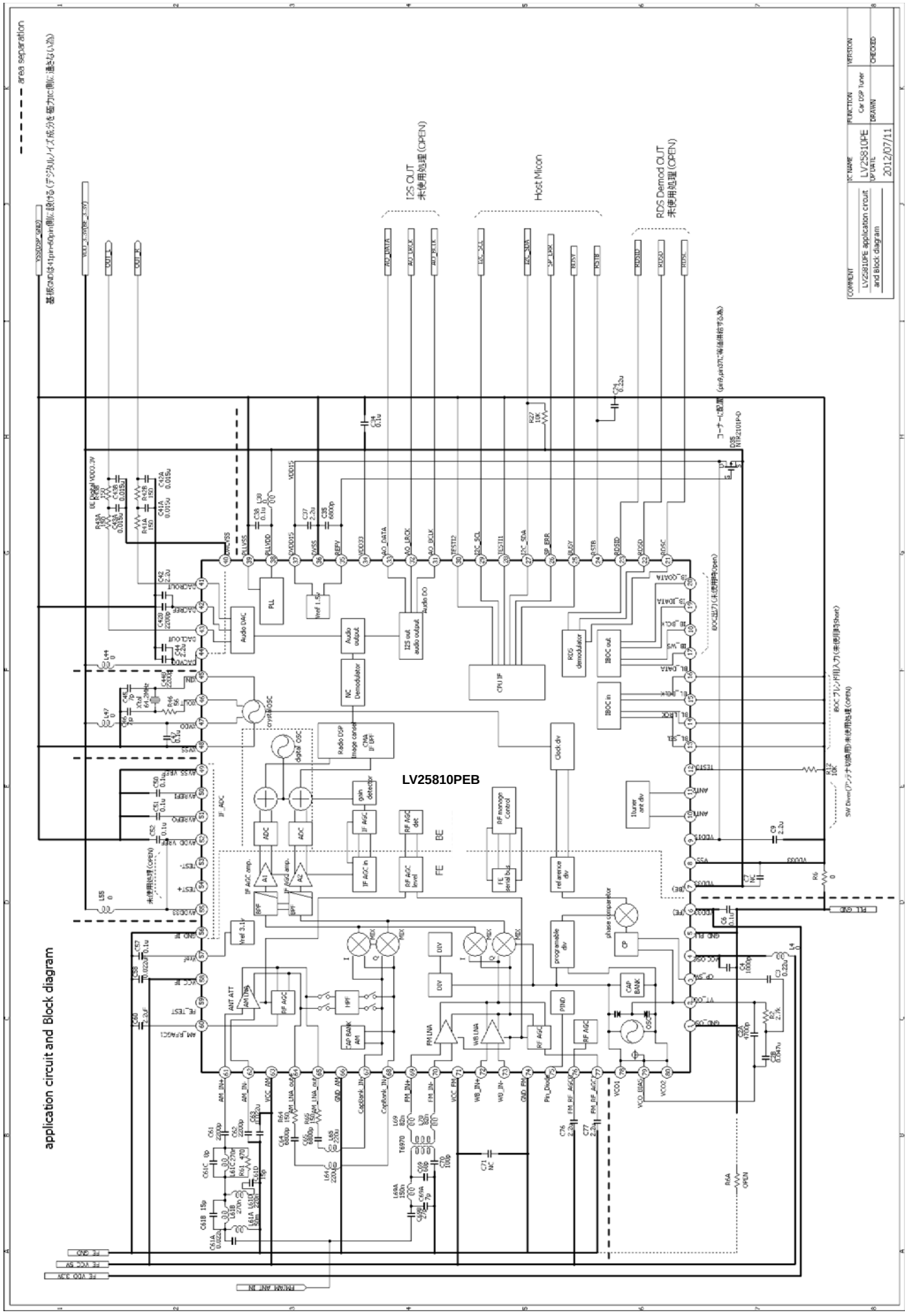


Controllable Items

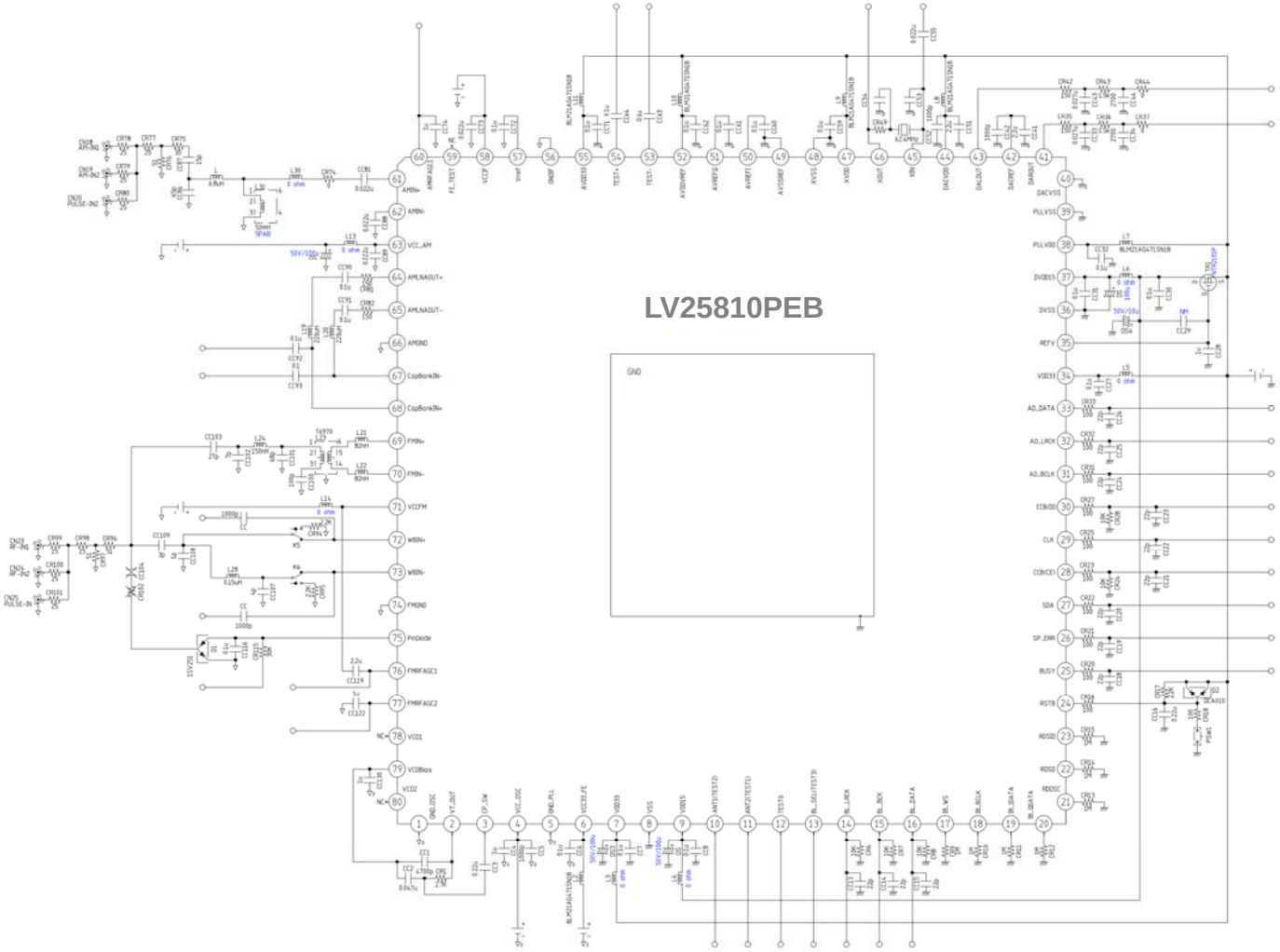
The following items are controllable. Details are shown in the software control manual.

- IF-BPF (Band Pass Filter)
- Local OSC
- AM RF Synchronization (Correct the difference of the AM CAP BANK)
- Image (Correct the amplitude error and phase error of the IQ signal)
- IF Offset (Correct the frequency mismatch of the IF signal)
- S-meter DC
- Separations

Application circuit



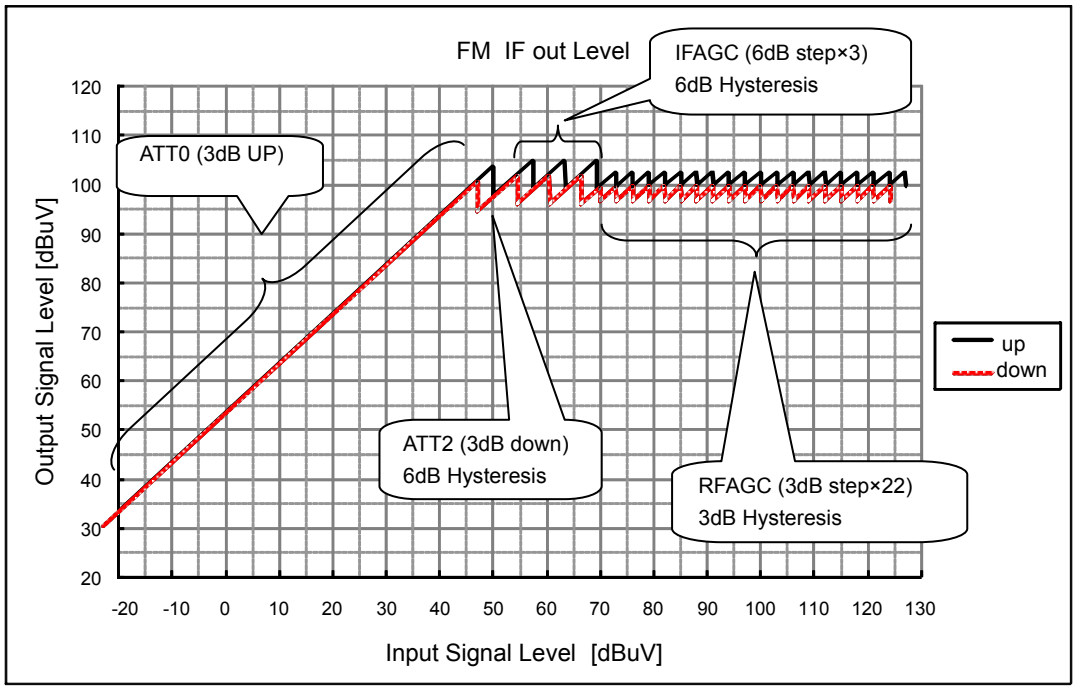
Measurement circuit



FM LNA+ RF AGC, WB LNA+ RF AGC (Including the IF-AFC)

When there is a FM (WB) RF signal at the ANT input, the output of MIX amplifier is about 25 dB. It attenuates by 3dB per steps by switching the LNA, a total of 22 steps in Attenuation. RF_AGC_1 operates when antenna input level is bout 75dBuV. RF_AGC_0 is the AGC for the LNA to improve the sensitivity and operates when antenna input level is about 60dBuV. A 65MHz~108MHz band pass filter in formed by the LC Antenna input.
(Details are shown in software control manual.)

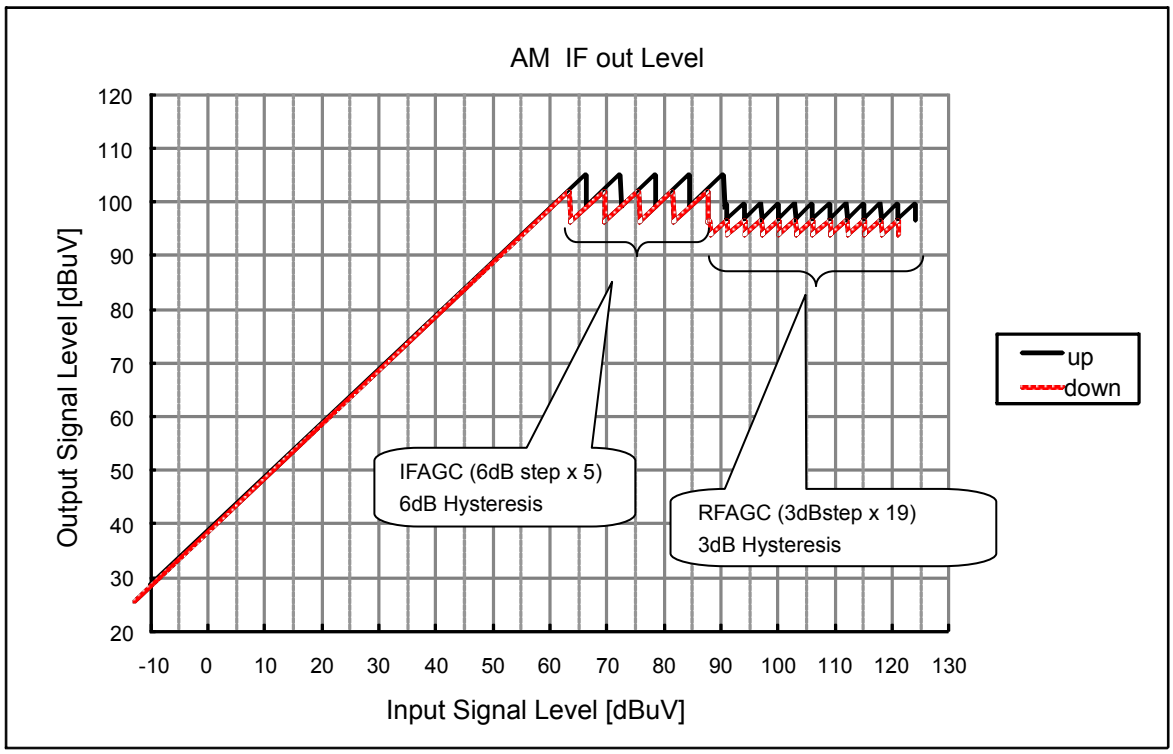
Signal processing Image



AM LNA+RF AGC (Including the IF-AGC)

The AM RF signal of the ANT input approximately 23 dB is feed into to the MIX.
LNA gain is controlled by 3dB per step, a total of 21 steps attenuation. RF AGC operates when antenna input is about 80dBuV.
In case of receiving the LW (144kHz – 281kHz), the RF signal output from LNA is input into the mixer via LPF. In case of receiving the MW (520kHz -1710kHz), the RF signal output from LNA is tuned by the capacitor bank and is input into the mixer.
In case of receiving the SW (2MHz – 30MHz), the RF signal output from LNA is input into the mixer via HPF.
The input LC antenna circuit makes 144 kHz – 30 MHz BPF.
(Details are shown in the software control manual.)

Signal Processing image



PLL

The LO_OSC frequency divider (P_CTR) output is compared with the reference frequency (R_CTR) so that they will have a zero phase difference. It makes output voltage of VT.

Local Oscillator

LO oscillator consists of the internal varactor and the internal inductor. The frequency of this oscillator is from 261.2MHz to 433.6MHz.

IF BPF・AGC AMP block

[Phase-Shift-Control, Level-Mismatch-Control]

Detect level differences and phase differences of I/Q.
Details are shown in software control manual.

[BPF, IF-AGC-Amp]

Gain and band-change function is included in the IF-BPF.
FM : +18dB (Full-Gain) to 0dB, 6dB steps
AM : +18dB (Full-Gain) to -12dB, 6dB steps
Details are shown in software control manual.

AM IQ MIX

The AM RF signal, from 144 kHz to 26.1 MHz, is converted into approximately 60 kHz IF signal which generates the I- and Q-signal. A +/– 45° phases down conversion output, which are added into the I-signal and Q-signal output, removes the square wave component (3^{rd}, 5^{th} order undesired elements) at the MIX output. The image component is removed in the IQ-mixer.

FM IQ MIX

The FM RF signal, from 65 MHz to 108 MHz, is converted into 300 kHz IF signal which generates the I- and Q-signal. A +/– 45° phases down conversion output, which are added into I-signal and Q-signal outputs, removes the square wave component (3^{rd}, 5^{th} order undesired elements) at the MIX output. The image component is removed in the IQ-mixer.

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LV25810PEB-6156H	QFP80(14X14) (Pb-Free / Halogen Free)	60 / Tray Foam

LifeElectronics
Живое партнерство

ООО «ЛайфЭлектроникс» **“LifeElectronics” LLC**

ИНН 7805602321 КПП 780501001 Р/С 40702810122510004610 ФАКБ "АБСОЛЮТ БАНК" (ЗАО) в г.Санкт-Петербурге К/С 30101810900000000703 БИК 044030703

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Мы предлагаем:

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- *Специальные условия для постоянных клиентов.*
- *Подбор аналогов.*
- *Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.*

- *Приемлемые сроки поставки, возможна ускоренная поставка.*
- *Доставку товара в любую точку России и стран СНГ.*
- *Комплексную поставку.*
- *Работу по проектам и поставку образцов.*
- *Формирование склада под заказчика.*

- *Сертификаты соответствия на поставляемую продукцию (по желанию клиента).*
- *Тестирование поставляемой продукции.*
- *Поставку компонентов, требующих военную и космическую приемку.*
- *Входной контроль качества.*
- *Наличие сертификата ISO.*

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- *Техническую поддержку проекта.*
- *Защиту от снятия компонента с производства.*
- *Оценку стоимости проекта по компонентам.*
- *Изготовление тестовой платы монтаж и пусконаладочные работы.*

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