MIC2124

Constant Frequency, Synchronous Current Mode Buck Controller

Hyper Speed Control™ Family

General Description

The Micrel MIC2124 is a member of the Hyper Speed Contro™l family of DC-DC controllers. It uses an adaptive on-time current mode control scheme and operates at a constant frequency.

The MIC2124 operates over a supply range of +3V to +18V, and is independent of the IC supply voltage V_{IN}. It operates at a fixed 300kHz switching frequency and can be used to provide up to 25A of output current. The output voltage is adjustable down to +0.8V.

The MIC2124 includes an EN/COMP pin that can be pulled low to shut down the converter. The MIC2124 optimizes performance and ensures stability with external compensation.

The UVLO is provided to ensure proper operation under power-sag conditions and to make sure that the external power MOSFET has enough voltage to work with. An internal digital soft-start ensures reduced inrush current. Cycle-by-cycle current limiting ensures FET protection.

The MIC2124 is available in a 10-pin MSOP package with a junction temperature operating range from –40ºC to +125ºC.

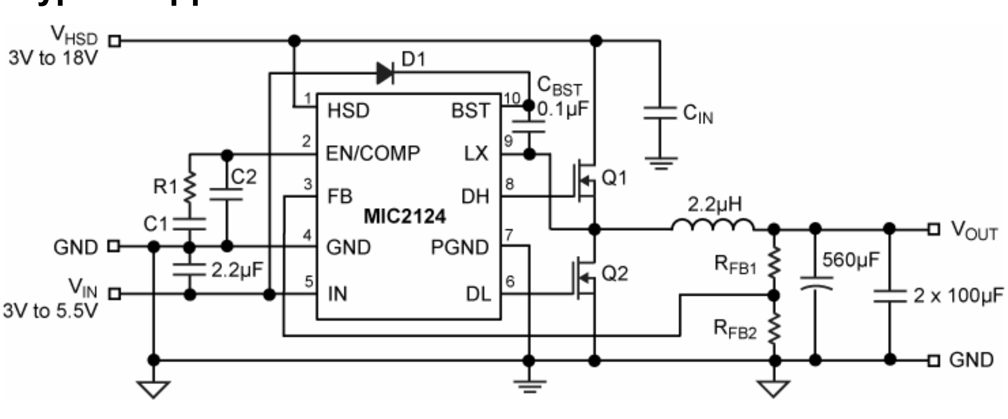
Features

- +3V to +18V input voltage
- 25A output current capability
- Any Capacitor™ stable
  - Zero ESR to high ESR
- Output down to 0.8V with ±1% FB accuracy
- Up to 94% efficiency
- 300kHz switching frequency
- All N-Channel MOSFET design
- Shutdown feature with EN/COMP
- No current-sense resistor needed
- Internal 4ms digital soft-start
- Thermal shutdown
- Pre-bias output safe
- Cycle-by-Cycle foldback current-limit protection
- 10-pin MSOP package
- –40ºC to +125ºC junction temperature range

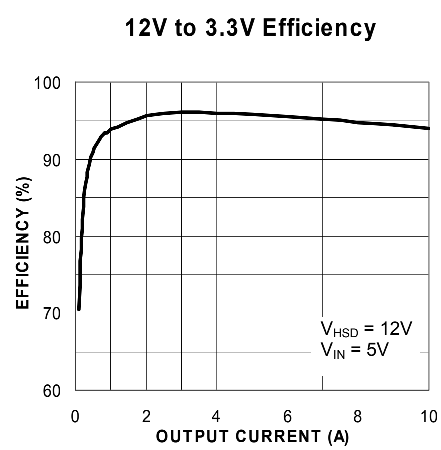
Applications

- Printers and scanners
- Graphic and video cards
- PCs and servers
- Microprocessor core supply
- Low-voltage distributed power
- Telecommunication and networking
- Set-top box, gateways and router

Typical Application



MIC2124 Adjustable Output 300kHz Buck Converter



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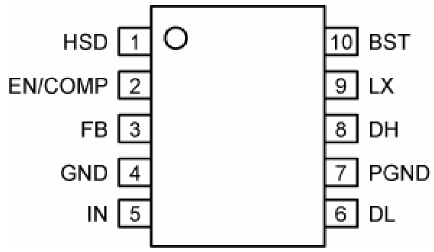
Ordering Information

Part Number	Voltage	Switching Frequency	Junction Temp. Range	Package	Lead Finish
MIC2124YMM	Adj.	300kHz	–40° to +125°C	10-Pin MSOP	Pb-Free

Pin Configuration



10-Pin MSOP (MM)

Pin Description

Pin Number	Pin Name	Pin Function
1	HSD	High-Side N-MOSFET Drain Connection (Input): Input voltage for the internal sensing of external power stage supply. The HSD operating voltage range is from 3V to 18V. Input capacitors between HSD and the power ground (PGND) are required.
2	EN/COMP	Enable (Input): Floating = enable, logic low = shutdown. In the off state, supply current of the device is greatly reduced (typically 1mA). COMP (Output): Output of the gm error amplifier and connects to the components for the external compensation.
3	FB	Feedback (Input): Input to the transconductance amplifier of the control loop. The FB pin is regulated to 0.8V. A resistor divider connecting the feedback to the output is used to adjust the desired output voltage.
4	GND	Signal ground. GND is the ground path for the device input voltage V_{IN} and the control circuitry. The loop for the signal ground should be separate from the power ground (PGND) loop.
5	IN	Input Voltage (Input): Power to the internal reference and control sections of the MIC2124. The IN operating voltage range is from 3V to 5.5V. A 2.2µF ceramic capacitors from IN to GND are recommended for clean operation. Connect IN to HSD when V_{HSD} < 5.5V.
6	DL	Low-Side Drive (Output): High-current driver output for external low-side MOSFET. The DL driving voltage swings from ground-to-IN.
7	PGND	Power Ground. PGND is the ground path for the MIC2124 buck converter power stage. The PGND pin connects to the sources of low-side N-Channel MOSFETs, the negative terminals of input capacitors, and the negative terminals of output capacitors. The loop for the power ground should be as small as possible and separate from the Signal ground (GND) loop.
8	DH	High-Side Drive (Output): High-current driver output for external high-side MOSFET. The DH driving voltage is floating on the switch node voltage (LX). It swings from V_{LX} to V_{BST}.
9	LX	Switch Node (Input): High-current output driver return. The LX pin connects directly to the switch node. Due to the high speed switching on this pin, the LX pin should be routed away from sensitive nodes. Current Sense input (Input): LX pin also senses the current for the current mode control and short circuit protection by monitoring the voltage across the low-side MOSFET during OFF time. In order to sense the current accurately, connect the low-side MOSFET drain to LX using a Kelvin connection.
10	BST	Boost (Output): Bootstrapped voltage to the high-side N-channel MOSFET driver. A Schottky diode is connected between the IN pin and the BST pin. A boost capacitor of 0.1µF is connected between the BST pin and the LX pin. Adding a small resistor at BST pin can slow down the turn-on time of high-side N-Channel MOSFETs.

Absolute Maximum Ratings[1]

IN, FB to GND ....-0.3V to +6V
BST to LX ....-0.3V to +6V
BST to GND ....-0.3V to +35V
DH to LX...-0.3V to (V_{BST} + 0.3V)
DL, COMP to GND ....-0.3V to (V_{IN} + 0.3V)
HSD to GND.. -0.3V to 29V
PGND to GND ....-0.3V to +0.3V
Power Dissipation T_A=70°C [3]..................Internally Limited
Storage Temperature (T_S)..........................-65°C to +150°C
Lead Temperature (soldering, 10sec)........................ 260°C

Operating Ratings[2]

Input Voltage (V_{IN})... 3.0V to 5.5V
Supply Voltage (V_{HSD}) .... 3.0V to 18V
Ambient Temperature (T_A)...........................-40°C to +85°C
Junction Temperature (T_J) ....-40°C to +125°C
Junction Thermal Resistance MSOP (θ_{JA}) ....130°C/W
Junction Thermal Resistance MSOP (θ_{JC}) ....43°C/W

Electrical Characteristics[5]

V_{HSD} = 13.2V, V_{IN} = 5V, V_{BST} - V_{LX} = 5V; T_A = 25°C, unless noted. **Bold** values indicate -40°C ≤ T_A ≤ +85°C.

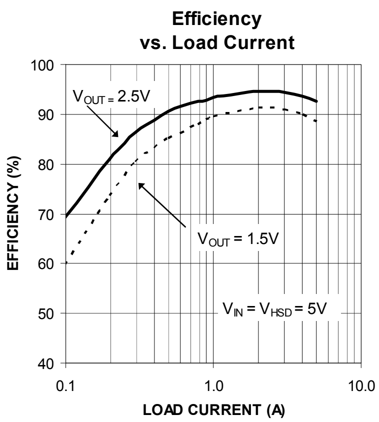
Parameter	Conditions	Min	Typ	Max	Units
General					
Operating Input Voltage (V_{IN}) [6]		**3.0**		**5.5**	V
HSD Voltage Range (V_{HSD})		**3.0**		**18**	V
Quiescent Supply Current	V_{FB} = 1.5V		1.4	**2**	mA
Shutdown Current	$V_{EN/COMP}$ = GND		1	**2**	mA
Under-Voltage Lockout					
Under-voltage Lockout Trip Level	Rising edge	**2.5**	2.7	**2.93**	V
UVLO Hysteresis			40		mV
DC-DC Controller					
Output-Voltage Adjust Range (V_{OUT})	Depends on external components and the maximum duty cycle.	**0.8**			V
Error Amplifier					
FB Regulation Voltage	0°C ≤ T_A ≤ 85°C	**-1**	±0.2	**1**	%
FB Regulation Voltage	-40°C ≤ T_A ≤ 85°C	**-2.5**	±0.2	**1**	%
Transconductance g_m		**70**	110	**160**	µS
COMP Output Voltage Swing		**0.5**		**2.3**	V
FB Input Leakage Current	V_{FB} = 0.8V		1	**500**	nA
On Timer					
Switching Frequency		**240**	300	**360**	kHz
Maximum Duty Cycle	V_{HSD} = 4V, V_{IN} = 5V, V_{LX} = 3.33V	**89**	91	**93**	%
Minimum Duty Cycle	FB > 0.8V		0		%
Short Current Protection					
Current Limit 1	V_{FB} = 0.8V	**110**	127	**145**	mV
Current Limit 2	V_{FB} = 0V	**21**	36	**51**	mV

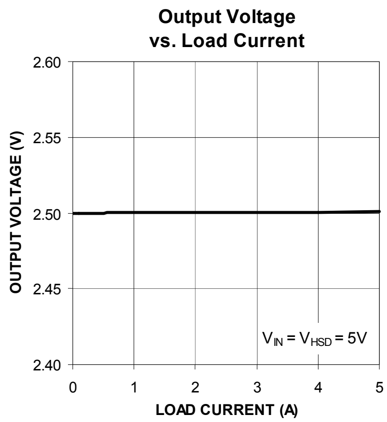
Parameter	Conditions	Min	Typ	Max	Units
FET Drivers					
DH, DL Output Low Voltage	I_{SINK} = 10mA			**0.1**	V
DH, DL Output High Voltage	I_{SOURCE} = 10mA, measured the difference between V_{BST}-V_{DH}, V_{IN}-V_{DL}	**0.1**			V
DH On-Resistance, High State			2	**3**	Ω
DH On-Resistance, Low State			1.5	**3**	Ω
DL On-Resistance, High State			2	**3**	Ω
DL On-Resistance, Low State			1	**2**	Ω
LX, BST, HSD Leakage Current	T_A = 25°C			30	µA
Thermal Protection					
Over-temperature Shutdown			160		°C
Over-temperature Shutdown Hysteresis			5		°C
Shutdown Control					
EN/COMP Logic Level High	3V < V_{IN} <5.5V	**0.5**	0.4		V
EN/COMP Logic Level Low	3V < V_{IN} <5.5V		0.4	**0.25**	V
EN/COMP Hysteresis	3V < V_{IN} <5.5V		26		mV
EN/COMP Pull-up Current	$V_{EN/COMP}$ = 0V		47	**100**	µA

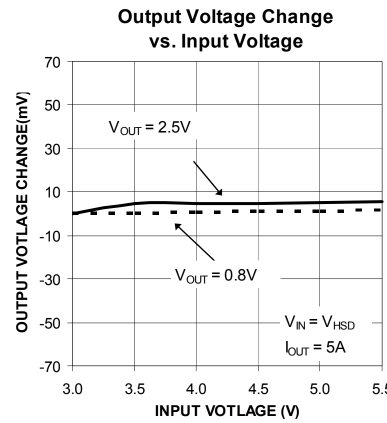
Notes:

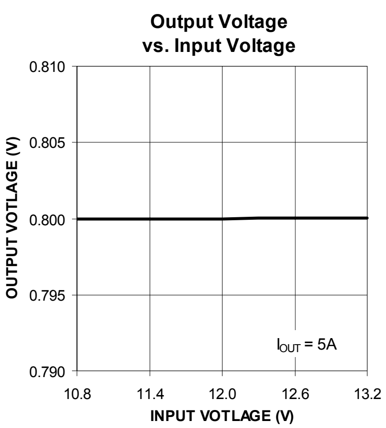
1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating.
3. The maximum allowable power dissipation of any T_A is $P_{D(max)} = (T_{J(max)} - T_A) / \theta_{JA}$. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the regulator will go into thermal shutdown.
4. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5k in series with 100pF.
5. Specification for packaged product only.
6. The application is fully functional at low IN (supply of the control section) if the external MOSFETs have enough low voltage V_{TH}.

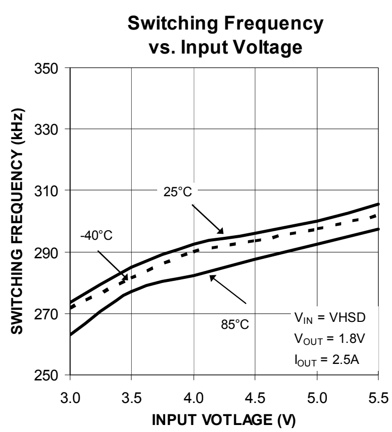
Typical Characteristics

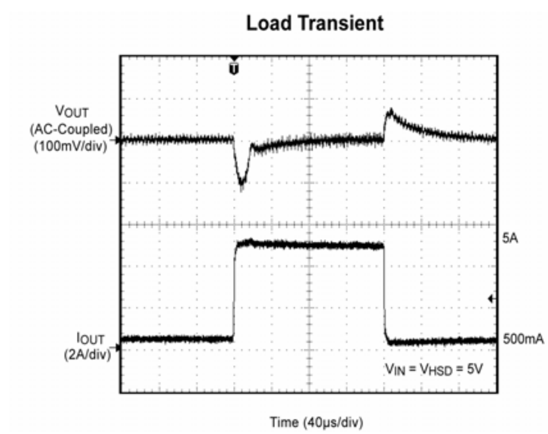






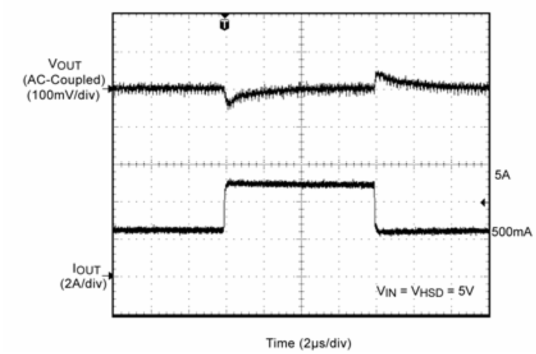




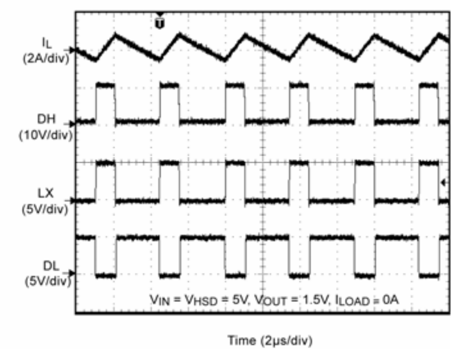


Functional Characteristics

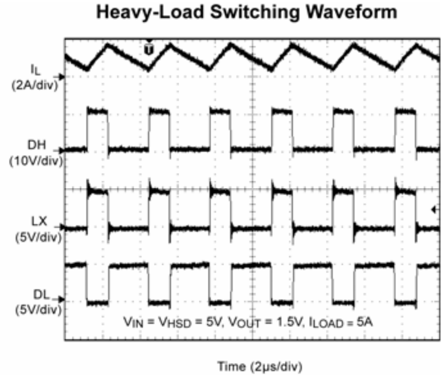
Load Transient



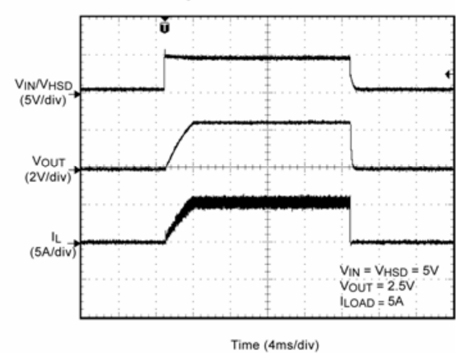
No-Load Switching Waveform



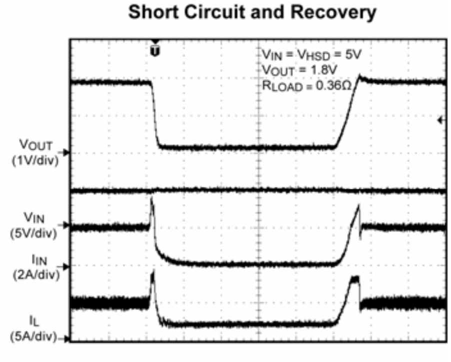
Heavy-Load Switching Waveform



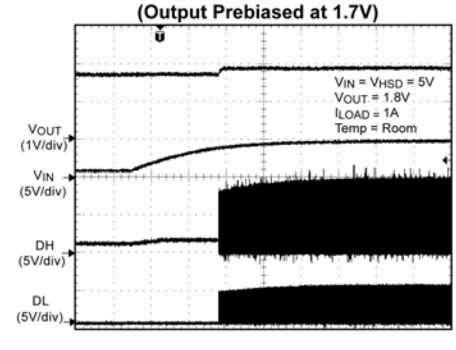
Power-Up/Power-Down Waveform



Short Circuit and Recovery

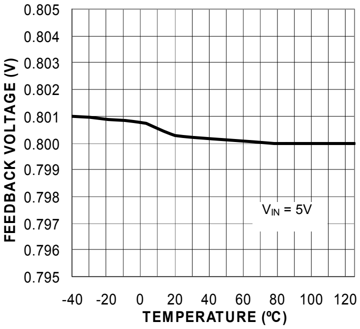


Startup into Prebiased Output
(Output Prebiased at 1.7V)

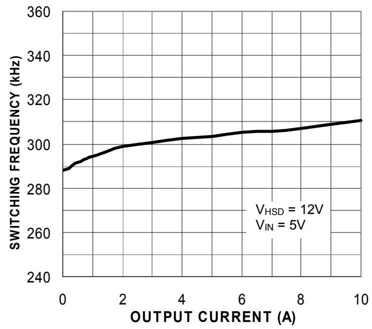


Typical Characteristics

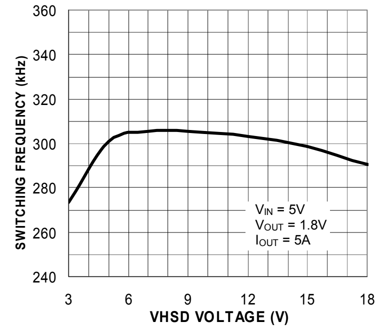
Feedback Voltage vs. Temperature



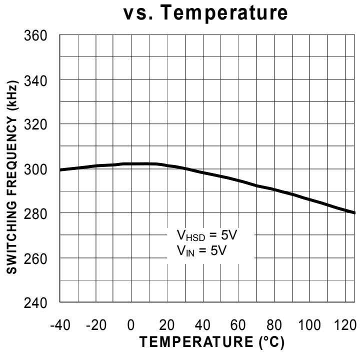
Switching Frequency vs. Load



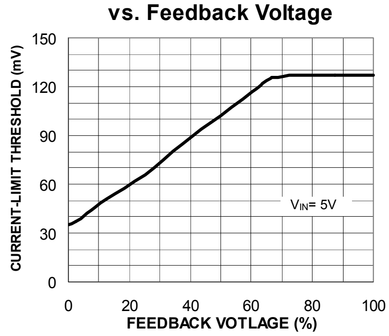
Switching Frequency vs. HSD Voltage



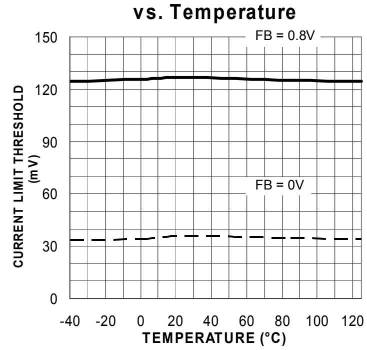
Switching Frequency vs. Temperature



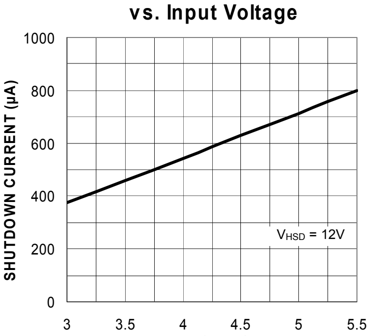
Current-Limit Threshold vs. Feedback Voltage



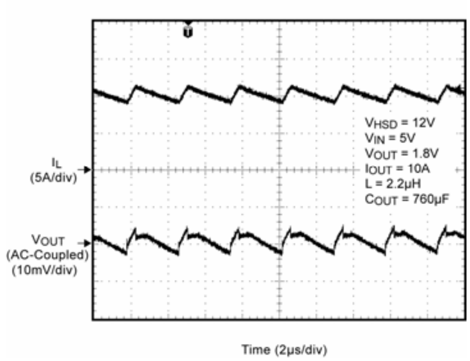
Current Limit Threshold vs. Temperature



Shutdown Current vs. Input Voltage



Output Voltage Ripple



Functional Diagram

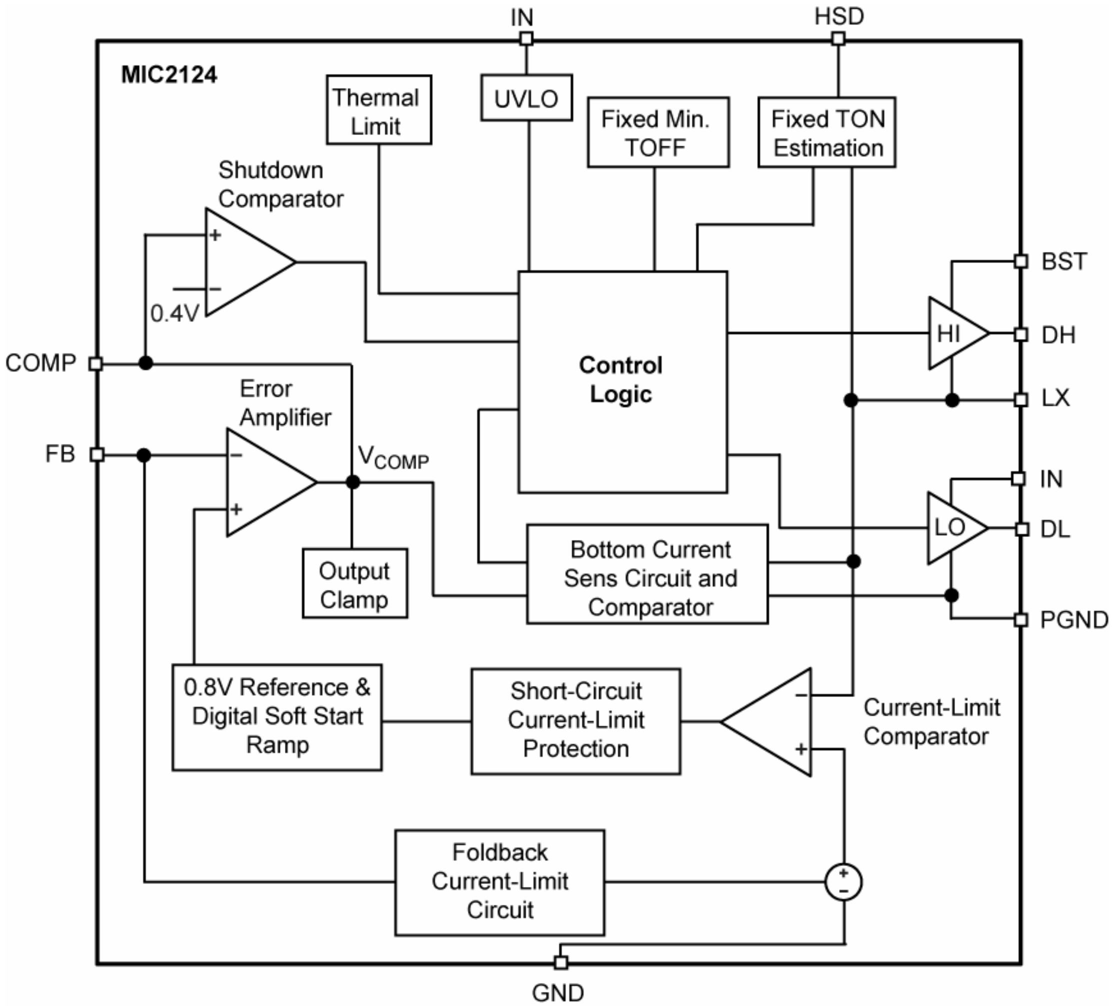


Figure 1. MIC2124 Block Diagram

Functional Description

The MIC2124 is an adaptive on-time current mode synchronous buck controller built for low cost and high performance. It is designed for wide input voltage range from 3V to 18V and for high output power buck converters. An estimated-ON-time method is applied in MIC2124 to obtain a constant switching frequency and to simplify the control compensation. The over-current protection is implemented without the use of an external sense resistor. It includes an internal soft-start function which reduces the power supply input surge current at start-up by controlling the output voltage rise time.

Theory of Operation

The MIC2124 is an adaptive on-time current mode buck controller. Figure 1 illustrates the block diagram for the control loop. The output voltage variation due to load or line changes will be sensed by the inverting input of the transconductance error amplifier via the feedback resistors (R_{FB1} and R_{FB2} in "Typical Application"), and compared to a reference voltage at the non-inverting input. This will cause a small change in the DC voltage level at the output of the error amplifier, or V_{COMP}. Meanwhile, the inductor current is sensed through the bottom MOSFET $R_{DS(ON)}$ and "Bottom Current Sense Circuit" as V_{IL}. If V_{IL} is lower than V_{COMP}, an ON-time period is triggered, in which DH pin is logic high and DL pin is logic low. The ON-time period length is predetermined by the "Fixed Ton Estimator" circuitry:

$$T_{ON(estimated)} = \frac{V_{OUT}}{V_{HSD} \cdot 300kHz} \qquad (1)$$

where V_{OUT} is the output voltage, V_{HSD} is the power stage input voltage.

After an ON-time period, the MIC2124 goes into the OFF-time period, in which DH pin is logic low and DL pin is logic high. The inductor current and V_{IL} decrease during OFF time. If V_{IL} is above V_{COMP}, the OFF status is maintained. When V_{IL} is below V_{COMP}, the ON-time period is triggered and the OFF-time period ends. If the OFF-time period determined by the inductor current and V_{COMP} is less than the minimum OFF time $T_{OFF(min)}$, which is 350ns typical, the MIC2124 control logic will apply the $T_{OFF(min)}$ instead. $T_{OFF(min)}$ is required to maintain enough energy in the Boost Capacitor (C_{BST}) to drive the high-side MOSFET. The maximum duty cycle is obtained from the 350ns $T_{OFF(min)}$:

$$D_{MAX} = \frac{T_S - T_{OFF(min)}}{T_S} = 1 - \frac{350ns}{T_S}$$

where T_S = 1/300kHz = 3.33μs. It is not recommended to use MIC2124 with a OFF-time close to $T_{OFF(min)}$ during steady state operation.

The estimated ON-time method results in a constant 300kHz switching frequency. The actual ON-time varies a little with the different rising and falling times of the external MOSFETs. Therefore, the type of the external MOSFETs, the output load current, and the control circuitry power supply V_{IN} will slightly modify the actual ON-time and the switching frequency. Also, the minimum T_{ON}, which is 140ns typical, results in a lower switching frequency in high V_{HSD} and low V_{OUT} applications, such as 18V to 0.8V. During the load transient, the switching frequency is changed due to the varying OFF-time.

To illustrate the control loop, the steady-state scenario and the load transient scenario are analyzed. V_{COMP} is defined as the output of the error amplifier. Figure 2 shows the MIC2124 control loop timing during the steady-state operation in continuous mode. V_{IL} represents the inductor current sensing voltage via the bottom MOSFET $R_{DS(ON)}$ and "Bottom Current Sense Circuit". When V_{IL} is below V_{COMP}, which means that the inductor current reaches the valley value, the OFF-time ends and ON-time is triggered. The ON-time is predetermined by the estimation.

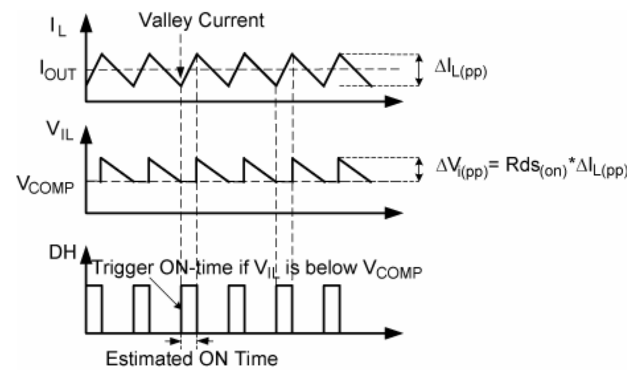


Figure 2. MIC2124 Control Loop Timing

Figure 3 shows the load transient operation of the MIC2124 converter. Assume the output voltage drops due to sudden load increase, which would cause the inverting input of the error amplifier, which is divided down version of V_{OUT}, to be slightly less than the reference voltage, causing the output voltage of the error amplifier V_{COMP} to go high. This will cause "CONTROL LOGIC" to trigger ON-time period. At the end of the ON-time period, a minimum OFF-time $T_{OFF(min)}$ is generated to charge BST since the inductor current V_{IL} is still below V_{COMP}. Then, the next ON-time period is triggered due to the high V_{COMP}. Therefore, the switching frequency changes during the load transient. Also the load regulation and transient load recovery is done by modulating the OFF-time. With the varying duty cycle and switching frequency, the output recovery time is fast and the output voltage deviation is small in MIC2124 converter.

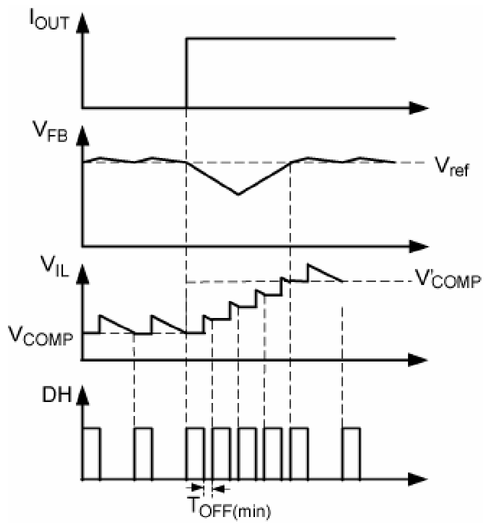


Figure 3. MIC2124 Load-Transient Response

Unlike in current-mode control, the MIC2124 uses adaptive ON-time current mode control. The MIC2124 predetermined ON-time control loop has the advantage of constant ON-time mode control and eliminates the need for the slope compensation.

Soft-Start

Soft-start reduces the power supply input surge current at startup by controlling the output voltage rise time. The input surge appears while the output capacitor is charged up. A slower output rise time will draw a lower input surge current.

The MIC2124 implements an internal digital soft-start by making the 0.8V reference voltage V_{REF} ramp from 0 to 100% in about 4ms. Therefore, the output voltage is controlled to increase slowly by a stair-case V_{REF} ramp. Once the soft-start cycle ends, the related circuitry is disabled to reduce current consumption. V_{IN} must be powered up no earlier than V_{HSD} to make the soft-start function behavior correctly.

Current Limit

The MIC2174/MIC2174C uses the RSD(ON) of the low-side power MOSFET to sense over-current conditions. This method will avoid adding cost, board space and power losses taken by a discrete current sense resistor. The low-side MOSFET is used because it displays much lower parasitic oscillations during switching than the high-side MOSFET.

In each switching cycle of the MIC2124 converter, the inductor current is sensed by monitoring the low-side MOSFET in the OFF period. The sensed voltage V_{LX} is compared with a current-limit threshold voltage V_{CL} after a blanking time of 150ns. If the sensed voltage V_{LX} is under V_{CL}, which is -127mV typical at 0.8V feedback voltage, the MIC2124 keeps the low-side MOSFET on until V_{LX} > -127mV, and then goes into the ON status with minimum ON-time. The current limit threshold V_{CL} has a fold back characteristic related to the FB voltage. Please refer to the "Typical Characteristics" for the curve of V_{CL} vs. FB voltage. The circuit in Figure 4 illustrates the MIC2124 current limiting circuit.

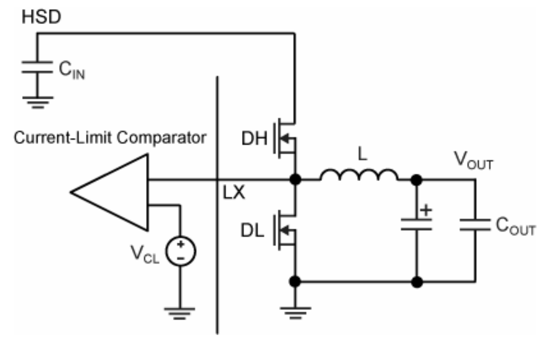


Figure 4. MIC2124 Current Limiting Circuit

Using the typical V_{CL} value of -127mV, the current limit value in the inductor is roughly estimated as:

$$I_{CL} \approx \frac{127\text{mV}}{R_{DS(ON)}}$$

For designs where the inductor current ripple is significant compared to the load current I_{OUT}, or for low duty cycle operation, calculating the load current limit $I_{CL(LOAD)}$ should take into account that one is sensing the peak inductor current.

$$I_{CL(LOAD)} = \frac{127\text{mV}}{R_{DS(ON)}} - \frac{\Delta I_{L(pp)}}{2} \tag{2}$$

$$\Delta I_{L(pp)} = \frac{V_{OUT} \times (1-D)}{f_{SW} \times L} \tag{3}$$

where:

V_{OUT} = The output voltage

$\Delta I_{L(pp)}$ = Inductor current ripple peak-to-peak value

D = Duty Cycle

f_{SW} = Switching frequency

The MOSFET $R_{DS(ON)}$ varies 30% to 40% with temperature; therefore, it is recommended to add 50% margin to $I_{CL(LOAD)}$ in the above equation to avoid false current limiting due to increased MOSFET junction temperature rise. It is also recommended to connect LX pin directly to the drain of the low-side MOSFET to accurately sense the MOSFETs $R_{DS(ON)}$

MOSFET Gate Drive

The MIC2124 high-side drive circuit is designed to switch an N-Channel MOSFET. The typical application circuit shows a bootstrap circuit, consisting of a Schottky diode D1 and 0.1µF boostrap capacitor C_{BST}, as shown in the typical application schematic on Page 1. This circuit supplies energy to the high-side drive circuit. Capacitor C_{BST} is charged while the low-side MOSFET is on and the voltage on the LX pin is approximately 0V. When the high-side MOSFET driver is turned on, energy from C_{BST} is used to turn the MOSFET on. As the high-side MOSFET turns on, the voltage on the LX pin increases to approximately V_{HSD}. Diode D1 is reversed biased and C_{BST} floats high while continuing to keep the high-side MOSFET on. The bias current of the high-side driver is less than 10mA so a 0.1µF to 1µF is sufficient to hold the gate voltage with minimal droop for the power stroke (high-side switching) cycle, i.e., ΔBST = 10mA x 3.33µs/0.1µF = 333mV. When the low-side MOSFET is turned back on, C_{BST} is recharged through D1. A small resistor R_G, which is in series with C_{BST}, can be used to slow down the turn-on time of the high-side N-Channel MOSFET.

The drive voltage is derived from the supply voltage V_{IN}. The nominal low-side gate drive voltage is V_{IN} and the nominal high-side gate drive voltage is approximately V_{IN} - V_{DIODE}, where V_{DIODE} is the voltage drop across D1. A dead-time of approximate 30ns between the high-side and low-side driver transitions is used to prevent current from simultaneously flowing unimpeded through both MOSFETs.

Application Information

MOSFET Selection

The MIC2124 controller works from input voltages of 3V to 18V and has an external 3V to 5.5V V_{IN} supply to provide power to turn the external N-Channel power MOSFETs for the high-side and low-side switches. For applications where V_{IN} < 5V, it is necessary that the power MOSFETs used are sub-logic level and are in full conduction mode for V_{GS} of 2.5V. For applications when V_{IN} > 5V; logic-level MOSFETs, whose operation is specified at V_{GS} = 4.5V must be used.

There are different criteria for choosing the high-side and low-side MOSFETs. These differences are more significant at lower duty cycles such as 12V to 1.8V conversion. In such an application, the high-side MOSFET is required to switch as quickly as possible to minimize transition losses, whereas the low-side MOSFET can switch slower, but must handle larger RMS currents. When the duty cycle approaches 50%, then the on-resistance of the high-side MOSFET starts to become critical.

It is important to note that the on-resistance of a MOSFET increases with increasing temperature. A 75°C rise in junction temperature will increase the channel resistance of the MOSFET by 50% to 75% of the resistance specified at 25°C. This change in resistance must be accounted for when calculating MOSFET power dissipation and in calculating the value of current limit.

Total gate charge is the charge required to turn the MOSFET on and off under specified operating conditions (V_{DS} and V_{GS}). The gate charge is supplied by the MIC2124 gate-drive circuit. At 300kHz switching frequency and above, the gate charge can be a significant source of power dissipation in the MIC2124. At low output load, this power dissipation is noticeable as a reduction in efficiency. The average current required to drive the high-side MOSFET is:

$$I_{G[high\text{-}side]}(avg) = Q_G \times f_{SW} \quad (4)$$

where:

$I_{G[high\text{-}side]}(avg)$ = Average high-side MOSFET gate current

Q_G = Total gate charge for the high-side MOSFET taken from the manufacturer's data sheet for $V_{GS} = V_{IN}$.

f_{SW} = Switching Frequency (300kHz)

The low-side MOSFET is turned on and off at V_{DS} = 0 because an internal body diode or external freewheeling diode is conducting during this time. The switching loss for the low-side MOSFET is usually negligible. Also, the gate-drive current for the low-side MOSFET is more accurately calculated using C_{ISS} at V_{DS} = 0 instead of gate charge.

For the low-side MOSFET:

$$I_{G[low\text{-}side]}(avg) = C_{ISS} \times V_{GS} \times f_{SW} \quad (5)$$

Since the current from the gate drive comes from the V_{IN}, the power dissipated in the MIC2124 due to gate drive is:

$$P_{GATEDRIVE} = V_{IN} \cdot (I_{G[high\text{-}side]}(avg) + I_{G[low\text{-}side]}(avg)) \quad (6)$$

A convenient figure of merit for switching MOSFETs is the on-resistance times the total gate charge $R_{DS(ON)} \times Q_G$. Lower numbers translate into higher efficiency. Low gate-charge logic-level MOSFETs are a good choice for use with the MIC2124. Also, the $R_{DS(ON)}$ of the low-side MOSFET will determine the current limit value. Please refer to "Current Limit" subsection in "Functional Description" for more details.

Parameters that are important to MOSFET switch selection are:

- Voltage rating
- On-resistance
- Total gate charge

The voltage ratings for the high-side and low-side MOSFETs are essentially equal to the power stage input voltage V_{HSD}. A safety factor of 20% should be added to the V_{DS}(max) of the MOSFETs to account for voltage spikes due to circuit parasitic elements.

The power dissipated in the MOSFETs is the sum of the conduction losses during the on-time ($P_{CONDUCTION}$) and the switching losses during the period of time when the MOSFETs turn on and off (P_{AC}).

$$P_{SW} = P_{CONDUCTION} + P_{AC} \quad (7)$$

$$P_{CONDUCTION} = I_{SW(RMS)}{}^2 \times R_{DS(ON)} \quad (8)$$

$$P_{AC} = P_{AC(off)} + P_{AC(on)} \quad (9)$$

where:

$R_{DS(ON)}$ = on-resistance of the MOSFET switch

D = Duty Cycle = V_{OUT} / V_{HSD}

Making the assumption that the turn-on and turn-off transition times are equal; the transition times can be approximated by:

$$t_T = \frac{C_{ISS} \times V_{IN} + C_{OSS} \times V_{HSD}}{I_G} \quad (10)$$

where:

C_{ISS} and C_{OSS} are measured at V_{DS} = 0

I_G = gate-drive current

The total high-side MOSFET switching loss is:

$$P_{AC} = (V_{HSD} + V_D) \times I_{PK} \times t_T \times f_{SW} \quad (11)$$

where:

t_T = Switching transition time

V_D = Body diode drop (0.5V)

f_{SW} = Switching Frequency (300kHz)

The low-side MOSFET switching losses are negligible and can be ignored for these calculations.

Inductor Selection

Values for inductance, peak, and RMS currents are required to select the output inductor. The input and output voltages and the inductance value determine the peak-to-peak inductor ripple current. Generally, higher inductance values are used with higher input voltages. Larger peak-to-peak ripple currents will increase the power dissipation in the inductor and MOSFETs. Larger output ripple currents will also require more output capacitance to smooth out the larger ripple current. Smaller peak-to-peak ripple currents require a larger inductance value and therefore a larger and more expensive inductor. A good compromise between size, loss and cost is to set the inductor ripple current to be equal to 20% of the maximum output current. The inductance value is calculated by the equation below.

$$L = \frac{V_{OUT} \cdot \left(V_{HSD(max)} - V_{OUT}\right)}{V_{HSD} \cdot f_{SW} \cdot 20\% \cdot I_{OUT(max)}} \quad (12)$$

where:

f_{SW} = switching frequency, 300 kHz

20% = ratio of AC ripple current to DC output current

$V_{HSD(max)}$ = maximum power stage input voltage

The peak-to-peak inductor current ripple is:

$$\Delta I_{L(PP)} = \frac{V_{OUT} \cdot (V_{HSD(max)} - V_{OUT})}{V_{HSD(max)} \cdot f_{SW} \cdot L} \quad (13)$$

The peak inductor current is equal to the average output current plus one half of the peak-to-peak inductor current ripple.

$$I_{L(pk)} = I_{OUT(max)} + 0.5 \times \Delta I_{L(PP)} \quad (14)$$

The RMS inductor current is used to calculate the I^2R losses in the inductor.

$$I_{L(RMS)} = \sqrt{{I_{OUT(max)}}^2 + \frac{{\Delta I_{L(PP)}}^2}{12}} \quad (15)$$

Maximizing efficiency requires the proper selection of core material and minimizing the winding resistance. The high frequency operation of the MIC2124 requires the use of ferrite materials for all but the most cost sensitive applications.

Lower cost iron powder cores may be used but the increase in core loss will reduce the efficiency of the power supply. This is especially noticeable at low output power. The winding resistance decreases efficiency at the higher output current levels. The winding resistance must be minimized although this usually comes at the expense of a larger inductor. The power dissipated in the inductor is equal to the sum of the core and copper losses. At higher output loads, the core losses are usually insignificant and can be ignored. At lower output currents, the core losses can be a significant contributor. Core loss information is usually available from the magnetics vendor. Copper loss in the inductor is calculated by the equation below:

$$P_{INDUCTOR_{Cu}} = {I_{L(RMS)}}^2 \cdot R_{WINDING} \quad (16)$$

The resistance of the copper wire, $R_{WINDING}$, increases with the temperature. The value of the winding resistance used should be at the operating temperature.

$$R_{WINDING(Ht)} = R_{WINDING(20°C)} \cdot \left(1 + 0.0042 \cdot (T_H - T_{20°C})\right) \quad (17)$$

where:

T_H = temperature of wire under full load

$T_{20°C}$ = ambient temperature

$R_{WINDING(20°C)}$ = room temperature winding resistance (usually specified by the manufacturer)

Output Capacitor Selection

The type of the output capacitor is usually determined by its ESR (equivalent series resistance). Voltage and RMS current capability are two other important factors for selecting the output capacitor. Recommended capacitors are tantalum, low-ESR aluminum electrolytic, OS-CON and POSCAPS. The output capacitor's ESR is usually the main cause of the output ripple. The output capacitor ESR also affects the control loop from a stability point of view. See "Feedback Loop Compensation" section for more information. The maximum value of ESR is calculated:

$$ESR_{C_{OUT}} \leq \frac{\Delta V_{OUT(PP)}}{\Delta I_{L(PP)}} \quad (18)$$

where:

$\Delta V_{OUT(PP)}$ = peak-to-peak output voltage ripple

$\Delta I_{L(PP)}$ = peak-to-peak inductor current ripple

The total output ripple is a combination of the ESR and output capacitance. The total ripple is calculated below:

$$\Delta V_{OUT(PP)} = \sqrt{\left(\frac{\Delta I_{L(PP)}}{C_{OUT} \cdot f_{SW} \cdot 8}\right)^2 + \left(\Delta I_{L(PP)} \cdot ESR_{C_{OUT}}\right)^2} \quad (19)$$

where:

D = duty cycle

C_{OUT} = output capacitance value

f_{SW} = switching frequency

The voltage rating of the capacitor should be twice the output voltage for a tantalum and 20% greater for aluminum electrolytic or OS-CON. The output capacitor RMS current is calculated below:

$$I_{C_{OUT}(RMS)} = \frac{\Delta I_{L(PP)}}{\sqrt{12}} \quad (20)$$

The power dissipated in the output capacitor is:

$$P_{DISS(C_{OUT})} = I_{C_{OUT}(RMS)}{}^2 \cdot ESR_{C_{OUT}} \quad (21)$$

Input Capacitor Selection

The input capacitor for the power stage input V_{HSD} should be selected for ripple current rating and voltage rating. Tantalum input capacitors may fail when subjected to high inrush currents, caused by turning the input supply on. A tantalum input capacitor's voltage rating should be at least two times the maximum input voltage to maximize reliability. Aluminum electrolytic, OS-CON, and multilayer polymer film capacitors can handle the higher inrush currents without voltage de-rating. The input voltage ripple will primarily depend on the input capacitor's ESR. The peak input current is equal to the peak inductor current, so:

$$\Delta V_{IN} = I_{L(pk)} \cdot ESR_{C_{IN}} \quad (22)$$

The input capacitor must be rated for the input current ripple. The RMS value of input capacitor current is determined at the maximum output current. Assuming the peak-to-peak inductor current ripple is low:

$$I_{C_{IN}(RMS)} \approx I_{OUT(MAX)} \cdot \sqrt{D \cdot (1-D)} \quad (23)$$

The power dissipated in the input capacitor is:

$$P_{DISS(C_{IN})} = I_{C_{IN}(RMS)}{}^2 \cdot ESR_{C_{IN}} \quad (24)$$

Voltage Setting Components

The MIC2124 requires two resistors to set the output voltage as shown in Figure 5.

The output voltage is determined by the equation:

$$V_{OUT} = V_{REF} \cdot (1 + \frac{R1}{R2}) \quad (25)$$

where V_{REF} = 0.8V. A typical value of R1 can be between 3kΩ and 10kΩ. If R1 is too large, it may allow noise to be introduced into the voltage feedback loop. If R1 is too small in value, it will decrease the efficiency of the power supply, especially at light loads. Once R1 is selected, R2 can be calculated using:

$$R2 = \frac{V_{REF} \cdot R1}{V_{OUT} - V_{REF}} \quad (26)$$

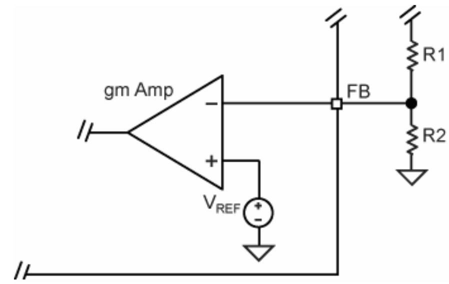


Figure 5. Voltage-Divider Configuration

External Schottky Diode (Optional)

An external freewheeling diode, which is not necessary, is used to keep the inductor current flow continuous while both MOSFETs are turned off. This dead-time prevents current from flowing unimpeded through both MOSFETs and is typically 30ns. The diode conducts twice during each switching cycle. Although the average current through this diode is small, the diode must be able to handle the peak current.

$$I_{D(avg)} = I_{OUT} \cdot 2 \cdot 30ns \cdot f_{SW} \quad (27)$$

The reverse voltage requirement of the diode is:

$$V_{DIODE(rrm)} = V_{HSD}$$

The power dissipated by the Schottky diode is:

$$P_{DIODE} = I_{D(avg)} \times V_F \quad (28)$$

where V_F = forward voltage at the peak diode current.

The external Schottky diode is not necessary for the circuit operation since the low-side MOSFET contains a parasitic body diode. The external diode will improve efficiency and decrease the high frequency noise. If the MOSFET body diode is used, it must be rated to handle the peak and average current. The body diode has a relatively slow reverse recovery time and a relatively high forward voltage drop. The power lost in the diode is proportional to the forward voltage drop of the diode. As the high-side MOSFET starts to turn on, the body diode becomes a short circuit for the reverse recovery period, dissipating additional power. The diode recovery and the circuit inductance will cause ringing during the high-side MOSFET turn-on.

An external Schottky diode conducts at a lower forward voltage preventing the body diode in the MOSFET from turning on. The lower forward voltage drop dissipates less power than the body diode. The lack of a reverse recovery mechanism in a Schottky diode causes less ringing and less power loss. Depending on the circuit components and operating conditions, an external Schottky diode will give a 0.5% to 1% improvement in efficiency.

Feedback Loop Compensation

The MIC2124 controller comes with an internal error amplifier used for optimizing control loop stability by placing a capacitor C1 in series with a resistor R1 and another capacitor C2 in parallel from the COMP pin to ground.

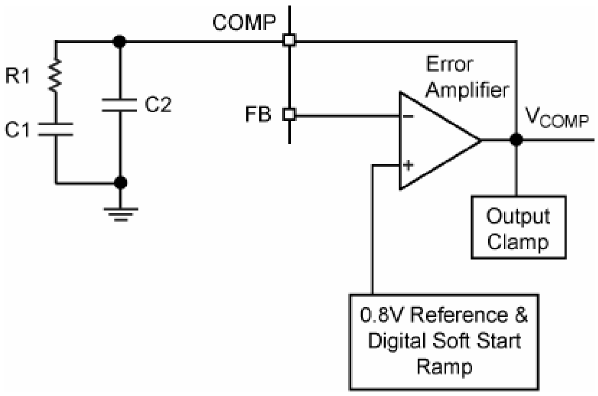


Figure 6. Loop Compensation

a. Power Stage

The adaptive on-time current mode control applied in MIC2124 controller eliminates the double-pole in the power stage, which is caused by the output inductor and output capacitor. At the frequency range which is far below the switching frequency ($f < f_{SW}/6$), the transfer function from the output of the error amplifier to the buck converter output can be approximated by the following equation:

$$G(s)_{con} \approx G_C \times \frac{1 + s \times C_{OUT} \times ESR_{C_{OUT}}}{1 + \frac{s}{\varpi_p}} \qquad (29)$$

where:

$$G_C = \frac{R_{LOAD}}{Ri} \times \frac{1}{1 + \frac{R_{LOAD}}{f_{SW} \times L} \times \frac{D}{2}}$$

$$\varpi_p = \frac{1}{C_{OUT} \times R_{LOAD}} + \frac{1}{f_{SW} \times L \times C_{OUT}} \times \frac{D}{2}$$

C_{OUT} = total output capacitors

ESR_{COUT} = electrical series resistance of the output capacitor

R_{LOAD} = load resistance

Ri = 2.4 x Rds(on)_bottom (low-side MOSFET Rds(on))

f_{SW} = switching frequency

L = inductance of the output inductor

D = duty cycle

According to equation (29), there is a pole and zero pair set by the load resistance R_{LOAD}, the output capacitor, and the output inductor in the power stage:

$$f_{z(con)} = \frac{1}{2\pi \times C_{OUT} \times ESR_{C_{OUT}}} \qquad (30)$$

$$f_{p(con)} = \frac{1}{2\pi} \times \left(\frac{1}{C_{OUT} \times R_{LOAD}} + \frac{1}{f_{SW} \times L \times C_{OUT}} \times \frac{D}{2}\right) \qquad (31)$$

Therefore, type II compensation, which is comprised by C1, R1 and C2, is able to achieve a stabilized loop for MIC2124 in most applications.

b. g_m Error Amplifier

It is undesirable to have high error amplifier gain at high frequencies because high frequency noise spikes would be picked up and transmitted at large amplitude to the output; thus, gain should be permitted to fall off at high frequencies. At low frequency, it is desired to have high open-loop gain to attenuate the power line ripple. Thus, the error amplifier gain should be allowed to increase rapidly at low frequencies.

The transfer function with R1, C1, and C2 for the internal g_m error amplifier can be expressed as:

$$G(s)_{err} = g_m \times \left[\frac{1 + s \times R1 \times C1}{s \times (C1 + C2) \times \left(1 + s \times R1 \times \frac{C1 \times C2}{C1 + C2}\right)}\right] \qquad (32)$$

One pole and one zero can be seen from the above transfer function at the following frequencies:

$$f_{z(err)} = \frac{1}{2\pi \times R1 \times C1} \qquad (33)$$

$$f_{p(err)} = \frac{1}{2\pi \times R1 \times \frac{C1 \times C2}{C1 + C2}} \qquad (34)$$

c. Total Open-Loop Response

The open-loop response for the MIC2124 controller is easily obtained by combining the power stage, the feedback resistor divider, and the error amplifier gains together.

$$G(s)_{total} = \frac{R_{FB2}}{R_{FB1} + R_{FB2}} \times G(s)_{con} \times G(s)_{err} \qquad (35)$$

where R_{FB1} and R_{FB2} are the voltage divider resistors, as shown in the typical application schematic on Page 1.

It is desirable to have the gain curve intersect zero dB at tens of kilohertz, this is commonly called crossover frequency; the phase margin at crossover frequency should be at least 45°.

12V to 1.8V @ 10A application is applied as an example to demonstrate the loop compensation for MIC2124. In this application:

D = 0.15

R_{LOAD} = 0.18Ω.

The output capacitor and the inductor parameters are:

C_{OUT} = 760μF

ESR_{COUT} = 0.002Ω

L = 2.2μH.

Also,

Ri = 0.007Ωx2.4

f_{SW} = 300kHz

Rfb1 = 10kΩ

Rfb2 = 8.06kΩ

The error amplifier gm and external compensation component are:

g_m = 110μS

R1 = 150kΩ

C1 = 220pF

C2 = 47pF

The gain and phase of the control-to-output transfer function predicted by the equation (29) are shown in Figure 7. The gain and phase of the error amplifier transfer function predicted by the equation (32) are shown in Figure 8. The total open-loop bode plot predicted by the equation (35) is shown in Figure 9.

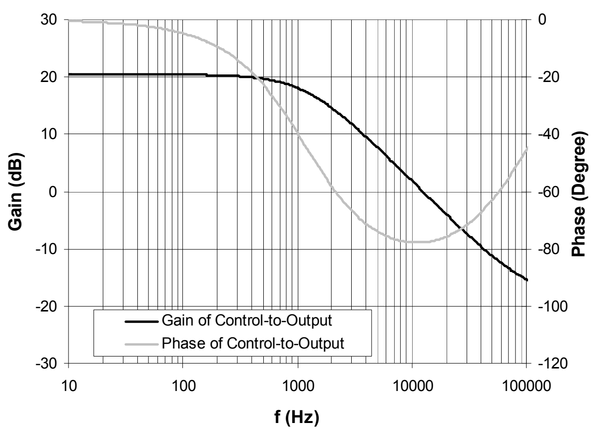


Figure 7. Control-to-Output Bode Plot

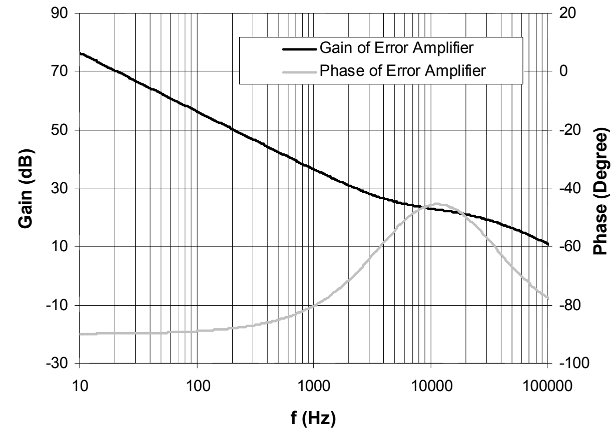


Figure 8. Error Amplifier Bode Plot

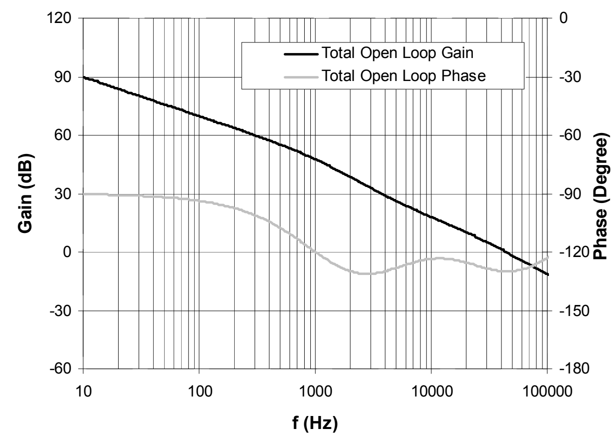


Figure 9. Total Open Loop Bode Plot

The crossover frequency of this MIC2124 buck converter is 40kHz and the phase margin is about 50°, as shown in Figure 9.

PCB Layout Guideline

Warning!!! To minimize EMI and output noise, follow these layout recommendations.

PCB Layout is critical to achieve reliable, stable and efficient performance. A ground plane is required to control EMI and minimize the inductance in power, signal and return paths.

The following guidelines should be followed to insure proper operation of the MIC2124 converter.

IC

- The 2.2µF ceramic capacitor, which connects to the V_{IN} terminal, must be located right at the IC. The V_{IN} terminal is very noise sensitive and placement of the capacitor is very critical. Use wide traces to connect to the IN and PGND pins.
- Place the IC and MOSFETs close to the point of load (POL).
- Use fat traces to route the input and output power lines.
- Signal and power grounds should be kept separate and connected at only one location.

Input Capacitor

- Place the HSD input capacitor next.
- Place the HSD input capacitors on the same side of the board and as close to the MOSFETs and the IC as possible.
- Keep both the HSD and PGND connections short.
- Place several vias to the ground plane close to the HSD input capacitor ground terminal.
- Use either X7R or X5R dielectric input capacitors. Do not use Y5V or Z5U type capacitors.
- Do not replace the ceramic input capacitor with any other type of capacitor. Any type of capacitor can be placed in parallel with the input capacitor.
- If a Tantalum input capacitor is placed in parallel with the input capacitor, it must be recommended for switching regulator applications and the operating voltage must be de-rated by 50%.
- In “Hot-Plug” applications, a Tantalum or Electrolytic bypass capacitor must be used to limit the over-voltage spike seen on the input supply with power is suddenly applied.
- An additional Tantalum or Electrolytic bypass input capacitor of 22uF or higher is required at the input power connection.
- The 2.2µF, which connect to the V_{IN} terminal, must be located right at the IC. The V_{IN} terminal is very noise sensitive and placement of the capacitor is very critical. Connections must be made with wide trace.

Inductor

- Keep the inductor connection to the switch node (LX) short.
- Do not route any digital lines underneath or close to the inductor.
- Keep the switch node (LX) away from the feedback (FB) pin.
- The LX pin should be connected directly to the drain of the low-side MOSFET to accurate sense the voltage across the low-side MOSFET.
- To minimize noise, place a ground plane underneath the inductor.

Output Capacitor

- Use a wide trace to connect the output capacitor ground terminal to the input capacitor ground terminal.
- Phase margin will change as the output capacitor value and ESR changes. Contact the factory if the output capacitor is different from what is shown in the BOM.
- The feedback trace should be separate from the power trace and connected as close as possible to the output capacitor. Sensing a long high current load trace can degrade the DC load regulation.

Schottky Diode (Optional)

- Place the Schottky diode on the same side of the board as the MOSFETs and HSD input capacitor.
- The connection from the Schottky diode’s Anode to the input capacitors ground terminal must be as short as possible.
- The diode’s Cathode connection to the switch node (LX) must be kept as short as possible.

RC Snubber

- Place the RC snubber on the same side of the board and as close to the MOSFETs as possible.

MOSFETS

- Low-side MOSFET gate drive trace (DL pin to MOSFET gate pin) must be short and routed over a ground plane. The ground plane should be the connection between the MOSFET source and PGND.
- Chose a low-side MOSFET with a high C_{GS}/C_{GD} ratio and a low internal gate resistance to minimize the effect of dv/dt inducted turn-on.
- Do not put a resistor between the LSD output and the gate.
- Use a 4.5V V_{GS} rated MOSFET. Its higher gate threshold voltage is more immune to glitches than a 2.5V or 3.3V rated MOSFET. MOSFETs that are rated for operation at less than 4.5V V_{GS} should not be used.

Others

- In order to accurately sense the voltage across the low-side MOSFET, the LX pin and PGND pin should be Kelvin connected to the drain and source of the low-side MOSFET.
- The feedback resistors R_{FB1} and R_{FB2} (refer to the typical application schematic on page 1) should be placed close to the FB pin. The top side of R_{FB1} should connect directly to the output node. Run this trace away from the switch node (junction of Q1, Q2, and the output inductor).
- The compensation resistor and capacitors should be placed right next to the COMP pin and the other side should connect directly to the GND pin on the MIC2124 rather than going to the plane.
- HSD pin is sensitive to the noise. Too much noise at HSD pin may cause the jittering at LX. A 10Ω resistor and 0.1µF capacitor low-pass filter at the HSD is able to mitigate the noise.

Evaluation Board Schematic

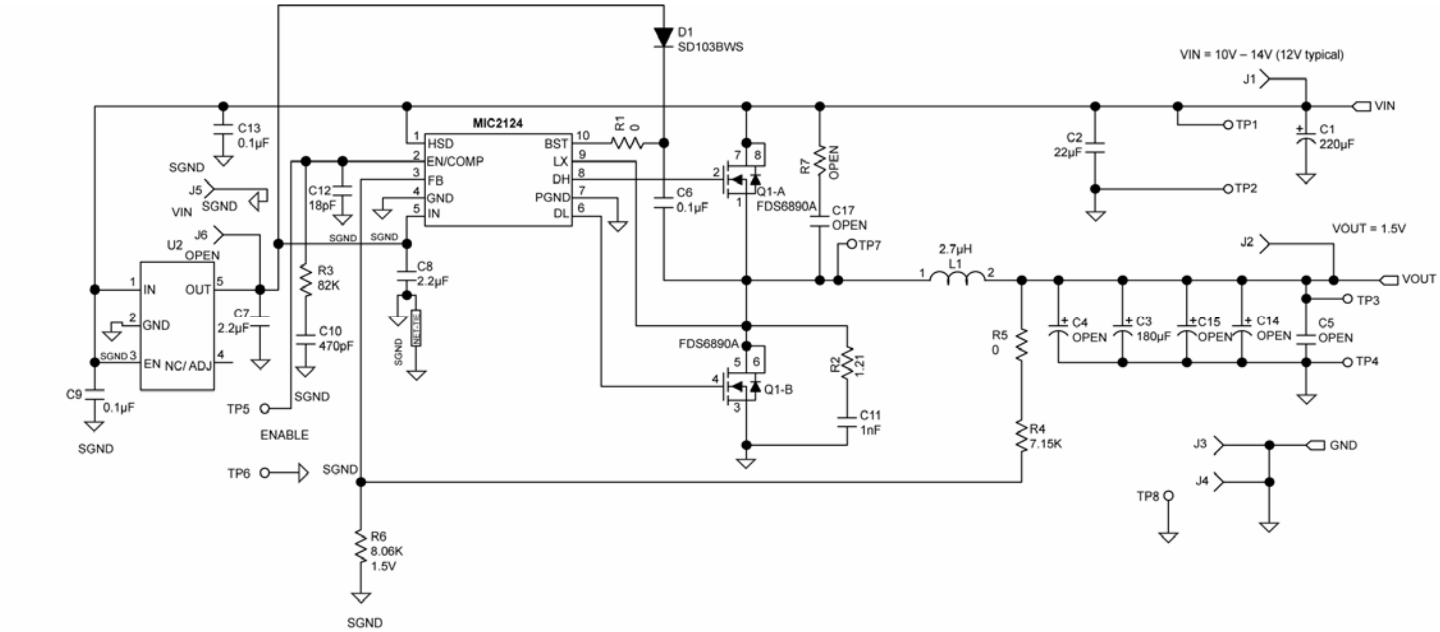


Figure 10. Schematic of MIC2124 5A Evaluation Board

Bill of Materials

Item	Part Name	Manufacturer	Description	Qty
C1	B41125A7227M	EPCOS[1]	220µF Aluminum Capacitor, SMD 35V	1
C2	1210YD226MAT2A	AVX[2]	22µF Ceramic Capacitor, X5R, Size 1210, 16V	1
	GRM32ER61C226ME20L	Murata[3]		
	C3225XR1C226M	TDK[4]		
C3	EEFSX0D181R	Panasonic[5]	180µF SP Capacitor, 9mΩ, 2V	1
C6, C9, C13	06035C10KAT2A	AVX	0.1µF Ceramic Capactior, X7R, Size 0603, 50V	3
	GRM21BR71A225KA01L	Murata		
	C1608X7R1H104K	TDK		
C7, C8	0805ZC225MAT2A	AVX	2.2µF Ceramic Capacitor, X7R, Size 0805, 10V	2
	GRM21BR71A225KA01L	Murata		
	C2012X7R1A225K	TDK		
C10	06035C471KAT2A	AVX	470pF Ceramic Capacitor, X7R, Size 0603, 50V	1
	GRM188R71H471KA01D	Murata		
	C1608X7R1H471K	TDK		
C11	06035C102KAT2A	AVX	1nF Ceramic Capacitor, X7R, Size 0603, 50V	1
	GRM188R71H102KA01D	Murata		
	C1608X7R1H102K	TDK		
C12	06035A180JAT2A	AVX	18pF Ceramic Capacitor, Size 0603, 50V	1
	GRM1885C1H180JA01D	Murata		
	C1608C0G1H180J	TDK		
D1	SD103BWS	MCC	30V small signal Schottky diode	1
	SD103BWS-7	DIODE INC[6]		
L1	DO316P-272HC	Coilcraft	2.7µH inductor, 6.6A saturation current	1
Q1	FDS6890A	Fairchild[7]	20V, 7.5A Dual N-MOSFET, 0.018Ω Rds (on) @ 4.5V	1
R1, R5	CRCW06030000Z0EA	Vishay/Dale[8]	0Ω resistor, size 0603, 1%	2
R2	CRCW08051R21FKEA	Vishay/Dale	1.21Ω resistor, size 0805, 1%	1
R3	CRCW060382K0FKEA	Vishay/Dale	82kΩ resistor, size 0603, 1%	1
R4	CRCW06037K15FKEA	Vishay/Dale	7.15kΩ resistor, size 0603, 1%	1
R6	CRCW06038K06FKEA	Vishay/Dale	8.06kΩ resistor, size 0603, 1%	1
R7			Open	
U1	**MIC2124YMM**	**Micrel, Inc[9]**	300kHz Buck Controller	1
U2[10]	**MIC5233-5.0YM5**	**Micrel, Inc**	LDO	1

Notes:

1. EPCOS: www.epcos.com
2. AVX: www.avx.com
3. Murata: www.murata.com
4. TDK: www.tdk.com
5. Panasonic: www.panasonic.com
6. Diodes Inc.: www.diodes.com
7. Fairchild: www.fairchildsemi.com
8. Vishay: www.vishay.com
9. **Micrel, Inc.: www.micrel.com**
10. Optional: Required if 5V supply is not available in the system.

PCB Layout

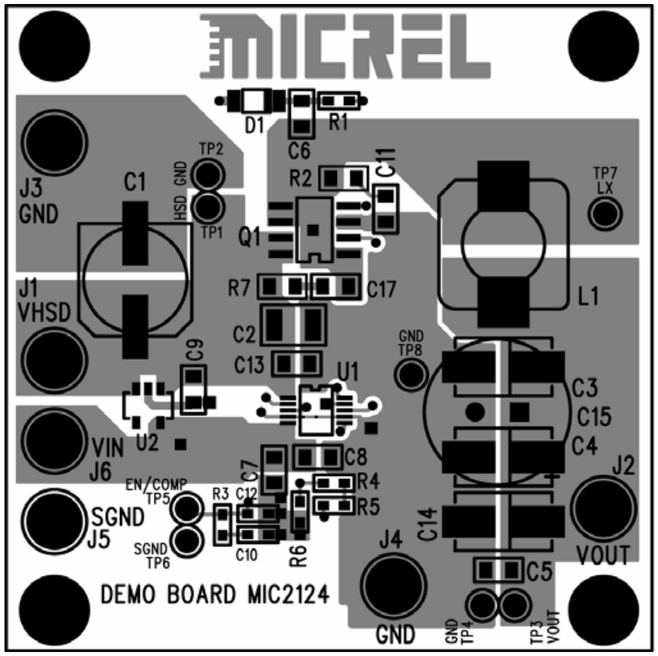


Figure 11. MIC2124 Evaluation Board Top layer

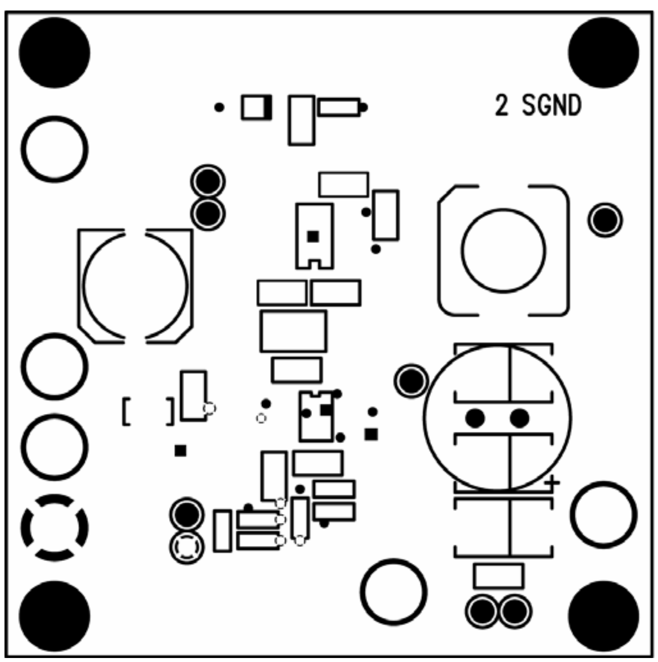


Figure 12. MIC2124 Evaluation Board Mid-Layer 1(Ground Plane)

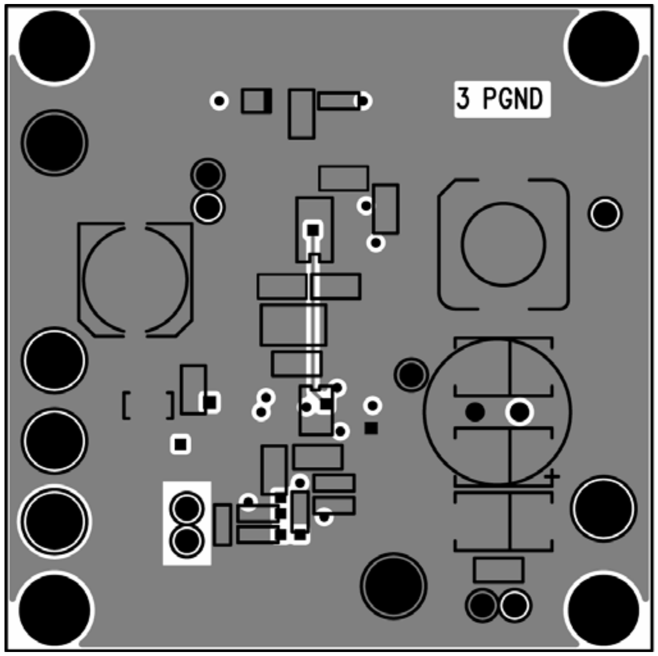


Figure 13. MIC2124 Evaluation Board Mid Layer 2

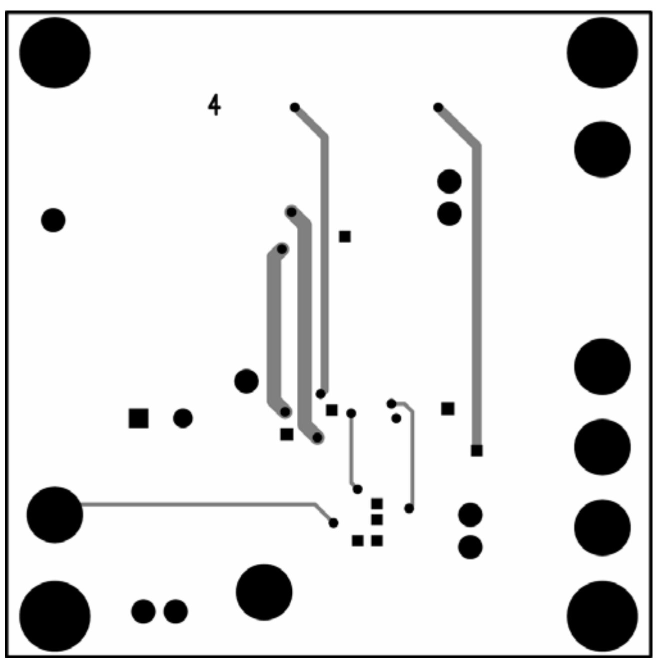
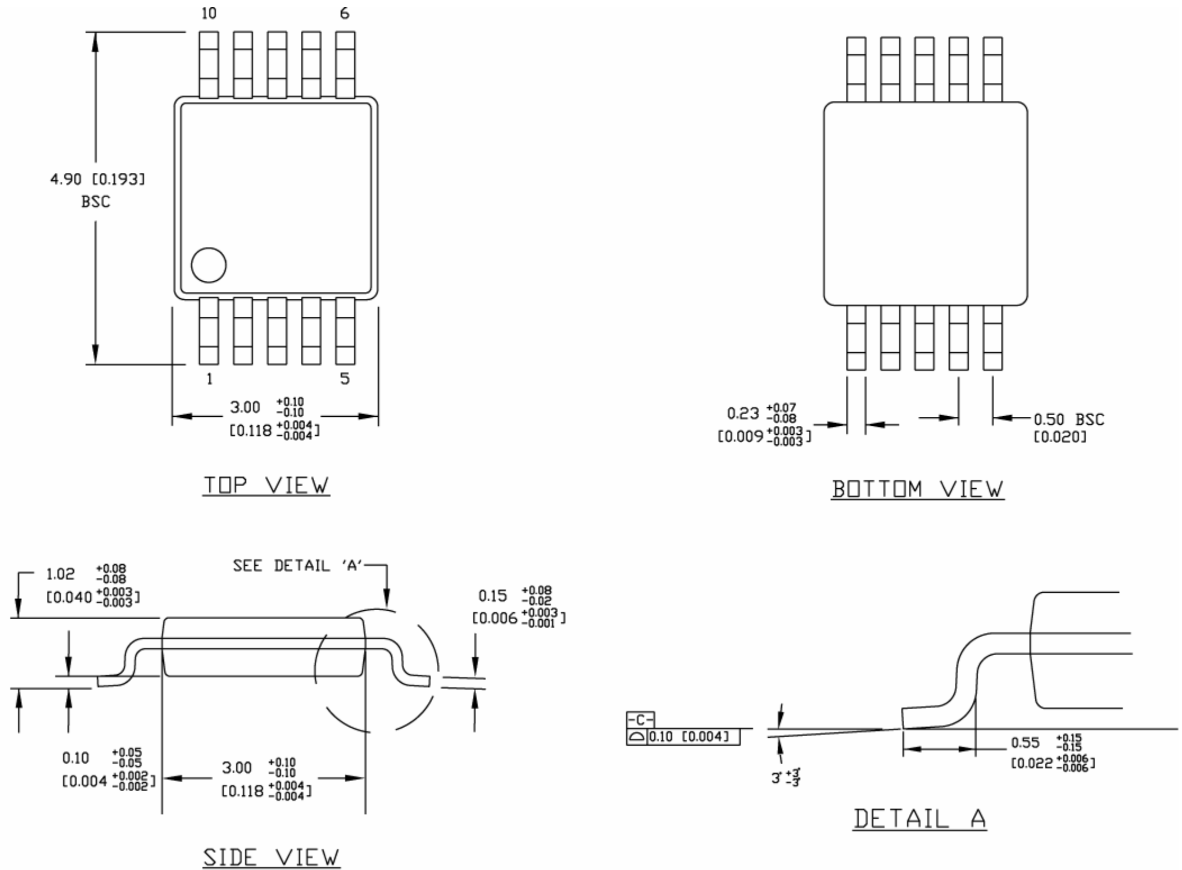


Figure 14. MIC2124 Evaluation Board Bottom Layer

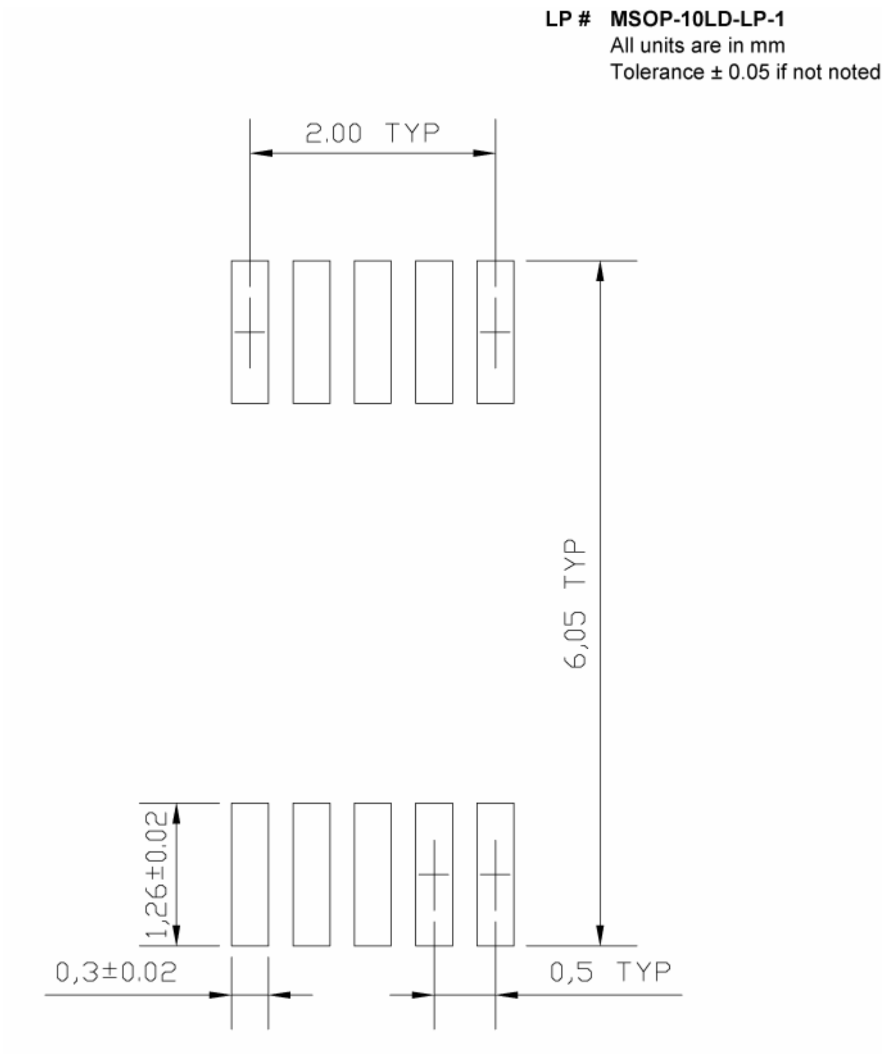
Package Information



NOTES:
1. DIMENSIONS ARE IN MM [INCHES].
2. CONTROLLING DIMENSION: MM
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.20 [0.008] PER SIDE.

10-Pin MSOP (MM)

Recommended Landing Pattern



MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA
TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB http://www.micrel.com

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- *Тестирование поставляемой продукции.*
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- *Техническую поддержку проекта.*
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