

# DATA SHEET

## **BT151U series C** Thyristors

Product specification

August 2018

## Thyristors

## BT151U series C

## GENERAL DESCRIPTION

Passivated thyristors in a plastic envelope, intended for use in applications requiring high bidirectional blocking voltage capability and high thermal cycling performance. Typical applications include motor control, industrial and domestic lighting, heating and static switching.

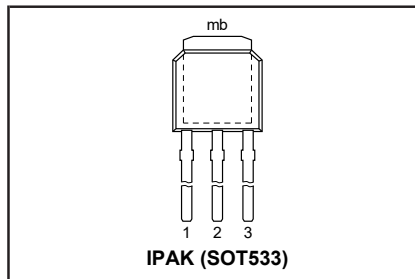
## QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	MAX.	UNIT
	<b>BT151U-</b>	<b>500C</b>	<b>650C</b>	<b>800C</b>	
$V_{DRM}, V_{RRM}$	Repetitive peak off-state voltages	500	650	800	V
$I_{T(AV)}$	Average on-state current	7.5	7.5	7.5	A
$I_{T(RMS)}$	RMS on-state current	12	12	12	A
$I_{TSM}$	Non-repetitive peak on-state current	100	100	100	A

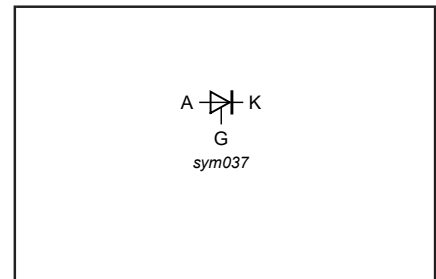
## PINNING - SOT533, (I-PAK)

PIN NUMBER	DESCRIPTION
1	cathode
2	anode
3	gate
tab	anode

## PIN CONFIGURATION



## SYMBOL



## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.			UNIT
$V_{DRM}, V_{RRM}$	Repetitive peak off-state voltages		-	<b>-500C</b> 500 <sup>1</sup>	<b>-650C</b> 650 <sup>1</sup>	<b>-800C</b> 800	V
$I_{T(AV)}$	Average on-state current	half sine wave; $T_{mb} \leq 104\text{ °C}$	-	7.5			A
$I_{T(RMS)}$	RMS on-state current	all conduction angles	-	12			A
$I_{TSM}$	Non-repetitive peak on-state current	half sine wave; $T_j = 25\text{ °C}$ prior to surge	-	100			A
		$t = 10\text{ ms}$	-	110			A
$I^2t$	$I^2t$ for fusing	$t = 8.3\text{ ms}$	-	50			A <sup>2</sup> s
$dI_T/dt$	Repetitive rate of rise of on-state current after triggering	$t = 10\text{ ms}$	-	50			A/μs
$I_{GM}$	Peak gate current	$I_{TM} = 20\text{ A}; I_G = 50\text{ mA}; dI_G/dt = 50\text{ mA/μs}$	-	2			A
$V_{RGM}$	Peak reverse gate voltage		-	5			V
$P_{GM}$	Peak gate power		-	5			W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5			W
$T_{stg}$	Storage temperature		-40	150			°C
$T_j$	Junction temperature		-	125			°C

<sup>1</sup> Although not recommended, off-state voltages up to 800V may be applied without damage, but the thyristor may switch to the on-state. The rate of rise of current should not exceed 15 A/μs.

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## THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j-mb}$	Thermal resistance junction to mounting base	in free air	-	-	1.3	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient		-	70	-	K/W

## STATIC CHARACTERISTICS

 $T_j = 25\text{ °C}$  unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{GT}$	Gate trigger current	$V_D = 12\text{ V}; I_T = 0.1\text{ A}$	-	2	15	mA
$I_L$	Latching current	$V_D = 12\text{ V}; I_{GT} = 0.1\text{ A}$	-	10	40	mA
$I_H$	Holding current	$V_D = 12\text{ V}; I_{GT} = 0.1\text{ A}$	-	7	20	mA
$V_T$	On-state voltage	$I_T = 23\text{ A}$	-	1.44	1.75	V
$V_{GT}$	Gate trigger voltage	$V_D = 12\text{ V}; I_T = 0.1\text{ A}$	-	0.6	1.5	V
$I_D, I_R$	Off-state leakage current	$V_D = V_{DRM(max)}; I_T = 0.1\text{ A}; T_j = 125\text{ °C}$	0.25	0.4	-	V
		$V_D = V_{DRM(max)}; V_R = V_{RRM(max)}; T_j = 125\text{ °C}$	-	0.1	0.5	mA

## DYNAMIC CHARACTERISTICS

 $T_j = 25\text{ °C}$  unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$dV_D/dt$	Critical rate of rise of off-state voltage	$V_{DM} = 67\% V_{DRM(max)}; T_j = 125\text{ °C};$ exponential waveform	-	-	-	-
$t_{gt}$	Gate controlled turn-on time	Gate open circuit $R_{GK} = 100\ \Omega$	50	130	-	V/ $\mu$ s
		$I_{TM} = 40\text{ A}; V_D = V_{DRM(max)}; I_G = 0.1\text{ A};$ $dI_G/dt = 5\text{ A}/\mu\text{s}$	200	1000	-	V/ $\mu$ s
$t_q$	Circuit commutated turn-off time	$V_D = 67\% V_{DRM(max)}; T_j = 125\text{ °C};$ $I_{TM} = 20\text{ A}; V_R = 25\text{ V}; dI_{TM}/dt = 30\text{ A}/\mu\text{s};$ $dV_D/dt = 50\text{ V}/\mu\text{s}; R_{GK} = 100\ \Omega$	-	70	-	$\mu$ s

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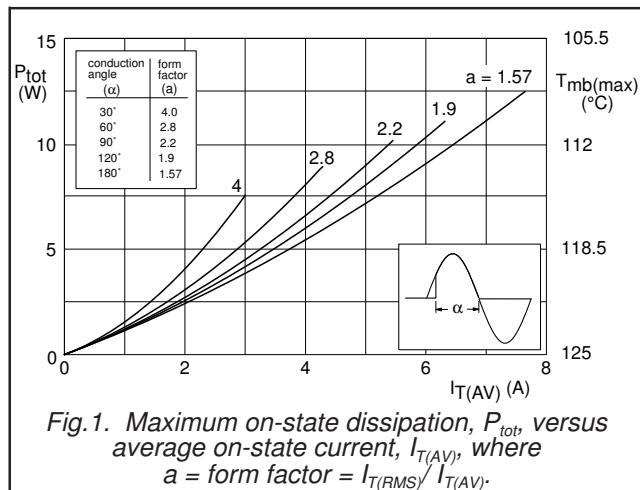


Fig.1. Maximum on-state dissipation,  $P_{tot}$ , versus average on-state current,  $I_{T(AV)}$ , where  $a = \text{form factor} = I_{T(RMS)}/I_{T(AV)}$ .

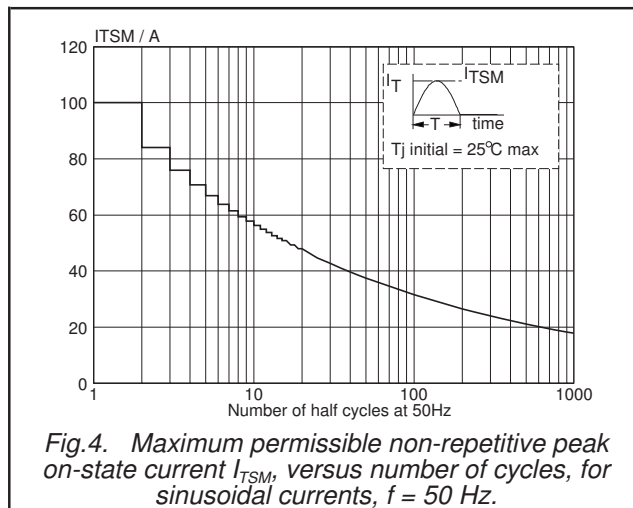


Fig.4. Maximum permissible non-repetitive peak on-state current  $I_{TSM}$ , versus number of cycles, for sinusoidal currents,  $f = 50 \text{ Hz}$ .

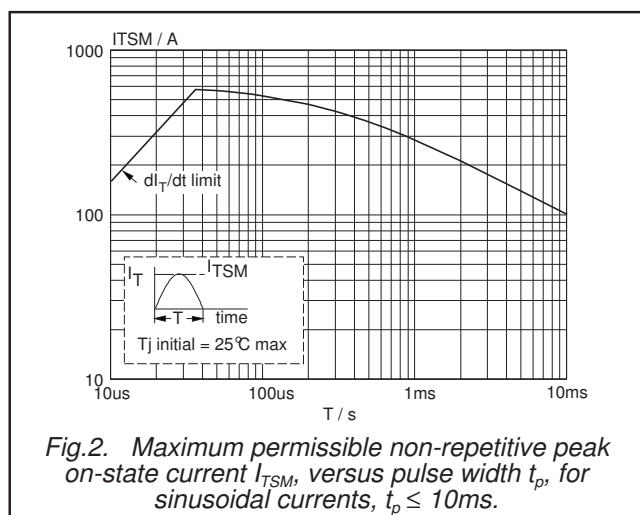


Fig.2. Maximum permissible non-repetitive peak on-state current  $I_{TSM}$ , versus pulse width  $t_p$ , for sinusoidal currents,  $t_p \leq 10 \text{ ms}$ .

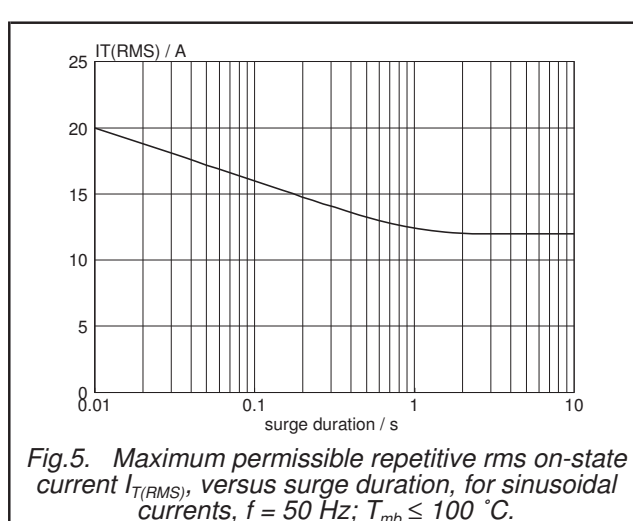


Fig.5. Maximum permissible repetitive rms on-state current  $I_{T(RMS)}$ , versus surge duration, for sinusoidal currents,  $f = 50 \text{ Hz}$ ;  $T_{mb} \leq 100^\circ\text{C}$ .

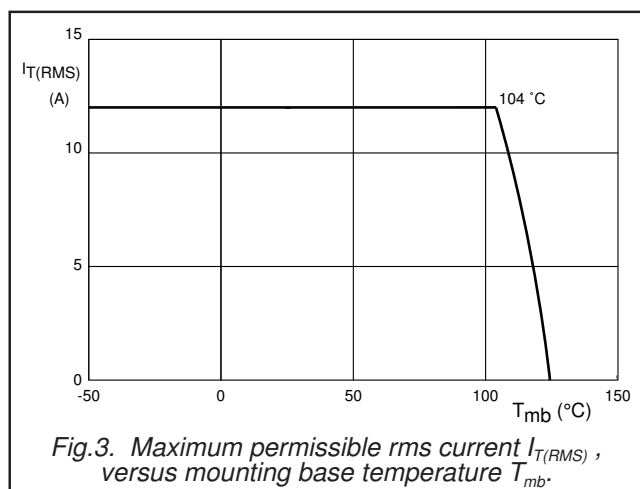


Fig.3. Maximum permissible rms current  $I_{T(RMS)}$ , versus mounting base temperature  $T_{mb}$ .

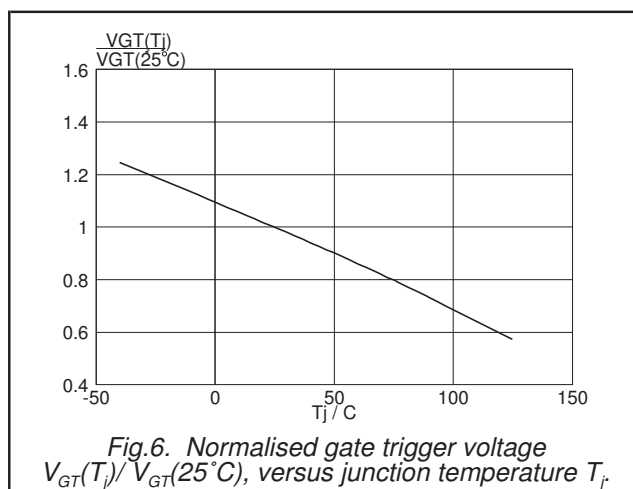
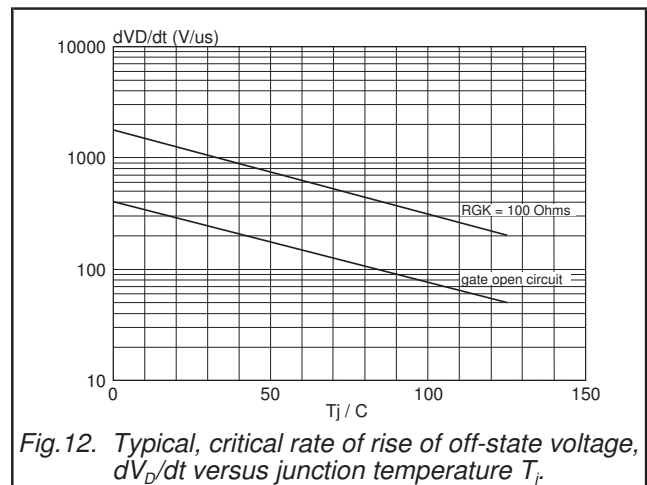
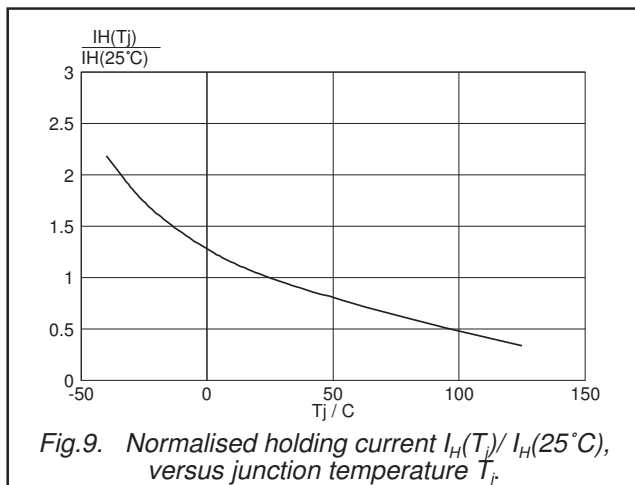
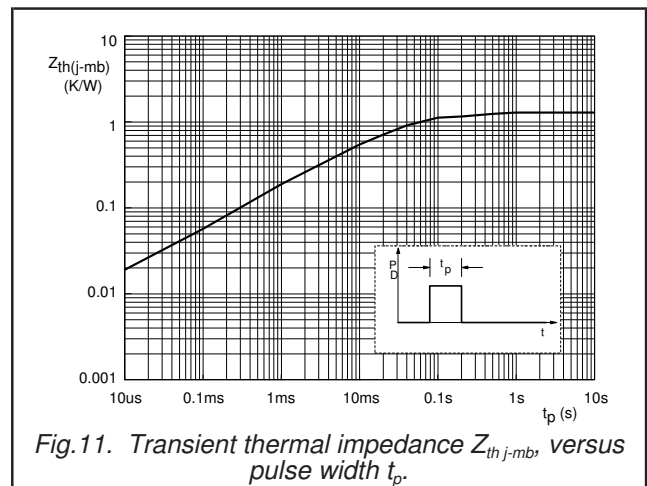
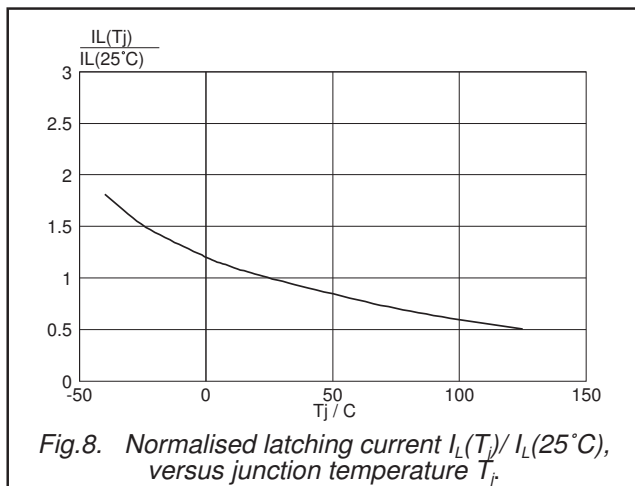
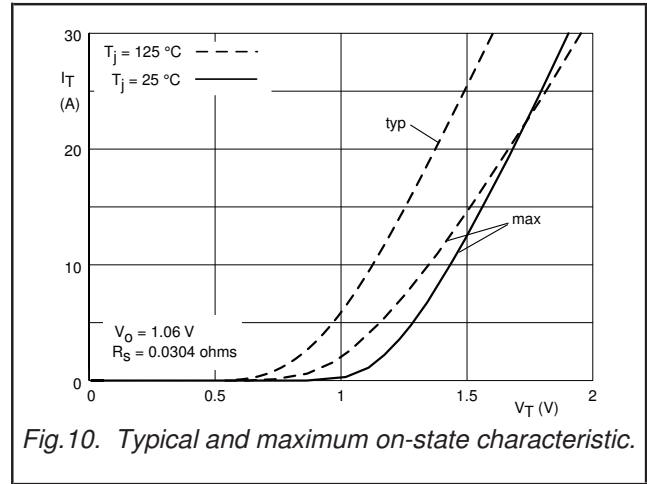
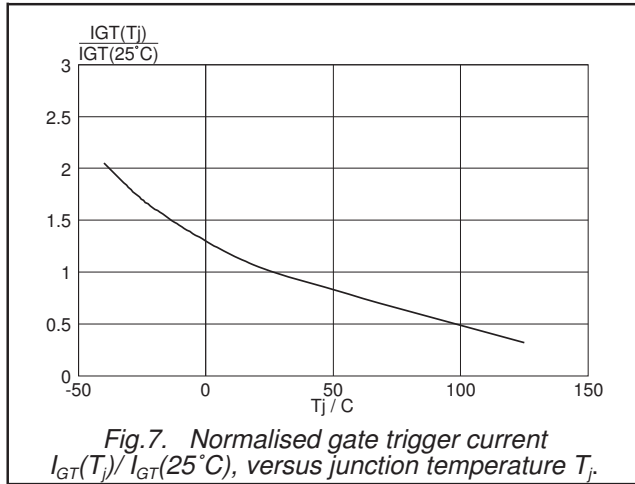


Fig.6. Normalised gate trigger voltage  $V_{GT}(T_j)/V_{GT}(25^\circ\text{C})$ , versus junction temperature  $T_j$ .

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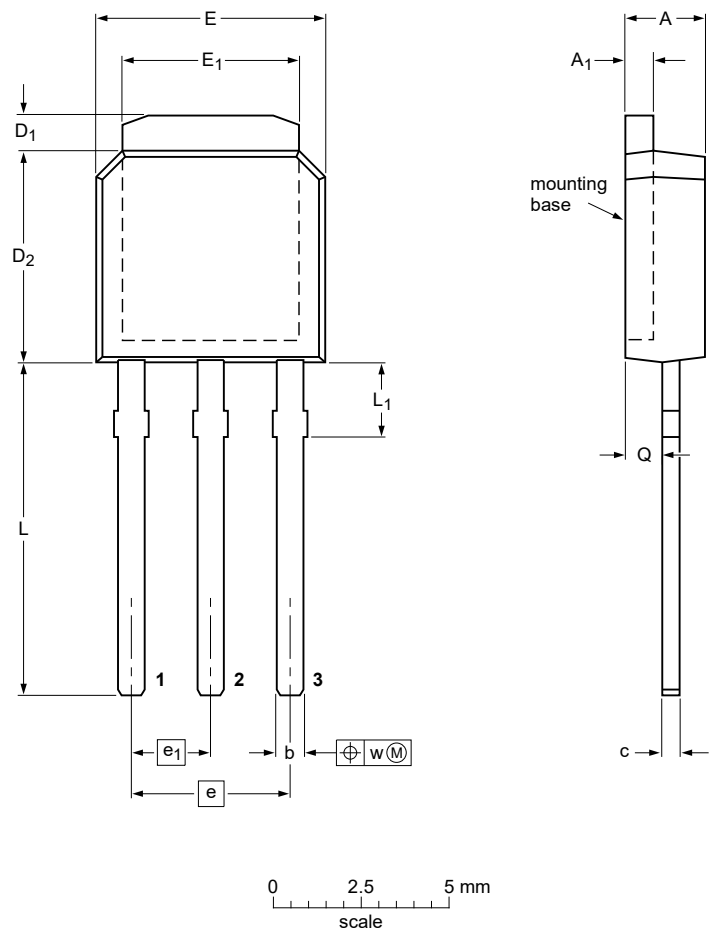
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MECHANICAL DATA

Plastic single-ended package (IPAK); 3 leads (in-line)

SOT533



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub>	b	c	D <sub>1</sub>	D <sub>2</sub>	E	E <sub>1</sub>	e	e <sub>1</sub>	L	L <sub>1</sub> <sup>(2)</sup> max	Q	w
mm	2.38 2.22	0.93 0.46	0.89 0.71	0.56 0.46	1.10 0.96	6.22 5.98	6.73 6.47	5.21 5.00	4.57 BSC <sup>(1)</sup>	2.285 BSC <sup>(1)</sup>	9.6 9.2	2.7	1.1 1.0	0.3

Notes

- 1. Basic spacing between centers.
- 2. Terminal dimensions are uncontrolled within zone L<sub>1</sub>.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT533		TO-251				05-02-11- 06-02-14

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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