SHARC Processor

# ADSP-21483/ADSP-21486/ADSP-21487/ADSP-21488/ADSP-21489

## SUMMARY

**High performance 32-bit/40-bit floating-point processor optimized for high performance audio processing**

**Single-instruction, multiple-data (SIMD) computational architecture**

**On-chip memory—5 Mbits on-chip RAM, 4 Mbits on-chip ROM**

**Up to 450 MHz operating frequency**

**Code compatible with all other members of the SHARC family**

**The ADSP-2148x processors are available with unique audio-centric peripherals, such as the digital applications interface, serial ports, precision clock generators, S/PDIF transceiver, asynchronous sample rate converters, input data port, and more**

**For complete ordering information, see Ordering Guide on Page 66**

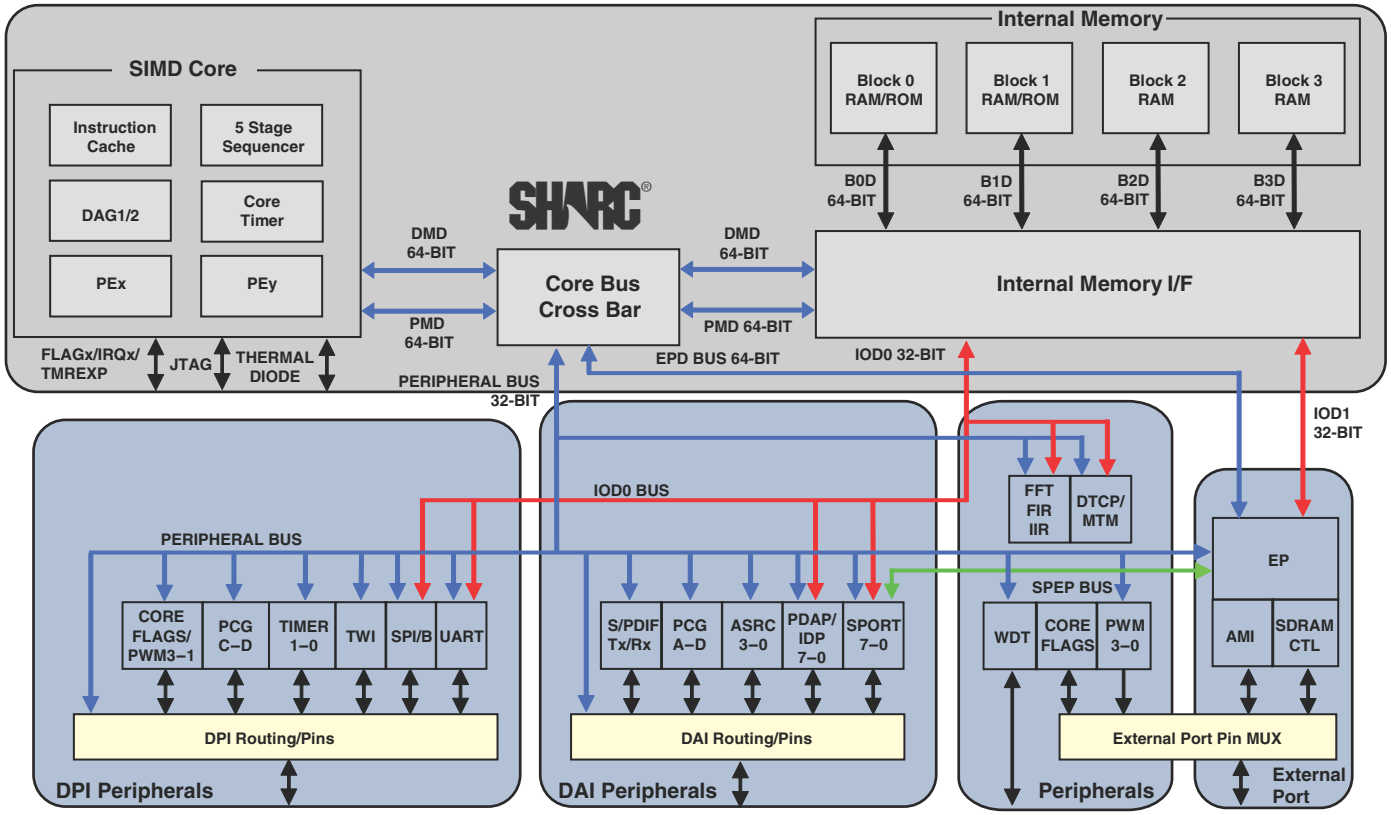


*Figure 1. Functional Block Diagram*

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**Rev. B** **Document Feedback**

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# TABLE OF CONTENTS


Summary ..... 1
General Description ..... 3
Family Core Architecture ..... 4
Family Peripheral Architecture ..... 7
I/O Processor Features ..... 10
System Design ..... 11
Development Tools ..... 12
Additional Information ..... 13
Related Signal Chains ..... 13
Pin Function Descriptions ..... 14
Specifications ..... 18
Operating Conditions ..... 18
Electrical Characteristics ..... 19
Absolute Maximum Ratings ..... 21
ESD Sensitivity ..... 21
Maximum Power Dissipation ..... 21
Package Information ..... 21
Timing Specifications ..... 22
Output Drive Currents ..... 55
Test Conditions ..... 55
Capacitive Loading ..... 55
Thermal Characteristics ..... 56
100-LQFP_EP Lead Assignment ..... 58
176-Lead LQFP_EP Lead Assignment ..... 60
Outline Dimensions ..... 64
Surface-Mount Design ..... 65
Automotive Products ..... 66
Ordering Guide ..... 66


## REVISION HISTORY

**3/13—Revision A to Revision B**

Corrected outstanding document errata.

Added section Static Voltage Scaling (SVS) ..... 11

Revised Development Tools ..... 12

Revised $\overline{MS}_{0-1}$ Pin Description in Pin Function Descriptions ..... 14

Revised Electrical Characteristics ..... 19

Revised Total Power Dissipation ..... 20

Added paragraph to SDRAM Interface Timing (166 MHz SDCLK) ..... 32

Added footnote 3 to Table 32 in AMI Read ..... 33

Changed Max values in Table 43 in Pulse-Width Modulation Generators (PWM) ..... 45

Added model to Automotive Product Table (Table 63) in Automotive Products ..... 66

Revised Ordering Guide ..... 66

Added 450 MHz products and information to the following:

- Tables 1 and 2 in General Description ..... 3
- Operating Conditions ..... 18
- Electrical Characteristics ..... 19
- Tables 14 and 15 in Total Power Dissipation ..... 20
- Table 20 in Clock Input ..... 24

# GENERAL DESCRIPTION

The ADSP-2148x SHARC® processors are members of the SIMD SHARC family of DSPs that feature Analog Devices' Super Harvard Architecture. The processors are source code compatible with the ADSP-2126x, ADSP-2136x, ADSP-2137x, ADSP-2146x, ADSP-2147x and ADSP-2116x DSPs, as well as with first generation ADSP-2106x SHARC processors in SISD (single-instruction, single-data) mode. The ADSP-2148x processors are 32-bit/40-bit floating point processors optimized for high performance audio applications with large on-chip SRAM, multiple internal buses to eliminate I/O bottlenecks, and an innovative digital applications interface (DAI).

Table 1 shows performance benchmarks for the ADSP-2148x processors. Table 2 shows the features of the individual product offerings.

**Table 1. Processor Benchmarks**

| Benchmark Algorithm | Speed (at 400 MHz) | Speed (at 450 MHz) |
|---|---|---|
| 1024 Point Complex FFT (Radix 4, with Reversal) | 23 µs | 20.44 µs |
| FIR Filter (per Tap)[1] | 1.25 ns | 1.1 ns |
| IIR Filter (per Biquad)[1] | 5 ns | 4.43 ns |
| Matrix Multiply (Pipelined) | | |
| [3 × 3] × [3 × 1] | 11.25 ns | 10.0 ns |
| [4 × 4] × [4 × 1] | 20 ns | 17.78 ns |
| Divide (y/×) | 7.5 ns | 6.67 ns |
| Inverse Square Root | 11.25 ns | 10.0 ns |

[1] Assumes two files in multichannel SIMD mode

**Table 2. ADSP-2148x Family Features**

| Feature | ADSP-21483 | ADSP-21486 | ADSP-21487 | ADSP-21488 | ADSP-21489 |
|---|---|---|---|---|---|
| Maximum Instruction Rate | 400 MHz | 400 MHz | 450 MHz | 400 MHz | 450 MHz |
| RAM | 3 Mbits | 5 Mbits | | 3 Mbits | 5 Mbits |
| ROM | 4 Mbits | | | No | |
| Audio Decoders in ROM[1] | Yes | | | No | |
| Pulse-Width Modulation | 4 Units (3 Units on 100-Lead Packages) | | | | |
| DTCP Hardware Accelerator | Contact Analog Devices | | | | |
| External Port Interface (SDRAM, AMI)[2] | Yes (16-bit) | AMI Only | Yes (16-bit) | | |
| Serial Ports | 8 | | | | |
| Direct DMA from SPORTs to External Port (External Memory) | Yes | | | | |
| FIR, IIR, FFT Accelerator | Yes | | | | |
| Watchdog Timer | Yes (176-Lead Package Only) | | | | |
| MediaLB Interface | Automotive Models Only | | | | |
| IDP/PDAP | Yes | | | | |
| UART | 1 | | | | |
| DAI (SRU)/DPI (SRU2) | Yes | | | | |
| S/PDIF Transceiver | Yes | | | | |
| SPI | Yes | | | | |
| TWI | 1 | | | | |
| SRC Performance[3] | –128 dB | | | | |
| Thermal Diode | Yes | | | | |
| VISA Support | Yes | | | | |
| Package[2] | 176-Lead LQFP EPAD<br>100-Lead LQFP EPAD | | 176-Lead LQFP EPAD | 176-Lead LQFP EPAD<br>100-Lead LQFP EPAD | |

[1] ROM is factory programmed with latest multichannel audio decoding and post-processing algorithms from Dolby® Labs and DTS®. Decoder/post-processor algorithm combination support varies depending upon the chip version and the system configurations. Please visit www.analog.com for complete information.

[2] The 100-lead packages do not contain an external port. The SDRAM controller pins must be disabled when using this package. For more information, see Pin Function Descriptions on Page 14. The ADSP-21486 processor in the 176-lead package also does not contain a SDRAM controller. For more information, see 176-Lead LQFP_EP Lead Assignment on page 60.

[3] Some models have –140 dB performance. For more information, see Ordering Guide on page 66.

The diagram on Page 1 shows the two clock domains that make up the ADSP-2148x processors. The core clock domain contains the following features:

- Two processing elements (PEx, PEy), each of which comprises an ALU, multiplier, shifter, and data register file
- Data address generators (DAG1, DAG2)
- Program sequencer with instruction cache
- PM and DM buses capable of supporting 2x64-bit data transfers between memory and the core at every core processor cycle
- One periodic interval timer with pinout
- On-chip SRAM (5 Mbit) and mask-programmable ROM (4 Mbit)
- JTAG test access port for emulation and boundary scan. The JTAG provides software debug through user breakpoints which allows flexible exception handling.

The block diagram of the ADSP-2148x on Page 1 also shows the peripheral clock domain (also known as the I/O processor) which contains the following features:

- IOD0 (peripheral DMA) and IOD1 (external port DMA) buses for 32-bit data transfers
- Peripheral and external port buses for core connection
- External port with an AMI and SDRAM controller
- 4 units for PWM control
- 1 memory-to-memory (MTM) unit for internal-to-internal memory transfers
- Digital applications interface that includes four precision clock generators (PCG), an input data port (IDP/PDAP) for serial and parallel interconnects, an S/PDIF receiver/transmitter, four asynchronous sample rate converters, eight serial ports, and a flexible signal routing unit (DAI SRU).
- Digital peripheral interface that includes two timers, a 2-wire interface (TWI), one UART, two serial peripheral interfaces (SPI), 2 precision clock generators (PCG), pulse width modulation (PWM), and a flexible signal routing unit (DPI SRU2).

As shown in the SHARC core block diagram on Page 5, the processor uses two computational units to deliver a significant performance increase over the previous SHARC processors on a range of DSP algorithms. With its SIMD computational hardware, the processors can perform 2.7 GFLOPS running at 450 MHz.

## FAMILY CORE ARCHITECTURE

The ADSP-2148x is code compatible at the assembly level with the ADSP-2147x, ADSP-2146x, ADSP-2137x, ADSP-2136x, ADSP-2126x, ADSP-21160, and ADSP-21161, and with the first generation ADSP-2106x SHARC processors. The ADSP-2148x shares architectural features with the ADSP-2126x, ADSP-2136x, ADSP-2137x, ADSP-2146x and ADSP-2116x SIMD SHARC processors, as shown in Figure 2 and detailed in the following sections.

### *SIMD Computational Engine*

The ADSP-2148x contains two computational processing elements that operate as a single-instruction, multiple-data (SIMD) engine. The processing elements are referred to as PEX and PEY and each contains an ALU, multiplier, shifter, and register file. PEx is always active, and PEy may be enabled by setting the PEYEN mode bit in the MODE1 register. SIMD mode allows the processor to execute the same instruction in both processing elements, but each processing element operates on different data. This architecture is efficient at executing math intensive DSP algorithms.

SIMD mode also affects the way data is transferred between memory and the processing elements because twice the data bandwidth is required to sustain computational operation in the processing elements. Therefore, entering SIMD mode also doubles the bandwidth between memory and the processing elements. When using the DAGs to transfer data in SIMD mode, two data values are transferred with each memory or register file access.

### *Independent, Parallel Computation Units*

Within each processing element is a set of computational units. The computational units consist of an arithmetic/logic unit (ALU), multiplier, and shifter. These units perform all operations in a single cycle and are arranged in parallel, maximizing computational throughput. Single multifunction instructions execute parallel ALU and multiplier operations. In SIMD mode, the parallel ALU and multiplier operations occur in both processing elements. These computation units support IEEE 32-bit single-precision floating-point, 40-bit extended precision floating-point, and 32-bit fixed-point data formats.

### *Timer*

The processor contains a core timer that can generate periodic software interrupts. The core timer can be configured to use FLAG3 as a timer expired signal.

### *Data Register File*

Each processing element contains a general-purpose data register file. The register files transfer data between the computation units and the data buses, and store intermediate results. These 10-port, 32-register (16 primary, 16 secondary) register files, combined with the processor's enhanced Harvard architecture, allow unconstrained data flow between computation units and internal memory. The registers in PEX are referred to as R0–R15 and in PEY as S0–S15.

### *Context Switch*

Many of the processor's registers have secondary registers that can be activated during interrupt servicing for a fast context switch. The data registers in the register file, the DAG registers, and the multiplier result registers all have secondary registers. The primary registers are active at reset, while the secondary registers are activated by control bits in a mode control register.

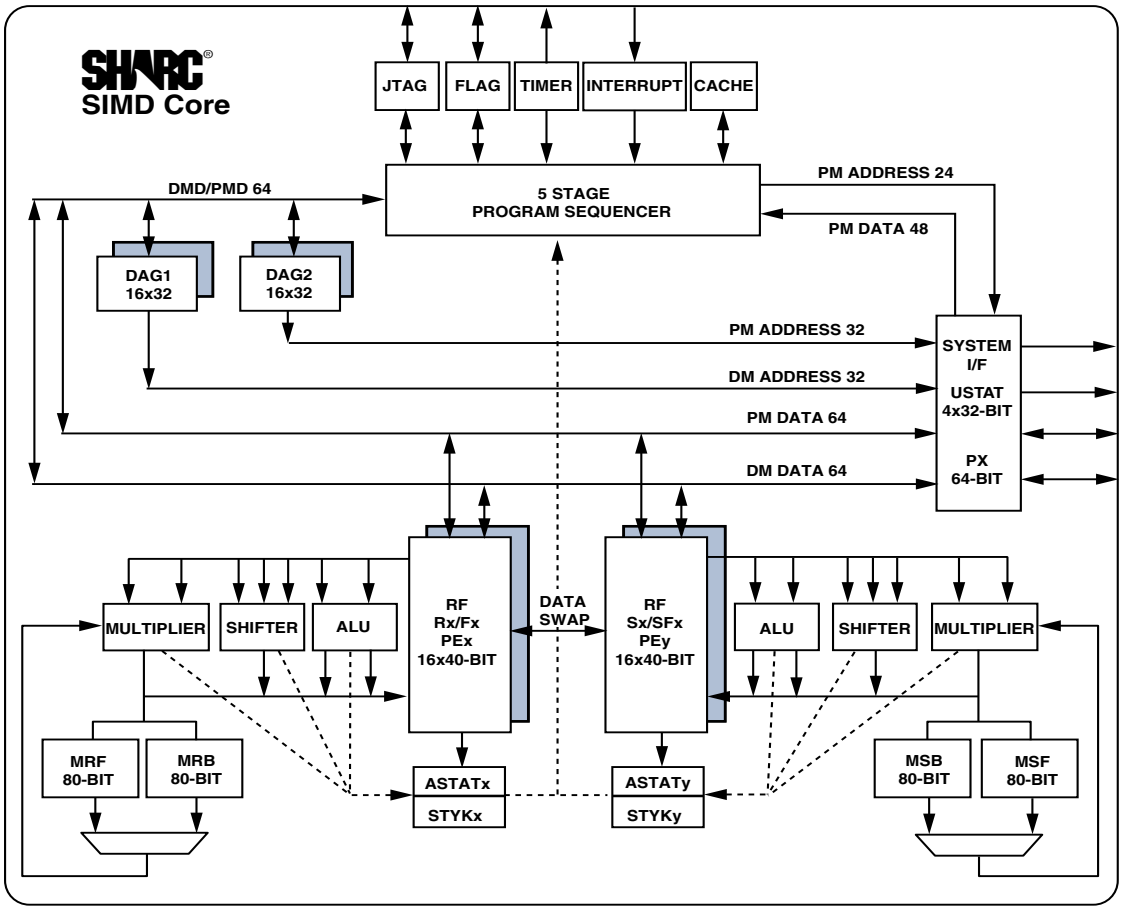


*Figure 2. SHARC Core Block Diagram*

### *Universal Registers*

These registers can be used for general-purpose tasks. The USTAT (4) registers allow easy bit manipulations (Set, Clear, Toggle, Test, XOR) for all peripheral registers (control/status).

The data bus exchange register (PX) permits data to be passed between the 64-bit PM data bus and the 64-bit DM data bus, or between the 40-bit register file and the PM/DM data bus. These registers contain hardware to handle the data width difference.

### *Single-Cycle Fetch of Instruction and Four Operands*

The ADSP-2148x features an enhanced Harvard architecture in which the data memory (DM) bus transfers data and the program memory (PM) bus transfers both instructions and data. With the its separate program and data memory buses and on-chip instruction cache, the processor can simultaneously fetch four operands (two over each data bus) and one instruction (from the cache), all in a single cycle.

### *Instruction Cache*

The processor includes an on-chip instruction cache that enables three-bus operation for fetching an instruction and four data values. The cache is selective—only the instructions whose fetches conflict with PM bus data accesses are cached. This cache allows full speed execution of core, looped operations such as digital filter multiply-accumulates, and FFT butterfly processing.

### *Data Address Generators With Zero-Overhead Hardware Circular Buffer Support*

The two data address generators (DAGs) are used for indirect addressing and implementing circular data buffers in hardware. Circular buffers allow efficient programming of delay lines and other data structures required in digital signal processing, and are commonly used in digital filters and Fourier transforms. The two DAGs contain sufficient registers to allow the creation of up to 32 circular buffers (16 primary register sets, 16 secondary). The DAGs automatically handle address pointer wraparound, reduce overhead, increase performance, and simplify implementation. Circular buffers can start and end at any memory location.

### *Flexible Instruction Set*

The 48-bit instruction word accommodates a variety of parallel operations, for concise programming. For example, the processor can conditionally execute a multiply, an add, and a

subtract in both processing elements while branching and fetching up to four 32-bit values from memory, all in a single instruction.

### *Variable Instruction Set Architecture (VISA)*

In addition to supporting the standard 48-bit instructions from previous SHARC processors, the ADSP-2148x supports new instructions of 16 and 32 bits. This feature, called Variable Instruction Set Architecture (VISA), drops redundant/unused bits within the 48-bit instruction to create more efficient and compact code. The program sequencer supports fetching these 16-bit and 32-bit instructions from both internal and external SDRAM memory. This support is not extended to the asynchronous memory interface (AMI). Source modules need to be built using the VISA option, in order to allow code generation tools to create these more efficient opcodes.

### *On-Chip Memory*

The ADSP-21483 and the ADSP-21488 processors contain 3 Mbits of internal RAM (Table 3) and the ADSP-21486, ADSP-21487, and ADSP-21489 processors contain 5 Mbits of internal RAM (Table 4). Each memory block supports single-cycle, independent accesses by the core processor and I/O processor.

**Table 3. Internal Memory Space (3 MBits—ADSP-21483/ADSP-21488)[1]**

| IOP Registers 0x0000 0000–0x0003 FFFF | | | |
|---|---|---|---|
| **Long Word (64 Bits)** | **Extended Precision Normal or Instruction Word (48 Bits)** | **Normal Word (32 Bits)** | **Short Word (16 Bits)** |
| Block 0 ROM (Reserved)<br>0x0004 0000–0x0004 7FFF | Block 0 ROM (Reserved)<br>0x0008 0000–0x0008 AAA9 | Block 0 ROM (Reserved)<br>0x0008 0000–0x0008 FFFF | Block 0 ROM (Reserved)<br>0x0010 0000–0x0011 FFFF |
| Reserved<br>0x0004 8000–0x0004 8FFF | Reserved<br>0x0008 AAAA–0x0008 BFFF | Reserved<br>0x0009 0000–0x0009 1FFF | Reserved<br>0x0012 0000–0x0012 3FFF |
| Block 0 SRAM<br>0x0004 9000–0x0004 CFFF | Block 0 SRAM<br>0x0008 C000–0x0009 1554 | Block 0 SRAM<br>0x0009 2000–0x0009 9FFF | Block 0 SRAM<br>0x0012 4000–0x0013 3FFF |
| Reserved<br>0x0004 D000–0x0004 FFFF | Reserved<br>0x0009 1555–0x0009 FFFF | Reserved<br>0x0009 A000–0x0009 FFFF | Reserved<br>0x0013 4000–0x0013 FFFF |
| Block 1 ROM (Reserved)<br>0x0005 0000–0x0005 7FFF | Block 1 ROM (Reserved)<br>0x000A 0000–0x000A AAA9 | Block 1 ROM (Reserved)<br>0x000A 0000–0x000A FFFF | Block 1 ROM (Reserved)<br>0x0014 0000–0x0015 FFFF |
| Reserved<br>0x0005 8000–0x0005 8FFF | Reserved<br>0x000A AAAA–0x000A BFFF | Reserved<br>0x000B 0000–0x000B 1FFF | Reserved<br>0x0016 0000–0x0016 3FFF |
| Block 1 SRAM<br>0x0005 9000–0x0005 CFFF | Block 1 SRAM<br>0x000A C000–0x000B 1554 | Block 1 SRAM<br>0x000B 2000–0x000B 9FFF | Block 1 SRAM<br>0x0016 4000–0x0017 3FFF |
| Reserved<br>0x0005 D000–0x0005 FFFF | Reserved<br>0x000B 1555–0x000B FFFF | Reserved<br>0x000B A000–0x000B FFFF | Reserved<br>0x0017 4000–0x0017 FFFF |
| Block 2 SRAM<br>0x0006 0000–0x0006 1FFF | Block 2 SRAM<br>0x000C 0000–0x000C 2AA9 | Block 2 SRAM<br>0x000C 0000–0x000C 3FFF | Block 2 SRAM<br>0x0018 0000–0x0018 7FFF |
| Reserved<br>0x0006 2000– 0x0006 FFFF | Reserved<br>0x000C 2AAA–0x000D FFFF | Reserved<br>0x000C 4000–0x000D FFFF | Reserved<br>0x0018 8000–0x001B FFFF |
| Block 3 SRAM<br>0x0007 0000–0x0007 1FFF | Block 3 SRAM<br>0x000E 0000–0x000E 2AA9 | Block 3 SRAM<br>0x000E 0000–0x000E 3FFF | Block 3 SRAM<br>0x001C 0000–0x001C 7FFF |
| Reserved<br>0x0007 2000–0x0007 FFFF | Reserved<br>0x000E 2AAA–0x000F FFFF | Reserved<br>0x000E 4000–0x000F FFFF | Reserved<br>0x001C 8000–0x001F FFFF |

[1] Some ADSP-2148x processors include a customer-definable ROM block. ROM addresses on these models are not reserved as shown in this table. Please contact your Analog Devices sales representative for additional details.

The processor's SRAM can be configured as a maximum of 160k words of 32-bit data, 320k words of 16-bit data, 106.7k words of 48-bit instructions (or 40-bit data), or combinations of different word sizes up to 5 megabits. All of the memory can be accessed as 16-bit, 32-bit, 48-bit, or 64-bit words. A 16-bit floating-point storage format is supported that effectively doubles the amount of data that may be stored on-chip. Conversion between the 32-bit floating-point and 16-bit floating-point formats is performed in a single instruction. While each memory block can store combinations of code and data, accesses are most efficient when one block stores data using the DM bus for transfers, and the other block stores instructions and data using the PM bus for transfers.

Using the DM bus and PM buses, with one bus dedicated to a memory block, assures single-cycle execution with two data transfers. In this case, the instruction must be available in the cache.

The memory maps in Table 3 and Table 4 display the internal memory address space of the processors. The 48-bit space section describes what this address range looks like to an

**Table 4. Internal Memory Space (5 MBits—ADSP-21486/ADSP-21487/ADSP-21489)[1]**

| IOP Registers 0x0000 0000–0x0003 FFFF | | | |
|---|---|---|---|
| **Long Word (64 Bits)** | **Extended Precision Normal or Instruction Word (48 Bits)** | **Normal Word (32 Bits)** | **Short Word (16 Bits)** |
| Block 0 ROM (Reserved)<br>0x0004 0000–0x0004 7FFF | Block 0 ROM (Reserved)<br>0x0008 0000–0x0008 AAA9 | Block 0 ROM (Reserved)<br>0x0008 0000–0x0008 FFFF | Block 0 ROM (Reserved)<br>0x0010 0000–0x0011 FFFF |
| Reserved<br>0x0004 8000–0x0004 8FFF | Reserved<br>0x0008 AAAA–0x0008 BFFF | Reserved<br>0x0009 0000–0x0009 1FFF | Reserved<br>0x0012 0000–0x0012 3FFF |
| Block 0 SRAM<br>0x0004 9000–0x0004 EFFF | Block 0 SRAM<br>0x0008 C000–0x0009 3FFF | Block 0 SRAM<br>0x0009 2000–0x0009 DFFF | Block 0 SRAM<br>0x0012 4000–0x0013 BFFF |
| Reserved<br>0x0004 F000–0x0004 FFFF | Reserved<br>0x0009 4000–0x0009 FFFF | Reserved<br>0x0009 E000–0x0009 FFFF | Reserved<br>0x0013 C000–0x0013 FFFF |
| Block 1 ROM (Reserved)<br>0x0005 0000–0x0005 7FFF | Block 1 ROM (Reserved)<br>0x000A 0000–0x000A AAA9 | Block 1 ROM (Reserved)<br>0x000A 0000–0x000A FFFF | Block 1 ROM (Reserved)<br>0x0014 0000–0x0015 FFFF |
| Reserved<br>0x0005 8000–0x0005 8FFF | Reserved<br>0x000A AAAA–0x000A BFFF | Reserved<br>0x000B 0000–0x000B 1FFF | Reserved<br>0x0016 0000–0x0016 3FFF |
| Block 1 SRAM<br>0x0005 9000–0x0005 EFFF | Block 1 SRAM<br>0x000A C000–0x000B 3FFF | Block 1 SRAM<br>0x000B 2000–0x000B DFFF | Block 1 SRAM<br>0x0016 4000–0x0017 BFFF |
| Reserved<br>0x0005 F000–0x0005 FFFF | Reserved<br>0x000B 4000–0x000B FFFF | Reserved<br>0x000B E000–0x000B FFFF | Reserved<br>0x0017 C000–0x0017 FFFF |
| Block 2 SRAM<br>0x0006 0000–0x0006 3FFF | Block 2 SRAM<br>0x000C 0000–0x000C 5554 | Block 2 SRAM<br>0x000C 0000–0x000C 7FFF | Block 2 SRAM<br>0x0018 0000–0x0018 FFFF |
| Reserved<br>0x0006 4000– 0x0006 FFFF | Reserved<br>0x000C 5555–0x000D FFFF | Reserved<br>0x000C 8000–0x000D FFFF | Reserved<br>0x0019 0000–0x001B FFFF |
| Block 3 SRAM<br>0x0007 0000–0x0007 3FFF | Block 3 SRAM<br>0x000E 0000–0x000E 5554 | Block 3 SRAM<br>0x000E 0000–0x000E 7FFF | Block 3 SRAM<br>0x001C 0000–0x001C FFFF |
| Reserved<br>0x0007 4000–0x0007 FFFF | Reserved<br>0x000E 5555–0x0000F FFFF | Reserved<br>0x000E 8000–0x000F FFFF | Reserved<br>0x001D 0000–0x001F FFFF |

[1] Some ADSP-2148x processors include a customer-definable ROM block and are not reserved as shown on this table. Please contact your Analog Devices sales representative for additional details.

instruction that retrieves 48-bit memory. The 32-bit section describes what this address range looks like to an instruction that retrieves 32-bit memory.

### *ROM Based Security*

The ADSP-2148x has a ROM security feature that provides hardware support for securing user software code by preventing unauthorized reading from the internal code. When using this feature, the processor does not boot-load any external code, executing exclusively from internal ROM. Additionally, the processor is not freely accessible via the JTAG port. Instead, a unique 64-bit key, which must be scanned in through the JTAG or Test Access Port will be assigned to each customer. The device will ignore a wrong key. Emulation features are available after the correct key is scanned.

### *On-Chip Memory Bandwidth*

The internal memory architecture allows programs to have four accesses at the same time to any of the four blocks (assuming there are no block conflicts). The total bandwidth is realized using the DMD and PMD buses (2 × 64-bits, CCLK speed) and the IOD0/1 buses (2 × 32-bit, PCLK speed).

## FAMILY PERIPHERAL ARCHITECTURE

The ADSP-2148x family contains a rich set of peripherals that support a wide variety of applications including high quality audio, medical imaging, communications, military, test equipment, 3D graphics, speech recognition, motor control, imaging, and other applications.

### *External Memory*

The external port interface supports access to the external memory through core and DMA accesses. The external memory address space is divided into four banks. Any bank can be programmed as either asynchronous or synchronous memory. The external ports are comprised of the following modules.

- An Asynchronous Memory Interface which communicates with SRAM, FLASH, and other devices that meet the standard asynchronous SRAM access protocol. The AMI supports 6M words of external memory in bank 0 and 8M words of external memory in bank 1, bank 2, and bank 3.
- A SDRAM controller that supports a glueless interface with any of the standard SDRAMs. The SDC supports 62M words of external memory in bank 0, and 64M words of external memory in bank 1, bank 2, and bank 3. NOTE: this feature is not available on the ADSP-21486 product.

- Arbitration logic to coordinate core and DMA transfers between internal and external memory over the external port.

Non-SDRAM external memory address space is shown in Table 5.

**Table 5. External Memory for Non-SDRAM Addresses**

| Bank | Size in Words | Address Range |
|---|---|---|
| Bank 0 | 6M | 0x0020 0000–0x007F FFFF |
| Bank 1 | 8M | 0x0400 0000–0x047F FFFF |
| Bank 2 | 8M | 0x0800 0000–0x087F FFFF |
| Bank 3 | 8M | 0x0C00 0000–0x0C7F FFFF |

### *External Port*

The external port provides a high performance, glueless interface to a wide variety of industry-standard memory devices. The external port, available on the 176-lead LQFP, may be used to interface to synchronous and/or asynchronous memory devices through the use of its separate internal memory controllers. The first is an SDRAM controller for connection of industry-standard synchronous DRAM devices while the second is an asynchronous memory controller intended to interface to a variety of memory devices. Four memory select pins enable up to four separate devices to coexist, supporting any desired combination of synchronous and asynchronous device types.

#### Asynchronous Memory Controller

The asynchronous memory controller provides a configurable interface for up to four separate banks of memory or I/O devices. Each bank can be independently programmed with different timing parameters, enabling connection to a wide variety of memory devices including SRAM, flash, and EPROM, as well as I/O devices that interface with standard memory control lines. Bank 0 occupies a 6M word window and banks 1, 2, and 3 occupy a 8M word window in the processor's address space but, if not fully populated, these windows are not made contiguous by the memory controller logic.

#### SDRAM Controller

The SDRAM controller provides an interface of up to four separate banks of industry-standard SDRAM devices at speeds up to $f_{SDCLK}$. Fully compliant with the SDRAM standard, each bank has its own memory select line ($\overline{MS0}$–$\overline{MS3}$), and can be configured to contain between 4M bytes and 256M bytes of memory. SDRAM external memory address space is shown in Table 6. NOTE: this feature is not available on the ADSP-21486 model.

**Table 6. External Memory for SDRAM Addresses**

| Bank | Size in Words | Address Range |
|---|---|---|
| Bank 0 | 62M | 0x0020 0000–0x03FF FFFF |
| Bank 1 | 64M | 0x0400 0000–0x07FF FFFF |
| Bank 2 | 64M | 0x0800 0000–0x0BFF FFFF |
| Bank 3 | 64M | 0x0C00 0000–0x0FFF FFFF |

A set of programmable timing parameters is available to configure the SDRAM banks to support slower memory devices. Note that 32-bit wide devices are not supported on the SDRAM and AMI interfaces.

The SDRAM controller address, data, clock, and control pins can drive loads up to distributed 30 pF. For larger memory systems, the SDRAM controller external buffer timing should be selected and external buffering should be provided so that the load on the SDRAM controller pins does not exceed 30 pF.

Note that the external memory bank addresses shown are for normal-word (32-bit) accesses. If 48-bit instructions as well as 32-bit data are both placed in the same external memory bank, care must be taken while mapping them to avoid overlap.

#### SIMD Access to External Memory

The SDRAM controller on the processor supports SIMD access on the 64-bit EPD (external port data bus) which allows access to the complementary registers on the PEy unit in the normal word space (NW). This removes the need to explicitly access the complimentary registers when the data is in external SDRAM memory.

#### VISA and ISA Access to External Memory

The SDRAM controller on the ADSP-2148x processors supports VISA code operation which reduces the memory load since the VISA instructions are compressed. Moreover, bus fetching is reduced because, in the best case, one 48-bit fetch contains three valid instructions. Code execution from the traditional ISA operation is also supported. Note that code execution is only supported from bank 0 regardless of VISA/ISA. Table 7 shows the address ranges for instruction fetch in each mode.

**Table 7. External Bank 0 Instruction Fetch**

| Access Type | Size in Words | Address Range |
|---|---|---|
| ISA (NW) | 4M | 0x0020 0000–0x005F FFFF |
| VISA (SW) | 10M | 0x0060 0000–0x00FF FFFF |

### *Pulse-Width Modulation*

The PWM module is a flexible, programmable, PWM waveform generator that can be programmed to generate the required switching patterns for various applications related to motor and engine control or audio power control. The PWM generator can generate either center-aligned or edge-aligned PWM waveforms. In addition, it can generate complementary signals on two outputs in paired mode or independent signals in non-paired mode (applicable to a single group of four PWM waveforms).

The entire PWM module has four groups of four PWM outputs generating 16 PWM outputs in total. Each PWM group produces two pairs of PWM signals on the four PWM outputs.

The PWM generator is capable of operating in two distinct modes while generating center-aligned PWM waveforms: single-update mode or double-update mode. In single-update mode the duty cycle values are programmable only once per PWM period. This results in PWM patterns that are symmetrical about the midpoint of the PWM period. In double-update mode, a second updating of the PWM registers is implemented at the midpoint of the PWM period. In this mode, it is possible to produce asymmetrical PWM patterns that produce lower harmonic distortion in three-phase PWM inverters.

PWM signals can be mapped to the external port address lines or to the DPI pins.

### *MediaLB*

The automotive models of the ADSP-2148x processors have an MLB interface which allows the processor to function as a media local bus device. It includes support for both 3-pin as well as 5-pin media local bus protocols. It supports speeds up to 1024 FS (49.25 Mbits/sec, FS = 48.1 kHz) and up to 31 logical channels, with up to 124 bytes of data per media local bus frame. For a list of automotive models, see Automotive Products on Page 66.

### *Digital Applications Interface (DAI)*

The digital applications interface (DAI) allows the connection of various peripherals to any of the DAI pins (DAI_P20–1). Programs make these connections using the signal routing unit (SRU).

The SRU is a matrix routing unit (or group of multiplexers) that enables the peripherals provided by the DAI to be interconnected under software control. This allows easy use of the DAI associated peripherals for a much wider variety of applications by using a larger set of algorithms than is possible with nonconfigurable signal paths.

The DAI includes eight serial ports, four precision clock generators (PCG), a S/PDIF transceiver, four ASRCs, and an input data port (IDP). The IDP provides an additional input path to the SHARC core, configurable as either eight channels of serial data, or a single 20-bit wide synchronous parallel data acquisition port. Each data channel has its own DMA channel that is independent from the processor's serial ports.

#### Serial Ports (SPORTs)

The ADSP-2148x features eight synchronous serial ports that provide an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices such as Analog Devices' AD183x family of audio codecs, ADCs, and DACs. The serial ports are made up of two data lines, a clock, and frame sync. The data lines can be programmed to either transmit or receive and each data line has a dedicated DMA channel.

Serial ports can support up to 16 transmit or 16 receive DMA channels of audio data when all eight SPORTs are enabled, or four full duplex TDM streams of 128 channels per frame.

Serial port data can be automatically transferred to and from on-chip memory/external memory via dedicated DMA channels. Each of the serial ports can work in conjunction with another serial port to provide TDM support. One SPORT provides two transmit signals while the other SPORT provides the two receive signals. The frame sync and clock are shared.

Serial ports operate in five modes:

- Standard serial mode
- Multichannel (TDM) mode
- $I^2S$ mode
- Packed $I^2S$ mode
- Left-justified mode

#### S/PDIF-Compatible Digital Audio Receiver/Transmitter

The S/PDIF receiver/transmitter has no separate DMA channels. It receives audio data in serial format and converts it into a biphase encoded signal. The serial data input to the receiver/transmitter can be formatted as left-justified, $I^2S$ or right-justified with word widths of 16, 18, 20, or 24 bits.

The serial data, clock, and frame sync inputs to the S/PDIF receiver/transmitter are routed through the signal routing unit (SRU). They can come from a variety of sources, such as the SPORTs, external pins, or the precision clock generators (PCGs), and are controlled by the SRU control registers.

#### Asynchronous Sample Rate Converter (SRC)

The asynchronous sample rate converter contains four SRC blocks and is the same core as that used in the AD1896 192 kHz stereo asynchronous sample rate converter and provides up to 128 dB SNR. The SRC block is used to perform synchronous or asynchronous sample rate conversion across independent stereo channels, without using internal processor resources. The four SRC blocks can also be configured to operate together to convert multichannel audio data without phase mismatches. Finally, the SRC can be used to clean up audio data from jittery clock sources such as the S/PDIF receiver.

#### Input Data Port

The IDP provides up to eight serial input channels—each with its own clock, frame sync, and data inputs. The eight channels are automatically multiplexed into a single 32-bit by eight-deep FIFO. Data is always formatted as a 64-bit frame and divided into two 32-bit words. The serial protocol is designed to receive audio channels in $I^2S$, left-justified sample pair, or right-justified mode.

The IDP also provides a parallel data acquisition port (PDAP), which can be used for receiving parallel data. The PDAP port has a clock input and a hold input. The data for the PDAP can be received from DAI pins or from the external port pins. The PDAP supports a maximum of 20-bit data and four different packing modes to receive the incoming data.

#### Precision Clock Generators

The precision clock generators (PCG) consist of four units, each of which generates a pair of signals (clock and frame sync) derived from a clock input signal. The units, A B, C, and D, are identical in functionality and operate independently of each other. The two signals generated by each unit are normally used as a serial bit clock/frame sync pair.

The outputs of PCG A and B can be routed through the DAI pins and the outputs of PCG C and D can be driven on to the DAI as well as the DPI pins.

### *Digital Peripheral Interface (DPI)*

The ADSP-2148x SHARC processors have a digital peripheral interface that provides connections to two serial peripheral interface ports (SPI), one universal asynchronous receiver-transmitter (UART), 12 flags, a 2-wire interface (TWI), three PWM modules (PWM3–1), and two general-purpose timers.

#### Serial Peripheral (Compatible) Interface (SPI)

The SPI is an industry-standard synchronous serial link, enabling the SPI-compatible port to communicate with other SPI compatible devices. The SPI consists of two data pins, one device select pin, and one clock pin. It is a full-duplex synchronous serial interface, supporting both master and slave modes. The SPI port can operate in a multimaster environment by interfacing with up to four other SPI-compatible devices, either acting as a master or slave device. The SPI-compatible peripheral implementation also features programmable baud rate and clock phase and polarities. The SPI-compatible port uses open drain drivers to support a multimaster configuration and to avoid data contention.

#### UART Port

The processors provide a full-duplex Universal Asynchronous Receiver/Transmitter (UART) port, which is fully compatible with PC-standard UARTs. The UART port provides a simplified UART interface to other peripherals or hosts, supporting full-duplex, DMA-supported, asynchronous transfers of serial data. The UART also has multiprocessor communication capability using 9-bit address detection. This allows it to be used in multidrop networks through the RS-485 data interface standard. The UART port also includes support for 5 to 8 data bits, 1 or 2 stop bits, and none, even, or odd parity. The UART port supports two modes of operation:

- PIO (programmed I/O)—The processor sends or receives data by writing or reading I/O-mapped UART registers. The data is double-buffered on both transmit and receive.
- DMA (direct memory access)—The DMA controller transfers both transmit and receive data. This reduces the number and frequency of interrupts required to transfer data to and from memory. The UART has two dedicated DMA channels, one for transmit and one for receive. These DMA channels have lower default priority than most DMA channels because of their relatively low service rates.

#### Timers

The ADSP-2148x has a total of three timers: a core timer that can generate periodic software interrupts and two general-purpose timers that can generate periodic interrupts and be independently set to operate in one of three modes:

- Pulse waveform generation mode
- Pulse width count/capture mode
- External event watchdog mode

The core timer can be configured to use FLAG3 as a timer expired signal, and the general-purpose timers have one bidirectional pin and four registers that implement its mode of operation: a 6-bit configuration register, a 32-bit count register, a 32-bit period register, and a 32-bit pulse width register. A single control and status register enables or disables the general-purpose timer.

#### 2-Wire Interface Port (TWI)

The TWI is a bidirectional 2-wire, serial bus used to move 8-bit data while maintaining compliance with the $I^2C$ bus protocol. The TWI master incorporates the following features:

- 7-bit addressing
- Simultaneous master and slave operation on multiple device systems with support for multi master data arbitration
- Digital filtering and timed event processing
- 100 kbps and 400 kbps data rates
- Low interrupt rate

## I/O PROCESSOR FEATURES

The I/O processors provide up to 65 channels of DMA, as well as an extensive set of peripherals.

### *DMA Controller*

The processor's on-chip DMA controller allows data transfers without processor intervention. The DMA controller operates independently and invisibly to the processor core, allowing DMA operations to occur while the core is simultaneously executing its program instructions. DMA transfers can occur between the ADSP-2148x's internal memory and its serial ports, the SPI-compatible (serial peripheral interface) ports, the IDP (input data port), the PDAP, or the UART. The DMA channel summary is shown in Table 8.

Programs can be downloaded to the ADSP-2148x using DMA transfers. Other DMA features include interrupt generation upon completion of DMA transfers and DMA chaining for automatic linked DMA transfers.

**Table 8. DMA Channels**

| Peripheral | DMA Channels |
|---|---|
| SPORTs | 16 |
| IDP/PDAP | 8 |
| SPI | 2 |
| UART | 2 |
| External Port | 2 |
| Accelerators | 2 |
| Memory-to-Memory | 2 |
| MLB[1] | 31 |

[1] Automotive models only.

**Delay Line DMA**

The processor provides delay line DMA functionality. This allows processor reads and writes to external delay line buffers (and hence to external memory) with limited core interaction.

**Scatter/Gather DMA**

The processor provides scatter/gather DMA functionality. This allows processor DMA reads/writes to/from non contiguous memory blocks.

### *FFT Accelerator*

The FFT accelerator implements a radix-2 complex/real input, complex output FFT with no core intervention. The FFT accelerator runs at the peripheral clock frequency.

### *FIR Accelerator*

The FIR (finite impulse response) accelerator consists of a 1024 word coefficient memory, a 1024 word deep delay line for the data, and four MAC units. A controller manages the accelerator. The FIR accelerator runs at the peripheral clock frequency.

### *IIR Accelerator*

The IIR (infinite impulse response) accelerator consists of a 1440 word coefficient memory for storage of biquad coefficients, a data memory for storing the intermediate data, and one MAC unit. A controller manages the accelerator. The IIR accelerator runs at the peripheral clock frequency.

### *Watchdog Timer*

The watchdog timer is used to supervise the stability of the system software. When used in this way, software reloads the watchdog timer in a regular manner so that the downward counting timer never expires. An expiring timer then indicates that system software might be out of control.

The 32-bit watchdog timer that can be used to implement a software watchdog function. A software watchdog can improve system reliability by forcing the processor to a known state through generation of a system reset, if the timer expires before being reloaded by software. Software initializes the count value of the timer, and then enables the timer. The watchdog timer resets both the core and the internal peripherals. Note that this feature is available on the 176-lead package only.

## SYSTEM DESIGN

The following sections provide an introduction to system design options and power supply issues.

### *Program Booting*

The internal memory of the ADSP-2148x boots at system power-up from an 8-bit EPROM via the external port, an SPI master, or an SPI slave. Booting is determined by the boot configuration (BOOT_CFG2–0) pins in Table 9 for the 176-lead package and Table 10 for the 100-lead package.

**Table 9. Boot Mode Selection, 176-Lead Package**

| BOOT_CFG2–0 | Booting Mode |
|---|---|
| 000 | SPI Slave Boot |
| 001 | SPI Master Boot |
| 010 | AMI User Boot (for 8-bit Flash Boot) |
| 011 | No boot (processor executes from internal ROM after reset) |
| 1xx | Reserved |

**Table 10. Boot Mode Selection, 100-Lead Package**

| BOOT_CFG1–0 | Booting Mode |
|---|---|
| 00 | SPI Slave Boot |
| 01 | SPI Master Boot |
| 10 | Reserved |
| 11 | No boot (processor executes from internal ROM after reset) |

The "Running Reset" feature allows a user to perform a reset of the processor core and peripherals, but without resetting the PLL and SDRAM controller, or performing a boot. The functionality of the RESETOUT/RUNRSTIN pin has now been extended to also act as the input for initiating a Running Reset. For more information, see the *ADSP-214xx SHARC Processor Hardware Reference*.

### *Power Supplies*

The processors have separate power supply connections for the internal ($V_{DD_INT}$) and external ($V_{DD_EXT}$) power supplies. The internal supply must meet the $V_{DD_INT}$ specifications. The external supply must meet the $V_{DD_EXT}$ specification. All external supply pins must be connected to the same power supply.

To reduce noise coupling, the PCB should use a parallel pair of power and ground planes for $V_{DD_INT}$ and GND.

### *Static Voltage Scaling (SVS)*

Some models of the ADSP-2148x feature Static Voltage Scaling (SVS) on the $V_{DD_INT}$ power supply. (See the Ordering Guide on Page 66 for model details.) This voltage specification technique can provide significant performance benefits including 450 MHz core frequency operation without a significant increase in power.

SVS optimizes the required $V_{DD_INT}$ voltage for each individual device to enable enhanced operating frequency up to 450 MHz. The optimized SVS voltage results in a reduction of maximum $I_{DD_INT}$ which enables 450 MHz operation at the same or lower maximum power than 400 MHz operation at a fixed voltage supply. Implementation of SVS requires a specific voltage regulator circuit design and initialization code.

Refer to the Engineer-to-Engineer Note *"Static Voltage Scaling for ADSP-2148x Processors"* (EE-357) for further information. The EE-Note details the requirements and process to implement a SVS power supply system to enable operation up to 450 MHz. This applies only to specific products within the ADSP-2148x family which are capable of supporting 450 MHz operation.

Details on power consumption and Static and Dynamic current consumption can be found at Total Power Dissipation on Page 20. Also see Operating Conditions on Page 18 for more information.

The following are SVS features.

- SVS is applicable only to 450 MHz models (not applicable to 400 MHz or lower frequency models).
- Each individual SVS device includes a register (SVS_DAT) containing the unique SVS voltage set at the factory, known as $SVS_{NOM}$.
- The $SVS_{NOM}$ value is the intended set voltage for the $V_{DD_INT}$ voltage regulator.
- No dedicated pins are required for SVS. The TWI serial bus is used to communicate $SVS_{NOM}$ to the voltage regulator.
- Analog Devices recommends a specific voltage regulator design and initialization code sequence that optimizes the power-up sequence.

  The Engineer-to-Engineer Note *"Static Voltage Scaling for ADSP-2148x Processors"* (EE-357) contains the details of the regulator design and the initialization requirements.
- Any differences from the Analog Devices recommended programmable regulator design must be reviewed by Analog Devices to ensure that it meets the voltage accuracy and range requirements.

### Target Board JTAG Emulator Connector

Analog Devices DSP Tools product line of JTAG emulators uses the IEEE 1149.1 JTAG test access port of the ADSP-2148x processors to monitor and control the target board processor during emulation. Analog Devices DSP Tools product line of JTAG emulators provides emulation at full processor speed, allowing inspection and modification of memory, registers, and processor stacks. The processor's JTAG interface ensures that the emulator will not affect target system loading or timing.

For complete information on Analog Devices' SHARC DSP Tools product line of JTAG emulator operation, see the appropriate emulator hardware user's guide.

## DEVELOPMENT TOOLS

Analog Devices supports its processors with a complete line of software and hardware development tools, including integrated development environments (which include CrossCore® Embedded Studio and/or VisualDSP++®), evaluation products, emulators, and a wide variety of software add-ins.

### Integrated Development Environments (IDEs)

For C/C++ software writing and editing, code generation, and debug support, Analog Devices offers two IDEs.

The newest IDE, CrossCore Embedded Studio, is based on the Eclipse™ framework. Supporting most Analog Devices processor families, it is the IDE of choice for future processors, including multicore devices. CrossCore Embedded Studio seamlessly integrates available software add-ins to support real time operating systems, file systems, TCP/IP stacks, USB stacks, algorithmic software modules, and evaluation hardware board support packages. For more information visit www.analog.com/cces.

The other Analog Devices IDE, VisualDSP++, supports processor families introduced prior to the release of CrossCore Embedded Studio. This IDE includes the Analog Devices VDK real time operating system and an open source TCP/IP stack. For more information visit www.analog.com/visualdsp. Note that VisualDSP++ will not support future Analog Devices processors.

### EZ-KIT Lite Evaluation Board

For processor evaluation, Analog Devices provides wide range of EZ-KIT Lite® evaluation boards. Including the processor and key peripherals, the evaluation board also supports on-chip emulation capabilities and other evaluation and development features. Also available are various EZ-Extenders®, which are daughter cards delivering additional specialized functionality, including audio and video processing. For more information visit www.analog.com and search on "ezkit" or "ezextender".

### EZ-KIT Lite Evaluation Kits

For a cost-effective way to learn more about developing with Analog Devices processors, Analog Devices offer a range of EZ-KIT Lite evaluation kits. Each evaluation kit includes an EZ-KIT Lite evaluation board, directions for downloading an evaluation version of the available IDE(s), a USB cable, and a power supply. The USB controller on the EZ-KIT Lite board connects to the USB port of the user's PC, enabling the chosen IDE evaluation suite to emulate the on-board processor in-circuit. This permits the customer to download, execute, and debug programs for the EZ-KIT Lite system. It also supports in-circuit programming of the on-board Flash device to store user-specific boot code, enabling standalone operation. With the full version of CrossCore Embedded Studio or VisualDSP++ installed (sold separately), engineers can develop software for supported EZ-KITs or any custom system utilizing supported Analog Devices processors.

### Software Add-Ins for CrossCore Embedded Studio

Analog Devices offers software add-ins which seamlessly integrate with CrossCore Embedded Studio to extend its capabilities and reduce development time. Add-ins include board support packages for evaluation hardware, various middleware packages, and algorithmic modules. Documentation, help, configuration dialogs, and coding examples present in these add-ins are viewable through the CrossCore Embedded Studio IDE once the add-in is installed.

### Board Support Packages for Evaluation Hardware

Software support for the EZ-KIT Lite evaluation boards and EZ-Extender daughter cards is provided by software add-ins called Board Support Packages (BSPs). The BSPs contain the required drivers, pertinent release notes, and select example code for the given evaluation hardware. A download link for a specific BSP is located on the web page for the associated EZ-KIT or EZ-Extender product. The link is found in the *Product Download* area of the product web page.

### *Middleware Packages*

Analog Devices separately offers middleware add-ins such as real time operating systems, file systems, USB stacks, and TCP/IP stacks. For more information see the following web pages:

- www.analog.com/ucos3
- www.analog.com/ucfs
- www.analog.com/ucusbd
- www.analog.com/lwip

### *Algorithmic Modules*

To speed development, Analog Devices offers add-ins that perform popular audio and video processing algorithms. These are available for use with both CrossCore Embedded Studio and VisualDSP++. For more information visit www.analog.com and search on "Blackfin software modules" or "SHARC software modules".

### *Designing an Emulator-Compatible DSP Board (Target)*

For embedded system test and debug, Analog Devices provides a family of emulators. On each JTAG DSP, Analog Devices supplies an IEEE 1149.1 JTAG Test Access Port (TAP). In-circuit emulation is facilitated by use of this JTAG interface. The emulator accesses the processor's internal features via the processor's TAP, allowing the developer to load code, set breakpoints, and view variables, memory, and registers. The processor must be halted to send data and commands, but once an operation is completed by the emulator, the DSP system is set to run at full speed with no impact on system timing. The emulators require the target board to include a header that supports connection of the DSP's JTAG port to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see the Engineer-to-Engineer Note *"Analog Devices JTAG Emulation Technical Reference"* (EE-68) on the Analog Devices website (www.analog.com)—use site search on "EE-68." This document is updated regularly to keep pace with improvements to emulator support.

## ADDITIONAL INFORMATION

This data sheet provides a general overview of the ADSP-2148x architecture and functionality. For detailed information on the ADSP-2148x family core architecture and instruction set, refer to the *SHARC Processor Programming Reference*.

## RELATED SIGNAL CHAINS

A *signal chain* is a series of signal-conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next. Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena. For more information about this term and related topics, see the "signal chain" entry in the Glossary of EE Terms on the Analog Devices website.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together well. A tool for viewing relationships between specific applications and related components is available on the www.analog.com website.

The Circuits from the Lab™ site (www.analog.com/circuits) provides:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

# PIN FUNCTION DESCRIPTIONS

**Table 11. Pin Descriptions**

| Name | Type | State During/ After Reset | Description |
|---|---|---|---|
| $ADDR_{23-0}$ | I/O/T (ipu) | High-Z/ driven low (boot) | **External Address.** The processor outputs addresses for external memory and peripherals on these pins. The ADDR pins can be multiplexed to support the external memory interface address, and FLAGS15–8 (I/O) and PWM (O). After reset, all ADDR pins are in external memory interface mode and FLAG(0–3) pins are in FLAGS mode (default). When configured in the IDP_PDAP_CTL register, IDP channel 0 scans the $ADDR_{23-4}$ pins for parallel input data. |
| $DATA_{15-0}$ | I/O/T (ipu) | High-Z | **External Data.** The data pins can be multiplexed to support the external memory interface data (I/O), and $FLAGS_{7-0}$ (I/O). |
| AMI_ACK | I (ipu) | | **Memory Acknowledge.** External devices can deassert AMI_ACK (low) to add wait states to an external memory access. AMI_ACK is used by I/O devices, memory controllers, or other peripherals to hold off completion of an external memory access. |
| $\overline{MS}_{0-1}$ | O/T (ipu) | High-Z | **Memory Select Lines 0–1.** These lines are asserted (low) as chip selects for the corresponding banks of external memory. The $\overline{MS}_{1-0}$ lines are decoded memory address lines that change at the same time as the other address lines. When no external memory access is occurring the $\overline{MS}_{1-0}$ lines are inactive; they are active however when a conditional memory access instruction is executed, when the condition evaluates as true. The $\overline{MS1}$ pin can be used in EPORT/FLASH boot mode. For more information, see the *ADSP-214xx SHARC Processor Hardware Reference*. |
| $\overline{AMI_RD}$ | O/T (ipu) | High-Z | **AMI Port Read Enable.** $\overline{AMI_RD}$ is asserted whenever the processor reads a word from external memory. |
| $\overline{AMI_WR}$ | O/T (ipu) | High-Z | **AMI Port Write Enable.** $\overline{AMI_WR}$ is asserted when the processor writes a word to external memory. |
| FLAG0/$\overline{IRQ0}$ | I/O (ipu) | FLAG[0] INPUT | **FLAG0/Interrupt Request0.** |
| FLAG1/$\overline{IRQ1}$ | I/O (ipu) | FLAG[1] INPUT | **FLAG1/Interrupt Request1.** |
| FLAG2/$\overline{IRQ2}$/$\overline{MS2}$ | I/O (ipu) | FLAG[2] INPUT | **FLAG2/Interrupt Request2/Memory Select2.** |
| FLAG3/TMREXP/$\overline{MS3}$ | I/O (ipu) | FLAG[3] INPUT | **FLAG3/Timer Expired/Memory Select3.** |

The following symbols appear in the Type column of this table: **A** = asynchronous, **I** = input, **O** = output, **S** = synchronous, **A/D** = active drive, **O/D** = open drain, and **T** = three-state, **ipd** = internal pull-down resistor, **ipu** = internal pull-up resistor.
The internal pull-up (ipu) and internal pull-down (ipd) resistors are designed to hold the internal path from the pins at the expected logic levels. To pull-up or pull-down the external pads to the expected logic levels, use external resistors. Internal pull-up/pull-down resistors cannot be enabled/disabled and the value of these resistors cannot be programmed. The range of an ipu resistor can be between 26 kΩ–63 kΩ. The range of an ipd resistor can be between 31 kΩ–85kΩ. The three-state voltage of ipu pads will not reach to the full $V_{DD_EXT}$ level; at typical conditions the voltage is in the range of 2.3 V to 2.7 V.
In this table, all pins are LVTTL compliant with the exception of the thermal diode pins.

**Table 11. Pin Descriptions (Continued)**

| Name | Type | State During/ After Reset | Description |
|---|---|---|---|
| $\overline{\text{SDRAS}}$ | O/T (ipu) | High-Z/ driven high | **SDRAM Row Address Strobe.** Connect to SDRAM's RAS pin. In conjunction with other SDRAM command pins, defines the operation for the SDRAM to perform. |
| $\overline{\text{SDCAS}}$ | O/T (ipu) | High-Z/ driven high | **SDRAM Column Address Select.** Connect to SDRAM's CAS pin. In conjunction with other SDRAM command pins, defines the operation for the SDRAM to perform. |
| $\overline{\text{SDWE}}$ | O/T (ipu) | High-Z/ driven high | **SDRAM Write Enable.** Connect to SDRAM's WE or W buffer pin. In conjunction with other SDRAM command pins, defines the operation for the SDRAM to perform. |
| SDCKE | O/T (ipu) | High-Z/ driven high | **SDRAM Clock Enable.** Connect to SDRAM's CKE pin. Enables and disables the CLK signal. For details, see the data sheet supplied with the SDRAM device. |
| SDA10 | O/T (ipu) | High-Z/ driven high | **SDRAM A10 Pin.** Enables applications to refresh an SDRAM in parallel with non-SDRAM accesses. This pin replaces the DSP's ADDR10 pin only during SDRAM accesses. |
| SDDQM | O/T (ipu) | High-Z/ driven high | **DQM Data Mask.** SDRAM Input mask signal for write accesses and output mask signal for read accesses. Input data is masked when DQM is sampled high during a write cycle. The SDRAM output buffers are placed in a High-Z state when DQM is sampled high during a read cycle. SDDQM is driven high from reset de-assertion until SDRAM initialization completes. Afterwards it is driven low irrespective of whether any SDRAM accesses occur or not. |
| SDCLK | O/T (ipd) | High-Z/ driving | **SDRAM Clock Output.** Clock driver for this pin differs from all other clock drivers. See Figure 41 on Page 55. For models in the 100-lead package, the SDRAM interface should be disabled to avoid unnecessary power switching by setting the DSDCTL bit in SDCTL register. For more information, see the *ADSP-214xx SHARC Processor Hardware Reference*. |
| DAI _$P_{20-1}$ | I/O/T (ipu) | High-Z | **Digital Applications Interface**. These pins provide the physical interface to the DAI SRU. The DAI SRU configuration registers define the combination of on-chip audio-centric peripheral inputs or outputs connected to the pin and to the pin's output enable. The configuration registers of these peripherals then determines the exact behavior of the pin. Any input or output signal present in the DAI SRU may be routed to any of these pins. |
| DPI _$P_{14-1}$ | I/O/T (ipu) | High-Z | **Digital Peripheral Interface.** These pins provide the physical interface to the DPI SRU. The DPI SRU configuration registers define the combination of on-chip peripheral inputs or outputs connected to the pin and to the pin's output enable. The configuration registers of these peripherals then determines the exact behavior of the pin. Any input or output signal present in the DPI SRU may be routed to any of these pins. |
| WDT_CLKIN | I | | **Watchdog Timer Clock Input.** This pin should be pulled low when not used. |
| WDT_CLKO | O | | **Watchdog Resonator Pad Output.** |
| $\overline{\text{WDTRSTO}}$ | O (ipu) | | **Watchdog Timer Reset Out.** |
| THD_P | I | | **Thermal Diode Anode.** When not used, this pin can be left floating. |
| THD_M | O | | **Thermal Diode Cathode.** When not used, this pin can be left floating. |

The following symbols appear in the Type column of this table: **A** = asynchronous, **I** = input, **O** = output, **S** = synchronous, **A/D** = active drive, **O/D** = open drain, and **T** = three-state, **ipd** = internal pull-down resistor, **ipu** = internal pull-up resistor.
The internal pull-up (ipu) and internal pull-down (ipd) resistors are designed to hold the internal path from the pins at the expected logic levels. To pull-up or pull-down the external pads to the expected logic levels, use external resistors. Internal pull-up/pull-down resistors cannot be enabled/disabled and the value of these resistors cannot be programmed. The range of an ipu resistor can be between 26 kΩ–63 kΩ. The range of an ipd resistor can be between 31 kΩ–85kΩ. The three-state voltage of ipu pads will not reach to the full $V_{DD_EXT}$ level; at typical conditions the voltage is in the range of 2.3 V to 2.7 V.
In this table, all pins are LVTTL compliant with the exception of the thermal diode pins.

**Table 11. Pin Descriptions (Continued)**

| Name | Type | State During/ After Reset | Description |
|---|---|---|---|
| MLBCLK[1] | I | | **Media Local Bus Clock.** This clock is generated by the MLB controller that is synchronized to the MOST network and provides the timing for the entire MLB interface at 49.152 MHz at FS=48 kHz. When the MLB controller is not used, this pin should be grounded. |
| MLBDAT[1] | I/O/T in 3 pin mode. I in 5 pin mode. | High-Z | **Media Local Bus Data.** The MLBDAT line is driven by the transmitting MLB device and is received by all other MLB devices including the MLB controller. The MLBDAT line carries the actual data. In 5-pin MLB mode, this pin is an input only. When the MLB controller is not used, this pin should be grounded. |
| MLBSIG[1] | I/O/T in 3 pin mode. I in 5 pin mode | High-Z | **Media Local Bus Signal.** This is a multiplexed signal which carries the Channel/Address generated by the MLB Controller, as well as the Command and RxStatus bytes from MLB devices. In 5-pin mode, this pin is input only. When the MLB controller is not used, this pin should be grounded. |
| MLBDO[1] | O/T | High-Z | **Media Local Bus Data Output (in 5 pin mode).** This pin is used only in 5-pin MLB mode. This serves as the output data pin in 5-pin mode. When the MLB controller is not used, this pin should be connected to ground. |
| MLBSO[1] | O/T | High-Z | **Media Local Bus Signal Output (in 5 pin mode).** This pin is used only in 5-pin MLB mode. This serves as the output signal pin in 5-pin mode. When the MLB controller is not used, this pin should be connected to ground. |
| TDI | I (ipu) | | **Test Data Input (JTAG).** Provides serial data for the boundary scan logic. |
| TDO | O/T | High-Z | **Test Data Output (JTAG).** Serial scan output of the boundary scan path. |
| TMS | I (ipu) | | **Test Mode Select (JTAG).** Used to control the test state machine. |
| TCK | I | | **Test Clock (JTAG).** Provides a clock for JTAG boundary scan. TCK must be asserted (pulsed low) after power-up or held low for proper operation of the device. |
| $\overline{\text{TRST}}$ | I (ipu) | | **Test Reset (JTAG).** Resets the test state machine. $\overline{\text{TRST}}$ must be asserted (pulsed low) after power-up or held low for proper operation of the processor. |
| $\overline{\text{EMU}}$ | O (O/D, ipu) | High-Z | **Emulation Status.** Must be connected to the ADSP-2148x Analog Devices DSP Tools product line of JTAG emulators target board connector only. |

The following symbols appear in the Type column of this table: **A** = asynchronous, **I** = input, **O** = output, **S** = synchronous, **A/D** = active drive, **O/D** = open drain, and **T** = three-state, **ipd** = internal pull-down resistor, **ipu** = internal pull-up resistor.
The internal pull-up (ipu) and internal pull-down (ipd) resistors are designed to hold the internal path from the pins at the expected logic levels. To pull-up or pull-down the external pads to the expected logic levels, use external resistors. Internal pull-up/pull-down resistors cannot be enabled/disabled and the value of these resistors cannot be programmed. The range of an ipu resistor can be between 26 kΩ–63 kΩ. The range of an ipd resistor can be between 31 kΩ–85kΩ. The three-state voltage of ipu pads will not reach to the full $V_{DD_EXT}$ level; at typical conditions the voltage is in the range of 2.3 V to 2.7 V.
In this table, all pins are LVTTL compliant with the exception of the thermal diode pins.

**Table 11. Pin Descriptions (Continued)**

| Name | Type | State During/ After Reset | Description |
|---|---|---|---|
| $CLK_CFG_{1-0}$ | I | | **Core to CLKIN Ratio Control.** These pins set the start up clock frequency. Note that the operating frequency can be changed by programming the PLL multiplier and divider in the PMCTL register at any time after the core comes out of reset. The allowed values are:<br>00 = 8:1<br>01 = 32:1<br>10 = 16:1<br>11 = reserved |
| CLKIN | I | | **Local Clock In.** Used in conjunction with XTAL. CLKIN is the clock input. It configures the processors to use either its internal clock generator or an external clock source. Connecting the necessary components to CLKIN and XTAL enables the internal clock generator. Connecting the external clock to CLKIN while leaving XTAL unconnected configures the processors to use the external clock source such as an external clock oscillator. CLKIN may not be halted, changed, or operated below the specified frequency. |
| XTAL | O | | **Crystal Oscillator Terminal.** Used in conjunction with CLKIN to drive an external crystal. |
| $\overline{\text{RESET}}$ | I | | **Processor Reset.** Resets the processor to a known state. Upon deassertion, there is a 4096 CLKIN cycle latency for the PLL to lock. After this time, the core begins program execution from the hardware reset vector address. The $\overline{\text{RESET}}$ input must be asserted (low) at power-up. |
| $\overline{\text{RESETOUT}}$/ $\overline{\text{RUNRSTIN}}$ | I/O (ipu) | | **Reset Out/Running Reset In.** The default setting on this pin is reset out. This pin also has a second function as RUNRSTIN which is enabled by setting bit 0 of the RUNRSTCTL register. For more information, see the *ADSP-214xx SHARC Processor Hardware Reference*. |
| $BOOT_CFG_{2-0}$ | I | | **Boot Configuration Select.** These pins select the boot mode for the processor (see Table 9). The BOOT_CFG pins must be valid before $\overline{\text{RESET}}$ (hardware and software) is asserted. |

The following symbols appear in the Type column of this table: **A** = asynchronous, **I** = input, **O** = output, **S** = synchronous, **A/D** = active drive, **O/D** = open drain, and **T** = three-state, **ipd** = internal pull-down resistor, **ipu** = internal pull-up resistor.
The internal pull-up (ipu) and internal pull-down (ipd) resistors are designed to hold the internal path from the pins at the expected logic levels. To pull-up or pull-down the external pads to the expected logic levels, use external resistors. Internal pull-up/pull-down resistors cannot be enabled/disabled and the value of these resistors cannot be programmed. The range of an ipu resistor can be between 26 kΩ–63 kΩ. The range of an ipd resistor can be between 31 kΩ–85kΩ. The three-state voltage of ipu pads will not reach to the full $V_{DD_EXT}$ level; at typical conditions the voltage is in the range of 2.3 V to 2.7 V.
In this table, all pins are LVTTL compliant with the exception of the thermal diode pins.

[1] The MLB pins are only available on the automotive models.

**Table 12. Pin List, Power and Ground**

| Name | Type | Description |
|---|---|---|
| $V_{DD_INT}$ | P | **Internal Power Supply** |
| $V_{DD_EXT}$ | P | **I/O Power Supply** |
| GND[1] | G | **Ground** |
| $V_{DD_THD}$ | P | **Thermal Diode Power Supply**. When not used, this pin can be left floating. |

[1] The exposed pad is required to be electrically and thermally connected to GND. Implement this by soldering the exposed pad to a GND PCB land that is the same size as the exposed pad. The GND PCB land should be *robustly* connected to the GND plane in the PCB for best electrical and thermal performance. No separate GND pins are provided in the package.

# SPECIFICATIONS

## OPERATING CONDITIONS

| Parameter[1] | Description | 300 MHz / 350 MHz / 400 MHz | | | 450 MHz | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Nom | Max | Min | Nom | Max | |
| $V_{DD_INT}$[2] | Internal (Core) Supply Voltage | 1.05 | 1.1 | 1.15 | $SVS_{NOM}$ – 25 mV | 1.0 – 1.15 | $SVS_{NOM}$ + 25 mV | V |
| $V_{DD_EXT}$ | External (I/O) Supply Voltage | 3.13 | | 3.47 | 3.13 | | 3.47 | V |
| $V_{DD_THD}$ | Thermal Diode Supply Voltage | 3.13 | | 3.47 | 3.13 | | 3.47 | V |
| $V_{IH}$[3] | High Level Input Voltage @ $V_{DD_EXT}$ = Max | 2.0 | | 3.6 | 2.0 | | 3.6 | V |
| $V_{IL}$[3] | Low Level Input Voltage @ $V_{DD_EXT}$ = Min | –0.3 | | 0.8 | –0.3 | | 0.8 | V |
| $V_{IH_CLKIN}$[4] | High Level Input Voltage @ $V_{DD_EXT}$ = Max | 2.2 | | $V_{DD_EXT}$ | 2.2 | | $V_{DD_EXT}$ | V |
| $V_{IL_CLKIN}$ | Low Level Input Voltage @ $V_{DD_EXT}$ = Min | –0.3 | | +0.8 | –0.3 | | +0.8 | V |
| $T_J$ | Junction Temperature 100-Lead LQFP_EP @ $T_{AMBIENT}$ 0°C to +70°C | 0 | | 110 | 0 | | 115 | °C |
| $T_J$ | Junction Temperature 100-Lead LQFP_EP @ $T_{AMBIENT}$ –40°C to +85°C | –40 | | 125 | NA | | NA | °C |
| $T_J$ | Junction Temperature 176-Lead LQFP_EP @ $T_{AMBIENT}$ 0°C to +70°C | 0 | | 110 | 0 | | 115 | °C |
| $T_J$ | Junction Temperature 176-Lead LQFP_EP @ $T_{AMBIENT}$ –40°C to +85°C | –40 | | 125 | NA | | NA | °C |

[1] Specifications subject to change without notice.

[2] $SVS_{NOM}$ refers to the nominal SVS voltage which is set between 1.0 V and 1.15 V at the factory for each individual device. Only the unique $SVS_{NOM}$ value in each chip may be used for 401 MHz to 450 MHz operation of that chip. This spec lists the possible range of the $SVS_{NOM}$ values for all devices. The initial VDD_INT voltage at power on is 1.1 V nominal and it transitions to SVS programmed voltage as outlined in Engineer-to-Engineer Note *"Static Voltage Scaling for ADSP-2148x Processors"* (EE-357).

[3] Applies to input and bidirectional pins: ADDR23–0, DATA15–0, FLAG3–0, DAI_Px, DPI_Px, BOOT_CFGx, CLK_CFGx, $\overline{\text{RUNRSTIN}}$, $\overline{\text{RESET}}$, TCK, TMS, TDI, $\overline{\text{TRST}}$, AMI_ACK, MLBCLK, MLBDAT, MLBSIG.

[4] Applies to input pins CLKIN, WDT_CLKIN.

## ELECTRICAL CHARACTERISTICS

| Parameter[1] | Description | Test Conditions | 300 MHz / 350 MHz / 400 MHz / 450 MHz Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{OH}$[2] | High Level Output Voltage | @ $V_{DD_EXT}$ = Min, $I_{OH}$ = –1.0 mA[3] | 2.4 | | | V |
| $V_{OL}$[2] | Low Level Output Voltage | @ $V_{DD_EXT}$ = Min, $I_{OL}$ = 1.0 mA[3] | | | 0.4 | V |
| $I_{IH}$[4, 5] | High Level Input Current | @ $V_{DD_EXT}$ = Max, $V_{IN}$ = $V_{DD_EXT}$ Max | | | 10 | µA |
| $I_{IL}$[4] | Low Level Input Current | @ $V_{DD_EXT}$ = Max, $V_{IN}$ = 0 V | | | 10 | µA |
| $I_{ILPU}$[5] | Low Level Input Current Pull-up | @ $V_{DD_EXT}$ = Max, $V_{IN}$ = 0 V | | | 200 | µA |
| $I_{OZH}$[6, 7] | Three-State Leakage Current | @ $V_{DD_EXT}$ = Max, $V_{IN}$ = $V_{DD_EXT}$ Max | | | 10 | µA |
| $I_{OZL}$[6] | Three-State Leakage Current | @ $V_{DD_EXT}$ = Max, $V_{IN}$ = 0 V | | | 10 | µA |
| $I_{OZLPU}$[7] | Three-State Leakage Current Pull-up | @ $V_{DD_EXT}$ = Max, $V_{IN}$ = 0 V | | | 200 | µA |
| $I_{OZHPD}$[8] | Three-State Leakage Current Pull-down | @ $V_{DD_EXT}$ = Max, $V_{IN}$ = $V_{DD_EXT}$ Max | | | 200 | µA |
| $I_{DD_INT}$[9] | Supply Current (Internal) | $f_{CCLK}$ > 0 MHz | | | Table 14 + Table 15 × ASF | mA |
| $I_{DD_INT}$ | Supply Current (Internal) | $V_{DDINT}$ = 1.1 V, ASF = 1, $T_J$ = 25°C | | 410 / 450 / 500 / 550 | | mA |
| $C_{IN}$[10, 11] | Input Capacitance | $T_{CASE}$ = 25°C | | | 5 | pF |

[1] Specifications subject to change without notice.
[2] Applies to output and bidirectional pins: ADDR23–0, DATA15–0, $\overline{AMI_RD}$, $\overline{AMI_WR}$, FLAG3–0, DAI_Px, DPI_Px, $\overline{EMU}$, TDO, $\overline{RESETOUT}$ MLBSIG, MLBDAT, MLBDO, MLBSO, $\overline{SDRAS}$, $\overline{SDCAS}$, $\overline{SDWE}$, SDCKE, SDA10, SDDQM, $\overline{MS0\text{-}1}$.
[3] See Output Drive Currents on Page 55 for typical drive current capabilities.
[4] Applies to input pins: BOOT_CFGx, CLK_CFGx, TCK, $\overline{RESET}$, CLKIN.
[5] Applies to input pins with internal pull-ups: $\overline{TRST}$, TMS, TDI.
[6] Applies to three-statable pin: TDO.
[7] Applies to three-statable pins with pull-ups: DAI_Px, DPI_Px, $\overline{EMU}$.
[8] Applies to three-statable pin with pull-down: SDCLK.
[9] See Engineer-to-Engineer Note *"Estimating Power Dissipation for ADSP-214xx SHARC Processors"* (EE-348) for further information.
[10] Applies to all signal pins.
[11] Guaranteed, but not tested.

### *Total Power Dissipation*

The information in this section should be augmented with the Engineer-to-Engineer Note *"Estimating Power for ADSP-214xx SHARC Processors"* (EE-348).

Total power dissipation has two components:

1. Internal power consumption is additionally comprised of two components:
   - Static current due to leakage. Table 14 shows the static current consumption ($I_{DD_INT_STATIC}$) as a function of junction temperature ($T_J$) and core voltage ($V_{DD_INT}$).
   - Dynamic current ($I_{DD_INT_DYNAMIC}$), due to transistor switching characteristics and activity level of the processor. The activity level is reflected by the Activity Scaling Factor (ASF), which represents the activity level of the application code running on the processor core and having various levels of peripheral and external port activity (Table 13).

     Dynamic current consumption is calculated by selecting the ASF that corresponds most closely with the user application and then multiplying that with the dynamic current consumption (Table 15).
2. External power consumption is due to the switching activity of the external pins.

**Table 13. Activity Scaling Factors (ASF)[1]**

| Activity | Scaling Factor (ASF) |
|---|---|
| Idle | 0.29 |
| Low | 0.53 |
| Medium Low | 0.61 |
| Medium High | 0.77 |
| Peak Typical (50:50)[2] | 0.85 |
| Peak Typical (60:40)[2] | 0.93 |
| Peak Typical (70:30)[2] | 1.00 |
| High Typical | 1.16 |
| High | 1.25 |
| Peak | 1.31 |

[1] See the Engineer-to-Engineer Note *"Estimating Power for ADSP-214xx SHARC Processors"* (EE-348) for more information on the explanation of the power vectors specific to the ASF table.

[2] Ratio of continuous instruction loop (core) to SDRAM control code reads and writes.

**Table 14. Static Current—$I_{DD_INT_STATIC}$ (mA)[1]**

| | $V_{DD_INT}$ (V) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| $T_J$ (°C) | 0.975 V | 1.0 V | 1.025 V | 1.05 V | 1.075 V | 1.10 V | 1.125 V | 1.15 V | 1.175 V |
| –45 | 68 | 77 | 86 | 96 | 107 | 118 | 131 | 144 | 159 |
| –35 | 74 | 83 | 92 | 103 | 114 | 126 | 140 | 154 | 170 |
| –25 | 82 | 92 | 101 | 113 | 125 | 138 | 153 | 168 | 185 |
| –15 | 94 | 104 | 115 | 127 | 140 | 155 | 171 | 187 | 205 |
| –5 | 109 | 121 | 133 | 147 | 161 | 177 | 194 | 212 | 233 |
| +5 | 129 | 142 | 156 | 171 | 188 | 206 | 225 | 245 | 268 |
| +15 | 152 | 168 | 183 | 201 | 219 | 240 | 261 | 285 | 309 |
| +25 | 182 | 199 | 216 | 237 | 257 | 280 | 305 | 331 | 360 |
| +35 | 217 | 237 | 256 | 279 | 303 | 329 | 358 | 388 | 420 |
| +45 | 259 | 282 | 305 | 331 | 359 | 389 | 421 | 455 | 492 |
| +55 | 309 | 334 | 361 | 391 | 423 | 458 | 495 | 533 | 576 |
| +65 | 369 | 398 | 429 | 464 | 500 | 539 | 582 | 626 | 675 |
| +75 | 437 | 471 | 506 | 547 | 588 | 633 | 682 | 731 | 789 |
| +85 | 519 | 559 | 599 | 645 | 693 | 746 | 802 | 860 | 926 |
| +95 | 615 | 662 | 707 | 761 | 816 | 877 | 942 | 1007 | 1083 |
| +105 | 727 | 779 | 833 | 897 | 958 | 1026 | 1103 | 1179 | 1266 |
| +115 | 853 | 914 | 975 | 1047 | 1119 | 1198 | 1285 | 1372 | 1473 |
| +125 | 997 | 1067 | 1138 | 1219 | 1305 | 1397 | 1498 | 1601 | 1716 |

[1] Valid temperature and voltage ranges are model-specific. See Operating Conditions on Page 18.

**Table 15. Dynamic Current in CCLK Domain—$I_{DD_INT_DYNAMIC}$ (mA, with ASF = 1.0)[1, 2]**

| $f_{CCLK}$ (MHz) | $V_{DD_INT}$ (V) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | 0.975 V | 1.0 V | 1.025 V | 1.05 V | 1.075 V | 1.10 V | 1.125 V | 1.15 V | 1.175 V |
| 100 | 76 | 77 | 81 | 84 | 87 | 88 | 90 | 92 | 95 |
| 150 | 117 | 119 | 123 | 126 | 130 | 133 | 136 | 139 | 144 |
| 200 | 153 | 156 | 161 | 165 | 170 | 174 | 179 | 183 | 188 |
| 250 | 190 | 195 | 201 | 207 | 212 | 217 | 223 | 229 | 235 |
| 300 | 227 | 233 | 240 | 246 | 253 | 260 | 266 | 273 | 280 |
| 350 | 263 | 272 | 278 | 286 | 294 | 302 | 309 | 318 | 325 |
| 400 | 300 | 309 | 317 | 326 | 335 | 344 | 352 | 361 | 370 |
| 450 | 339 | 349 | 356 | 365 | 374 | 385 | 394 | 405 | 415 |

[1] The values are not guaranteed as standalone maximum specifications. They must be combined with static current per the equations of Electrical Characteristics on Page 19.
[2] Valid frequency and voltage ranges are model-specific. See Operating Conditions on Page 18.

## ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in Table 16 may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Table 16. Absolute Maximum Ratings**

| Parameter | Rating |
|---|---|
| Internal (Core) Supply Voltage ($V_{DD_INT}$) | –0.3 V to +1.32 V |
| External (I/O) Supply Voltage ($V_{DD_EXT}$) | –0.3 V to +3.6 V |
| Thermal Diode Supply Voltage ($V_{DD_THD}$) | –0.3 V to +3.6 V |
| Input Voltage | –0.5 V to +3.6 V |
| Output Voltage Swing | –0.5 V to $V_{DD_EXT}$ +0.5 V |
| Storage Temperature Range | –65°C to +150°C |
| Junction Temperature While Biased | 125°C |

## ESD SENSITIVITY

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## MAXIMUM POWER DISSIPATION

See Engineer-to-Engineer Note *"Estimating Power Dissipation for ADSP-214xx SHARC Processors"* (EE-348) for detailed thermal and power information regarding maximum power dissipation. For information on package thermal specifications, see Thermal Characteristics on Page 56.

## PACKAGE INFORMATION

The information presented in Figure 3 provides details about the package branding for the ADSP-2148x processors. For a complete listing of product availability, see Ordering Guide on Page 66.

*Figure 3. Typical Package Brand*

**Table 17. Package Brand Information[1]**

| Brand Key | Field Description |
|---|---|
| t | Temperature Range |
| pp | Package Type |
| Z | RoHS Compliant Option |
| cc | See Ordering Guide |
| vvvvvv.x | Assembly Lot Code |
| n.n | Silicon Revision |
| # | RoHS Compliant Designation |
| yyww | Date Code |

[1] Non automotive only. For branding information specific to automotive products, contact Analog Devices Inc.

## TIMING SPECIFICATIONS

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, it is not meaningful to add parameters to derive longer times. See Figure 43 on Page 55 for voltage reference levels.

*Switching Characteristics* specify how the processor changes its signals. Circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics describe what the processor will do in a given circumstance. Use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

*Timing Requirements* apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

### *Core Clock Requirements*

The processor's internal clock (a multiple of CLKIN) provides the clock signal for timing internal memory, the processor core, and the serial ports. During reset, program the ratio between the processor's internal clock frequency and external (CLKIN) clock frequency with the CLK_CFG1–0 pins.

The processor's internal clock switches at higher frequencies than the system input clock (CLKIN). To generate the internal clock, the processor uses an internal phase-locked loop (PLL, see Figure 4). This PLL-based clocking minimizes the skew between the system clock (CLKIN) signal and the processor's internal clock.

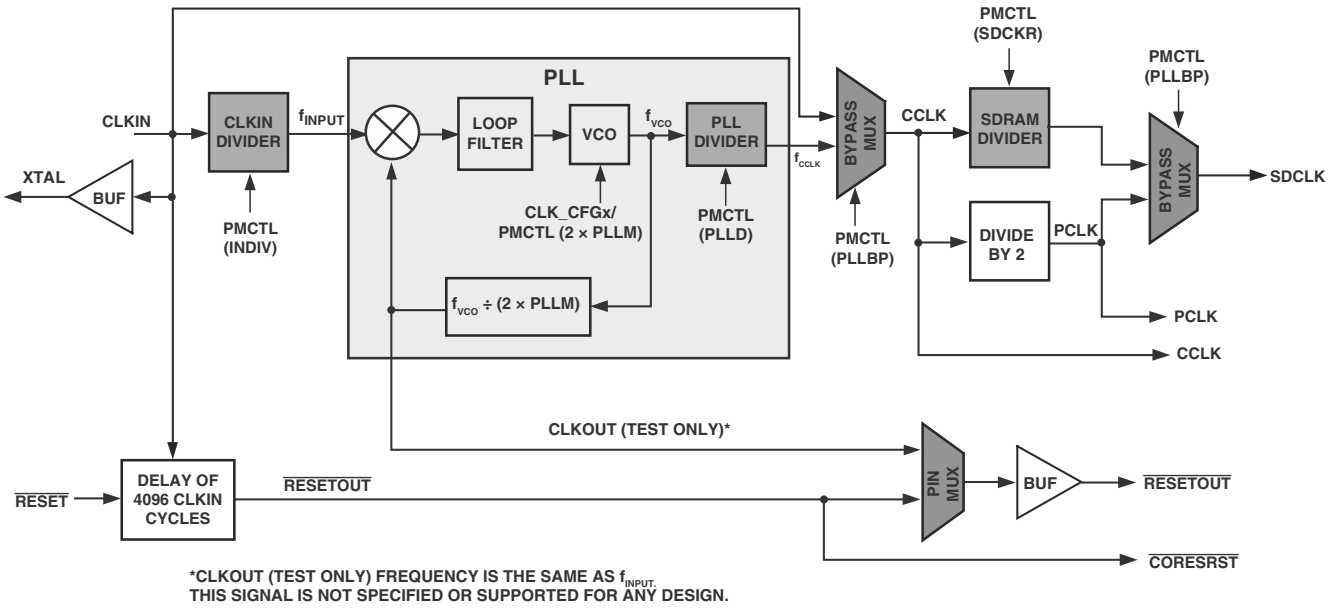


*Figure 4. Core Clock and System Clock Relationship to CLKIN*

#### Voltage Controlled Oscillator (VCO)

In application designs, the PLL multiplier value should be selected in such a way that the VCO frequency never exceeds $f_{VCO}$ specified in Table 20.

- The product of CLKIN and PLLM must never exceed 1/2 of $f_{VCO}$ (max) in Table 20 if the input divider is not enabled (INDIV = 0).
- The product of CLKIN and PLLM must never exceed $f_{VCO}$ (max) in Table 20 if the input divider is enabled (INDIV = 1).

The VCO frequency is calculated as follows:

$$f_{VCO} = 2 \times PLLM \times f_{INPUT}$$
$$f_{CCLK} = (2 \times PLLM \times f_{INPUT}) \div PLLD$$

where:

$f_{VCO}$ = VCO output

*PLLM* = Multiplier value programmed in the PMCTL register. During reset, the PLLM value is derived from the ratio selected using the CLK_CFG pins in hardware.

*PLLD* = 2, 4, 8, or 16 based on the divider value programmed on the PMCTL register. During reset this value is 2.

$f_{INPUT}$ = is the input frequency to the PLL.

$f_{INPUT}$ = CLKIN when the input divider is disabled or

$f_{INPUT}$ = CLKIN ÷ 2 when the input divider is enabled

Note the definitions of the clock periods that are a function of CLKIN and the appropriate ratio control shown in Table 18. All of the timing specifications for the ADSP-2148x peripherals are defined in relation to $t_{PCLK}$. See the peripheral specific section for each peripheral's timing information.

**Table 18. Clock Periods**

| Timing Requirements | Description |
|---|---|
| $t_{CK}$ | CLKIN Clock Period |
| $t_{CCLK}$ | Processor Core Clock Period |
| $t_{PCLK}$ | Peripheral Clock Period = 2 × $t_{CCLK}$ |
| $t_{SDCLK}$ | SDRAM Clock Period = ($t_{CCLK}$) × SDCKR |

Figure 4 shows core to CLKIN relationships with external oscillator or crystal. The shaded divider/multiplier blocks denote where clock ratios can be set through hardware or software using the power management control register (PMCTL). For more information, see the *ADSP-214xx SHARC Processor Hardware Reference*.

### *Power-Up Sequencing*

The timing requirements for processor startup are given in Table 19. While no specific power-up sequencing is required between $V_{DD_EXT}$ and $V_{DD_INT}$, there are some considerations that system designs should take into account.

- No power supply should be powered up for an extended period of time (> 200 ms) before another supply starts to ramp up.
- If the $V_{DD_INT}$ power supply comes up after $V_{DD_EXT}$, any pin, such as $\overline{\text{RESETOUT}}$ and $\overline{\text{RESET}}$, may actually drive momentarily until the $V_{DD_INT}$ rail has powered up. Systems sharing these signals on the board must determine if there are any issues that need to be addressed based on this behavior.

Note that during power-up, when the $V_{DD_INT}$ power supply comes up after $V_{DD_EXT}$, a leakage current of the order of three-state leakage current pull-up, pull-down may be observed on any pin, even if that is an input only (for example the $\overline{\text{RESET}}$ pin) until the $V_{DD_INT}$ rail has powered up.

**Table 19. Power Up Sequencing Timing Requirements (Processor Startup)**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Timing Requirements* | | | | |
| $t_{RSTVDD}$ | $\overline{\text{RESET}}$ Low Before $V_{DD_EXT}$ or $V_{DD_INT}$ On | 0 | | ms |
| $t_{IVDDEVDD}$ | $V_{DD_INT}$ On Before $V_{DD_EXT}$ | –200 | +200 | ms |
| $t_{CLKVDD}$[1] | CLKIN Valid After $V_{DD_INT}$ and $V_{DD_EXT}$ Valid | 0 | 200 | ms |
| $t_{CLKRST}$ | CLKIN Valid Before $\overline{\text{RESET}}$ Deasserted | 10[2] | | µs |
| $t_{PLLRST}$ | PLL Control Setup Before $\overline{\text{RESET}}$ Deasserted | 20[3] | | µs |
| *Switching Characteristic* | | | | |
| $t_{CORERST}$[4, 5] | Core Reset Deasserted After $\overline{\text{RESET}}$ Deasserted | 4096 × $t_{CK}$ + 2 × $t_{CCLK}$ | | |

[1] Valid $V_{DD_INT}$ and $V_{DD_EXT}$ assumes that the supplies are fully ramped to their nominal values (it does not matter which supply comes up first). Voltage ramp rates can vary from microseconds to hundreds of milliseconds depending on the design of the power supply subsystem.

[2] Assumes a stable CLKIN signal, after meeting worst-case startup timing of crystal oscillators. Refer to your crystal oscillator manufacturer's data sheet for startup time. Assume a 25 ms maximum oscillator startup time if using the XTAL pin and internal oscillator circuit in conjunction with an external crystal.

[3] Based on CLKIN cycles.

[4] Applies after the power-up sequence is complete. Subsequent resets require a minimum of four CLKIN cycles for $\overline{\text{RESET}}$ to be held low in order to properly initialize and propagate default states at all I/O pins.

[5] The 4096 cycle count depends on $t_{SRST}$ specification in Table 21. If setup time is not met, one additional CLKIN cycle may be added to the core reset time, resulting in 4097 cycles maximum.

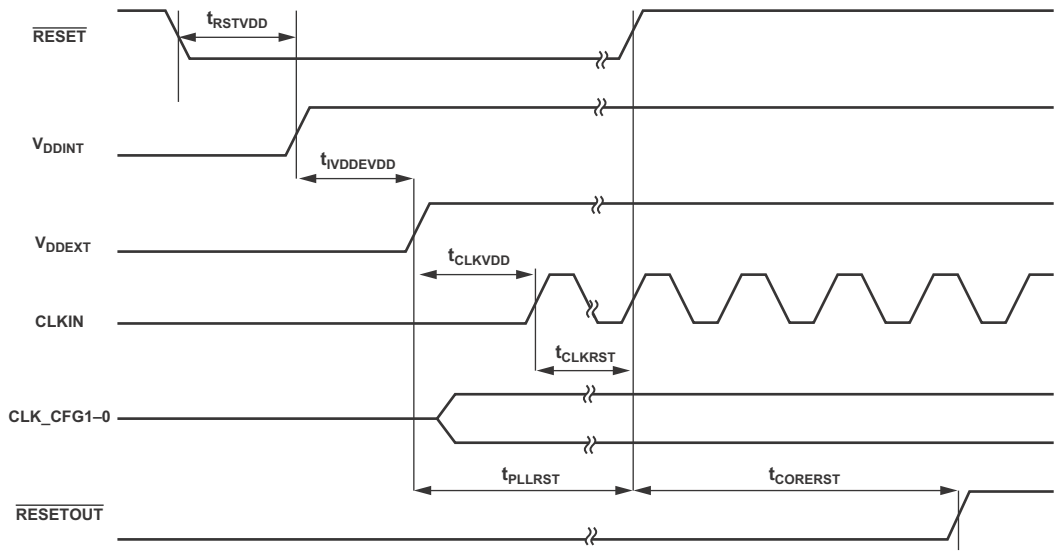


*Figure 5. Power-Up Sequencing*

### *Clock Input*

**Table 20. Clock Input**

| Parameter | | 300 MHz Min | 300 MHz Max | 350 MHz Min | 350 MHz Max | 400 MHz Min | 400 MHz Max | 450 MHz Min | 450 MHz Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| *Timing Requirements* | | | | | | | | | | |
| $t_{CK}$ | CLKIN Period | 26.66[1] | 100[2] | 22.8[1] | 100[2] | 20[1] | 100[2] | 17.75[1] | 100[2] | ns |
| $t_{CKL}$ | CLKIN Width Low | 13 | 45 | 11 | 45 | 10 | 45 | 8.875 | 45 | ns |
| $t_{CKH}$ | CLKIN Width High | 13 | 45 | 11 | 45 | 10 | 45 | 8.875 | 45 | ns |
| $t_{CKRF}$[3] | CLKIN Rise/Fall (0.4 V to 2.0 V) | | 3 | | 3 | | 3 | | 3 | ns |
| $t_{CCLK}$[4] | CCLK Period | 3.33 | 10 | 2.85 | 10 | 2.5 | 10 | 2.22 | 10 | ns |
| $f_{VCO}$[5] | VCO Frequency | 200 | 800 | 200 | 800 | 200 | 800 | 200 | 900 | MHz |
| $t_{CKJ}$[6, 7] | CLKIN Jitter Tolerance | –250 | +250 | –250 | +250 | –250 | +250 | –250 | +250 | ps |

[1] Applies only for CLK_CFG1–0 = 00 and default values for PLL control bits in PMCTL.
[2] Applies only for CLK_CFG1–0 = 01 and default values for PLL control bits in PMCTL.
[3] Guaranteed by simulation but not tested on silicon.
[4] Any changes to PLL control bits in the PMCTL register must meet core clock timing specification $t_{CCLK}$.
[5] See Figure 4 on Page 22 for VCO diagram.
[6] Actual input jitter should be combined with ac specifications for accurate timing analysis.
[7] Jitter specification is maximum peak-to-peak time interval error (TIE) jitter.

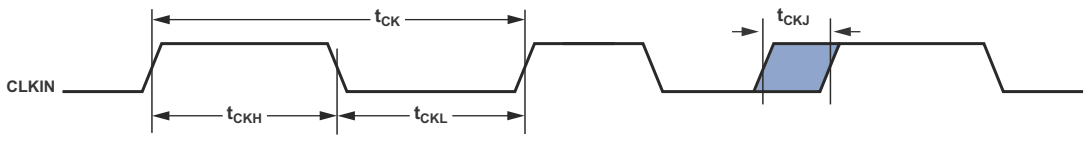


*Figure 6. Clock Input*

### *Clock Signals*

The ADSP-2148x can use an external clock or a crystal. See the CLKIN pin description in Table 11 on Page 14. Programs can configure the processor to use its internal clock generator by connecting the necessary components to CLKIN and XTAL. Figure 7 shows the component connections used for a crystal operating in fundamental mode. Note that the clock rate is achieved using a 25 MHz crystal and a PLL multiplier ratio 16:1 (CCLK:CLKIN achieves a clock speed of 400 MHz). To achieve the full core clock rate, programs need to configure the multiplier bits in the PMCTL register.

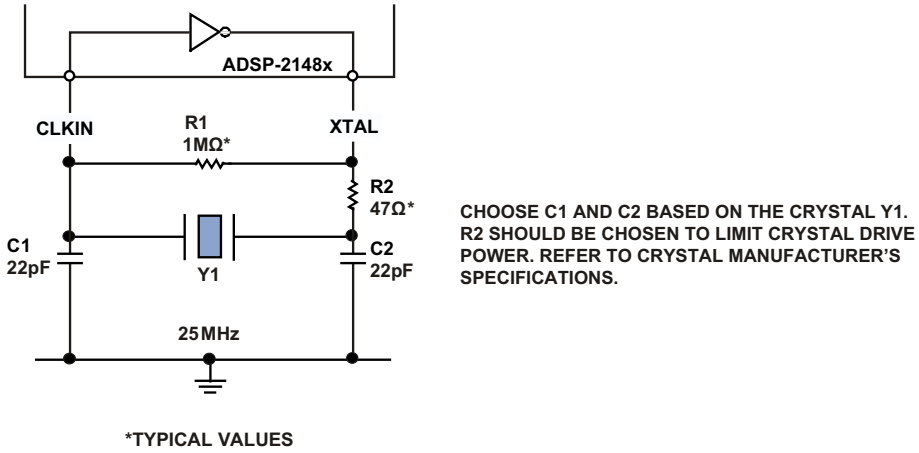


*Figure 7. Recommended Circuit for Fundamental Mode Crystal Operation*

### *Reset*

**Table 21. Reset**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Timing Requirements* | | | | |
| $t_{WRST}$[1] | $\overline{\text{RESET}}$ Pulse Width Low | $4 \times t_{CK}$ | | ns |
| $t_{SRST}$ | $\overline{\text{RESET}}$ Setup Before CLKIN Low | 8 | | ns |

[1] Applies after the power-up sequence is complete. At power-up, the processor's internal phase-locked loop requires no more than 100 μσ while $\overline{\text{RESET}}$ is low, assuming stable $V_{DD}$ and CLKIN (not including start-up time of external clock oscillator).

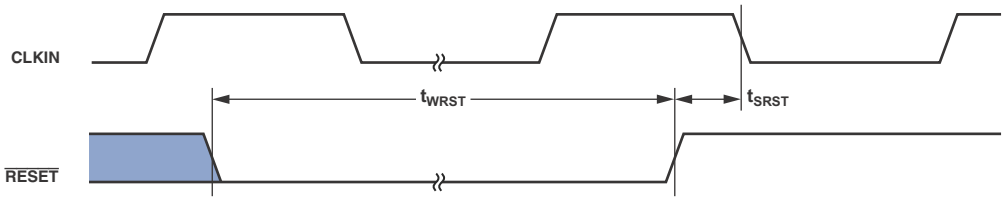


*Figure 8. Reset*

### *Running Reset*

The following timing specification applies to $\overline{\text{RESETOUT}}$/$\overline{\text{RUNRSTIN}}$ pin when it is configured as $\overline{\text{RUNRSTIN}}$.

**Table 22. Running Reset**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Timing Requirements* | | | | |
| $t_{WRUNRST}$ | Running $\overline{\text{RESET}}$ Pulse Width Low | $4 \times t_{CK}$ | | ns |
| $t_{SRUNRST}$ | Running $\overline{\text{RESET}}$ Setup Before CLKIN High | 8 | | ns |

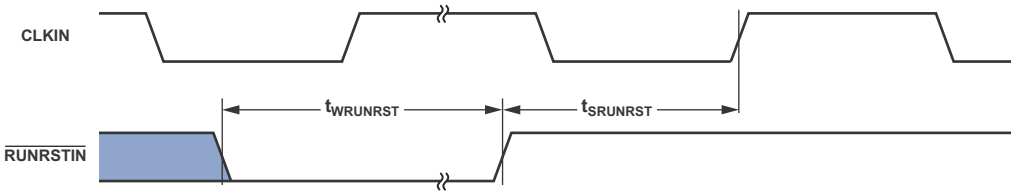


*Figure 9. Running Reset*

### *Interrupts*

The following timing specification applies to the FLAG0, FLAG1, and FLAG2 pins when they are configured as $\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$, and $\overline{\text{IRQ2}}$ interrupts, as well as the DAI_P20–1 and DPI_P14–1 pins when they are configured as interrupts.

**Table 23. Interrupts**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Timing Requirement* | | | | |
| $t_{IPW}$ | $\overline{\text{IRQx}}$ Pulse Width | $2 \times t_{PCLK} + 2$ | | ns |

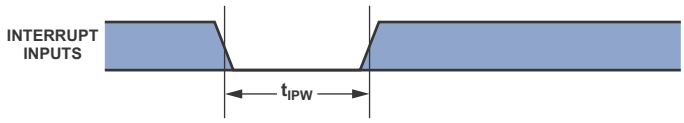


*Figure 10. Interrupts*

### *Core Timer*

The following timing specification applies to FLAG3 when it is configured as the core timer (TMREXP).

**Table 24. Core Timer**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Switching Characteristic* | | | | |
| $t_{WCTIM}$ | TMREXP Pulse Width | $4 \times t_{PCLK} - 1$ | | ns |

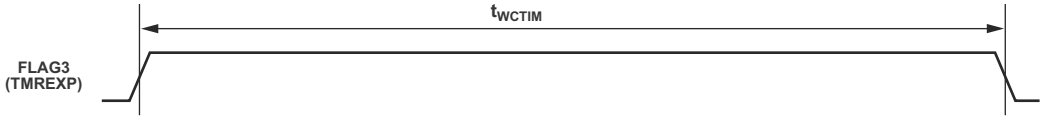


*Figure 11. Core Timer*

### *Timer PWM_OUT Cycle Timing*

The following timing specification applies to timer0 and timer1 in PWM_OUT (pulse-width modulation) mode. Timer signals are routed to the DPI_P14–1 pins through the DPI SRU. Therefore, the timing specifications provided below are valid at the DPI_P14–1 pins.

**Table 25. Timer PWM_OUT Timing**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Switching Characteristic* | | | | |
| $t_{PWMO}$ | Timer Pulse Width Output | $2 \times t_{PCLK} - 1.2$ | $2 \times (2^{31} - 1) \times t_{PCLK}$ | ns |

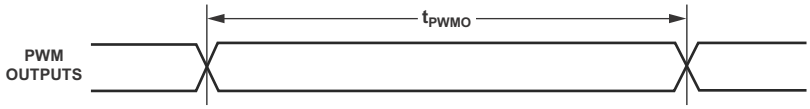


*Figure 12. Timer PWM_OUT Timing*

### *Timer WDTH_CAP Timing*

The following timing specification applies to timer0 and timer1, and in WDTH_CAP (pulse-width count and capture) mode. Timer signals are routed to the DPI_P14–1 pins through the SRU. Therefore, the timing specification provided below is valid at the DPI_P14–1 pins.

**Table 26. Timer Width Capture Timing**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Timing Requirement* | | | | |
| $t_{PWI}$ | Timer Pulse Width | $2 \times t_{PCLK}$ | $2 \times (2^{31} - 1) \times t_{PCLK}$ | ns |

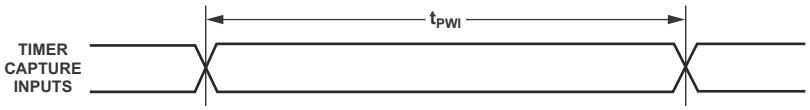


*Figure 13. Timer Width Capture Timing*

### *Watchdog Timer Timing*

**Table 27. Watchdog Timer Timing**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Timing Requirement* | | | | |
| $t_{WDTCLKPER}$ | | 100 | 1000 | ns |
| Switching Characteristics | | | | |
| $t_{RST}$ | WDT Clock Rising Edge to Watchdog Timer $\overline{\text{RESET}}$ Falling Edge | 3 | 6.4 | ns |
| $t_{RSTPW}$ | Reset Pulse Width | $64 \times t_{WDTCLKPER}$ | | ns |

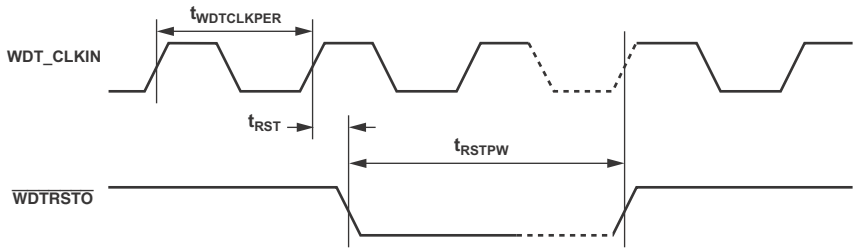


*Figure 14. Watchdog Timer Timing*

### *Pin to Pin Direct Routing (DAI and DPI)*

For direct pin connections only (for example DAI_PB01_I to DAI_PB02_O).

**Table 28. DAI/DPI Pin to Pin Routing**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Timing Requirement* | | | | |
| $t_{DPIO}$ | Delay DAI/DPI Pin Input Valid to DAI/DPI Output Valid | 1.5 | 12 | ns |

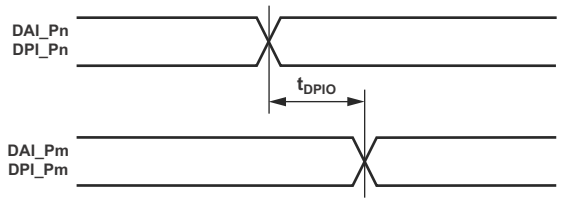


*Figure 15. DAI Pin to Pin Direct Routing*

### *Precision Clock Generator (Direct Pin Routing)*

This timing is only valid when the SRU is configured such that the precision clock generator (PCG) takes its inputs directly from the DAI pins (via pin buffers) and sends its outputs directly to the DAI pins. For the other cases, where the PCG's inputs and outputs are not directly routed to/from DAI pins (via pin buffers), there is no timing data available. All timing parameters and switching characteristics apply to external DAI pins (DAI_P01 – DAI_P20).

**Table 29. Precision Clock Generator (Direct Pin Routing)**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Timing Requirements* | | | | |
| $t_{PCGIW}$ | Input Clock Period | $t_{PCLK} \times 4$ | | ns |
| $t_{STRIG}$ | PCG Trigger Setup Before Falling Edge of PCG Input Clock | 4.5 | | ns |
| $t_{HTRIG}$ | PCG Trigger Hold After Falling Edge of PCG Input Clock | 3 | | ns |
| *Switching Characteristics* | | | | |
| $t_{DPCGIO}$ | PCG Output Clock and Frame Sync Active Edge Delay After PCG Input Clock | 2.5 | 10 | ns |
| $t_{DTRIGCLK}$ | PCG Output Clock Delay After PCG Trigger | $2.5 + (2.5 \times t_{PCGIP})$ | $10 + (2.5 \times t_{PCGIP})$ | ns |
| $t_{DTRIGFS}$ | PCG Frame Sync Delay After PCG Trigger | $2.5 + ((2.5 + D - PH) \times t_{PCGIP})$ | $10 + ((2.5 + D - PH) \times t_{PCGIP})$ | ns |
| $t_{PCGOW}$[1] | Output Clock Period | $2 \times t_{PCGIP} - 1$ | | ns |

D = FSxDIV, PH = FSxPHASE. For more information, see the *ADSP-214xx SHARC Processor Hardware Reference*, "Precision Clock Generators" chapter.

[1] Normal mode of operation.

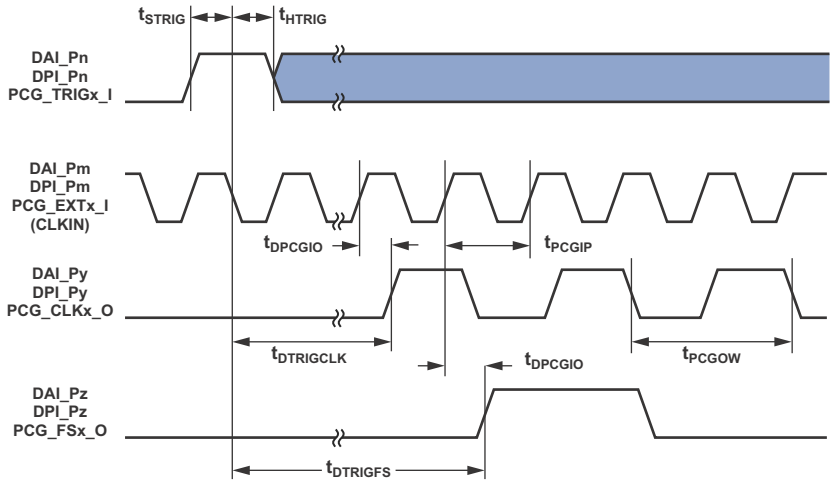


*Figure 16. Precision Clock Generator (Direct Pin Routing)*

### *Flags*

The timing specifications provided below apply to the DPI_P14–1, ADDR7–0, ADDR23–8, DATA7–0, and FLAG3–0 pins when configured as FLAGS. See Table 11 on Page 14 for more information on flag use.

**Table 30. Flags**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Timing Requirement* | | | | |
| $t_{FIPW}$[1] | FLAGs IN Pulse Width | $2 \times t_{PCLK} + 3$ | | ns |
| *Switching Characteristic* | | | | |
| $t_{FOPW}$[1] | FLAGs OUT Pulse Width | $2 \times t_{PCLK} - 3$ | | ns |

[1] This is applicable when the Flags are connected to DPI_P14–1, ADDR7–0, ADDR23–8, DATA7–0 and FLAG3–0 pins.

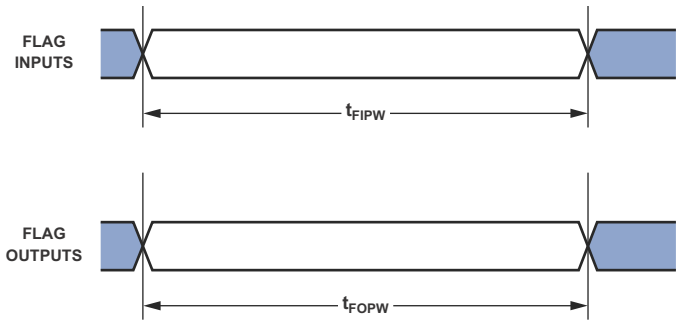


*Figure 17. Flags*

### *SDRAM Interface Timing (166 MHz SDCLK)*

The maximum frequency for SDRAM is 166 MHz. For information on SDRAM frequency and programming, see the *ADSP-214xx SHARC Processor Hardware Reference*, Engineer-to-Engineer Note *"Interfacing SDRAM Memories to SHARC Processors"* (EE-286), and the SDRAM vendor data sheet.

**Table 31. SDRAM Interface Timing**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Timing Requirements* | | | | |
| $t_{SSDAT}$ | DATA Setup Before SDCLK | 0.7 | | ns |
| $t_{HSDAT}$ | DATA Hold After SDCLK | 1.23 | | ns |
| *Switching Characteristics* | | | | |
| $t_{SDCLK}$[1] | SDCLK Period | 6 | | ns |
| $t_{SDCLKH}$ | SDCLK Width High | 2.2 | | ns |
| $t_{SDCLKL}$ | SDCLK Width Low | 2.2 | | ns |
| $t_{DCAD}$[2] | Command, ADDR, Data Delay After SDCLK | | 4 | ns |
| $t_{HCAD}$[2] | Command, ADDR, Data Hold After SDCLK | 1 | | ns |
| $t_{DSDAT}$ | Data Disable After SDCLK | | 5.3 | ns |
| $t_{ENSDAT}$ | Data Enable After SDCLK | 0.3 | | ns |

[1] Systems should use the SDRAM model with a speed grade higher than the desired SDRAM controller speed. For example, to run the SDRAM controller at 166 MHz the SDRAM model with a speed grade of 183 MHz or above should be used. See Engineer-to-Engineer Note *"Interfacing SDRAM Memories to SHARC Processors"* (EE-286) for more information on hardware design guidelines for the SDRAM interface.
[2] Command pins include: $\overline{\text{SDCAS}}$, $\overline{\text{SDRAS}}$, $\overline{\text{SDWE}}$, $\overline{\text{MSx}}$, SDA10, SDCKE.

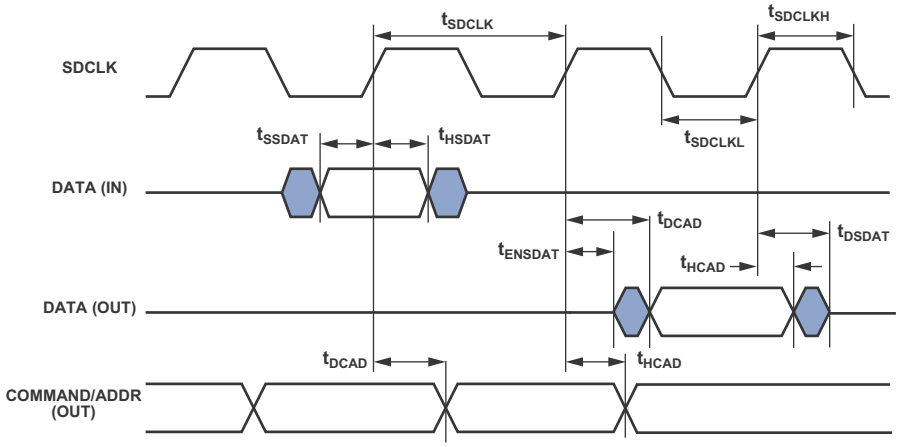


*Figure 18. SDRAM Interface Timing*

### *AMI Read*

Use these specifications for asynchronous interfacing to memories. Note that timing for AMI_ACK, ADDR, DATA, $\overline{\text{AMI_RD}}$, $\overline{\text{AMI_WR}}$, and strobe timing parameters only apply to asynchronous access mode.

**Table 32. AMI Read**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Timing Requirements* | | | | |
| $t_{DAD}$[1, 2, 3] | Address Selects Delay to Data Valid | | W + $t_{SDCLK}$ –5.4 | ns |
| $t_{DRLD}$[1, 3] | $\overline{\text{AMI_RD}}$ Low to Data Valid | | W – 3.2 | ns |
| $t_{SDS}$ | Data Setup to $\overline{\text{AMI_RD}}$ High | 2.5 | | ns |
| $t_{HDRH}$[4, 5] | Data Hold from $\overline{\text{AMI_RD}}$ High | 0 | | ns |
| $t_{DAAK}$[2, 6] | AMI_ACK Delay from Address, Selects | | $t_{SDCLK}$ –9.5 + W | ns |
| $t_{DSAK}$[4] | AMI_ACK Delay from $\overline{\text{AMI_RD}}$ Low | | W – 7 | ns |
| *Switching Characteristics* | | | | |
| $t_{DRHA}$ | Address Selects Hold After $\overline{\text{AMI_RD}}$ High | RHC + 0.20 | | ns |
| $t_{DARL}$[2] | Address Selects to $\overline{\text{AMI_RD}}$ Low | $t_{SDCLK}$ – 3.8 | | ns |
| $t_{RW}$ | $\overline{\text{AMI_RD}}$ Pulse Width | W – 1.4 | | ns |
| $t_{RWR}$ | $\overline{\text{AMI_RD}}$ High to $\overline{\text{AMI_RD}}$ Low | HI + $t_{SDCLK}$ – 1 | | ns |

W = (number of wait states specified in AMICTLx register) × $t_{SDCLK}$.
RHC = (number of Read Hold Cycles specified in AMICTLx register) × $t_{SDCLK}$
Where PREDIS = 0
HI = RHC: Read to Read from same bank
HI = RHC + IC: Read to Read from different bank
HI = RHC + Max (IC, (4 × $t_{SDCLK}$)): Read to Write from same or different bank
Where PREDIS = 1
HI = RHC + Max (IC, (4 × $t_{SDCLK}$)): Read to Write from same or different bank
HI = RHC + (3 × $t_{SDCLK}$): Read to Read from same bank
HI = RHC + Max (IC, (3 × $t_{SDCLK}$): Read to Read from different bank
IC = (number of idle cycles specified in AMICTLx register) × $t_{SDCLK}$
H = (number of hold cycles specified in AMICTLx register) × tSDCLK

[1] Data delay/setup: System must meet $t_{DAD}$, $t_{DRLD}$, or $t_{SDS}$.
[2] The falling edge of $\overline{\text{MS}}$x, is referenced.
[3] The maximum limit of timing requirement values for $t_{DAD}$ and $t_{DRLD}$ parameters are applicable for the case where AMI_ACK is always high and when the ACK feature is not used.
[4] Note that timing for AMI_ACK, ADDR, DATA, $\overline{\text{AMI_RD}}$, $\overline{\text{AMI_WR}}$, and strobe timing parameters only apply to asynchronous access mode.
[5] Data hold: User must meet $t_{HDRH}$ in asynchronous access mode. See Test Conditions on Page 55 for the calculation of hold times given capacitive and dc loads.
[6] AMI_ACK delay/setup: User must meet $t_{DAAK}$, or $t_{DSAK}$, for deassertion of AMI_ACK (low).

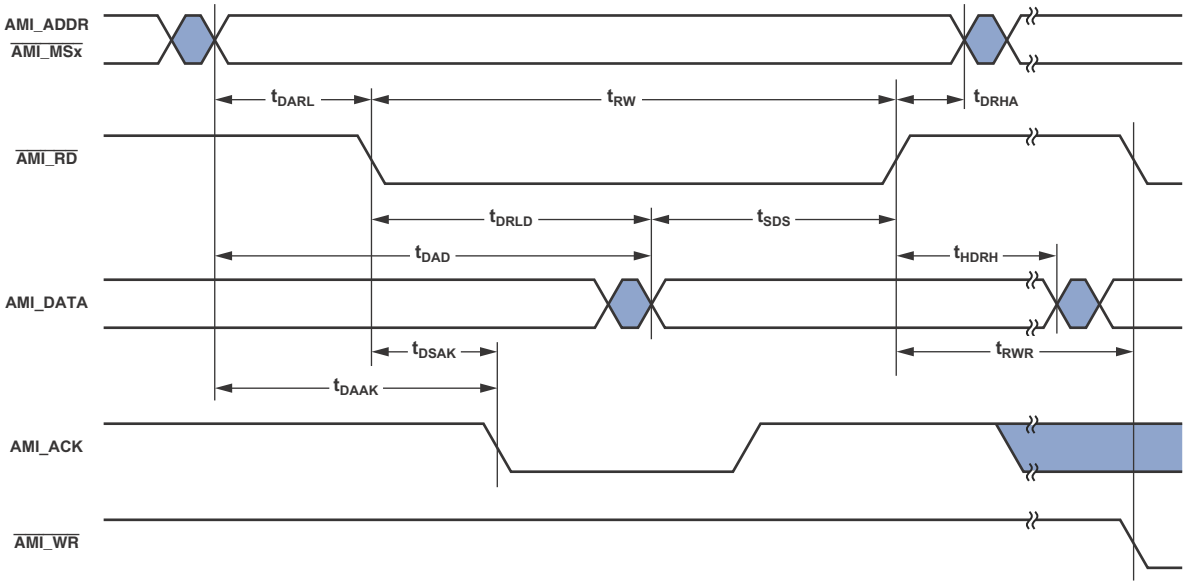


*Figure 19. AMI Read*

### *AMI Write*

Use these specifications for asynchronous interfacing to memories. Note that timing for AMI_ACK, ADDR, DATA, $\overline{\text{AMI_RD}}$, $\overline{\text{AMI_WR}}$, and strobe timing parameters only apply to asynchronous access mode.

**Table 33. AMI Write**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Timing Requirements* | | | | |
| $t_{DAAK}$[1, 2] | AMI_ACK Delay from Address, Selects | | $t_{SDCLK}$ – 9.7 + W | ns |
| $t_{DSAK}$[1, 3] | AMI_ACK Delay from $\overline{\text{AMI_WR}}$ Low | | W – 6 | ns |
| *Switching Characteristics* | | | | |
| $t_{DAWH}$[2] | Address Selects to $\overline{\text{AMI_WR}}$ Deasserted | $t_{SDCLK}$ – 3.1 + W | | ns |
| $t_{DAWL}$[2] | Address Selects to $\overline{\text{AMI_WR}}$ Low | $t_{SDCLK}$ – 3 | | ns |
| $t_{WW}$ | $\overline{\text{AMI_WR}}$ Pulse Width | W – 1.3 | | ns |
| $t_{DDWH}$ | Data Setup Before $\overline{\text{AMI_WR}}$ High | $t_{SDCLK}$ – 3.7 + W | | ns |
| $t_{DWHA}$ | Address Hold After $\overline{\text{AMI_WR}}$ Deasserted | H + 0.15 | | ns |
| $t_{DWHD}$ | Data Hold After $\overline{\text{AMI_WR}}$ Deasserted | H | | ns |
| $t_{DATRWH}$[4] | Data Disable After $\overline{\text{AMI_WR}}$ Deasserted | $t_{SDCLK}$ – 4.3 + H | $t_{SDCLK}$ + 4.9 + H | ns |
| $t_{WWR}$[5] | $\overline{\text{AMI_WR}}$ High to $\overline{\text{AMI_WR}}$ Low | $t_{SDCLK}$ – 1.5 + H | | ns |
| $t_{DDWR}$ | Data Disable Before $\overline{\text{AMI_RD}}$ Low | 2 × $t_{SDCLK}$ – 6 | | ns |
| $t_{WDE}$ | $\overline{\text{AMI_WR}}$ Low to Data Enabled | $t_{SDCLK}$ – 3.7 | | ns |

W = (number of wait states specified in AMICTLx register) × $t_{SDCLK}$
H = (number of hold cycles specified in AMICTLx register) × $t_{SDCLK}$

[1] AMI_ACK delay/setup: System must meet $t_{DAAK}$, or $t_{DSAK}$, for deassertion of AMI_ACK (low).
[2] The falling edge of $\overline{\text{MSx}}$ is referenced.
[3] Note that timing for AMI_ACK, $\overline{\text{AMI_RD}}$, $\overline{\text{AMI_WR}}$, and strobe timing parameters only applies to asynchronous access mode.
[4] See Test Conditions on Page 55 for calculation of hold times given capacitive and dc loads.
[5] For Write to Write: $t_{SDCLK}$ + H, for both same bank and different bank. For Write to Read: 3 × $t_{SDCLK}$ + H, for the same bank and different banks.

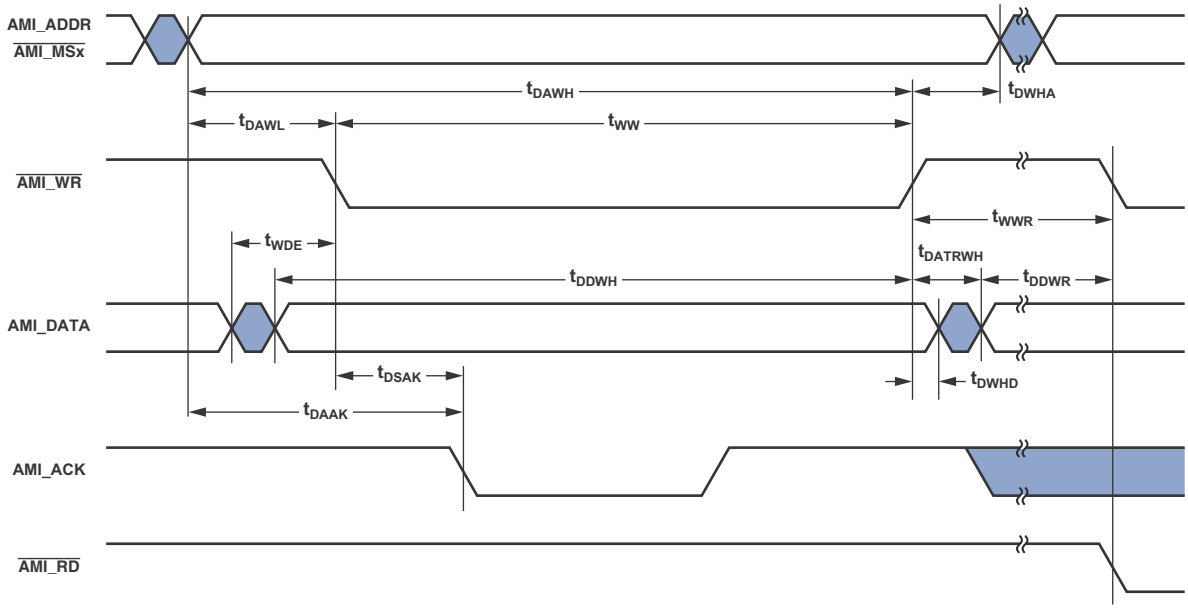


*Figure 20. AMI Write*

### *Serial Ports*

In slave transmitter mode and master receiver mode, the maximum serial port frequency is $f_{PCLK}/8$. In master transmitter mode and slave receiver mode, the maximum serial port clock frequency is $f_{PCLK}/4$. To determine whether communication is possible between two devices at clock speed n, the following specifications must be confirmed: 1) frame sync delay and frame sync setup and hold; 2) data delay and data setup and hold; and 3) SCLK width.

Serial port signals (SCLK, frame sync, Data Channel A, Data Channel B) are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

**Table 34. Serial Ports—External Clock**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Timing Requirements* | | | | |
| $t_{SFSE}$[1] | Frame Sync Setup Before SCLK (Externally Generated Frame Sync in either Transmit or Receive Mode) | 2.5 | | ns |
| $t_{HFSE}$[1] | Frame Sync Hold After SCLK (Externally Generated Frame Sync in either Transmit or Receive Mode) | 2.5 | | ns |
| $t_{SDRE}$[1] | Receive Data Setup Before Receive SCLK | 1.9 | | ns |
| $t_{HDRE}$[1] | Receive Data Hold After SCLK | 2.5 | | ns |
| $t_{SCLKW}$ | SCLK Width | $(t_{PCLK} \times 4) \div 2 - 1.5$ | | ns |
| $t_{SCLK}$ | SCLK Period | $t_{PCLK} \times 4$ | | ns |
| *Switching Characteristics* | | | | |
| $t_{DFSE}$[2] | Frame Sync Delay After SCLK (Internally Generated Frame Sync in either Transmit or Receive Mode) | | 10.25 | ns |
| $t_{HOFSE}$[2] | Frame Sync Hold After SCLK (Internally Generated Frame Sync in either Transmit or Receive Mode) | 2 | | ns |
| $t_{DDTE}$[2] | Transmit Data Delay After Transmit SCLK | | 9 | ns |
| $t_{HDTE}$[2] | Transmit Data Hold After Transmit SCLK | 2 | | ns |

[1] Referenced to sample edge.
[2] Referenced to drive edge.

**Table 35. Serial Ports—Internal Clock**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Timing Requirements* | | | | |
| $t_{SFSI}$[1] | Frame Sync Setup Before SCLK (Externally Generated Frame Sync in either Transmit or Receive Mode) | 7 | | ns |
| $t_{HFSI}$[1] | Frame Sync Hold After SCLK (Externally Generated Frame Sync in either Transmit or Receive Mode) | 2.5 | | ns |
| $t_{SDRI}$[1] | Receive Data Setup Before SCLK | 7 | | ns |
| $t_{HDRI}$[1] | Receive Data Hold After SCLK | 2.5 | | ns |
| *Switching Characteristics* | | | | |
| $t_{DFSI}$[2] | Frame Sync Delay After SCLK (Internally Generated Frame Sync in Transmit Mode) | | 4 | ns |
| $t_{HOFSI}$[2] | Frame Sync Hold After SCLK (Internally Generated Frame Sync in Transmit Mode) | –1 | | ns |
| $t_{DFSIR}$[2] | Frame Sync Delay After SCLK (Internally Generated Frame Sync in Receive Mode) | | 9.75 | ns |
| $t_{HOFSIR}$[2] | Frame Sync Hold After SCLK (Internally Generated Frame Sync in Receive Mode) | –1 | | ns |
| $t_{DDTI}$[2] | Transmit Data Delay After SCLK | | 3.25 | ns |
| $t_{HDTI}$[2] | Transmit Data Hold After SCLK | –2 | | ns |
| $t_{SCKLIW}$ | Transmit or Receive SCLK Width | $2 \times t_{PCLK} - 1.5$ | $2 \times t_{PCLK} + 1.5$ | ns |

[1] Referenced to the sample edge.
[2] Referenced to drive edge.

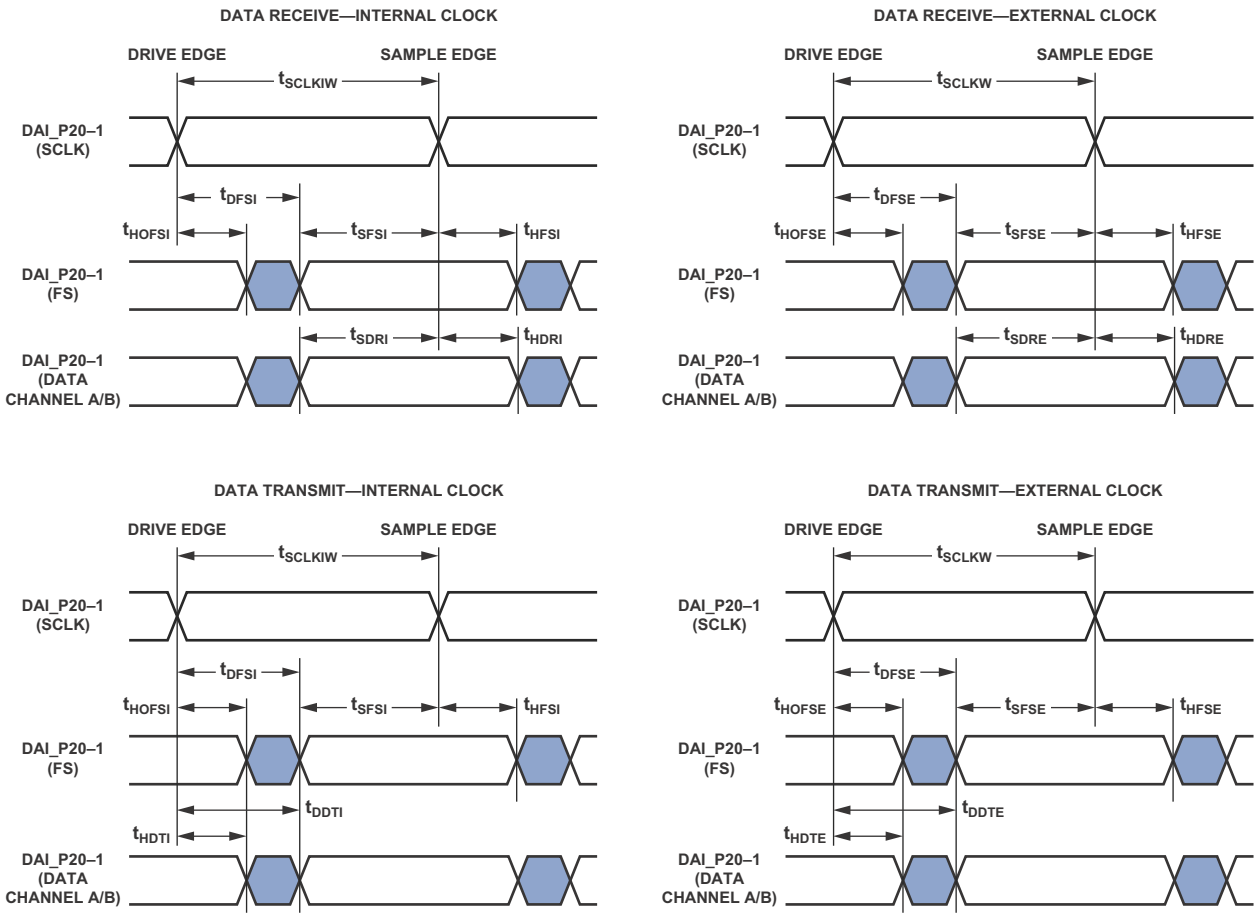


*Figure 21. Serial Ports*

**Table 36. Serial Ports—External Late Frame Sync**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Switching Characteristics* | | | | |
| $t_{DDTLFSE}$[1] | Data Delay from Late External Transmit Frame Sync or External Receive Frame Sync with MCE = 1, MFD = 0 | | 8.5 | ns |
| $t_{DDTENFS}$[1] | Data Enable for MCE = 1, MFD = 0 | 0.5 | | ns |

[1] The $t_{DDTLFSE}$ and $t_{DDTENFS}$ parameters apply to left-justified, as well as DSP serial mode, and MCE = 1, MFD = 0.

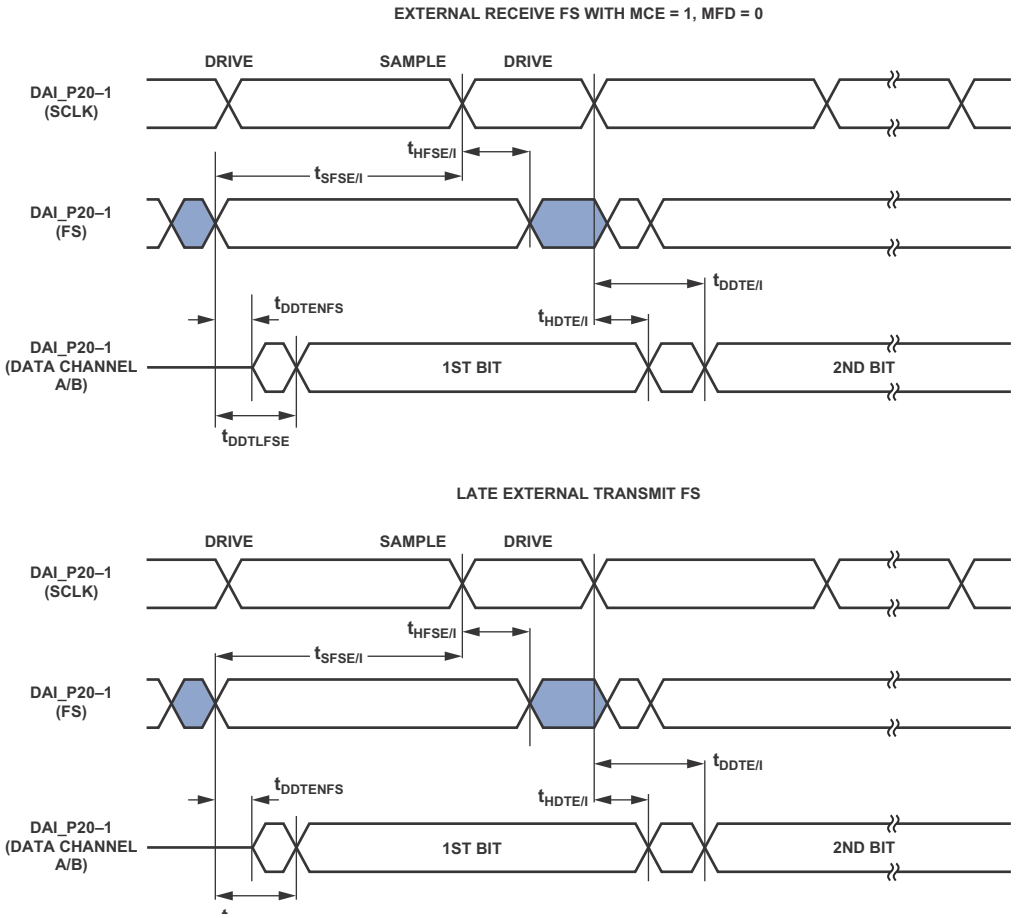


*Figure 22. External Late Frame Sync*[1]

[1] This figure reflects changes made to support left-justified mode.

**Table 37. Serial Ports—Enable and Three-State**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Switching Characteristics* | | | | |
| $t_{DDTEN}$[1] | Data Enable from External Transmit SCLK | 2 | | ns |
| $t_{DDTTE}$[1] | Data Disable from External Transmit SCLK | | 11.5 | ns |
| $t_{DDTIN}$[1] | Data Enable from Internal Transmit SCLK | –1.5 | | ns |

[1] Referenced to drive edge.

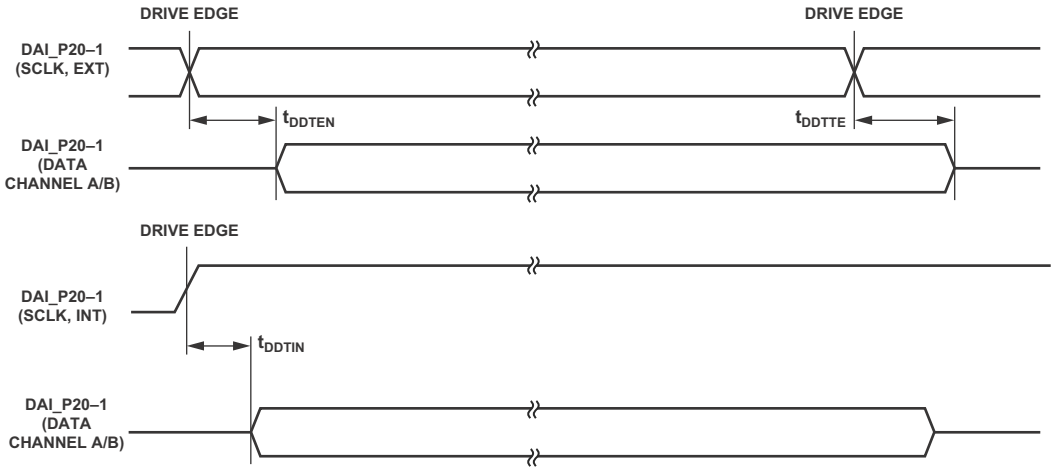


*Figure 23. Serial Ports—Enable and Three-State*

The SPORTx_TDV_O output signal (routing unit) becomes active in SPORT multichannel mode. During transmit slots (enabled with active channel selection registers) the SPORTx_TDV_O is asserted for communication with external devices.

**Table 38. Serial Ports—TDV (Transmit Data Valid)**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Switching Characteristics*[1] | | | | |
| $t_{DRDVEN}$ | TDV Assertion Delay from Drive Edge of External Clock | 3 | | ns |
| $t_{DFDVEN}$ | TDV Deassertion Delay from Drive Edge of External Clock | | 8 | ns |
| $t_{DRDVIN}$ | TDV Assertion Delay from Drive Edge of Internal Clock | –1 | | ns |
| $t_{DFDVIN}$ | TDV Deassertion Delay from Drive Edge of Internal Clock | | 2 | ns |

[1] Referenced to drive edge.

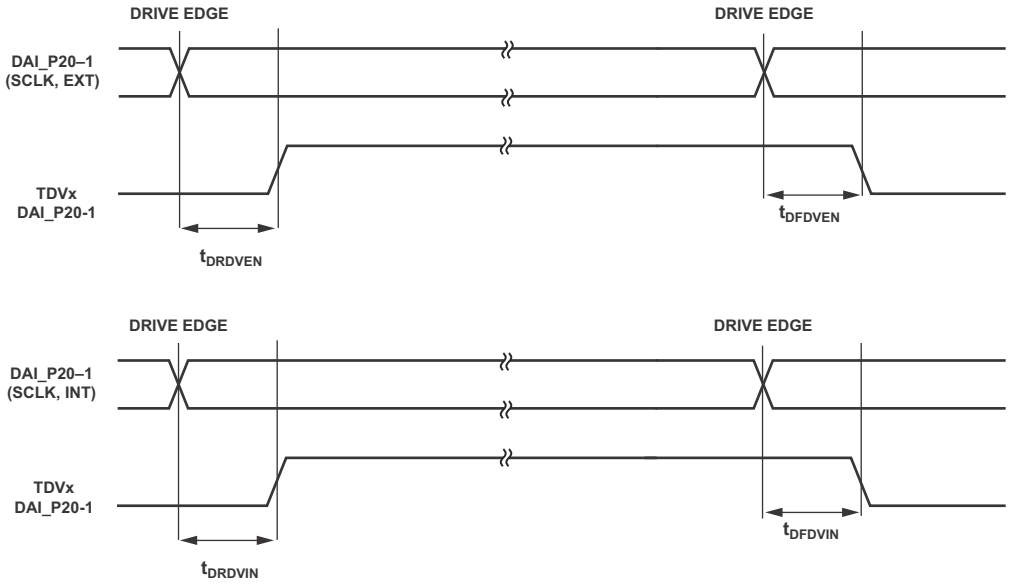


*Figure 24. Serial Ports—TDM Internal and External Clock*

### *Input Data Port (IDP)*

The timing requirements for the IDP are given in Table 39. IDP signals are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

**Table 39. Input Data Port (IDP)**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Timing Requirements* | | | | |
| $t_{SISFS}$[1] | Frame Sync Setup Before Serial Clock Rising Edge | 3.8 | | ns |
| $t_{SIHFS}$[1] | Frame Sync Hold After Serial Clock Rising Edge | 2.5 | | ns |
| $t_{SISD}$[1] | Data Setup Before Serial Clock Rising Edge | 2.5 | | ns |
| $t_{SIHD}$[1] | Data Hold After Serial Clock Rising Edge | 2.5 | | ns |
| $t_{IDPCLKW}$ | Clock Width | $(t_{PCLK} \times 4) \div 2 - 1$ | | ns |
| $t_{IDPCLK}$ | Clock Period | $t_{PCLK} \times 4$ | | ns |

[1] The serial clock, data, and frame sync signals can come from any of the DAI pins. The serial clock and frame sync signals can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

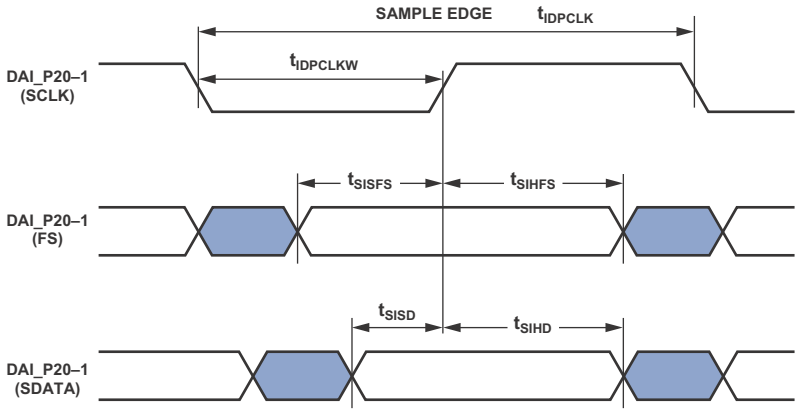


*Figure 25. IDP Master Timing*

### *Parallel Data Acquisition Port (PDAP)*

The timing requirements for the PDAP are provided in Table 40. PDAP is the parallel mode operation of Channel 0 of the IDP. For details on the operation of the PDAP, see the PDAP chapter of the *ADSP-214xx SHARC Processor Hardware Reference*. Note that the 20 bits of external PDAP data can be provided through the ADDR23–4 pins or over the DAI pins.

**Table 40. Parallel Data Acquisition Port (PDAP)**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Timing Requirements* | | | | |
| $t_{SPHOLD}$[1] | PDAP_HOLD Setup Before PDAP_CLK Sample Edge | 2.5 | | ns |
| $t_{HPHOLD}$[1] | PDAP_HOLD Hold After PDAP_CLK Sample Edge | 2.5 | | ns |
| $t_{PDSD}$[1] | PDAP_DAT Setup Before PDAP_CLK Sample Edge | 3.85 | | ns |
| $t_{PDHD}$[1] | PDAP_DAT Hold After PDAP_CLK Sample Edge | 2.5 | | ns |
| $t_{PDCLKW}$ | Clock Width | $(t_{PCLK} \times 4) \div 2 - 3$ | | ns |
| $t_{PDCLK}$ | Clock Period | $t_{PCLK} \times 4$ | | ns |
| *Switching Characteristics* | | | | |
| $t_{PDHLDD}$ | Delay of PDAP Strobe After Last PDAP_CLK Capture Edge for a Word | $2 \times t_{PCLK} + 3$ | | ns |
| $t_{PDSTRB}$ | PDAP Strobe Pulse Width | $2 \times t_{PCLK} - 1.5$ | | ns |

[1] Source pins of PDAP_DATA are ADDR23–4 or DAI pins. Source pins for PDAP_CLK and PDAP_HOLD are 1) DAI pins; 2) CLKIN through PCG; 3) DAI pins through PCG; or 4) ADDR3–2 pins.

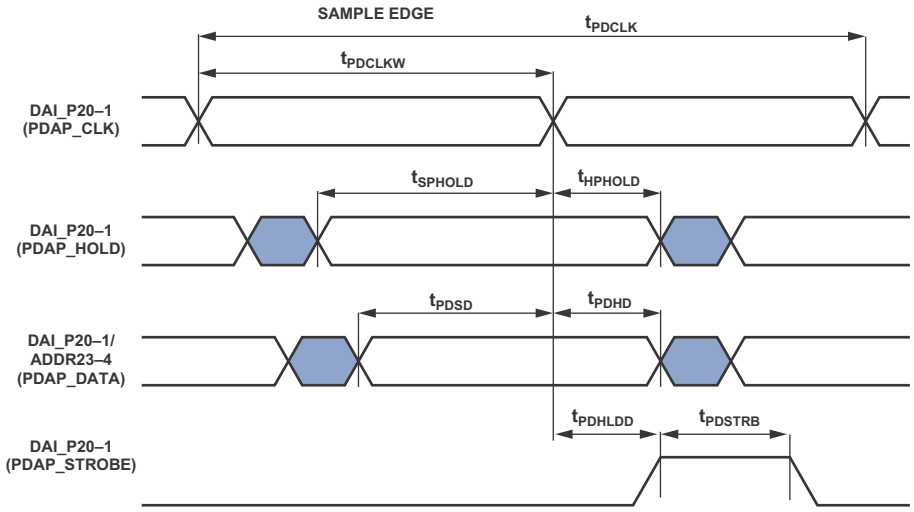


*Figure 26. PDAP Timing*

### *Sample Rate Converter—Serial Input Port*

The ASRC input signals are routed from the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided in Table 41 are valid at the DAI_P20–1 pins.

**Table 41. ASRC, Serial Input Port**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Timing Requirements* | | | | |
| $t_{SRCSFS}$[1] | Frame Sync Setup Before Serial Clock Rising Edge | 4 | | ns |
| $t_{SRCHFS}$[1] | Frame Sync Hold After Serial Clock Rising Edge | 5.5 | | ns |
| $t_{SRCSD}$[1] | Data Setup Before Serial Clock Rising Edge | 4 | | ns |
| $t_{SRCHD}$[1] | Data Hold After Serial Clock Rising Edge | 5.5 | | ns |
| $t_{SRCCLKW}$ | Clock Width | $(t_{PCLK} \times 4) \div 2 - 1$ | | ns |
| $t_{SRCCLK}$ | Clock Period | $t_{PCLK} \times 4$ | | ns |

[1] The serial clock, data, and frame sync signals can come from any of the DAI pins. The serial clock and frame sync signals can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

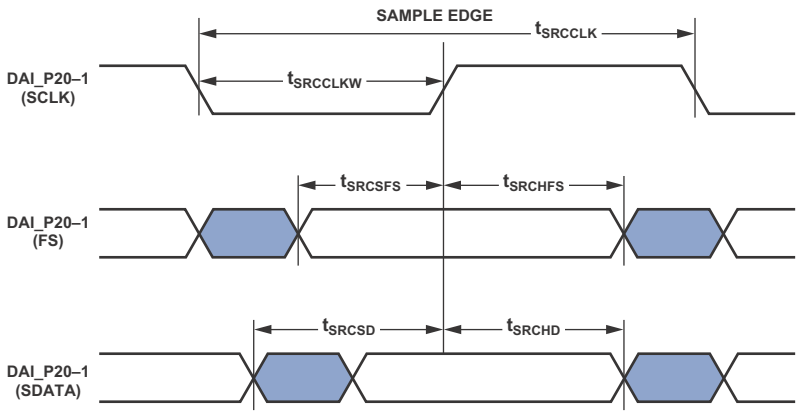


*Figure 27. ASRC Serial Input Port Timing*

### *Sample Rate Converter—Serial Output Port*

For the serial output port, the frame sync is an input, and it should meet setup and hold times with regard to SCLK on the output port. The serial data output has a hold time and delay specification with regard to serial clock. Note that serial clock rising edge is the sampling edge, and the falling edge is the drive edge.

**Table 42. ASRC, Serial Output Port**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Timing Requirements* | | | | |
| $t_{SRCSFS}$[1] | Frame Sync Setup Before Serial Clock Rising Edge | 4 | | ns |
| $t_{SRCHFS}$[1] | Frame Sync Hold After Serial Clock Rising Edge | 5.5 | | ns |
| $t_{SRCCLKW}$ | Clock Width | $(t_{PCLK} \times 4) \div 2 - 1$ | | ns |
| $t_{SRCCLK}$ | Clock Period | $t_{PCLK} \times 4$ | | ns |
| *Switching Characteristics* | | | | |
| $t_{SRCTDD}$[1] | Transmit Data Delay After Serial Clock Falling Edge | | 9.9 | ns |
| $t_{SRCTDH}$[1] | Transmit Data Hold After Serial Clock Falling Edge | 1 | | ns |

[1] The serial clock, data, and frame sync signals can come from any of the DAI pins. The serial clock and frame sync signals can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

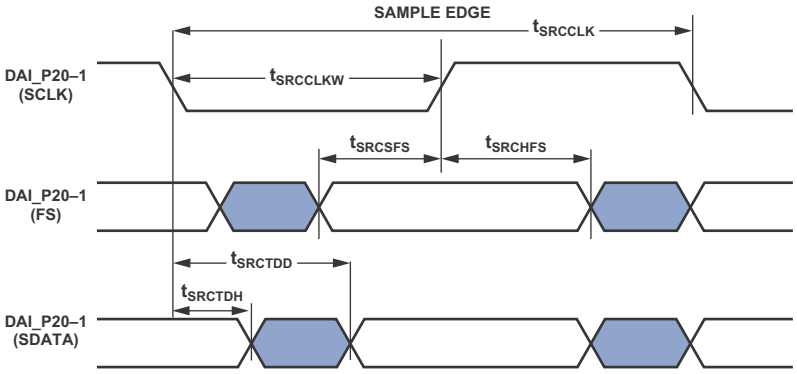


*Figure 28. ASRC Serial Output Port Timing*

### *Pulse-Width Modulation Generators (PWM)*

The following timing specifications apply when the ADDR23–8/DPI_14–1 pins are configured as PWM.

**Table 43. Pulse-Width Modulation (PWM) Timing**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Switching Characteristics* | | | | |
| $t_{PWMW}$ | PWM Output Pulse Width | $t_{PCLK} - 2$ | $(2^{16} - 2) \times t_{PCLK}$ | ns |
| $t_{PWMP}$ | PWM Output Period | $2 \times t_{PCLK} - 1.5$ | $(2^{16} - 1) \times t_{PCLK}$ | ns |

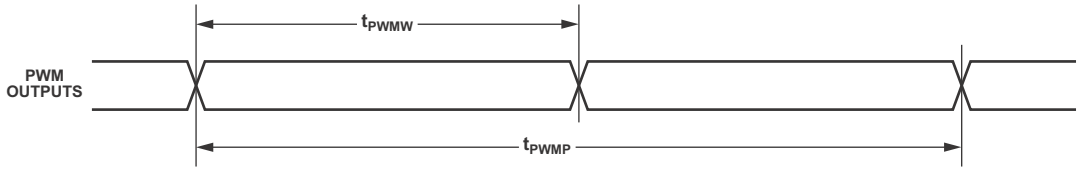


*Figure 29. PWM Timing*

### *S/PDIF Transmitter*

Serial data input to the S/PDIF transmitter can be formatted as left-justified, I²S, or right-justified with word widths of 16, 18, 20, or 24 bits. The following sections provide timing for the transmitter.

#### S/PDIF Transmitter-Serial Input Waveforms

Figure 30 shows the right-justified mode. Frame sync is high for the left channel and low for the right channel. Data is valid on the rising edge of serial clock. The MSB is delayed the minimum in 24-bit output mode or the maximum in 16-bit output mode from a frame sync transition, so that when there are 64 serial clock periods per frame sync period, the LSB of the data is right-justified to the next frame sync transition.

**Table 44. S/PDIF Transmitter Right-Justified Mode**

| Parameter | | Nominal | Unit |
|---|---|---|---|
| *Timing Requirement* | | | |
| $t_{RJD}$ | Frame Sync to MSB Delay in Right-Justified Mode | | |
| | 16-Bit Word Mode | 16 | SCLK |
| | 18-Bit Word Mode | 14 | SCLK |
| | 20-Bit Word Mode | 12 | SCLK |
| | 24-Bit Word Mode | 8 | SCLK |

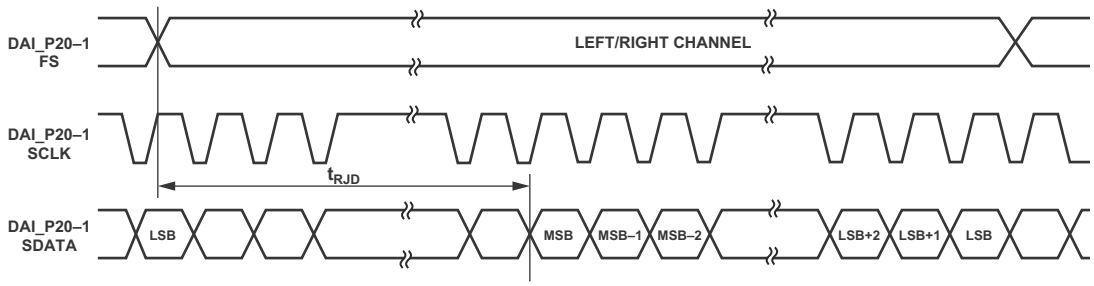


*Figure 30. Right-Justified Mode*

Figure 31 shows the default I²S-justified mode. The frame sync is low for the left channel and HI for the right channel. Data is valid on the rising edge of serial clock. The MSB is left-justified to the frame sync transition but with a delay.

**Table 45. S/PDIF Transmitter I²S Mode**

| Parameter | | Nominal | Unit |
|---|---|---|---|
| *Timing Requirement* | | | |
| $t_{I2SD}$ | Frame Sync to MSB Delay in I²S Mode | 1 | SCLK |

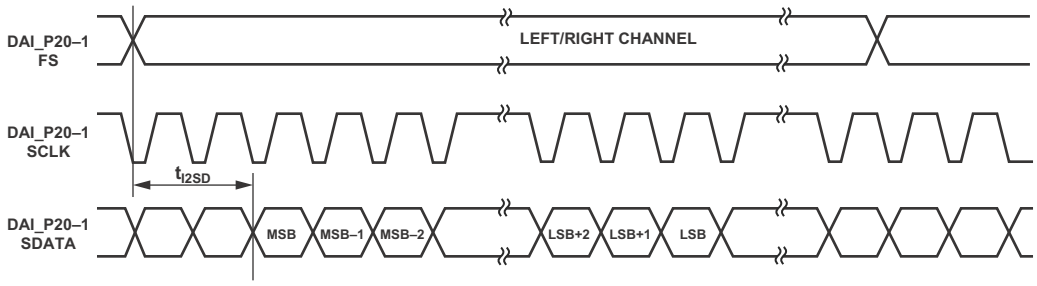


*Figure 31. I²S-Justified Mode*

Figure 32 shows the left-justified mode. The frame sync is high for the left channel and low for the right channel. Data is valid on the rising edge of serial clock. The MSB is left-justified to the frame sync transition with no delay.

**Table 46. S/PDIF Transmitter Left-Justified Mode**

| Parameter | | Nominal | Unit |
|---|---|---|---|
| *Timing Requirement* | | | |
| $t_{LJD}$ | Frame Sync to MSB Delay in Left-Justified Mode | 0 | SCLK |

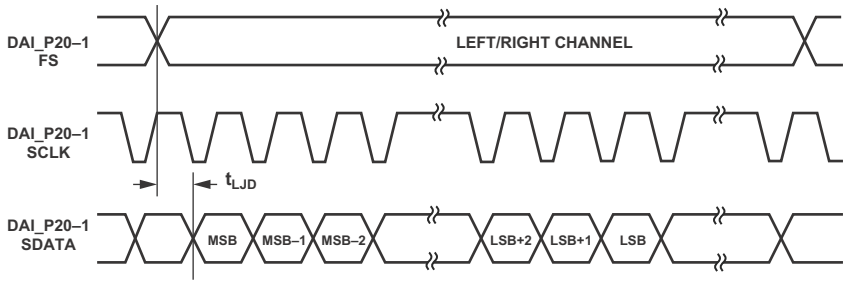


*Figure 32. Left-Justified Mode*

### S/PDIF Transmitter Input Data Timing

The timing requirements for the S/PDIF transmitter are given in Table 47. Input signals are routed to the DAI_P20–1 pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI_P20–1 pins.

**Table 47. S/PDIF Transmitter Input Data Timing**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Timing Requirements* | | | | |
| $t_{SISFS}$[1] | Frame Sync Setup Before Serial Clock Rising Edge | 3 | | ns |
| $t_{SIHFS}$[1] | Frame Sync Hold After Serial Clock Rising Edge | 3 | | ns |
| $t_{SISD}$[1] | Data Setup Before Serial Clock Rising Edge | 3 | | ns |
| $t_{SIHD}$[1] | Data Hold After Serial Clock Rising Edge | 3 | | ns |
| $t_{SITXCLKW}$ | Transmit Clock Width | 9 | | ns |
| $t_{SITXCLK}$ | Transmit Clock Period | 20 | | ns |
| $t_{SISCLKW}$ | Clock Width | 36 | | ns |
| $t_{SISCLK}$ | Clock Period | 80 | | ns |

[1] The serial clock, data, and frame sync signals can come from any of the DAI pins. The serial clock and frame sync signals can also come via PCG or SPORTs. PCG's input can be either CLKIN or any of the DAI pins.

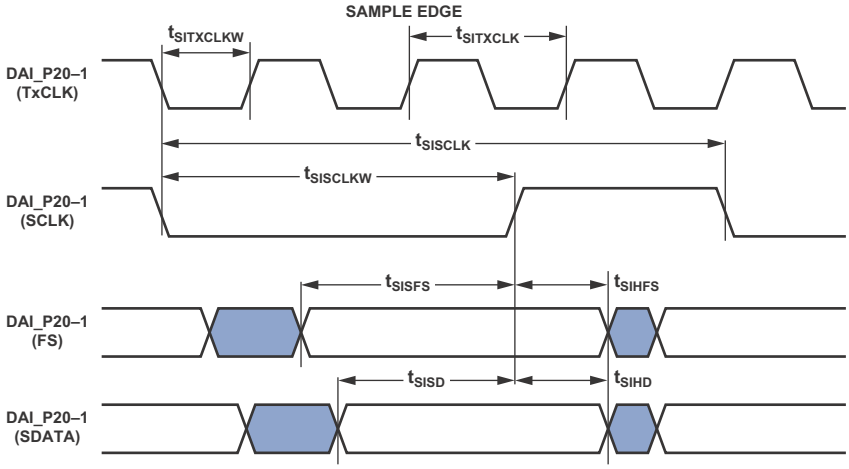


*Figure 33. S/PDIF Transmitter Input Timing*

### Oversampling Clock (TxCLK) Switching Characteristics

The S/PDIF transmitter requires an oversampling clock input. This high frequency clock (TxCLK) input is divided down to generate the internal biphase clock.

**Table 48. Oversampling Clock (TxCLK) Switching Characteristics**

| Parameter | Max | Unit |
|---|---|---|
| Frequency for TxCLK = 384 × Frame Sync | Oversampling Ratio × Frame Sync <= $1/t_{SITXCLK}$ | MHz |
| Frequency for TxCLK = 256 × Frame Sync | 49.2 | MHz |
| Frame Rate (FS) | 192.0 | kHz |

### *S/PDIF Receiver*

The following section describes timing as it relates to the S/PDIF receiver.

#### Internal Digital PLL Mode

In the internal digital phase-locked loop mode the internal PLL (digital PLL) generates the 512 × FS clock.

**Table 49. S/PDIF Receiver Internal Digital PLL Mode Timing**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Switching Characteristics* | | | | |
| $t_{DFSI}$ | Frame Sync Delay After Serial Clock | | 5 | ns |
| $t_{HOFSI}$ | Frame Sync Hold After Serial Clock | –2 | | ns |
| $t_{DDTI}$ | Transmit Data Delay After Serial Clock | | 5 | ns |
| $t_{HDTI}$ | Transmit Data Hold After Serial Clock | –2 | | ns |
| $t_{SCLKIW}$[1] | Transmit Serial Clock Width | $8 \times t_{PCLK} - 2$ | | ns |

[1] SCLK frequency is 64 × FS where FS = the frequency of frame sync.

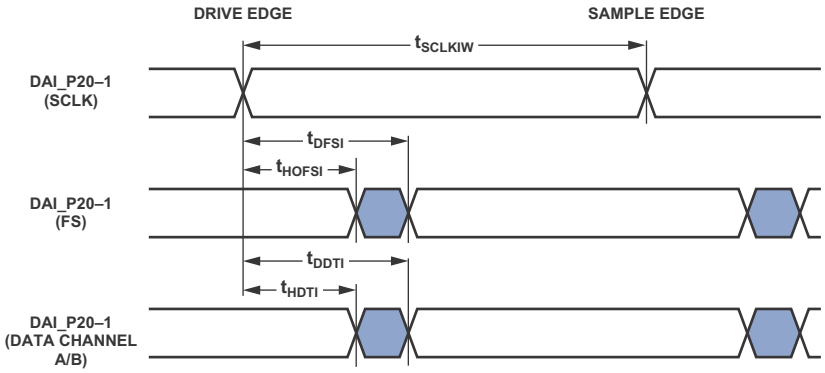


*Figure 34. S/PDIF Receiver Internal Digital PLL Mode Timing*

### *SPI Interface—Master*

The ADSP-2148x contains two SPI ports. Both primary and secondary are available through DPI only. The timing provided in Table 50 and Table 51 applies to both.

**Table 50. SPI Interface Protocol—Master Switching and Timing Specifications**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Timing Requirements* | | | | |
| $t_{SSPIDM}$ | Data Input Valid to SPICLK Edge (Data Input Setup Time) | 8.2 | | ns |
| $t_{HSPIDM}$ | SPICLK Last Sampling Edge to Data Input Not Valid | 2 | | ns |
| *Switching Characteristics* | | | | |
| $t_{SPICLKM}$ | Serial Clock Cycle | $8 \times t_{PCLK} - 2$ | | ns |
| $t_{SPICHM}$ | Serial Clock High Period | $4 \times t_{PCLK} - 2$ | | ns |
| $t_{SPICLM}$ | Serial Clock Low Period | $4 \times t_{PCLK} - 2$ | | ns |
| $t_{DDSPIDM}$ | SPICLK Edge to Data Out Valid (Data Out Delay Time) | | 2.5 | ns |
| $t_{HDSPIDM}$ | SPICLK Edge to Data Out Not Valid (Data Out Hold Time) | $4 \times t_{PCLK} - 2$ | | ns |
| $t_{SDSCIM}$ | DPI Pin (SPI Device Select) Low to First SPICLK Edge | $4 \times t_{PCLK} - 2$ | | ns |
| $t_{HDSM}$ | Last SPICLK Edge to DPI Pin (SPI Device Select) High | $4 \times t_{PCLK} - 2$ | | ns |
| $t_{SPITDM}$ | Sequential Transfer Delay | $4 \times t_{PCLK} - 1.2$ | | ns |

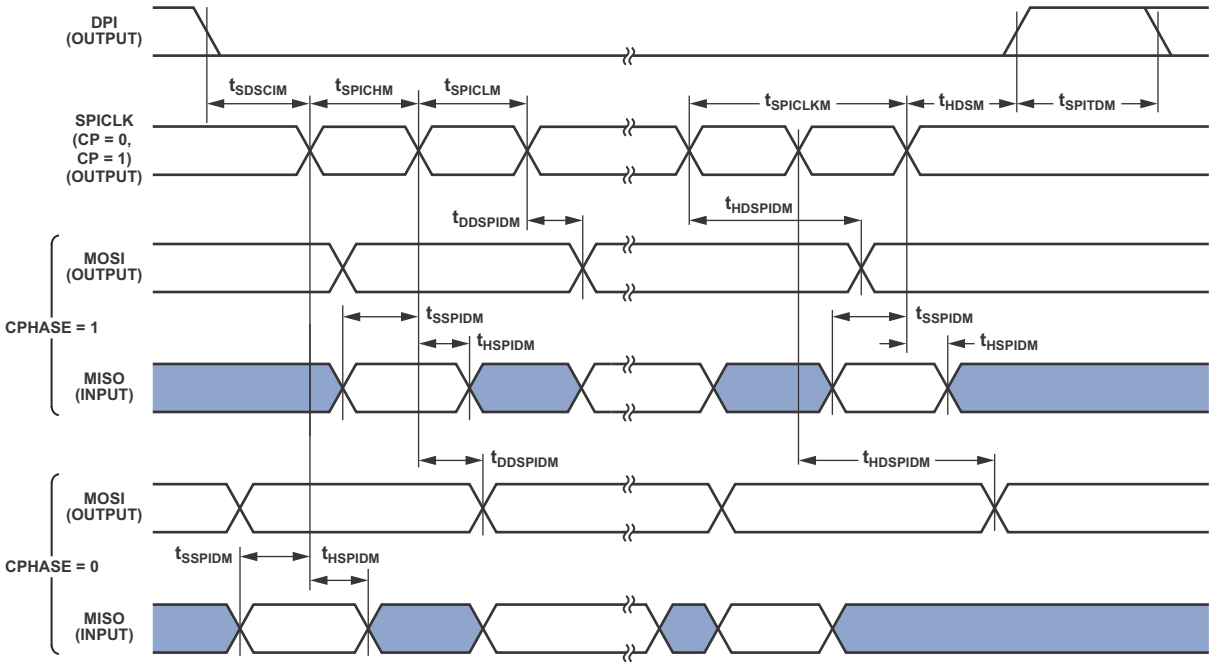


*Figure 35. SPI Master Timing*

### *SPI Interface—Slave*

**Table 51. SPI Interface Protocol—Slave Switching and Timing Specifications**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Timing Requirements* | | | | |
| $t_{SPICLKS}$ | Serial Clock Cycle | $4 \times t_{PCLK} - 2$ | | ns |
| $t_{SPICHS}$ | Serial Clock High Period | $2 \times t_{PCLK} - 2$ | | ns |
| $t_{SPICLS}$ | Serial Clock Low Period | $2 \times t_{PCLK} - 2$ | | ns |
| $t_{SDSCO}$ | $\overline{SPIDS}$ Assertion to First SPICLK Edge<br>CPHASE = 0<br>CPHASE = 1 | $2 \times t_{PCLK}$ | | ns |
| $t_{HDS}$ | Last SPICLK Edge to $\overline{SPIDS}$ Not Asserted, CPHASE = 0 | $2 \times t_{PCLK}$ | | ns |
| $t_{SSPIDS}$ | Data Input Valid to SPICLK edge (Data Input Set-up Time) | 2 | | ns |
| $t_{HSPIDS}$ | SPICLK Last Sampling Edge to Data Input Not Valid | 2 | | ns |
| $t_{SDPPW}$ | $\overline{SPIDS}$ Deassertion Pulse Width (CPHASE=0) | $2 \times t_{PCLK}$ | | ns |
| *Switching Characteristics* | | | | |
| $t_{DSOE}$ | $\overline{SPIDS}$ Assertion to Data Out Active | 0 | 7.5 | ns |
| $t_{DSOE}$[1] | $\overline{SPIDS}$ Assertion to Data Out Active (SPI2) | 0 | 7.5 | ns |
| $t_{DSDHI}$ | $\overline{SPIDS}$ Deassertion to Data High Impedance | 0 | 10.5 | ns |
| $t_{DSDHI}$[1] | $\overline{SPIDS}$ Deassertion to Data High Impedance (SPI2) | 0 | 10.5 | ns |
| $t_{DDSPIDS}$ | SPICLK Edge to Data Out Valid (Data Out Delay Time) | | 9.5 | ns |
| $t_{HDSPIDS}$ | SPICLK Edge to Data Out Not Valid (Data Out Hold Time) | $2 \times t_{PCLK}$ | | ns |
| $t_{DSOV}$ | $\overline{SPIDS}$ Assertion to Data Out Valid (CPHASE = 0) | | $5 \times t_{PCLK}$ | ns |

[1] The timing for these parameters applies when the SPI is routed through the signal routing unit. For more information, see the processor hardware reference, "Serial Peripheral Interface Port" chapter.

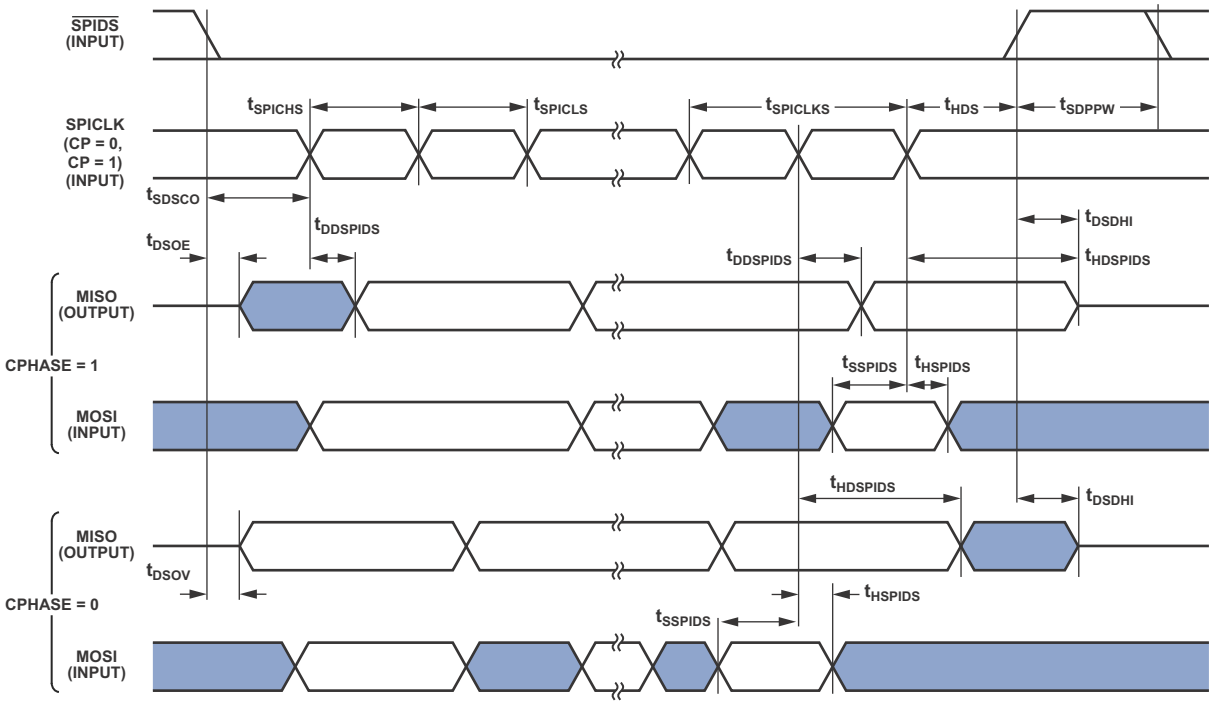


*Figure 36. SPI Slave Timing*

### *Media Local Bus*

All the numbers given are applicable for all speed modes (1024 FS, 512 FS and 256 FS for 3-pin; 512 FS and 256 FS for 5-pin), unless otherwise specified. Please refer to the MediaLB specification document revision 3.0 for more details.

**Table 52. MLB Interface, 3-Pin Specifications**

| Parameter | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| *3-Pin Characteristics* | | | | | |
| $t_{MLBCLK}$ | MLB Clock Period | | | | |
| | 1024 FS | | 20.3 | | ns |
| | 512 FS | | 40 | | ns |
| | 256 FS | | 81 | | ns |
| $t_{MCKL}$ | MLBCLK Low Time | | | | |
| | 1024 FS | 6.1 | | | ns |
| | 512 FS | 14 | | | ns |
| | 256 FS | 30 | | | ns |
| $t_{MCKH}$ | MLBCLK High Time | | | | |
| | 1024 FS | 9.3 | | | ns |
| | 512 FS | 14 | | | ns |
| | 256 FS | 30 | | | ns |
| $t_{MCKR}$ | MLBCLK Rise Time ($V_{IL}$ to $V_{IH}$) | | | | |
| | 1024 FS | | | 1 | ns |
| | 512 FS/256 FS | | | 3 | ns |
| $t_{MCKF}$ | MLBCLK Fall Time ($V_{IH}$ to $V_{IL}$) | | | | |
| | 1024 FS | | | 1 | ns |
| | 512 FS/256 FS | | | 3 | ns |
| $t_{MPWV}$[1] | MLBCLK Pulse Width Variation | | | | |
| | 1024 FS | | | 0.7 | nspp |
| | 512 FS/256 | | | 2.0 | nspp |
| $t_{DSMCF}$ | DAT/SIG Input Setup Time | 1 | | | ns |
| $t_{DHMCF}$ | DAT/SIG Input Hold Time | 2 | | | ns |
| $t_{MCFDZ}$ | DAT/SIG Output Time to Three-state | 0 | | 15 | ns |
| $t_{MCDRV}$ | DAT/SIG Output Data Delay From MLBCLK Rising Edge | | | 8 | ns |
| $t_{MDZH}$[2] | Bus Hold Time | | | | |
| | 1024 FS | 2 | | | ns |
| | 512 FS/256 | 4 | | | ns |
| $C_{MLB}$ | DAT/SIG Pin Load | | | | |
| | 1024 FS | | | 40 | pf |
| | 512 FS/256 | | | 60 | pf |

[1] Pulse width variation is measured at 1.25 V by triggering on one edge of MLBCLK and measuring the spread on the other edge, measured in ns peak-to-peak (pp).
[2] The board must be designed to ensure that the high-impedance bus does not leave the logic state of the final driven bit for this time period. Therefore, coupling must be minimized while meeting the maximum capacitive load listed.

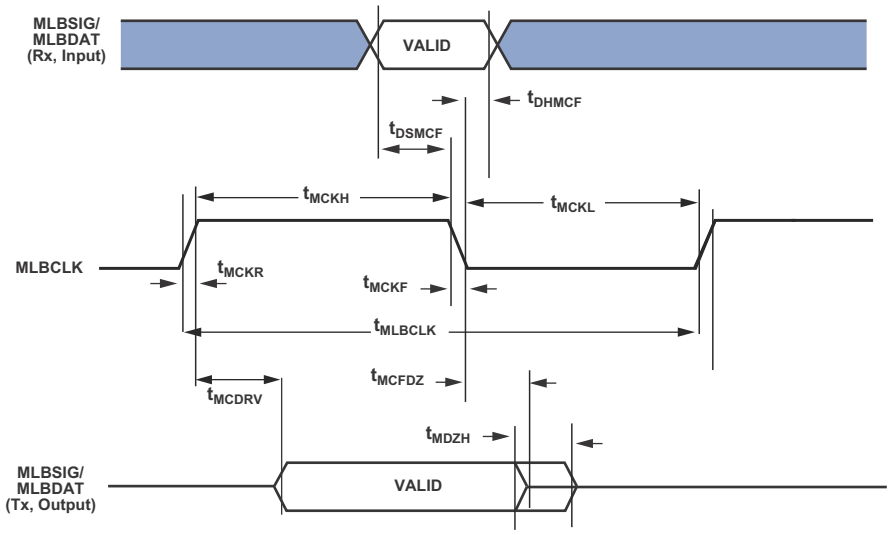


*Figure 37. MLB Timing (3-Pin Interface)*

**Table 53. MLB Interface, 5-Pin Specifications**

| Parameter | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| *5-Pin Characteristics* | | | | | |
| $t_{MLBCLK}$ | MLB Clock Period | | | | |
| | 512 FS | | 40 | | ns |
| | 256 FS | | 81 | | ns |
| $t_{MCKL}$ | MLBCLK Low Time | | | | |
| | 512 FS | 15 | | | ns |
| | 256 FS | 30 | | | ns |
| $t_{MCKH}$ | MLBCLK High Time | | | | |
| | 512 FS | 15 | | | ns |
| | 256 FS | 30 | | | ns |
| $t_{MCKR}$ | MLBCLK Rise Time ($V_{IL}$ to $V_{IH}$) | | | 6 | ns |
| $t_{MCKF}$ | MLBCLK Fall Time ($V_{IH}$ to $V_{IL}$) | | | 6 | ns |
| $t_{MPWV}$[1] | MLBCLK Pulse Width Variation | | | 2 | nspp |
| $t_{DSMCF}$[2] | DAT/SIG Input Setup Time | 3 | | | ns |
| $t_{DHMCF}$ | DAT/SIG Input Hold Time | 5 | | | ns |
| $t_{MCDRV}$ | DS/DO Output Data Delay From MLBCLK Rising Edge | | | 8 | ns |
| $t_{MCRDL}$[3] | DO/SO Low From MLBCLK High | | | | |
| | 512 FS | | | 10 | ns |
| | 256 FS | | | 20 | ns |
| $C_{MLB}$ | DS/DO Pin Load | | | 40 | pf |

[1] Pulse width variation is measured at 1.25 V by triggering on one edge of MLBCLK and measuring the spread on the other edge, measured in ns peak-to-peak (pp).
[2] Gate Delays due to OR'ing logic on the pins must be accounted for.
[3] When a node is not driving valid data onto the bus, the MLBSO and MLBDO output lines shall remain low. If the output lines can float at anytime, including while in reset, external pull-down resistors are required to keep the outputs from corrupting the MediaLB signal lines when not being driven.

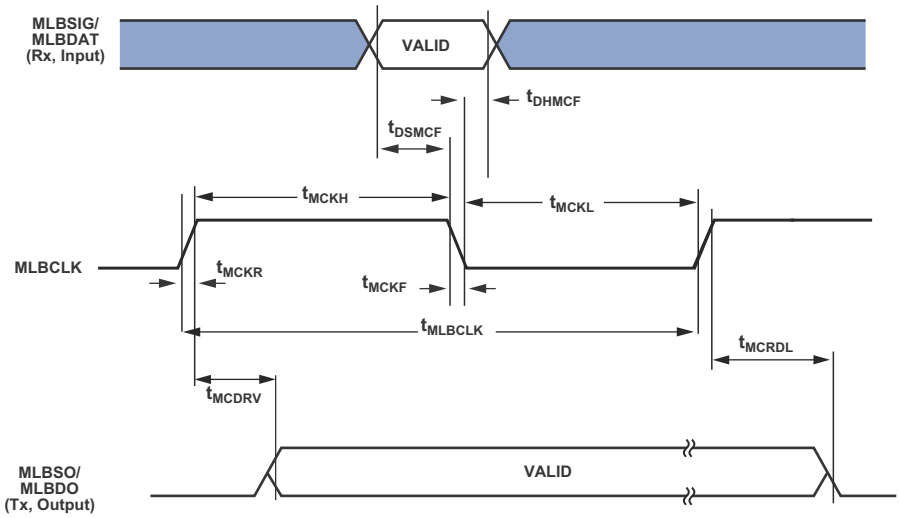


*Figure 38. MLB Timing (5-Pin Interface)*

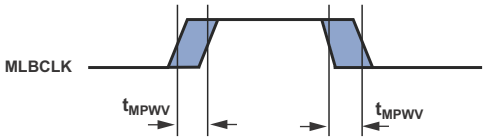


*Figure 39. MLB 3-Pin and 5-Pin MLBCLK Pulse Width Variation Timing*

### *Universal Asynchronous Receiver-Transmitter (UART) Ports—Receive and Transmit Timing*

For information on the UART port receive and transmit operations, see the *ADSP-214xx SHARC Hardware Reference Manual*.

### *2-Wire Interface (TWI)—Receive and Transmit Timing*

For information on the TWI receive and transmit operations, see the *ADSP-214xx SHARC Hardware Reference Manual*.

### *JTAG Test Access Port and Emulation*

**Table 54. JTAG Test Access Port and Emulation**

| Parameter | | Min | Max | Unit |
|---|---|---|---|---|
| *Timing Requirements* | | | | |
| $t_{TCK}$ | TCK Period | 20 | | ns |
| $t_{STAP}$ | TDI, TMS Setup Before TCK High | 5 | | ns |
| $t_{HTAP}$ | TDI, TMS Hold After TCK High | 6 | | ns |
| $t_{SSYS}$[1] | System Inputs Setup Before TCK High | 7 | | ns |
| $t_{HSYS}$[1] | System Inputs Hold After TCK High | 18 | | ns |
| $t_{TRSTW}$ | $\overline{\text{TRST}}$ Pulse Width | $4t_{CK}$ | | ns |
| *Switching Characteristics* | | | | |
| $t_{DTDO}$ | TDO Delay from TCK Low | | 10 | ns |
| $t_{DSYS}$[2] | System Outputs Delay After TCK Low | | $t_{TCK} \div 2 + 7$ | ns |

[1] System Inputs = DATA15–0, CLK_CFG1–0, $\overline{\text{RESET}}$, BOOT_CFG2–0, DAI_Px, DPI_Px, and FLAG3–0.
[2] System Outputs = DAI_Px, DPI_Px ADDR23–0, $\overline{\text{AMI_RD}}$, $\overline{\text{AMI_WR}}$, FLAG3–0, $\overline{\text{SDRAS}}$, $\overline{\text{SDCAS}}$, $\overline{\text{SDWE}}$, SDCKE, SDA10, SDDQM, SDCLK and $\overline{\text{EMU}}$.

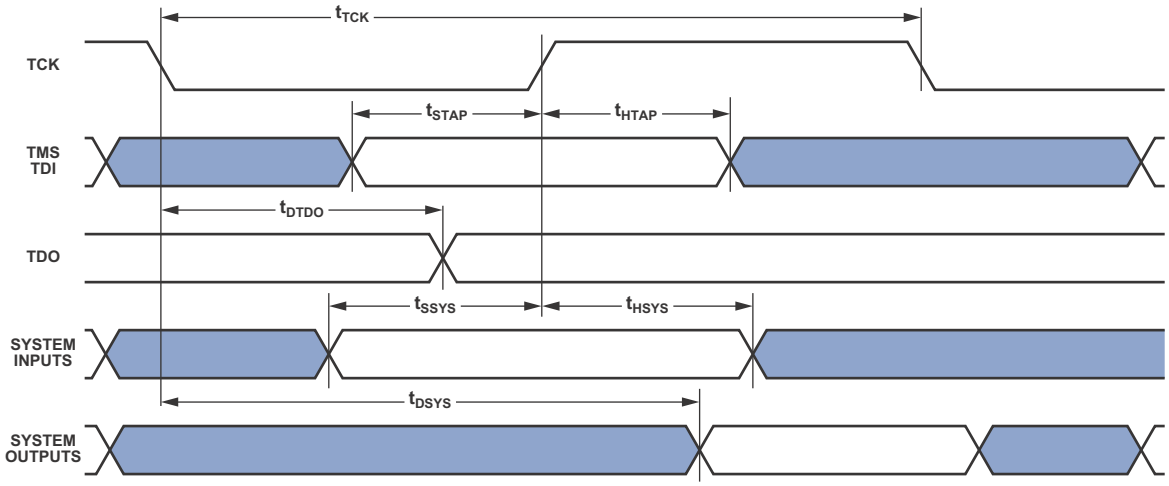


*Figure 40. IEEE 1149.1 JTAG Test Access Port*

## OUTPUT DRIVE CURRENTS

Figure 41 shows typical I-V characteristics for the output drivers of the ADSP-2148x, and Table 55 shows the pins associated with each driver. The curves represent the current drive capability of the output drivers as a function of output voltage.

**Table 55. Driver Types**

| Driver Type | Associated Pins |
|---|---|
| A | FLAG[0–3], AMI_ADDR[0–23], DATA[0–15], $\overline{\text{AMI_RD}}$, $\overline{\text{AMI_WR}}$, AMI_ACK, $\overline{\text{MS}}$[1-0], $\overline{\text{SDRAS}}$, $\overline{\text{SDCAS}}$, $\overline{\text{SDWE}}$, SDDQM, SDCKE, SDA10, $\overline{\text{EMU}}$, TDO, $\overline{\text{RESETOUT}}$, DPI[1–14], DAI[1–20], $\overline{\text{WDTRSTO}}$, MLBDAT, MLBSIG, MLBSO, MLBDO, MLBCLK |
| B | SDCLK |

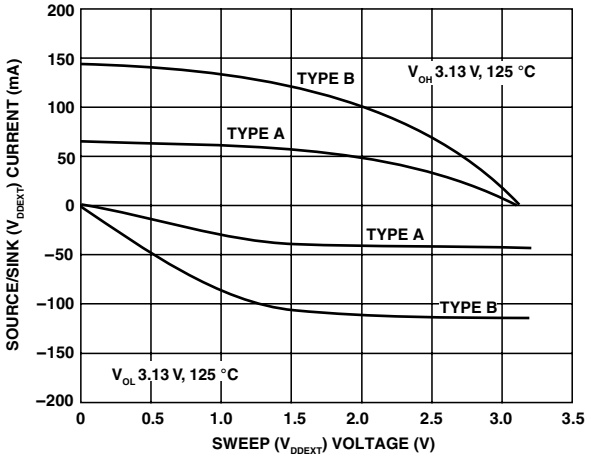


*Figure 41. Typical Drive at Junction Temperature*

## TEST CONDITIONS

The ac signal specifications (timing parameters) appear in Table 21 on Page 26 through Table 54 on Page 54. These include output disable time, output enable time, and capacitive loading. The timing specifications for the SHARC apply for the voltage reference levels in Figure 42.

Timing is measured on signals when they cross the 1.5 V level as described in Figure 43. All delays (in nanoseconds) are measured between the point that the first signal reaches 1.5 V and the point that the second signal reaches 1.5 V.

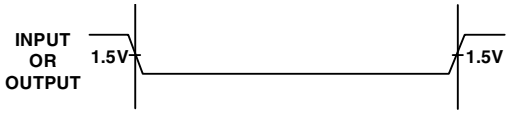


*Figure 43. Voltage Reference Levels for AC Measurements*

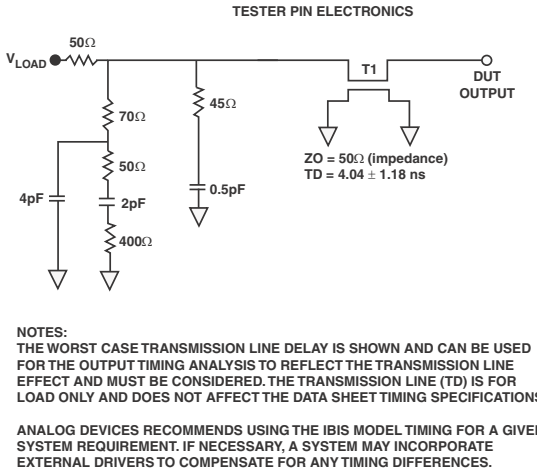


*Figure 42. Equivalent Device Loading for AC Measurements (Includes All Fixtures)*

## CAPACITIVE LOADING

Output delays and holds are based on standard capacitive loads: 30 pF on all pins (see Figure 42). Figure 46 and Figure 47 show graphically how output delays and holds vary with load capacitance. The graphs of Figure 44 through Figure 47 may not be linear outside the ranges shown for Typical Output Delay vs. Load Capacitance and Typical Output Rise Time (20% to 80%, V = Min) vs. Load Capacitance.

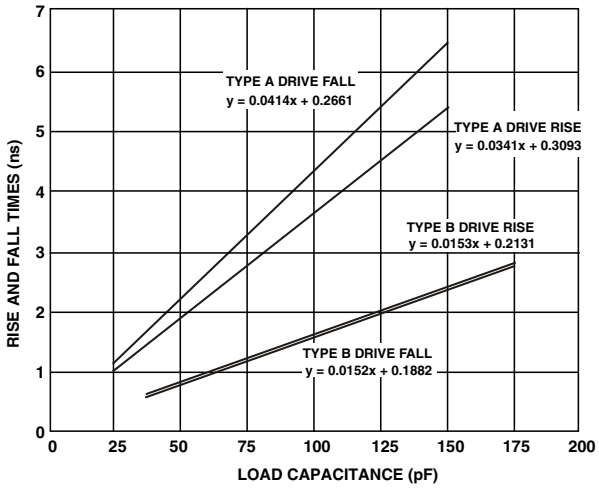


*Figure 44. Typical Output Rise/Fall Time (20% to 80%, $V_{DD_EXT}$ = Max)*

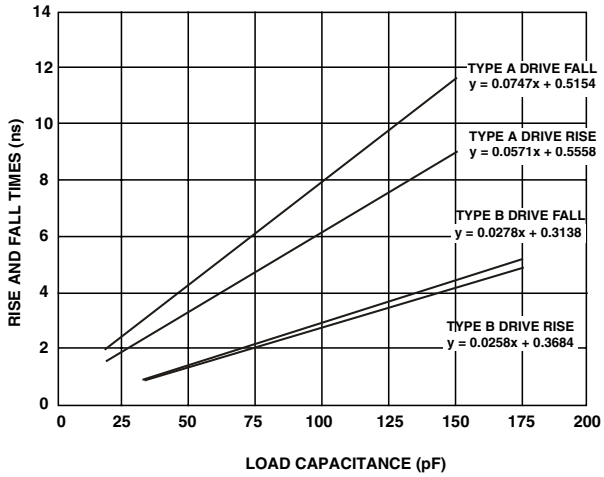


*Figure 45. Typical Output Rise/Fall Time (20% to 80%, $V_{DD_EXT}$ = Min)*

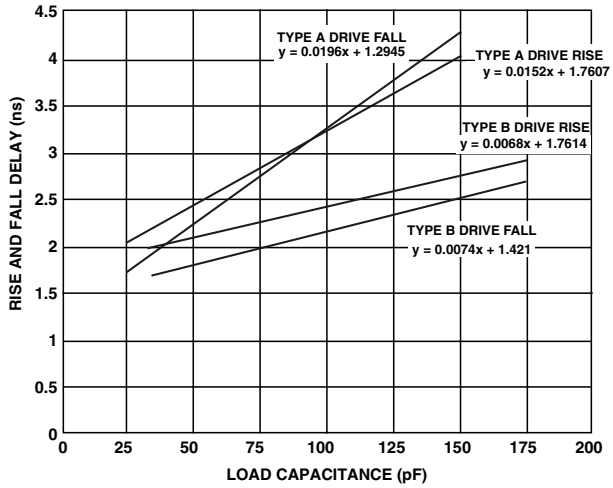


*Figure 46. Typical Output Rise/Fall Delay ($V_{DD_EXT}$ = Max)*

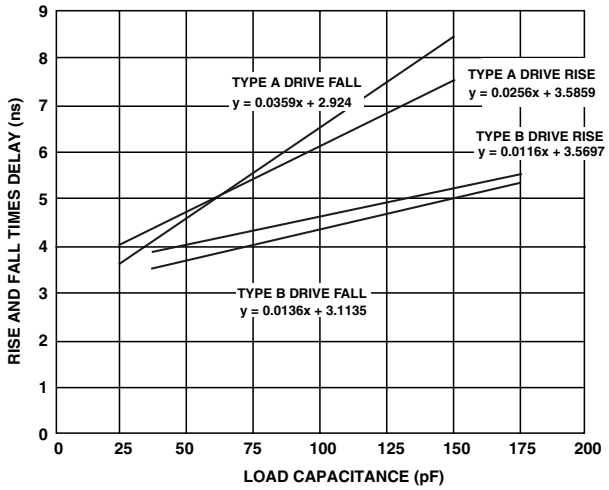


*Figure 47. Typical Output Rise/Fall Delay ($V_{DD_EXT}$ = Min)*

## THERMAL CHARACTERISTICS

The ADSP-2148x processor is rated for performance over the temperature range specified in Operating Conditions on Page 18.

Table 57 airflow measurements comply with JEDEC standards JESD51-2 and JESD51-6, and the junction-to-board measurement complies with JESD51-8. Test board design complies with JEDEC standards JESD51-7 (LQFP_EP). The junction-to-case measurement complies with MIL- STD-883. All measurements use a 2S2P JEDEC test board.

To determine the junction temperature of the device while on the application PCB, use:

$$T_J = T_{CASE} + (\Psi_{JT} \times P_D)$$

where:

$T_J$ = junction temperature °C

$T_{CASE}$ = case temperature (°C) measured at the top center of the package

$\Psi_{JT}$ = junction-to-top (of package) characterization parameter is the Typical value from Table 57.

$P_D$ = power dissipation

Values of $\theta_{JA}$ are provided for package comparison and PCB design considerations. $\theta_{JA}$ can be used for a first order approximation of $T_J$ by the equation:

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where:

$T_A$ = ambient temperature °C

Values of $\theta_{JC}$ are provided for package comparison and PCB design considerations when an external heatsink is required.

Note that the thermal characteristics values provided in Table 56 and Table 57 are modeled values.

**Table 56. Thermal Characteristics for 100-Lead LQFP_EP**

| Parameter | Condition | Typical | Unit |
|---|---|---|---|
| $\theta_{JA}$ | Airflow = 0 m/s | 17.8 | °C/W |
| $\theta_{JMA}$ | Airflow = 1 m/s | 15.4 | °C/W |
| $\theta_{JMA}$ | Airflow = 2 m/s | 14.6 | °C/W |
| $\theta_{JC}$ | | 2.4 | °C/W |
| $\Psi_{JT}$ | Airflow = 0 m/s | 0.24 | °C/W |
| $\Psi_{JMT}$ | Airflow = 1 m/s | 0.37 | °C/W |
| $\Psi_{JMT}$ | Airflow = 2 m/s | 0.51 | °C/W |

**Table 57. Thermal Characteristics for 176-Lead LQFP_EP**

| Parameter | Condition | Typical | Unit |
|---|---|---|---|
| $\theta_{JA}$ | Airflow = 0 m/s | 16.9 | °C/W |
| $\theta_{JMA}$ | Airflow = 1 m/s | 14.6 | °C/W |
| $\theta_{JMA}$ | Airflow = 2 m/s | 13.8 | °C/W |
| $\theta_{JC}$ | | 2.3 | °C/W |
| $\Psi_{JT}$ | Airflow = 0 m/s | 0.21 | °C/W |
| $\Psi_{JMT}$ | Airflow = 1 m/s | 0.32 | °C/W |
| $\Psi_{JMT}$ | Airflow = 2 m/s | 0.41 | °C/W |

### *Thermal Diode*

The ADSP-2148x processors incorporate thermal diode/s to monitor the die temperature. The thermal diode of is a grounded collector, PNP Bipolar Junction Transistor (BJT). The THD_P pin is connected to the emitter and the THD_M pin is connected to the base of the transistor. These pins can be used by an external temperature sensor (such as ADM 1021A or LM86 or others) to read the die temperature of the chip.

The technique used by the external temperature sensor is to measure the change in VBE when the thermal diode is operated at two different currents. This is shown in the following equation:

$$\Delta V_{BE} = n \times \frac{kT}{q} \times ln(N)$$

where:

$n$ = multiplication factor close to 1, depending on process variations

$k$ = Boltzmann's constant

$T$ = temperature (°C)

$q$ = charge of the electron

$N$ = ratio of the two currents

The two currents are usually in the range of 10 micro Amperes to 300 micro Amperes for the common temperature sensor chips available.

Table 58 contains the thermal diode specifications using the transistor model.

**Table 58. Thermal Diode Parameters – Transistor Model[1]**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $I_{FW}$[2] | Forward Bias Current | 10 | | 300 | µA |
| $I_E$ | Emitter Current | 10 | | 300 | µA |
| $n_Q$[3, 4] | Transistor Ideality | 1.012 | 1.015 | 1.017 | |
| $R_T$[3, 5] | Series Resistance | 0.12 | 0.2 | 0.28 | Ω |

[1] See Engineer-to-Engineer Note *"Using the On-Chip Thermal Diode on Analog Devices Processors"* (EE-346).
[2] Analog Devices does not recommend operation of the thermal diode under reverse bias.
[3] Specified by design characterization.
[4] The ideality factor, nQ, represents the deviation from ideal diode behavior as exemplified by the diode equation: $I_C = I_S \times (e^{qVBE/nqkT} - 1)$ where $I_S$ = saturation current, q = electronic charge, $V_{BE}$ = voltage across the diode, k = Boltzmann Constant, and T = absolute temperature (Kelvin).
[5] The series resistance ($R_T$) can be used for more accurate readings as needed.

# 100-LQFP_EP LEAD ASSIGNMENT

**Table 59. 100-Lead LQFP_EP Lead Assignments (Numerical by Lead Number)**

| Lead Name | Lead No. | Lead Name | Lead No. | Lead Name | Lead No. | Lead Name | Lead No. |
|---|---|---|---|---|---|---|---|
| $V_{DD_INT}$ | 1 | $V_{DD_EXT}$ | 26 | DAI_P10 | 51 | $V_{DD_INT}$ | 76 |
| CLK_CFG1 | 2 | DPI_P08 | 27 | $V_{DD_INT}$ | 52 | FLAG0 | 77 |
| BOOT_CFG0 | 3 | DPI_P07 | 28 | $V_{DD_EXT}$ | 53 | $V_{DD_INT}$ | 78 |
| $V_{DD_EXT}$ | 4 | $V_{DD_INT}$ | 29 | DAI_P20 | 54 | $V_{DD_INT}$ | 79 |
| $V_{DD_INT}$ | 5 | DPI_P09 | 30 | $V_{DD_INT}$ | 55 | FLAG1 | 80 |
| BOOT_CFG1 | 6 | DPI_P10 | 31 | DAI_P08 | 56 | FLAG2 | 81 |
| GND | 7 | DPI_P11 | 32 | DAI_P04 | 57 | FLAG3 | 82 |
| NC | 8 | DPI_P12 | 33 | DAI_P14 | 58 | MLBCLK | 83 |
| NC | 9 | DPI_P13 | 34 | DAI_P18 | 59 | MLBDAT | 84 |
| CLK_CFG0 | 10 | DAI_P03 | 35 | DAI_P17 | 60 | MLBDO | 85 |
| $V_{DD_INT}$ | 11 | DPI_P14 | 36 | DAI_P16 | 61 | $V_{DD_EXT}$ | 86 |
| CLKIN | 12 | $V_{DD_INT}$ | 37 | DAI_P15 | 62 | MLBSIG | 87 |
| XTAL | 13 | $V_{DD_INT}$ | 38 | DAI_P12 | 63 | $V_{DD_INT}$ | 88 |
| $V_{DD_EXT}$ | 14 | $V_{DD_INT}$ | 39 | $V_{DD_INT}$ | 64 | MLBSO | 89 |
| $V_{DD_INT}$ | 15 | DAI_P13 | 40 | DAI_P11 | 65 | $\overline{TRST}$ | 90 |
| $V_{DD_INT}$ | 16 | DAI_P07 | 41 | $V_{DD_INT}$ | 66 | $\overline{EMU}$ | 91 |
| $\overline{RESETOUT}$/$\overline{RUNRSTIN}$ | 17 | DAI_P19 | 42 | $V_{DD_INT}$ | 67 | TDO | 92 |
| $V_{DD_INT}$ | 18 | DAI_P01 | 43 | GND | 68 | $V_{DD_EXT}$ | 93 |
| DPI_P01 | 19 | DAI_P02 | 44 | THD_M | 69 | $V_{DD_INT}$ | 94 |
| DPI_P02 | 20 | $V_{DD_INT}$ | 45 | THD_P | 70 | TDI | 95 |
| DPI_P03 | 21 | $V_{DD_EXT}$ | 46 | $V_{DD_THD}$ | 71 | TCK | 96 |
| $V_{DD_INT}$ | 22 | $V_{DD_INT}$ | 47 | $V_{DD_INT}$ | 72 | $V_{DD_INT}$ | 97 |
| DPI_P05 | 23 | DAI_P06 | 48 | $V_{DD_INT}$ | 73 | $\overline{RESET}$ | 98 |
| DPI_P04 | 24 | DAI_P05 | 49 | $V_{DD_INT}$ | 74 | TMS | 99 |
| DPI_P06 | 25 | DAI_P09 | 50 | $V_{DD_INT}$ | 75 | $V_{DD_INT}$ | 100 |
| | | | | | | GND | 101* |

MLB pins (pins 83, 84, 85, 87, and 89) are available for automotive models only. For non-automotive models, these pins should be connected to ground (GND).
* Pin no. 101 is the GND supply (see Figure 48 and Figure 49) for the processor; this pad must be **robustly** connected to GND.

Figure 48 shows the top view of the 100-lead LQFP_EP lead configuration. Figure 49 shows the bottom view of the 100-lead LQFP_EP lead configuration.

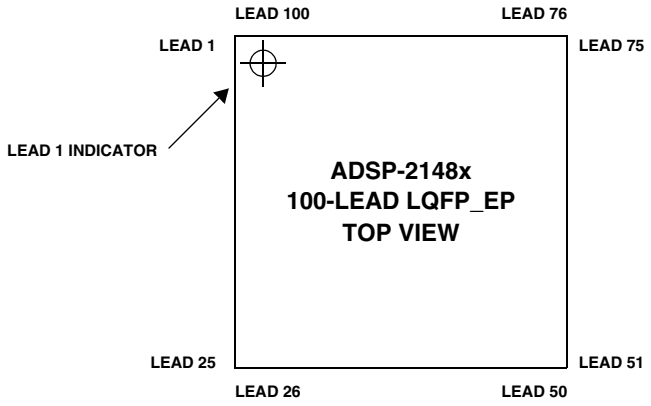


*Figure 48. 100-Lead LQFP_EP Lead Configuration (Top View)*

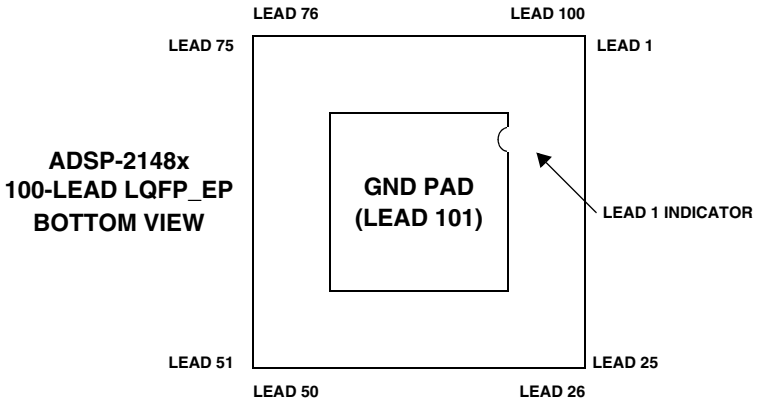


*Figure 49. 100-Lead LQFP_EP Lead Configuration (Bottom View)*

# 176-LEAD LQFP_EP LEAD ASSIGNMENT

**Table 60. ADSP-21486 176-Lead LQFP_EP Lead Assignment (Numerical by Lead Number)**

| Lead Name | Lead No. | Lead Name | Lead No. | Lead Name | Lead No. | Lead Name | Lead No. |
|---|---|---|---|---|---|---|---|
| NC | 1 | $V_{DD_EXT}$ | 45 | DAI_P10 | 89 | $V_{DD_INT}$ | 133 |
| $\overline{MS0}$ | 2 | DPI_P08 | 46 | $V_{DD_INT}$ | 90 | FLAG0 | 134 |
| NC | 3 | DPI_P07 | 47 | $V_{DD_EXT}$ | 91 | FLAG1 | 135 |
| $V_{DD_INT}$ | 4 | $V_{DD_INT}$ | 48 | DAI_P20 | 92 | FLAG2 | 136 |
| CLK_CFG1 | 5 | DPI_P09 | 49 | $V_{DD_INT}$ | 93 | GND | 137 |
| ADDR0 | 6 | DPI_P10 | 50 | DAI_P08 | 94 | FLAG3 | 138 |
| BOOT_CFG0 | 7 | DPI_P11 | 51 | DAI_P14 | 95 | GND | 139 |
| $V_{DD_EXT}$ | 8 | DPI_P12 | 52 | DAI_P04 | 96 | GND | 140 |
| ADDR1 | 9 | DPI_P13 | 53 | DAI_P18 | 97 | $V_{DD_EXT}$ | 141 |
| ADDR2 | 10 | DPI_P14 | 54 | DAI_P17 | 98 | GND | 142 |
| ADDR3 | 11 | DAI_P03 | 55 | DAI_P16 | 99 | $V_{DD_INT}$ | 143 |
| ADDR4 | 12 | NC | 56 | DAI_P12 | 100 | $\overline{TRST}$ | 144 |
| ADDR5 | 13 | $V_{DD_EXT}$ | 57 | DAI_P15 | 101 | GND | 145 |
| BOOT_CFG1 | 14 | NC | 58 | $V_{DD_INT}$ | 102 | $\overline{EMU}$ | 146 |
| GND | 15 | NC | 59 | DAI_P11 | 103 | DATA0 | 147 |
| ADDR6 | 16 | NC | 60 | $V_{DD_EXT}$ | 104 | DATA1 | 148 |
| ADDR7 | 17 | NC | 61 | $V_{DD_INT}$ | 105 | DATA2 | 149 |
| NC | 18 | $V_{DD_INT}$ | 62 | BOOT_CFG2 | 106 | DATA3 | 150 |
| NC | 19 | NC | 63 | $V_{DD_INT}$ | 107 | TDO | 151 |
| ADDR8 | 20 | NC | 64 | AMI_ACK | 108 | DATA4 | 152 |
| ADDR9 | 21 | $V_{DD_INT}$ | 65 | GND | 109 | $V_{DD_EXT}$ | 153 |
| CLK_CFG0 | 22 | NC | 66 | THD_M | 110 | DATA5 | 154 |
| $V_{DD_INT}$ | 23 | NC | 67 | THD_P | 111 | DATA6 | 155 |
| CLKIN | 24 | $V_{DD_INT}$ | 68 | $V_{DD_THD}$ | 112 | $V_{DD_INT}$ | 156 |
| XTAL | 25 | NC | 69 | $V_{DD_INT}$ | 113 | DATA7 | 157 |
| ADDR10 | 26 | $\overline{WDTRSTO}$ | 70 | $V_{DD_INT}$ | 114 | TDI | 158 |
| NC | 27 | NC | 71 | $\overline{MS1}$ | 115 | NC | 159* |
| $V_{DD_EXT}$ | 28 | $V_{DD_EXT}$ | 72 | $V_{DD_INT}$ | 116 | $V_{DD_EXT}$ | 160 |
| $V_{DD_INT}$ | 29 | DAI_P07 | 73 | WDT_CLKO | 117 | DATA8 | 161 |
| ADDR11 | 30 | DAI_P13 | 74 | WDT_CLKIN | 118 | DATA9 | 162 |
| ADDR12 | 31 | DAI_P19 | 75 | $V_{DD_EXT}$ | 119 | DATA10 | 163 |
| ADDR17 | 32 | DAI_P01 | 76 | ADDR23 | 120 | TCK | 164 |
| ADDR13 | 33 | DAI_P02 | 77 | ADDR22 | 121 | DATA11 | 165 |
| $V_{DD_INT}$ | 34 | $V_{DD_INT}$ | 78 | ADDR21 | 122 | DATA12 | 166 |
| ADDR18 | 35 | NC | 79 | $V_{DD_INT}$ | 123 | DATA14 | 167 |
| $\overline{RESETOUT}$/$\overline{RUNRSTIN}$ | 36 | NC | 80 | ADDR20 | 124 | DATA13 | 168 |
| $V_{DD_INT}$ | 37 | NC | 81 | ADDR19 | 125 | $V_{DD_INT}$ | 169 |
| DPI_P01 | 38 | NC | 82 | $V_{DD_EXT}$ | 126 | DATA15 | 170 |
| DPI_P02 | 39 | NC | 83 | ADDR16 | 127 | NC | 171 |
| DPI_P03 | 40 | $V_{DD_EXT}$ | 84 | ADDR15 | 128 | NC | 172 |
| $V_{DD_INT}$ | 41 | $V_{DD_INT}$ | 85 | $V_{DD_INT}$ | 129 | $\overline{RESET}$ | 173 |
| DPI_P05 | 42 | DAI_P06 | 86 | ADDR14 | 130 | TMS | 174 |
| DPI_P04 | 43 | DAI_P05 | 87 | $\overline{AMI_WR}$ | 131 | NC | 175 |
| DPI_P06 | 44 | DAI_P09 | 88 | $\overline{AMI_RD}$ | 132 | $V_{DD_INT}$ | 176 |
| | | | | | | GND | 177** |

*No external connection should be made to this pin. Use as NC only.

** Lead no. 177 is the GND supply (see Figure 50 and Figure 51) for the processor; this pad must be **robustly** connected to GND.

**Table 61. ADSP-21483, ADSP-21487, ADSP-21488, and ADSP-21489 176-Lead LQFP_EP Lead Assignment (Numerical by Lead Number)**

| Lead Name | Lead No. | Lead Name | Lead No. | Lead Name | Lead No. | Lead Name | Lead No. |
|---|---|---|---|---|---|---|---|
| SDDQM | 1 | $V_{DD_EXT}$ | 45 | DAI_P10 | 89 | $V_{DD_INT}$ | 133 |
| $\overline{MS0}$ | 2 | DPI_P08 | 46 | $V_{DD_INT}$ | 90 | FLAG0 | 134 |
| SDCKE | 3 | DPI_P07 | 47 | $V_{DD_EXT}$ | 91 | FLAG1 | 135 |
| $V_{DD_INT}$ | 4 | $V_{DD_INT}$ | 48 | DAI_P20 | 92 | FLAG2 | 136 |
| CLK_CFG1 | 5 | DPI_P09 | 49 | $V_{DD_INT}$ | 93 | GND | 137 |
| ADDR0 | 6 | DPI_P10 | 50 | DAI_P08 | 94 | FLAG3 | 138 |
| BOOT_CFG0 | 7 | DPI_P11 | 51 | DAI_P14 | 95 | GND | 139 |
| $V_{DD_EXT}$ | 8 | DPI_P12 | 52 | DAI_P04 | 96 | GND | 140 |
| ADDR1 | 9 | DPI_P13 | 53 | DAI_P18 | 97 | $V_{DD_EXT}$ | 141 |
| ADDR2 | 10 | DPI_P14 | 54 | DAI_P17 | 98 | GND | 142 |
| ADDR3 | 11 | DAI_P03 | 55 | DAI_P16 | 99 | $V_{DD_INT}$ | 143 |
| ADDR4 | 12 | NC | 56 | DAI_P12 | 100 | $\overline{TRST}$ | 144 |
| ADDR5 | 13 | $V_{DD_EXT}$ | 57 | DAI_P15 | 101 | GND | 145 |
| BOOT_CFG1 | 14 | NC | 58 | $V_{DD_INT}$ | 102 | $\overline{EMU}$ | 146 |
| GND | 15 | NC | 59 | DAI_P11 | 103 | DATA0 | 147 |
| ADDR6 | 16 | NC | 60 | $V_{DD_EXT}$ | 104 | DATA1 | 148 |
| ADDR7 | 17 | NC | 61 | $V_{DD_INT}$ | 105 | DATA2 | 149 |
| NC | 18 | $V_{DD_INT}$ | 62 | BOOT_CFG2 | 106 | DATA3 | 150 |
| NC | 19 | NC | 63 | $V_{DD_INT}$ | 107 | TDO | 151 |
| ADDR8 | 20 | NC | 64 | AMI_ACK | 108 | DATA4 | 152 |
| ADDR9 | 21 | $V_{DD_INT}$ | 65 | GND | 109 | $V_{DD_EXT}$ | 153 |
| CLK_CFG0 | 22 | NC | 66 | THD_M | 110 | DATA5 | 154 |
| $V_{DD_INT}$ | 23 | NC | 67 | THD_P | 111 | DATA6 | 155 |
| CLKIN | 24 | $V_{DD_INT}$ | 68 | $V_{DD_THD}$ | 112 | $V_{DD_INT}$ | 156 |
| XTAL | 25 | NC | 69 | $V_{DD_INT}$ | 113 | DATA7 | 157 |
| ADDR10 | 26 | $\overline{WDTRSTO}$ | 70 | $V_{DD_INT}$ | 114 | TDI | 158 |
| SDA10 | 27 | NC | 71 | $\overline{MS1}$ | 115 | SDCLK | 159 |
| $V_{DD_EXT}$ | 28 | $V_{DD_EXT}$ | 72 | $V_{DD_INT}$ | 116 | $V_{DD_EXT}$ | 160 |
| $V_{DD_INT}$ | 29 | DAI_P07 | 73 | WDT_CLKO | 117 | DATA8 | 161 |
| ADDR11 | 30 | DAI_P13 | 74 | WDT_CLKIN | 118 | DATA9 | 162 |
| ADDR12 | 31 | DAI_P19 | 75 | $V_{DD_EXT}$ | 119 | DATA10 | 163 |
| ADDR17 | 32 | DAI_P01 | 76 | ADDR23 | 120 | TCK | 164 |
| ADDR13 | 33 | DAI_P02 | 77 | ADDR22 | 121 | DATA11 | 165 |
| $V_{DD_INT}$ | 34 | $V_{DD_INT}$ | 78 | ADDR21 | 122 | DATA12 | 166 |
| ADDR18 | 35 | NC | 79 | $V_{DD_INT}$ | 123 | DATA14 | 167 |
| $\overline{RESETOUT}$/$\overline{RUNRSTIN}$ | 36 | NC | 80 | ADDR20 | 124 | DATA13 | 168 |
| $V_{DD_INT}$ | 37 | NC | 81 | ADDR19 | 125 | $V_{DD_INT}$ | 169 |
| DPI_P01 | 38 | NC | 82 | $V_{DD_EXT}$ | 126 | DATA15 | 170 |
| DPI_P02 | 39 | NC | 83 | ADDR16 | 127 | $\overline{SDWE}$ | 171 |
| DPI_P03 | 40 | $V_{DD_EXT}$ | 84 | ADDR15 | 128 | $\overline{SDRAS}$ | 172 |
| $V_{DD_INT}$ | 41 | $V_{DD_INT}$ | 85 | $V_{DD_INT}$ | 129 | $\overline{RESET}$ | 173 |
| DPI_P05 | 42 | DAI_P06 | 86 | ADDR14 | 130 | TMS | 174 |
| DPI_P04 | 43 | DAI_P05 | 87 | $\overline{AMI_WR}$ | 131 | $\overline{SDCAS}$ | 175 |
| DPI_P06 | 44 | DAI_P09 | 88 | $\overline{AMI_RD}$ | 132 | $V_{DD_INT}$ | 176 |
| | | | | | | GND | 177* |

* Lead no. 177 is the GND supply (see Figure 50 and Figure 51) for the processor; this pad must be **robustly** connected to GND.

**Table 62. Automotive Models ADSP-21488, and ADSP-21489 176-Lead LQFP_EP Lead Assignment (Numerical by Lead Number)**

| Lead Name | Lead No. | Lead Name | Lead No. | Lead Name | Lead No. | Lead Name | Lead No. |
|---|---|---|---|---|---|---|---|
| SDDQM | 1 | $V_{DD_EXT}$ | 45 | DAI_P10 | 89 | $V_{DD_INT}$ | 133 |
| $\overline{MS0}$ | 2 | DPI_P08 | 46 | $V_{DD_INT}$ | 90 | FLAG0 | 134 |
| SDCKE | 3 | DPI_P07 | 47 | $V_{DD_EXT}$ | 91 | FLAG1 | 135 |
| $V_{DD_INT}$ | 4 | $V_{DD_INT}$ | 48 | DAI_P20 | 92 | FLAG2 | 136 |
| CLK_CFG1 | 5 | DPI_P09 | 49 | $V_{DD_INT}$ | 93 | MLBCLK | 137 |
| ADDR0 | 6 | DPI_P10 | 50 | DAI_P08 | 94 | FLAG3 | 138 |
| BOOT_CFG0 | 7 | DPI_P11 | 51 | DAI_P14 | 95 | MLBDAT | 139 |
| $V_{DD_EXT}$ | 8 | DPI_P12 | 52 | DAI_P04 | 96 | MLBDO | 140 |
| ADDR1 | 9 | DPI_P13 | 53 | DAI_P18 | 97 | $V_{DD_EXT}$ | 141 |
| ADDR2 | 10 | DPI_P14 | 54 | DAI_P17 | 98 | MLBSIG | 142 |
| ADDR3 | 11 | DAI_P03 | 55 | DAI_P16 | 99 | $V_{DD_INT}$ | 143 |
| ADDR4 | 12 | NC | 56 | DAI_P12 | 100 | $\overline{TRST}$ | 144 |
| ADDR5 | 13 | $V_{DD_EXT}$ | 57 | DAI_P15 | 101 | MLBSO | 145 |
| BOOT_CFG1 | 14 | NC | 58 | $V_{DD_INT}$ | 102 | $\overline{EMU}$ | 146 |
| GND | 15 | NC | 59 | DAI_P11 | 103 | DATA0 | 147 |
| ADDR6 | 16 | NC | 60 | $V_{DD_EXT}$ | 104 | DATA1 | 148 |
| ADDR7 | 17 | NC | 61 | $V_{DD_INT}$ | 105 | DATA2 | 149 |
| NC | 18 | $V_{DD_INT}$ | 62 | BOOT_CFG2 | 106 | DATA3 | 150 |
| NC | 19 | NC | 63 | $V_{DD_INT}$ | 107 | TDO | 151 |
| ADDR8 | 20 | NC | 64 | AMI_ACK | 108 | DATA4 | 152 |
| ADDR9 | 21 | $V_{DD_INT}$ | 65 | GND | 109 | $V_{DD_EXT}$ | 153 |
| CLK_CFG0 | 22 | NC | 66 | THD_M | 110 | DATA5 | 154 |
| $V_{DD_INT}$ | 23 | NC | 67 | THD_P | 111 | DATA6 | 155 |
| CLKIN | 24 | $V_{DD_INT}$ | 68 | $V_{DD_THD}$ | 112 | $V_{DD_INT}$ | 156 |
| XTAL | 25 | NC | 69 | $V_{DD_INT}$ | 113 | DATA7 | 157 |
| ADDR10 | 26 | $\overline{WDTRSTO}$ | 70 | $V_{DD_INT}$ | 114 | TDI | 158 |
| SDA10 | 27 | NC | 71 | $\overline{MS1}$ | 115 | SDCLK | 159 |
| $V_{DD_EXT}$ | 28 | $V_{DD_EXT}$ | 72 | $V_{DD_INT}$ | 116 | $V_{DD_EXT}$ | 160 |
| $V_{DD_INT}$ | 29 | DAI_P07 | 73 | WDT_CLKO | 117 | DATA8 | 161 |
| ADDR11 | 30 | DAI_P13 | 74 | WDT_CLKIN | 118 | DATA9 | 162 |
| ADDR12 | 31 | DAI_P19 | 75 | $V_{DD_EXT}$ | 119 | DATA10 | 163 |
| ADDR17 | 32 | DAI_P01 | 76 | ADDR23 | 120 | TCK | 164 |
| ADDR13 | 33 | DAI_P02 | 77 | ADDR22 | 121 | DATA11 | 165 |
| $V_{DD_INT}$ | 34 | $V_{DD_INT}$ | 78 | ADDR21 | 122 | DATA12 | 166 |
| ADDR18 | 35 | NC | 79 | $V_{DD_INT}$ | 123 | DATA14 | 167 |
| $\overline{RESETOUT}$/$\overline{RUNRSTIN}$ | 36 | NC | 80 | ADDR20 | 124 | DATA13 | 168 |
| $V_{DD_INT}$ | 37 | NC | 81 | ADDR19 | 125 | $V_{DD_INT}$ | 169 |
| DPI_P01 | 38 | NC | 82 | $V_{DD_EXT}$ | 126 | DATA15 | 170 |
| DPI_P02 | 39 | NC | 83 | ADDR16 | 127 | $\overline{SDWE}$ | 171 |
| DPI_P03 | 40 | $V_{DD_EXT}$ | 84 | ADDR15 | 128 | $\overline{SDRAS}$ | 172 |
| $V_{DD_INT}$ | 41 | $V_{DD_INT}$ | 85 | $V_{DD_INT}$ | 129 | $\overline{RESET}$ | 173 |
| DPI_P05 | 42 | DAI_P06 | 86 | ADDR14 | 130 | TMS | 174 |
| DPI_P04 | 43 | DAI_P05 | 87 | $\overline{AMI_WR}$ | 131 | $\overline{SDCAS}$ | 175 |
| DPI_P06 | 44 | DAI_P09 | 88 | $\overline{AMI_RD}$ | 132 | $V_{DD_INT}$ | 176 |
| | | | | | | GND | 177* |

* Lead no. 177 is the GND supply (see Figure 50 and Figure 51) for the processor; this pad must be **robustly** connected to GND.

Figure 50 shows the top view of the 176-lead LQFP_EP lead configuration. Figure 51 shows the bottom view of the 176-lead LQFP_EP lead configuration.

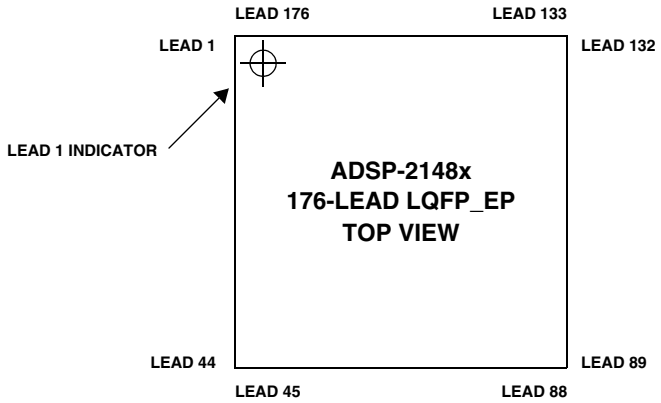


*Figure 50. 176-Lead LQFP_EP Lead Configuration (Top View)*

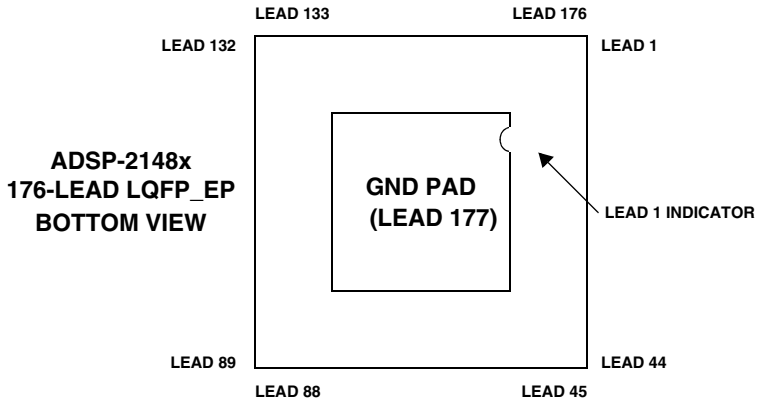


*Figure 51. 176-Lead LQFP_EP Lead Configuration (Bottom View)*

# OUTLINE DIMENSIONS

The ADSP-2148x processors are available in 100-lead and 176-lead LQFP_EP RoHS compliant packages.

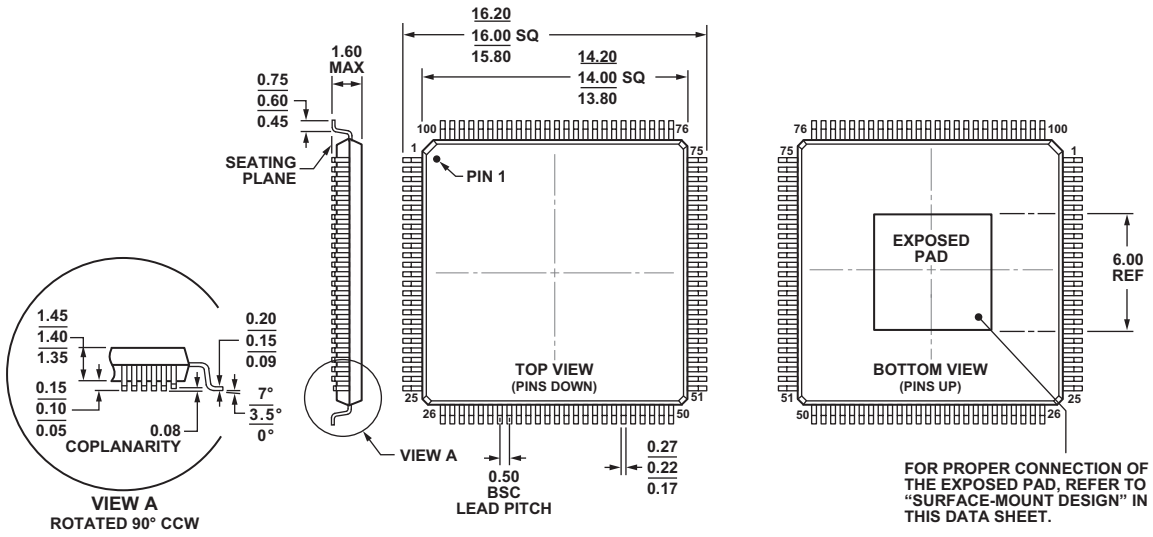


*Figure 52. 100-Lead Low Profile Quad Flat Package, Exposed Pad [LQFP_EP[1]]*
*(SW-100-2)*
*Dimensions shown in millimeters*

[1] For information relating to the exposed pad on the SW-100-2 package, see the table endnote on Page 58.

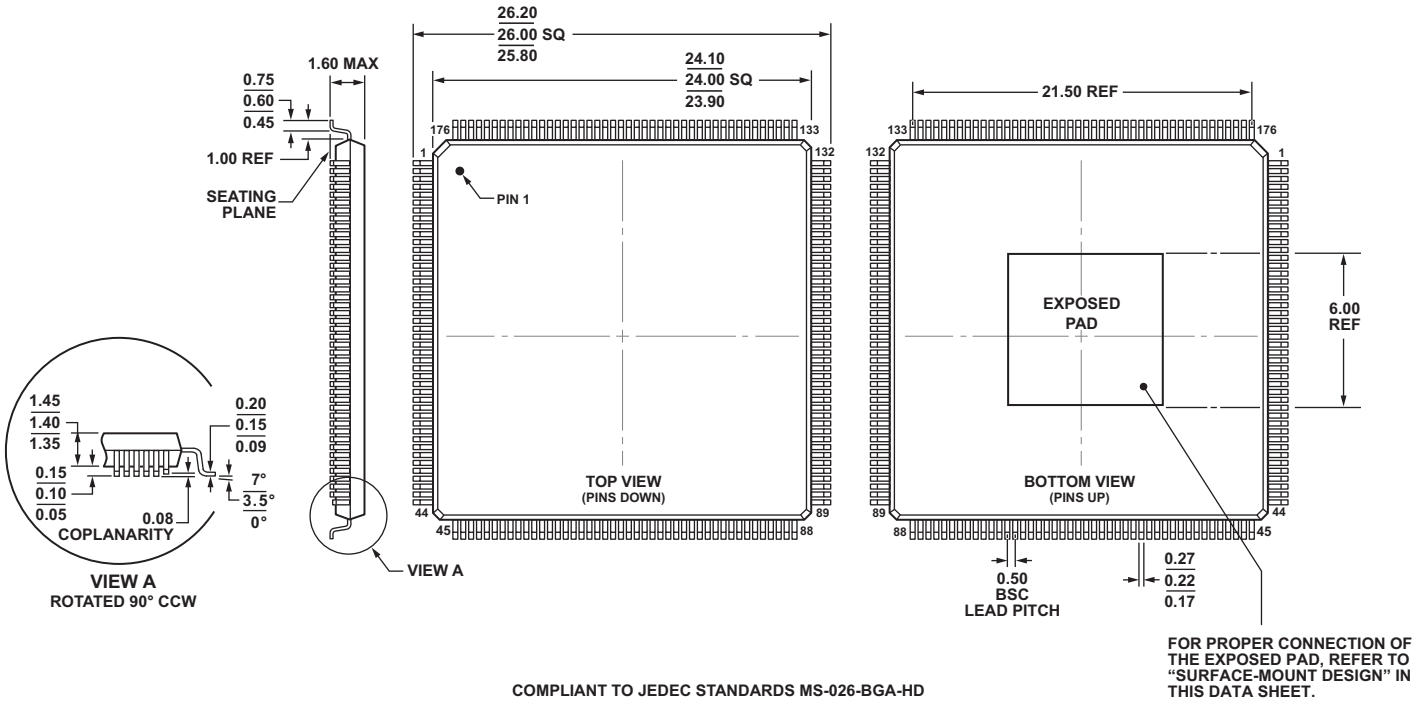


*Figure 53. 176-Lead Low Profile Quad Flat Package, Exposed Pad [LQFP_EP[1]]*
*(SW-176-2)*
*Dimensions shown in millimeters*

[1] For information relating to the exposed pad on the SW-176-2 package, see the table endnote on Page 60.

## SURFACE-MOUNT DESIGN

The exposed pad is required to be electrically and thermally connected to GND. Implement this by soldering the exposed pad to a GND PCB land that is the same size as the exposed pad. The GND PCB land should be robustly connected to the GND plane in the PCB for best electrical and thermal performance. No separate GND pins are provided in the package.

## AUTOMOTIVE PRODUCTS

The following models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models and designers should review the product Specifications section of this data sheet carefully. Only the automotive grade products shown in Table 63 are available for use in automotive applications. Contact your local ADI account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

**Table 63. Automotive Products**

| Model[1] | Notes | Temperature Range[2] | RAM | Processor Instruction Rate (Max) | Package Description | Package Option |
|---|---|---|---|---|---|---|
| AD21486WBSWZ4xx | [3] | –40°C to +85°C | 5 Mbit | 400 MHz | 100-Lead LQFP_EP | SW-100-2 |
| AD21488WBSWZ4xx | | –40°C to +85°C | 3 Mbit | 400 MHz | 100-Lead LQFP_EP | SW-100-2 |
| AD21488WBSWZ4Bxx | | –40°C to +85°C | 3 Mbit | 400 MHz | 176-Lead LQFP_EP | SW-176-2 |
| AD21489WBSWZ4xx | | –40°C to +85°C | 5 Mbit | 400 MHz | 100-Lead LQFP_EP | SW-100-2 |
| AD21489WBSWZ4Bxx | | –40°C to +85°C | 5 Mbit | 400 MHz | 176-Lead LQFP_EP | SW-176-2 |

[1] Z =RoHS compliant part.
[2] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions on Page 18 for junction temperature ($T_J$) specification which is the only temperature specification.
[3] This product contains IP from Dolby, DTS and DTLA. Proper software licenses required. Contact ADI for information.

## ORDERING GUIDE

| Model[1] | Notes | Temperature Range[2] | RAM | Processor Instruction Rate (Max) | Package Description | Package Option |
|---|---|---|---|---|---|---|
| ADSP-21483KSWZ-2B | [3] | 0°C to +70°C | 3 Mbit | 300 MHz | 176-Lead LQFP_EP | SW-176-2 |
| ADSP-21483KSWZ-3B | [3] | 0°C to +70°C | 3 Mbit | 350 MHz | 176-Lead LQFP_EP | SW-176-2 |
| ADSP-21483KSWZ-3AB | [3] | 0°C to +70°C | 3 Mbit | 350 MHz | 100-Lead LQFP_EP | SW-100-2 |
| ADSP-21483KSWZ-4B | [3] | 0°C to +70°C | 3 Mbit | 400 MHz | 176-Lead LQFP_EP | SW-176-2 |
| ADSP-21486KSWZ-2A | [3] | 0°C to +70°C | 5 Mbit | 300 MHz | 100-Lead LQFP_EP | SW-100-2 |
| ADSP-21486KSWZ-2B | [3] | 0°C to +70°C | 5 Mbit | 300 MHz | 176-Lead LQFP_EP | SW-176-2 |
| ADSP-21486KSWZ-2AB | [3] | 0°C to +70°C | 5 Mbit | 300 MHz | 100-Lead LQFP_EP | SW-100-2 |
| ADSP-21486KSWZ-2BB | [3] | 0°C to +70°C | 5 Mbit | 300 MHz | 176-Lead LQFP_EP | SW-176-2 |
| ADSP-21486KSWZ-3A | [3] | 0°C to +70°C | 5 Mbit | 350 MHz | 100-Lead LQFP_EP | SW-100-2 |
| ADSP-21486KSWZ-3B | [3] | 0°C to +70°C | 5 Mbit | 350 MHz | 176-Lead LQFP_EP | SW-176-2 |
| ADSP-21486KSWZ-3AB | [3] | 0°C to +70°C | 5 Mbit | 350 MHz | 100-Lead LQFP_EP | SW-100-2 |
| ADSP-21486KSWZ-3BB | [3] | 0°C to +70°C | 5 Mbit | 350 MHz | 176-Lead LQFP_EP | SW-176-2 |
| ADSP-21486KSWZ-4A | [3] | 0°C to +70°C | 5 Mbit | 400 MHz | 100-Lead LQFP_EP | SW-100-2 |
| ADSP-21486KSWZ-4AB | [3] | 0°C to +70°C | 5 Mbit | 400 MHz | 100-Lead LQFP_EP | SW-100-2 |
| ADSP-21487KSWZ-2B | [3] | 0°C to +70°C | 5 Mbit | 300 MHz | 176-Lead LQFP_EP | SW-176-2 |
| ADSP-21487KSWZ-2BB | [3] | 0°C to +70°C | 5 Mbit | 300 MHz | 176-Lead LQFP_EP | SW-176-2 |
| ADSP-21487KSWZ-3B | [3] | 0°C to +70°C | 5 Mbit | 350 MHz | 176-Lead LQFP_EP | SW-176-2 |
| ADSP-21487KSWZ-3BB | [3] | 0°C to +70°C | 5 Mbit | 350 MHz | 176-Lead LQFP_EP | SW-176-2 |
| ADSP-21487KSWZ-4B | [3] | 0°C to +70°C | 5 Mbit | 400 MHz | 176-Lead LQFP_EP | SW-176-2 |
| ADSP-21487KSWZ-4BB | [3] | 0°C to +70°C | 5 Mbit | 400 MHz | 176-Lead LQFP_EP | SW-176-2 |
| ADSP-21487KSWZ-5B | [3, 4] | 0°C to +70°C | 5 Mbit | 450 MHz | 176-Lead LQFP_EP | SW-176-2 |
| ADSP-21487KSWZ-5BB | [3, 4] | 0°C to +70°C | 5 Mbit | 450 MHz | 176-Lead LQFP_EP | SW-176-2 |

| Model[1] | Notes | Temperature Range[2] | RAM | Processor Instruction Rate (Max) | Package Description | Package Option |
|---|---|---|---|---|---|---|
| ADSP-21488BSWZ-3A | | –40°C to +85°C | 3 Mbit | 350 MHz | 100-Lead LQFP_EP | SW-100-2 |
| ADSP-21488KSWZ-3A | | 0°C to +70°C | 3 Mbit | 350 MHz | 100-Lead LQFP_EP | SW-100-2 |
| ADSP-21488KSWZ-3A1 | 5 | 0°C to +70°C | 3 Mbit | 350 MHz | 100-Lead LQFP_EP | SW-100-2 |
| ADSP-21488KSWZ-3B | | 0°C to +70°C | 3 Mbit | 350 MHz | 176-Lead LQFP_EP | SW-176-2 |
| ADSP-21488BSWZ-3B | | –40°C to +85°C | 3 Mbit | 350 MHz | 176-Lead LQFP_EP | SW-176-2 |
| ADSP-21488KSWZ-4A | | 0°C to +70°C | 3 Mbit | 400 MHz | 100-Lead LQFP_EP | SW-100-2 |
| ADSP-21488BSWZ-4A | | –40°C to +85°C | 3 Mbit | 400 MHz | 100-Lead LQFP_EP | SW-100-2 |
| ADSP-21488KSWZ-4B | | 0°C to +70°C | 3 Mbit | 400 MHz | 176-Lead LQFP_EP | SW-176-2 |
| ADSP-21488BSWZ-4B | | –40°C to +85°C | 3 Mbit | 400 MHz | 176-Lead LQFP_EP | SW-176-2 |
| ADSP-21488KSWZ-4B1 | 5 | 0°C to +70°C | 3 Mbit | 400 MHz | 176-Lead LQFP_EP | SW-176-2 |
| ADSP-21489KSWZ-3A | | 0°C to +70°C | 5 Mbit | 350 MHz | 100-Lead LQFP_EP | SW-100-2 |
| ADSP-21489BSWZ-3A | | –40°C to +85°C | 5 Mbit | 350 MHz | 100-Lead LQFP_EP | SW-100-2 |
| ADSP-21489KSWZ-3B | | 0°C to +70°C | 5 Mbit | 350 MHz | 176-Lead LQFP_EP | SW-176-2 |
| ADSP-21489BSWZ-3B | | –40°C to +85°C | 5 Mbit | 350 MHz | 176-Lead LQFP_EP | SW-176-2 |
| ADSP-21489KSWZ-4A | | 0°C to +70°C | 5 Mbit | 400 MHz | 100-Lead LQFP_EP | SW-100-2 |
| ADSP-21489BSWZ-4A | | –40°C to +85°C | 5 Mbit | 400 MHz | 100-Lead LQFP_EP | SW-100-2 |
| ADSP-21489KSWZ-4B | | 0°C to +70°C | 5 Mbit | 400 MHz | 176-Lead LQFP_EP | SW-176-2 |
| ADSP-21489BSWZ-4B | | –40°C to +85°C | 5 Mbit | 400 MHz | 176-Lead LQFP_EP | SW-176-2 |
| ADSP-21489KSWZ-5B | 4 | 0°C to +70°C | 5 Mbit | 450 MHz | 176-Lead LQFP_EP | SW-176-2 |

[1] Z = RoHS compliant part.

[2] Referenced temperature is ambient temperature. The ambient temperature is not a specification. Please see Operating Conditions on Page 18 for junction temperature ($T_J$) specification, which is the only temperature specification.

[3] The ADSP-21483, ADSP-21486, and ADSP-21487 models are available with factory programmed ROM including the latest multichannel audio decoding and post-processing algorithms from Dolby Labs and DTS. ROM contents may vary depending on chip version and silicon revision. Please visit www.analog.com for complete information.

[4] See Engineer-to-Engineer Note *"Static Voltage Scaling for ADSP-2148x Processors"* (EE-357) for operating ADSP-2148x processors at 450 MHz.

[5] This product contains a –140 dB sample rate converter.

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D09018-0-3/13(B)

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