MCP25612FD

Dual CAN Flexible Data-Rate Transceiver

Features

- Supports both “classic” CAN 2.0 and CAN FD physical layer requirements
- Optimized for CAN FD (Flexible Data-Rate) at 2, 5 and 8 Mbps Operation:
  - Maximum Propagation Delay: 120 ns
  - Loop Delay Symmetry: -10%/+10% (2 Mbps)
- Implements ISO-11898-2 and ISO-11898-5 Standard Physical Layer Requirements
- Very Low Standby Current (5 µA per transceiver, typical)
- Two Fully Independent V_{DDX} and V_{SSX} Pins per CAN FD Transceiver for Added Flexibility and Reliability:
  - Optimal for redundant CAN networks
- Compatible to 5V MCUs
- Functional Behavior Predictable Under All Supply Conditions:
  - Device is in Unpowered mode if V_{DDX} drops below undervoltage level
  - An unpowered node or brown-out event will not load the CAN bus
- Detection of Ground Fault:
  - Permanent dominant detection on T_{XDX}
  - Permanent dominant detection on bus
- Power-on Reset and Undervoltage Lock-out on V_{DDX} Pin
- Protection against Damage due to Short-Circuit Conditions (positive or negative battery voltage)
- Protection against High-Voltage Transients in Automotive Environments
- Automatic Thermal Shutdown Protection
- Suitable for 12V and 24V Systems
- Meets or exceeds Stringent Automotive Design Requirements, including *“Hardware Requirements for LIN, CAN and FlexRay™ Interfaces in Automotive Applications”*, Version 1.3, May 2012:
  - Conducted emissions @ 2 Mbps with Common-Mode Choke (CMC)
  - Direct Power Injection (DPI) @ 2 Mbps with CMC
- Meets SAE J2962/2 *“Communication Transceivers Qualification Requirements – CAN”*:
  - Passes radiated emissions at 2 Mbps without a CMC
- High Noise Immunity due to Differential Bus Implementation
- High ESD Protection on CANHx and CANLx, Meets IEC61000-4-2, up to ±6 kV
- Available in 14-Lead SOIC
- Temperature Ranges:
  - Extended (E): -40°C to +125°C
  - High (H): -40°C to +150°C

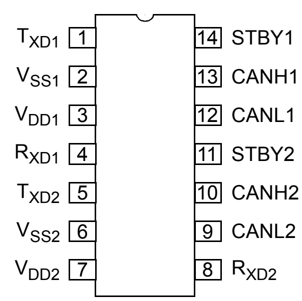
Description

The MCP25612FD is a second generation, dual CAN FD transceiver from Microchip Technology Inc. It offers all of the features from two fully independent MCP2561FD CAN transceivers, except for the SPLIT pin. It ensures Loop Delay Symmetry in order to support the higher data rates required for CAN FD. The maximum propagation delay is improved to support a longer bus length.

The device meets the automotive requirements for CAN FD bit rates, low quiescent current, robust Electromagnetic Compatibility (EMC) and Electrostatic Discharge (ESD).

Package Types

MCP25612FD
SOIC



Typical Applications

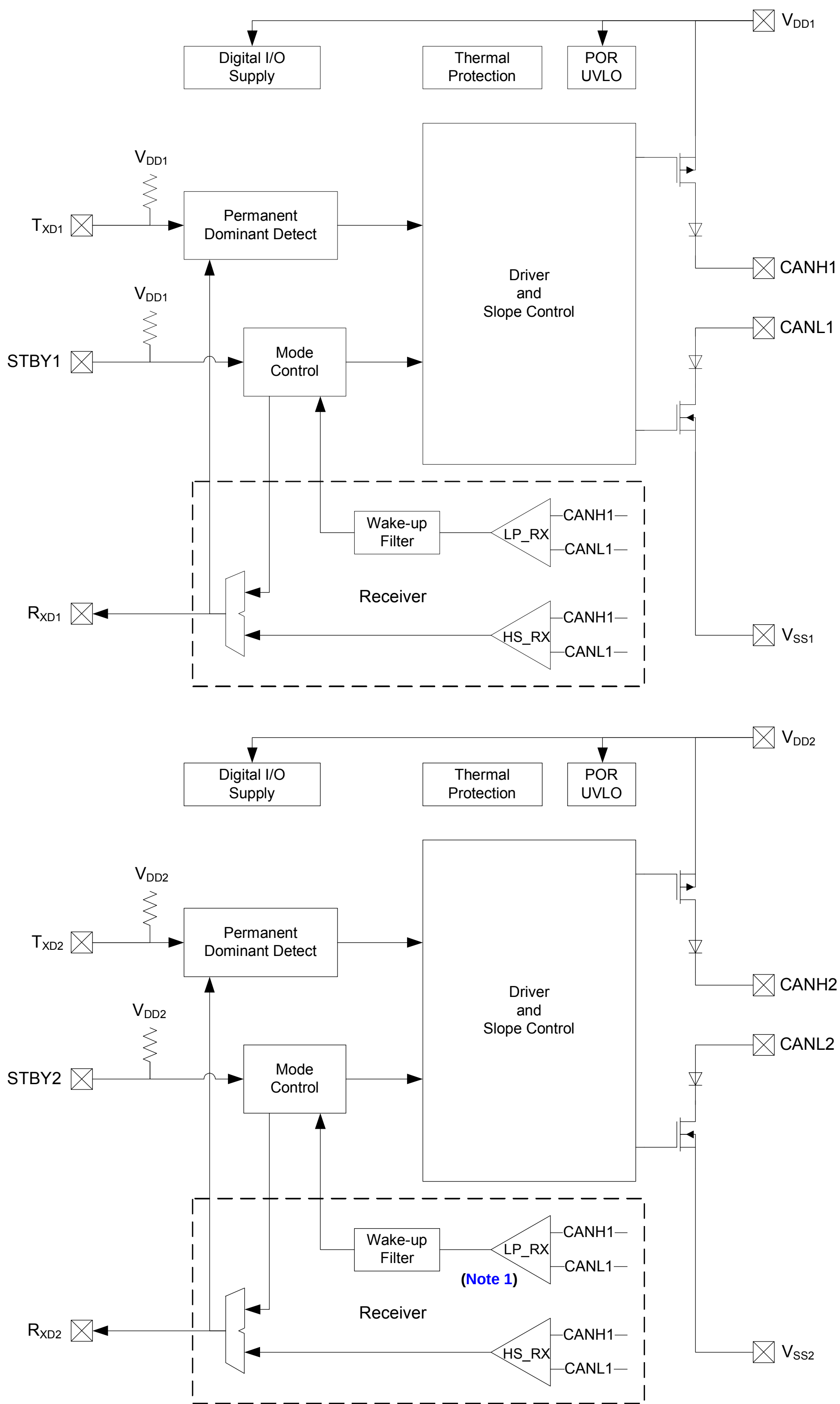
<u>Automotive</u>

- Powertrain
- Body Control
- Gateway
- Chassis and Safety
- Infotainment

<u>Industrial</u>

- Factory Automation
- Gateway
- Server Backplanes
- Elevators
- Robotics

Device Block Diagram



Note 1: There is only one receiver implemented. The receiver can operate in either Low-Power or High-Speed mode.

1.0 DEVICE OVERVIEW

The MCP25612FD is a dual fully independent, CAN FD transceiver Fault tolerant device that serves as the interface between a CAN protocol controller and the physical bus. The MCP25612FD device provides differential transmit and receive capability for the CAN protocol controller, and is fully compatible with the ISO 11898-2 and ISO 11898-5 standards.

The Loop Delay Symmetry is ensured to support data rates up to 8 Mbps for CAN FD (Flexible Data-Rate). The maximum propagation delay was improved to support longer bus length.

Typically, each node in a CAN system must have a device to convert the digital signals generated by a CAN controller to signals suitable for transmission over the bus cabling (differential output). It also provides a buffer between the CAN controller and the high-voltage spikes that can be generated on the CAN bus by outside sources.

1.1 Mode Control Block

The MCP25612FD supports two modes of operation between the two CAN transceivers independently:

- Normal Mode
- Standby Mode

These modes are summarized in Table 1-1.

1.1.1 NORMAL MODE

Normal mode is selected by applying low-level voltage to the STBYx pin. The driver block is operational and can drive the bus pins. The slopes of the output signals on CANHx and CANLx are optimized to produce minimal Electromagnetic Emissions (EME).

The high-speed differential receiver is active.

1.1.2 STANDBY MODE

The device may be placed in Standby mode by applying a high-level voltage to the STBYx pin. In Standby mode, the transmitter and the high-speed part of the receiver are switched off to minimize power consumption. The low-power receiver and the wake-up filter blocks are enabled to monitor the bus for activity. The Receive pin (R_{XDX}) will show a delayed representation of the CAN bus due to the wake-up filter.

The CAN controller gets interrupted by a negative edge on the R_{XDX} pin (Dominant state on the CAN bus). The CAN controller must put the MCP25612FD back into Normal mode, using the STBYx pin, in order to enable high-speed data communication.

The CAN bus wake-up function requires V_{DDX} to be in valid range.

TABLE 1-1: MODES OF OPERATION

Mode	STBYx Pin	R_{XDX} Pin	
		Low	High
Normal	Low	Bus is dominant	Bus is recessive
Standby	High	Wake-up request is detected	No wake-up request detected

1.2 Transmitter Function

The CAN bus has two states:

- Dominant state
- Recessive state

A Dominant state occurs when the differential voltage between CANHx and CANLx is greater than $V_{DIFFX(D)(I)}$. A Recessive state occurs when the differential voltage is less than $V_{DIFFX(R)(I)}$. The Dominant and Recessive states correspond to the Low and High state of the T_{XDX} input pin, respectively. However, a Dominant state initiated by another CAN node will override a Recessive state on the CAN bus.

1.3 Receiver Function

In Normal mode, the R_{XDX} output pin reflects the differential bus voltage between CANHx and CANLx. The Low and High states of the R_{XDX} output pin correspond to the Dominant and Recessive states of the CAN bus, respectively.

1.4 Internal Protection

CANHx and CANLx are protected against battery short circuits and electrical transients that can occur on the CAN bus. This feature prevents destruction of the transmitter output stage during such a Fault condition.

The device is further protected from excessive current loading by thermal shutdown circuitry that disables the output drivers when the junction temperature exceeds a nominal limit of +175°C. All other parts of the chip remain operational and the chip temperature is lowered due to the decreased power dissipation in the transmitter outputs. This protection is essential to protect against bus line short-circuit induced damage. The activation of the internal protection in one of the transceivers will not affect the other one since these are fully independent.

1.5 Permanent Dominant Detection

The MCP25612FD device prevents two conditions:

- Permanent dominant condition on T_{XDX}
- Permanent dominant condition on the bus

In Normal mode, if the MCP25612FD detects an extended Low state on the T_{XDX} input, it will disable the CANHx and CANLx output drivers in order to prevent the corruption of data on the CAN bus. The drivers will remain disabled until T_{XDX} goes to the High state.

In Standby mode, if the MCP25612FD detects an extended Dominant condition on the bus, it will set the R_{XDX} pin to the Recessive state. This allows the attached controller to go to Low-Power mode until the dominant issue is corrected. R_{XDX} is latched high until a Recessive state is detected on the bus and the wake-up function is enabled again.

Both conditions have a time-out of 1.25 ms (typical). This implies a maximum bit time of 69.44 µs (14.4 kHz), allowing up to 18 consecutive dominant bits on the bus. The permanent dominant detection in one of the transceivers will not affect the other one since these are fully independent.

1.6 Power-on Reset (POR) and Undervoltage Detection

The MCP25612FD has undervoltage detection on the V_{DDX} supply pin. The typical undervoltage threshold is 4V.

When the device is powered on, CANHx and CANLx remain in a High-Impedance state until V_{DDX} exceeds its undervoltage level. Once powered on, CANHx and CANLx will enter a High-Impedance state if the voltage level at V_{DDX} drops below the undervoltage level, providing voltage brown-out protection during normal operation.

In Normal mode, the receiver output is forced to the Recessive state during an undervoltage condition on V_{DDX}. In Standby mode, the low-power receiver is only enabled when the V_{DDX} supply voltage rises above its undervoltage threshold. Once the threshold voltage is reached, the low-power receiver is no longer controlled by the POR comparator and remains operational down to about 2.5V on the V_{DDX} supply.

2.0 ELECTRICAL CHARACTERISTICS

2.1 Absolute Maximum Ratings†

V_{DDX} 7.0V
DC Voltage at T_{XDX}, R_{XDX}, STBYx and V_{SSX} .... -0.3V to V_{DDX} + 0.3V
DC Voltage at CANHx and CANLx .... -58V to +58V
Transient Voltage on CANHx, CANLx (ISO-7637) (see Figure 2-4) .... -150V to +100V
Storage Temperature .... -55°C to +150°C
Operating Ambient Temperature .... -40°C to +150°C
Virtual Junction Temperature, T_{VJ} (IEC60747-1) .... -40°C to +190°C
Soldering Temperature of Leads (10 seconds) .... +300°C
ESD Protection on CANHx and CANLx Pins (IEC 61000-4-2); 330Ω/150 pF; Unpowered; Contact Discharge .... ±6 kV
ESD Protection on CANHx and CANLx Pins (IEC 801; Human Body Model); 1500Ω/100 pF .... ±8 kV
ESD Protection on All Other Pins (IEC 801; Human Body Model); 1500Ω/100 pF .... ±4 kV
ESD Protection on All Pins (IEC 801; Machine Model); 0Ω/200 pF .... ±300V
ESD Protection on All Pins (IEC 801; Charge Device Model) .... ±750V

† **NOTICE:** Stresses above those listed under “Maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2.2 Specifications

TABLE 2-1: DC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Extended (E): T_{AMB} = -40°C to +125°C; High (H): T_{AMB} = -40°C to +150°C; V_{DDX} = 4.5V to 5.5V, R_{LX} = 60Ω, C_{LX} = 100 pF; unless otherwise specified.

Characteristic	Sym	Min	Typ	Max	Units	Conditions
Supply (V_{DDX} Pin)						
Voltage Range	V_{DDX}	4.5	—	5.5		
Supply Current (per transceiver)	I_{DD}	—	5	10	mA	Recessive; V_{TXDX} = V_{DDX}
		—	45	70		Dominant; V_{TXDX} = 0V
Standby Current (per transceiver)	I_{DDS}	—	5	15	µA	
High Level of the POR Comparator	V_{PORH}	3.8	—	4.3	V	
Low Level of the POR Comparator	V_{PORL}	3.4	—	4.0	V	
Hysteresis of the POR Comparator	V_{PORD}	0.3	—	0.8	V	

Note 1: Characterized; not 100% tested.
2: -12V to 12V is ensured by characterization, tested from -2V to 7V.

TABLE 2-1: DC ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Extended (E): T_{AMB} = -40°C to +125°C; High (H): T_{AMB} = -40°C to +150°C;
V_{DDX} = 4.5V to 5.5V, R_{LX} = 60Ω, C_{LX} = 100 pF; unless otherwise specified.

Characteristic	Sym	Min	Typ	Max	Units	Conditions
Bus Line Transmitter (CANHx, CANLx)						
CANHx, CANLx: Recessive Bus Output Voltage	$V_{O(R)}$	2.0	0.5 V_{DDX}	3.0	V	V_{TXDX} = V_{DDX}; no load
CANHx, CANLx: Bus Output Voltage in Standby	$V_{O(S)}$	-0.1	0.0	+0.1	V	STBYx = V_{TXDX} = V_{DDX}; no load
Recessive Output Current	$I_{O(R)}$	-5	—	+5	mA	-24V < V_{CAN} < +24V
CANHx: Dominant Output Voltage	$V_{O(D)}$	2.75	3.50	4.50	V	T_{TXDX} = 0; R_{LX} = 50 to 65Ω
CANLx: Dominant Output Voltage		0.50	1.50	2.25		R_{LX} = 50 to 65Ω
Symmetry of Dominant Output Voltage ($V_{DDX} – V_{CANHX} – V_{CANLX}$)	$V_{O(D)(M)}$	-400	0	+400	mV	V_{TXDX} = V_{SSX} **(Note 1)**
Dominant: Differential Output Voltage	$V_{O(DIFF)}$	1.5	2.0	3.0	V	V_{TXDX} = V_{SSX}; R_{LX} = 50 to 65Ω (see Figure 2-1 and Figure 2-3)
Recessive: Differential Output Voltage		-120	0	12	mV	V_{TXDX} = V_{DDX} (see Figure 2-1 and Figure 2-3)
		-500	0	50	mV	V_{TXDX} = V_{DDX}; no load (see Figure 2-1 and Figure 2-3)
CANHx: Short-Circuit Output Current	$I_{O(SC)}$	-120	85	—	mA	V_{TXDX} = V_{SSX}; V_{CANHX} = 0V; CANLx: Floating
		-100	—	—	mA	Same as above, but V_{DDX} = 5V; T_{AMB} = +25°C **(Note 1)**
CANLx: Short-Circuit Output Current		—	75	+120	mA	V_{TXDX} = V_{SSX}; V_{CANLX} = 18V; CANHx: Floating
		—	—	+100	mA	Same as above, but V_{DDX} = 5V; T_{AMB} = +25°C **(Note 1)**
Bus Line Receiver (CANHx, CANLx)						
Recessive Differential Input Voltage	$V_{DIFFX(R)(I)}$	-1.0	—	+0.5	V	Normal mode; -12V < $V_{(CANHX, CANLX)}$ < +12V (see Figure 2-5) **(Note 2)**
		-1.0	—	+0.4		Standby mode; -12V < $V_{(CANHX, CANLX)}$ < +12V (see Figure 2-5) **(Note 2)**
Dominant Differential Input Voltage	$V_{DIFFX(D)(I)}$	0.9	—	V_{DDX}	V	Normal mode; -12V < $V_{(CANHX, CANLX)}$ < +12V (see Figure 2-5) **(Note 2)**
		1.0	—	V_{DDX}		Standby mode; -12V < $V_{(CANHX, CANLX)}$ < +12V (see Figure 2-5) **(Note 2)**

Note 1: Characterized; not 100% tested.
2: -12V to 12V is ensured by characterization, tested from -2V to 7V.

TABLE 2-1: DC ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Extended (E): T_{AMB} = -40°C to +125°C; High (H): T_{AMB} = -40°C to +150°C; V_{DDX} = 4.5V to 5.5V, R_{LX} = 60Ω, C_{LX} = 100 pF; unless otherwise specified.

Characteristic	Sym	Min	Typ	Max	Units	Conditions
Bus Line Receiver (CANHx, CANLx) (Continued)						
Differential Receiver Threshold	$V_{TH(DIFF)}$	0.5	0.7	0.9	V	Normal mode; -12V < $V_{(CANHX, CANLX)}$ < +12V (see Figure 2-5) (**Note 2**)
		0.4	—	1.0		Standby mode; -12V < $V_{(CANHX, CANLX)}$ < +12V (see Figure 2-5) (**Note 2**)
Differential Input Hysteresis	$V_{HYS(DIFF)}$	50	—	200	mV	Normal mode (see Figure 2-5) (**Note 1**)
Common-Mode Input Resistance	R_{IN}	10	—	30	kΩ	(**Note 1**)
Common-Mode Resistance Matching	$R_{IN(M)}$	-1	0	+1	%	$V_{CANHX} = V_{CANLX}$ (**Note 1**)
Differential Input Resistance	$R_{IN(DIFF)}$	10	—	100	kΩ	(**Note 1**)
Common-Mode Input Capacitance	$C_{IN(CM)}$	—	—	20	pF	$V_{TXDX} = V_{DDX}$ (**Note 1**)
Differential Input Capacitance	$C_{IN(DIFF)}$	—	—	10		$V_{TXDX} = V_{DDX}$ (**Note 1**)
CANHx, CANLx: Input Leakage	I_{LI}	-5	—	+5	µA	$V_{DDX} = V_{TXDX} = V_{STBYX}$ = 0V; $V_{CANHX} = V_{CANLX}$ = 5V
Digital Input Pins (T_{XDX}, STBYx)						
High-Level Input Voltage	V_{IH}	0.7 V_{DDX}	—	V_{DDX} + 0.3	V	
Low-Level Input Voltage	V_{IL}	-0.3	—	0.3 V_{DDX}	V	
High-Level Input Current	I_{IH}	-1	—	+1	µA	
T_{XDX}: Low-Level Input Current	$I_{IL(TXDX)}$	-270	-150	-30	µA	
STBYx: Low-Level Input Current	$I_{IL(STBYX)}$	-30	—	-1	µA	
Receive Data Output (R_{XDX})						
High-Level Output Voltage	V_{OHX}	V_{DDX} – 0.4	—	—	V	I_{OH} = -2 mA; typical -4 mA
Low-Level Output Voltage	V_{OLX}	—	—	0.4	V	I_{OL} = 4 mA; typical 8 mA
Thermal Shutdown						
Shutdown Junction Temperature	$T_{J(SD)}$	165	175	185	°C	-12V < $V_{(CANHX, CANLX)}$ < +12V (**Note 1**)
Shutdown Temperature Hysteresis	$T_{J(HYST)}$	20	—	30	°C	-12V < $V_{(CANHX, CANLX)}$ < +12V (**Note 1**)

Note 1: Characterized; not 100% tested.

2: -12V to 12V is ensured by characterization, tested from -2V to 7V.

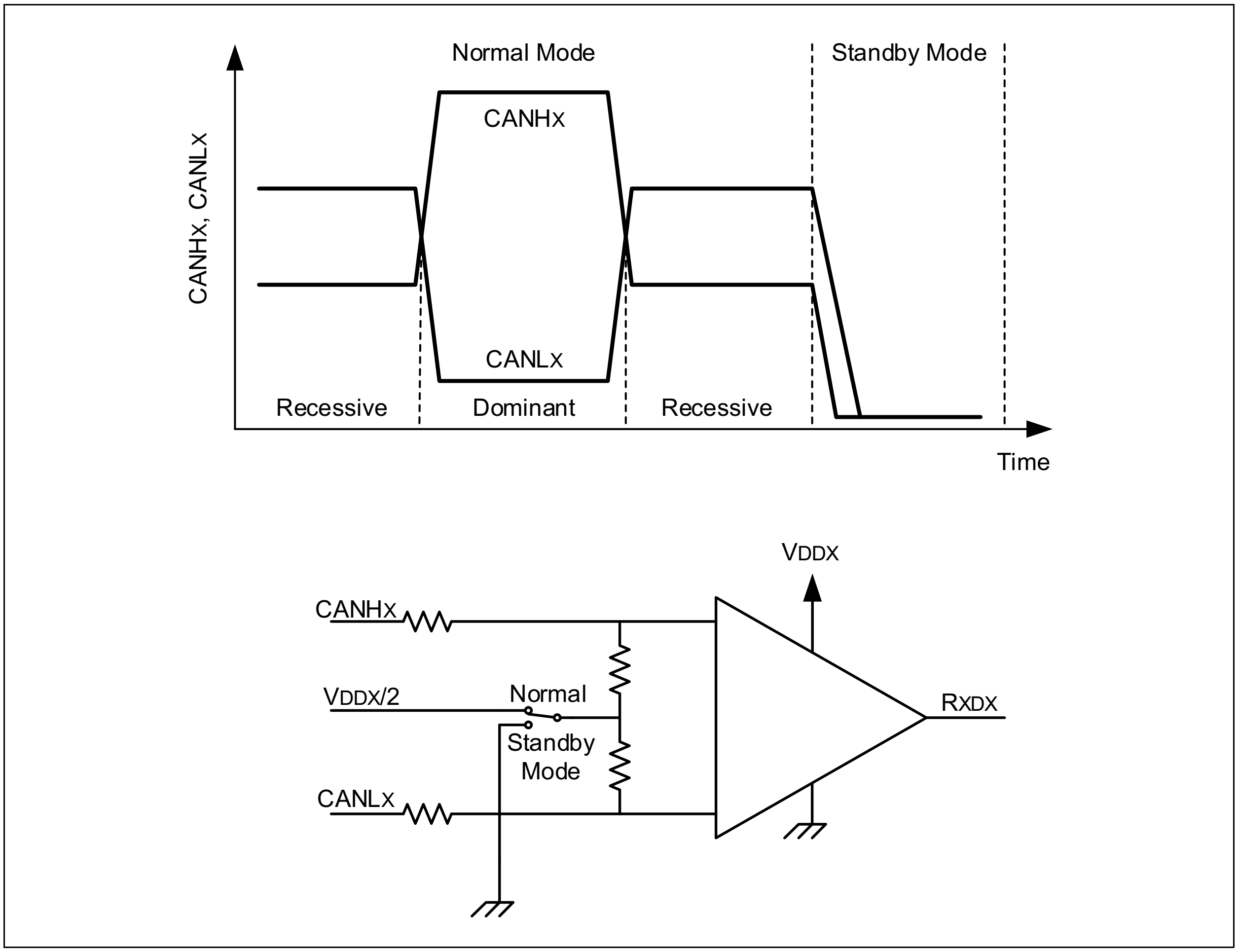


FIGURE 2-1: *Physical Bit Representation and Simplified Bias Implementation.*

TABLE 2-2: AC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Extended (E): T_{AMB} = -40°C to +125°C; High (H): T_{AMB} = -40°C to +150°C; V_{DDX} = 4.5V to 5.5V, R_{LX} = 60Ω, C_{LX} = 100 pF; unless otherwise specified.							
Param. No.	**Sym**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
1	t_{BIT}	Bit Time	0.125	—	69.44	µs	
2	f_{BIT}	Bit Frequency	14.4	—	8000	kHz	
3	$t_{TXDX-BUSON}$	Delay T_{XDX} Low to Bus Dominant	—	65	—	ns	**(Note 1)**
4	$t_{TXDX-BUSOFF}$	Delay T_{XDX} High to Bus Recessive	—	90	—	ns	**(Note 1)**
5	$t_{BUSON-RXDX}$	Delay Bus Dominant to R_{XDX}	—	60	—	ns	**(Note 1)**
6	$t_{BUSOFF-RXDX}$	Delay Bus Recessive to R_{XDX}	—	65	—	ns	**(Note 1)**
7	$t_{TXDX-RXDX}$	Propagation Delay T_{XDX} to R_{XDX}	—	90	120	ns	
			—	120	180	ns	R_{LX} = 120Ω, C_{LX} = 200 pF **(Note 1)**
8a	$t_{BIT(RXDX),2M}$	Recessive Bit Time on R_{XDX} – 2 Mbps, Loop Delay Symmetry	450	485	550	ns	$t_{BIT(TXDX)}$ = 500 ns (see Figure 2-10)
			400	460	550	ns	$t_{BIT(TXDX)}$ = 500 ns (see Figure 2-10); R_{LX} = 120Ω, C_{LX} = 200 pF **(Note 1)**
8b	$t_{BIT(RXDX),5M}$	Recessive Bit Time on R_{XDX} – 5 Mbps, Loop Delay Symmetry	160	185	220	ns	$t_{BIT(TXDX)}$ = 200 ns (see Figure 2-10)
8c	$t_{BIT(RXDX),8M}$	Recessive Bit Time on R_{XDX} – 8 Mbps, Loop Delay Symmetry	85	105	140	ns	$t_{BIT(TXDX)}$ = 120 ns (see Figure 2-10) **(Note 1)**
9	$t_{FLTR(WAKE)}$	Delay Bus Dominant to R_{XDX} (Standby mode)	0.5	1	4	µs	Standby mode
10	t_{WAKE}	Delay Standby to Normal Mode	5	25	40	µs	Negative edge on STBYx
11	t_{PDT}	Permanent Dominant Detect Time	—	1.25	—	ms	T_{XDX} = 0V
12	t_{PDTR}	Permanent Dominant Timer Reset	—	100	—	ns	The shortest Recessive pulse on T_{XDX} or CAN bus to reset Permanent Dominant Timer

Note 1: Characterized, not 100% tested.

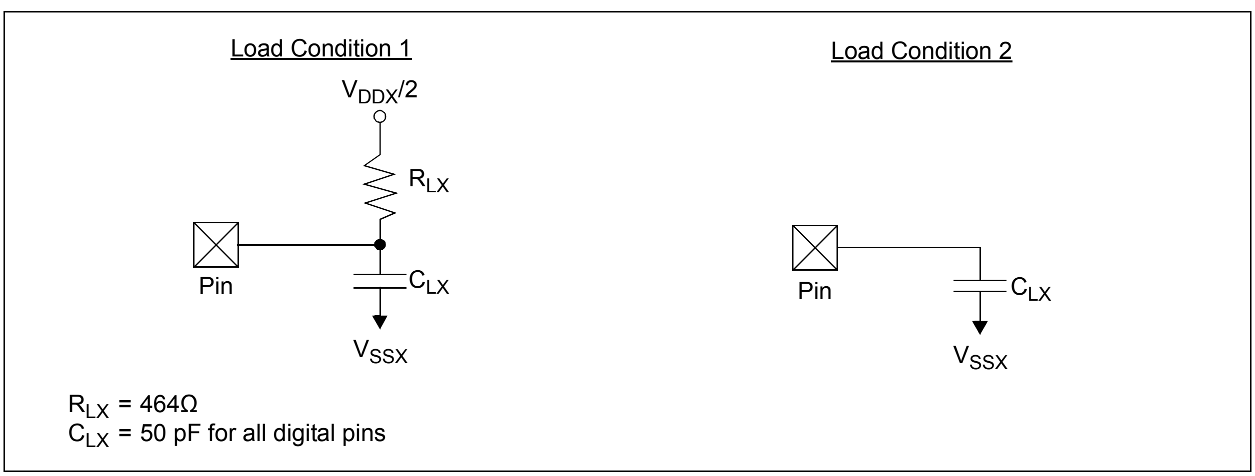


FIGURE 2-2: *Test Load Conditions.*

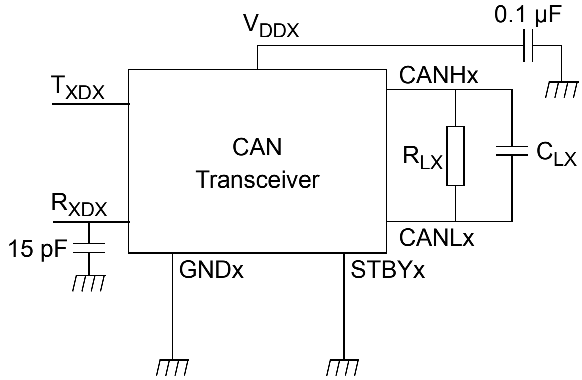
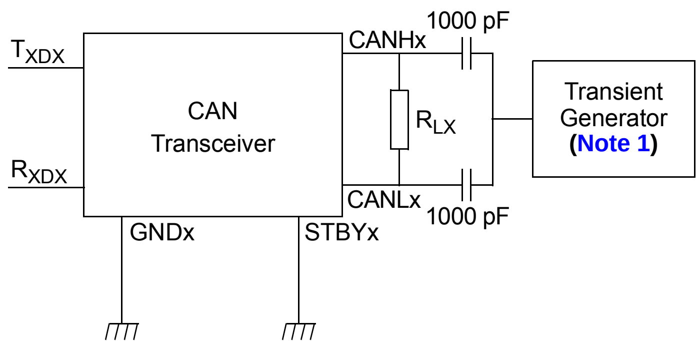


FIGURE 2-3: *Test Circuit for Electrical Characteristics.*



Note 1: The waveforms of the applied transients shall be in accordance with ISO-7637, Part 1, Test Pulses 1, 2, 3a and 3b.

FIGURE 2-4: *Test Circuit for Automotive Transients.*

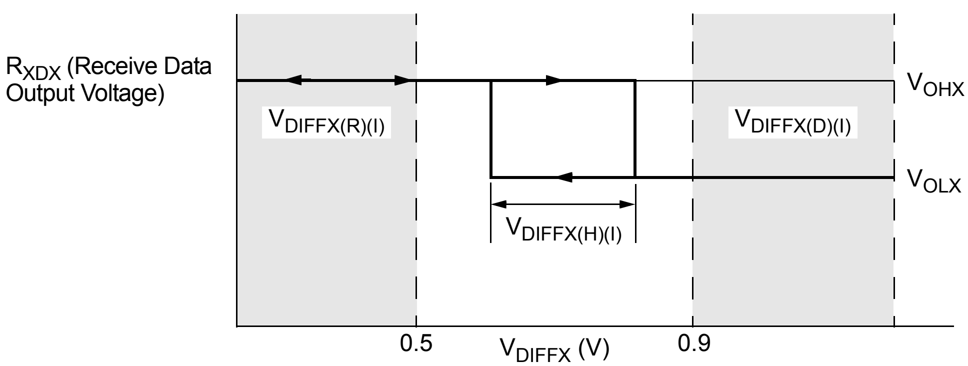


FIGURE 2-5: *Hysteresis of the Receiver.*

2.3 Terms and Definitions

A number of terms are defined in ISO-11898 that are used to describe the electrical characteristics of a CAN transceiver device. These terms and definitions are summarized in this section.

2.3.1 BUS VOLTAGE

V_{CANLX} and V_{CANHX} denote the voltages of the bus line wires, CANLx and CANHx, relative to the ground of each individual CAN node.

2.3.2 COMMON-MODE BUS VOLTAGE RANGE

Boundary voltage levels of V_{CANLX} and V_{CANHX}, with respect to ground, for which proper operation will occur if up to the maximum number of CAN nodes are connected to the bus.

2.3.3 DIFFERENTIAL INTERNAL CAPACITANCE, C_{DIFF} (OF A CAN NODE)

Capacitance seen between CANLx and CANHx during the Recessive state, when the CAN node is disconnected from the bus (see Figure 2-6).

2.3.4 DIFFERENTIAL INTERNAL RESISTANCE, R_{DIFF} (OF A CAN NODE)

Resistance seen between CANLx and CANHx, during the Recessive state, when the CAN node is disconnected from the bus (see Figure 2-6).

2.3.5 DIFFERENTIAL VOLTAGE, V_{DIFFX} (OF CAN BUS)

Differential voltage of the two-wire CAN bus value: $V_{DIFFX} = V_{CANHX} - V_{CANLX}$.

2.3.6 INTERNAL CAPACITANCE, C_{IN} (OF A CAN NODE)

Capacitance seen between CANLx (or CANHx) and ground, during the Recessive state, when the CAN node is disconnected from the bus (see Figure 2-6).

2.3.7 INTERNAL RESISTANCE, R_{IN} (OF A CAN NODE)

Resistance seen between CANLx (or CANHx) and ground, during the Recessive state, when the CAN node is disconnected from the bus (see Figure 2-6).

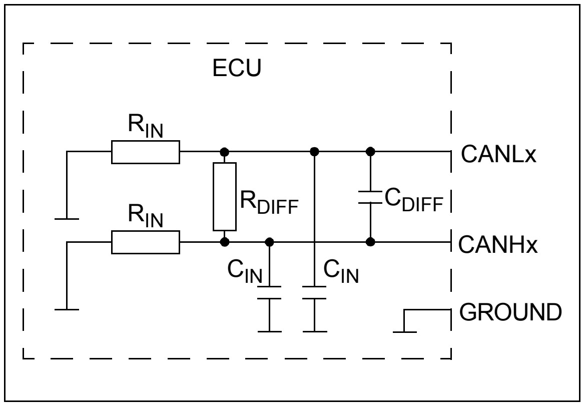


FIGURE 2-6: *Physical Layer Definitions.*

2.4 Timing Diagrams and Specifications

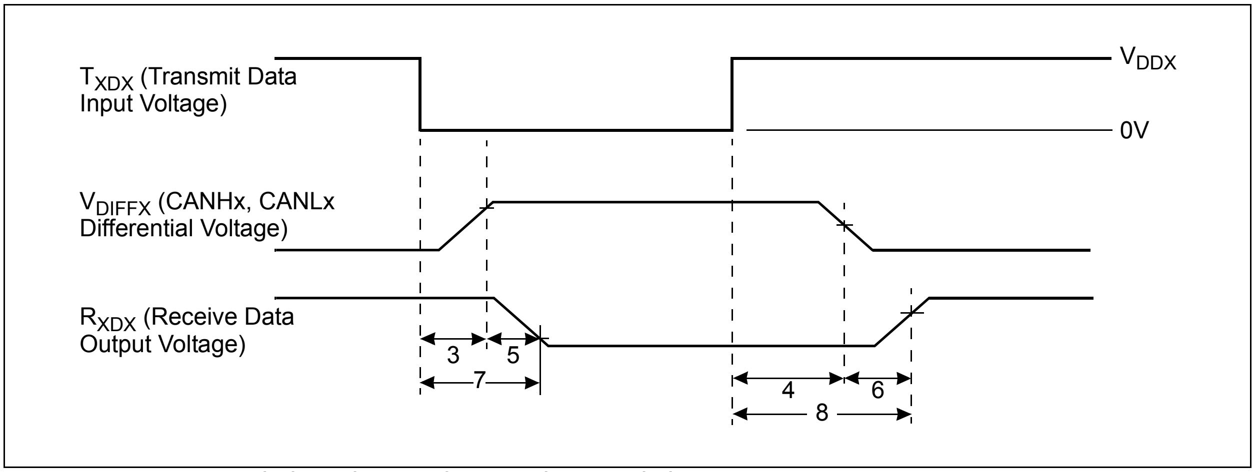


FIGURE 2-7: *Timing Diagram for AC Characteristics.*

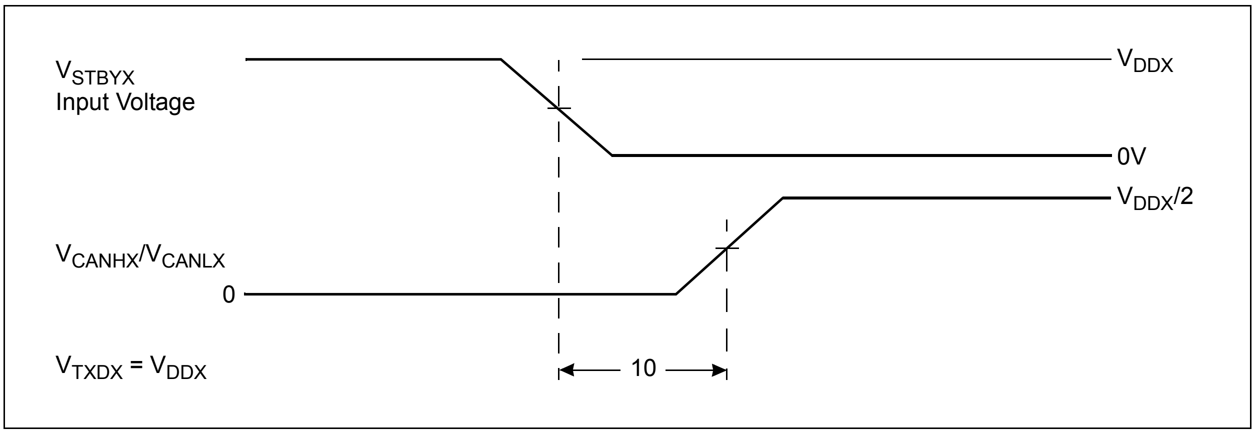


FIGURE 2-8: *Timing Diagram for Wake-up from Standby.*

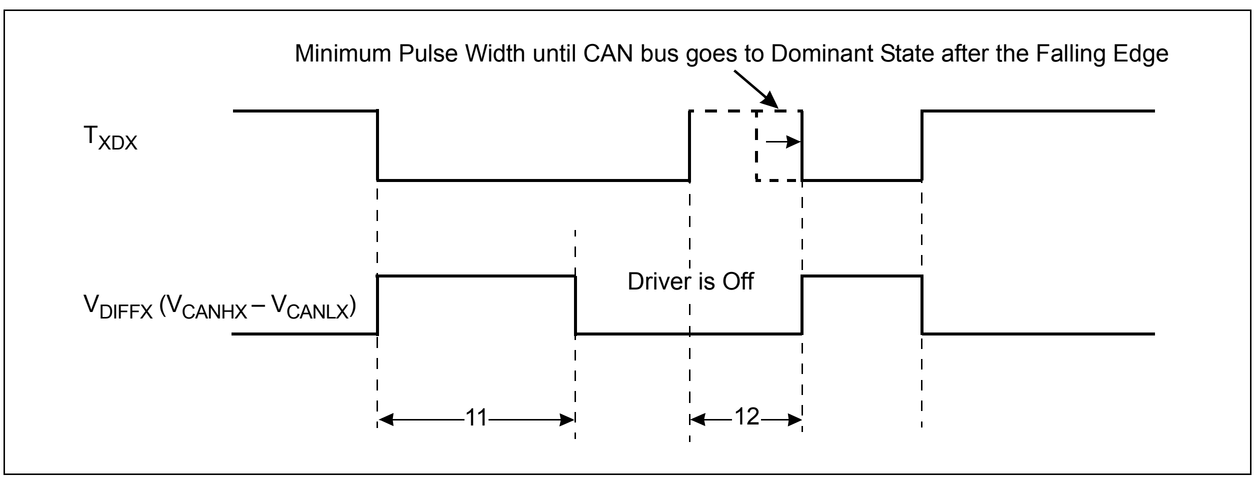
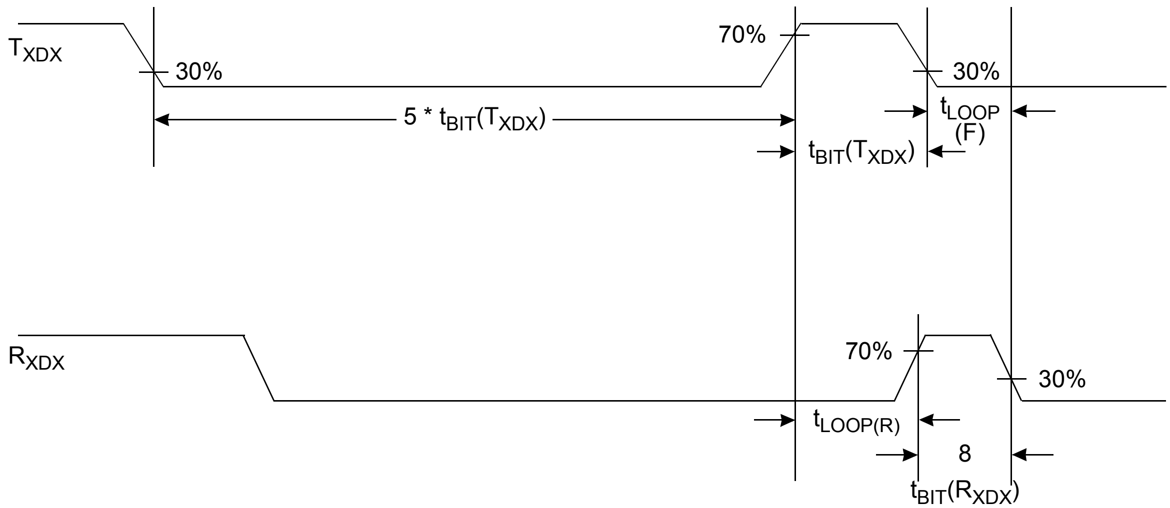


FIGURE 2-9: *Permanent Dominant Timer Reset Detect.*



Note: The bit time of a recessive bit, after five dominant bits, is measured on the R_{XDX} pin. Due to asymmetry of the loop delay, and the CAN transceiver not being a push-pull driver, the recessive bits tend to shorten.

FIGURE 2-10: *Timing Diagram for Loop Delay Symmetry.*

TABLE 2-3: THERMAL SPECIFICATIONS

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	
		-40	—	+150		
Operating Temperature Range	T_A	-40	—	+150	°C	
Storage Temperature Range	T_A	-55	—	+150	°C	
Thermal Package Resistance						
Thermal Resistance, 14L-SOIC	θ_{JA}	—	90.8	—	°C/W	

3.0 PIN DESCRIPTIONS

Table 3-1 describes the MCP25612FD device pinout.

TABLE 3-1: MCP25612FD PIN FUNCTIONS

SOIC	Pin Name	Pin Type	Pin Function
1	T_{XD1}	I	Transmit Data Input
2	V_{SS1}	Power	Ground
3	V_{DD1}	Power	Transceiver Supply Voltage
4	R_{XD1}	O	Receive Data Output
5	T_{XD2}	I	Transmit Data Input
6	V_{SS2}	Power	Ground
7	V_{DD2}	Power	Transceiver Supply Voltage
8	R_{XD2}	O	Receive Data Output
9	CANL2	I/O	CAN Low-Level Bus Line
10	CANH2	I/O	CAN High-Level Bus Line
11	STBY2	I	Standby Mode Input (active-high)
12	CANL1	I/O	CAN Low-Level Bus Line
13	CANH1	I/O	CAN High-Level Bus Line
14	STBY1	I	Standby Mode Input (active-high)

3.1 Transmitter Data Input Pin (T_{XDX})

The CAN transceivers drive the differential output pins, CANHx and CANLx, according to T_{XDX}. T_{XDX} is usually connected to the transmitter data output of the CAN controller device. When T_{XDX} is low, CANHx and CANLx are in the Dominant state. When T_{XDX} is high, CANHx and CANLx are in the Recessive state, provided that another CAN node is not driving the CAN bus with a Dominant state. T_{XDX} is connected to an internal pull-up resistor (nominal 33 kΩ) to V_{DDX}.

3.2 Ground Supply Pin (V_{SSX})

Ground supply pin.

3.3 Supply Voltage Pin (V_{DDX})

Positive supply voltage pin. Supplies the transmitter and receiver, including the wake-up receiver.

3.4 Receiver Data Output Pin (R_{XDX})

R_{XDX} is a CMOS-compatible output that drives high or low, depending on the differential signals on the CANHx and CANLx pins, and is usually connected to the receiver data input of the CAN controller device. R_{XDX} is high when the CAN bus is in the Recessive state and low in the Dominant state. R_{XDX} is supplied by V_{DDX}.

3.5 CAN Low Pin (CANLx)

The CANLx output drives the low side of the CAN differential bus. This pin is also tied internally to the receive input comparator. CANLx disconnects from the bus when MCP25612FD is not powered.

3.6 CAN High Pin (CANHx)

The CANHx output drives the high side of the CAN differential bus. This pin is also tied internally to the receive input comparator. CANHx disconnects from the bus when MCP25612FD is not powered.

3.7 Standby Mode Input Pin (STBYx)

This pin selects between Normal or Standby mode. In Standby mode, the transmitter and high-speed receiver are turned off; only the low-power receiver and wake-up filter are active. STBYx is connected to an internal MOS pull-up resistor to V_{DDX}. The typical value is 660 kΩ.

4.0 TYPICAL APPLICATIONS

In order to meet some EMC/EMI requirements, a Common-Mode Choke (CMC) may be needed for data rates greater than 1 Mbps.

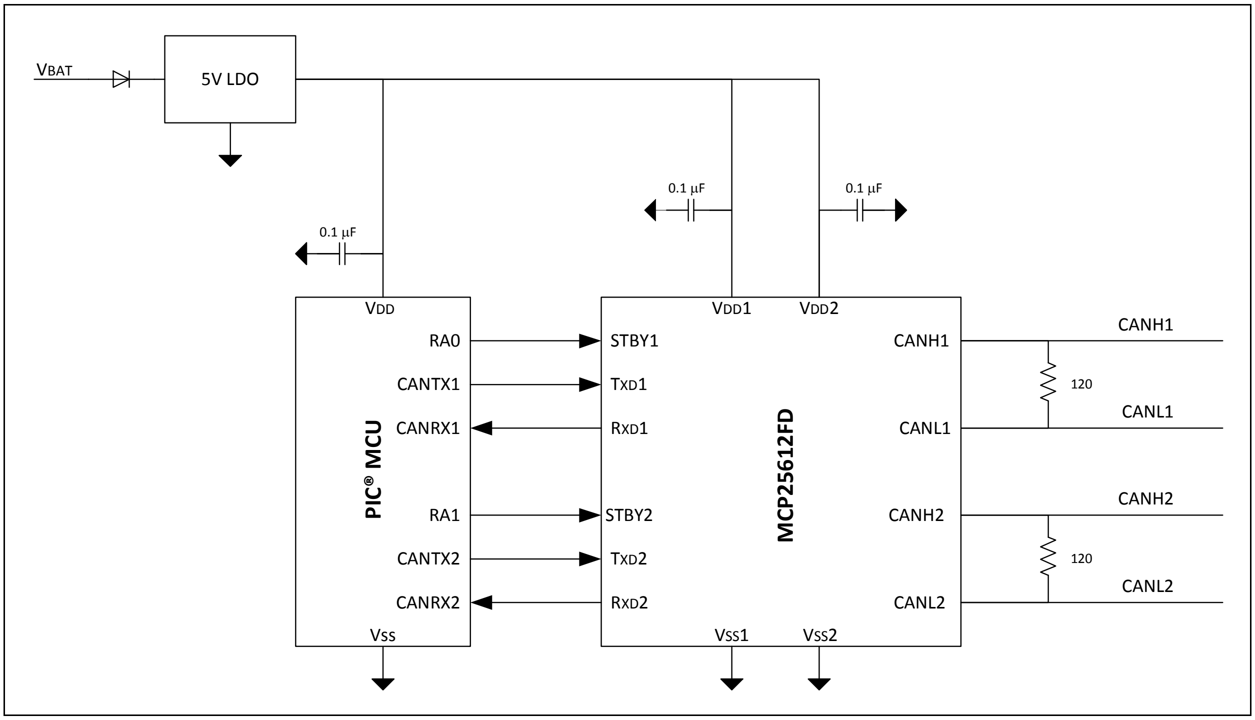
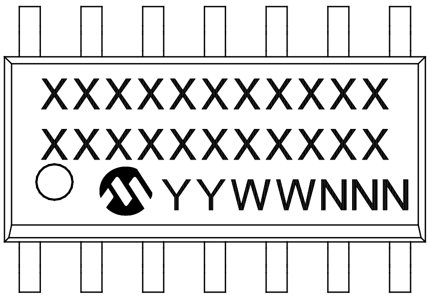


FIGURE 4-1: *MCP25612FD Application.*

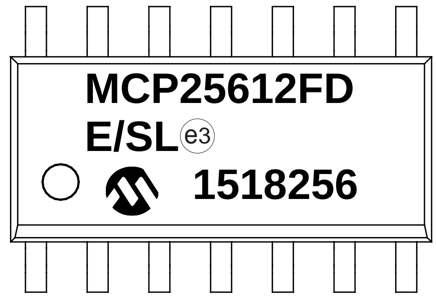
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

14-Lead SOIC (3.90 mm)



Example



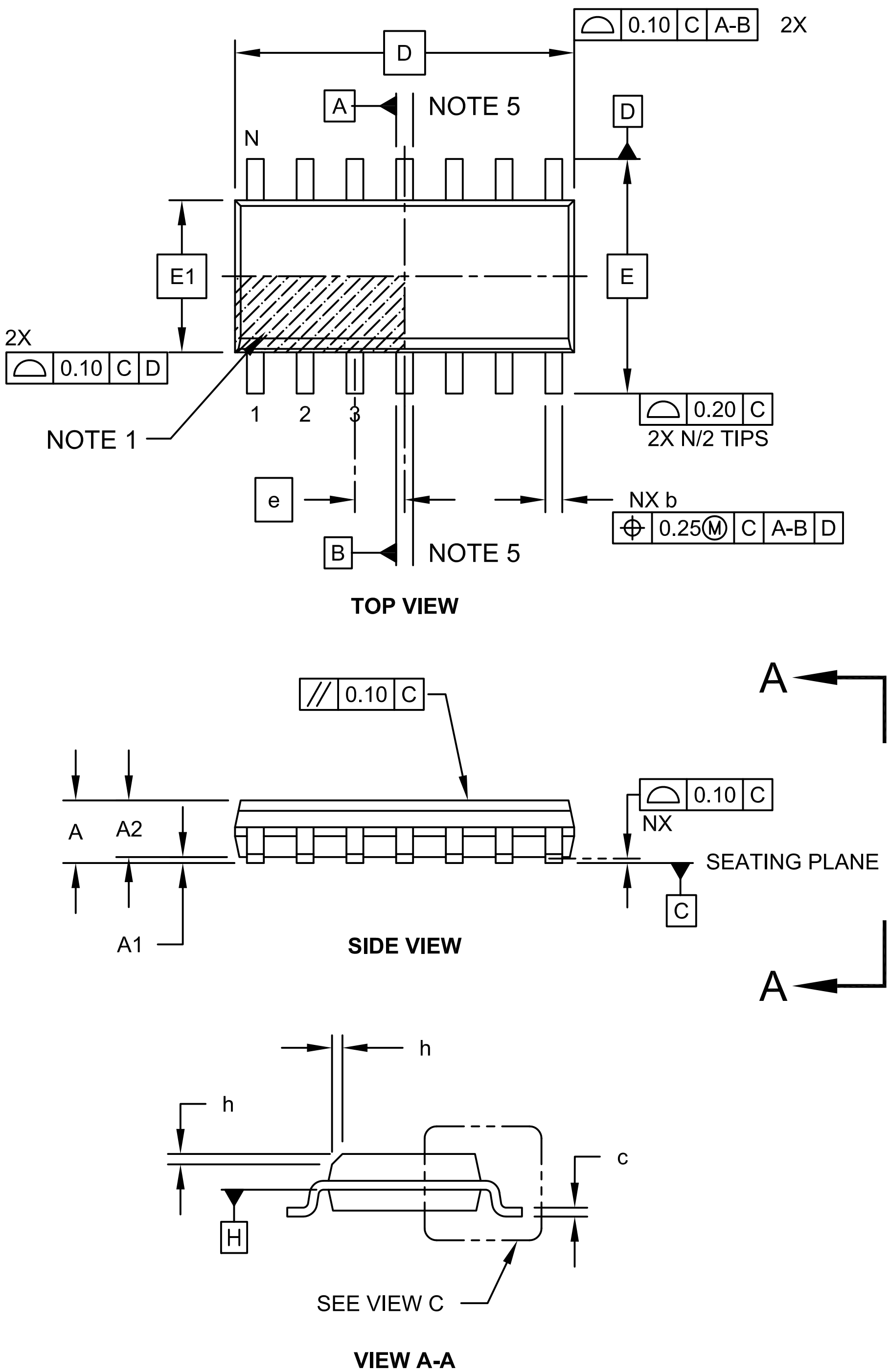
Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

5.2 Package Details

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

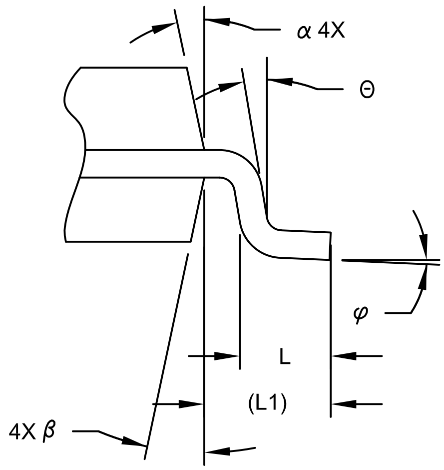
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



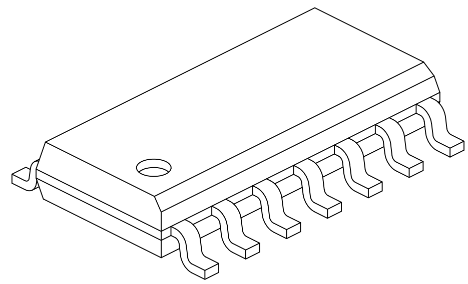
Microchip Technology Drawing No. C04-065C Sheet 1 of 2

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



VIEW C



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		14	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		8.65 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.10	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

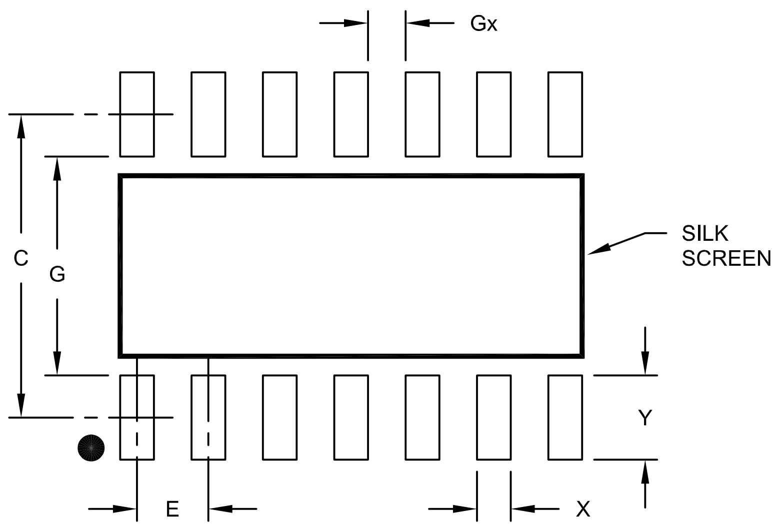
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-065C Sheet 2 of 2

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

		Units	MILLIMETERS		
Dimension Limits			MIN	NOM	MAX
Contact Pitch	E		1.27 BSC		
Contact Pad Spacing	C			5.40	
Contact Pad Width	X				0.60
Contact Pad Length	Y				1.50
Distance Between Pads	Gx		0.67		
Distance Between Pads	G		3.90		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2065A

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (June 2015)

Original release of this document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact the factory or one of the sales offices listed on the back page.

PART NO.	-X	/XX
Device	Temperature Range	Package

Device:	MCP25612FD:	Dual CAN FD Transceiver
	MCP25612FDT:	Dual CAN FD Transceiver (Tape and Reel)
Temperature Range:	E =	-40°C to +125°C (Extended)
	H =	-40°C to +150°C (High)
Package:	SL =	14-Lead Plastic Small Outline - Narrow, 3.90 mm Body

Examples:

a) MCP25612FD-E/SL: Extended Temperature, 14LD SOIC package

b) MCP25612FDT-E/SL: Tape and Reel, Extended Temperature, 14LD SOIC package

c) MCP25612FD-H/SL: High Temperature, 14LD SOIC package.

d) MCP25612FDT-H/SL: Tape and Reel, High Temperature, 14LD SOIC package

NOTES:

ISBN: 978-1-63277-484-2

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