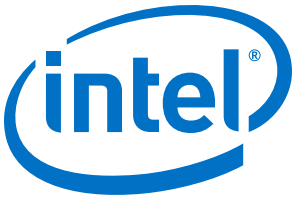

Intel® Stratix® 10 GX Transceiver Signal Integrity Development Kit User Guide

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Contents

1. Overview

For the Intel® Stratix® 10 GX Transceiver Signal Integrity Development Kit, there are two versions in production listed below.

Table 1. Development Kit Versions in Production

Board Ordering Part Number (OPN)	Device Ordering Part Number (OPN)
DK-SI-1SGX-L-A	1SG280LU2F50E2VG
DK-SI-1SGX-H-A	1SG280HU1F50E2VG

1.1. General Board Description

The Intel Stratix 10 GX Transceiver Signal Integrity Development Kit is a complete design environment that includes both hardware and software you need to develop Intel Stratix 10 GX FPGA designs.

The following list describes what you can accomplish with the kit:

- Evaluate transceiver performance up to 17.4 Gbps for L-Tile and 28.3 Gbps for H-Tile version.
- Generate and check pseudo-random binary sequence (PRBS) patterns
- Dynamically change differential output voltage (VOD) pre-emphasis and equalization settings to optimize transceiver performance for your channel
- Perform jitter analysis
- Verify physical medium attachment (PMA) compliance to PCI Express* (PCIe*), 1G/10G/40G/100G Ethernet and other major standards.

Related Information

Stratix 10 Support

1.2. Recommended Operating Conditions

The recommended operating conditions for this development kit are:

- Recommended ambient operating temperature range: 0C to 45C
- Maximum ICC load current: 130 A
- Maximum ICC load transient percentage: 30%
- FPGA maximum power supported by the supplied heatsink/fan: 200 W

1.3. Handling the Development Board

When handling the board, it is important to observe static discharge precautions.

Caution: Without proper anti-static handling, the board can be damaged. Therefore, use anti-static handling precautions when touching the board.

Caution: This development kit should not be operated in a Vibration Environment.

2. Getting Started

2.1. Installing the Quartus Prime software

The Intel Quartus® Prime design software is a multiplatform design environment that easily adapts to your specific needs in all phases of FPGA, CPLD, and SoC designs. The Intel Quartus Prime software delivers the highest performance and productivity for Intel FPGAs, CPLDs, and SoCs.

Design software must enable dramatically increased design productivity in order to take advantage of devices with multi-million logic elements with increased capabilities that provide designers with an ideal platform to meet next-generation design opportunities.

The new Intel Quartus Prime Design Suite design software includes everything needed to design for Intel FPGAs, SoCs and CPLDs from design entry and synthesis to optimization, verification and simulation. The Intel Quartus Prime Design Suite software includes an additional Spectra-Q® engine that is optimized for Intel Stratix 10 and future devices. The Spectra-Q engine enables new levels of design productivity for next generation programmable devices with a set of faster and more scalable algorithms, a hierarchical database infrastructure and a unified compiler technology.

Intel Quartus Prime Pro Edition

The Intel Quartus Prime Design Suite software is available in three editions based on specific design requirements: Pro, Standard, and Lite Edition.

The Intel Quartus Prime Pro Edition is optimized to support the advanced features in Intel's next generation FPGAs and SoCs and requires a paid license.

Included in the Intel Quartus Prime Pro Edition are the Intel Quartus Prime software, Nios® II EDS and the MegaCore IP Library.

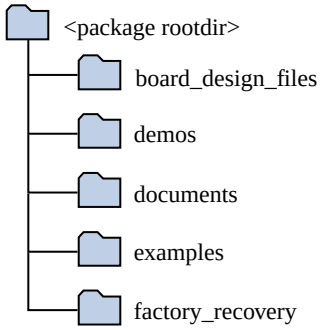
To install Intel's development tools, download the Intel Quartus Prime Pro Edition software from the Quartus Prime Pro Edition page in the Download Center of Intel's website.

2.2. Installing the Development Board

To install the Intel Stratix 10 GX Transceiver Signal Integrity Development Board, perform the following steps:

1. Download the development kit installer from the Stratix 10 GX Transceiver Signal Integrity Development Kit link on the Intel website.
2. Unzip the Intel Stratix 10 Transceiver Signal Integrity Development Kit installer package.
3. The installer package creates the development kit directory structure shown in the figure below.

Figure 1. Development Kit Directory Structure



The table below lists the file directory names and a description of their contents

Table 2. Installed Development Kit Directory Structure

File Directory Name	Description of Directory Contents
`board_design_files`	Contains schematics, layout, assembly and bill of material board design files. Use these files as a starting point for a new prototype board design
`demos`	Contains demonstration applications when available
`documents`	Contains the development kit documentation
`examples`	Contains the sample design files for the development kit
`factory_recovery`	Contains the original data programmed onto the board before shipment. Use this data to restore the board with its original factory contents.

Note: To view the the layout `*.brd` files in the board package, you can download the Cadence® Allegro®/OrCAD® Free Viewer from Cadence's website.

Related Information

Cadence Allegro Downloads

2.3. Installing the Intel FPGA Download Cable Driver

The Intel Stratix 10 GX Transceiver Signal Integrity Development Kit includes embedded Intel FPGA Download Cable circuits for FPGA and MAX® V programming. However, for the host computer and board to communicate, you must install the Intel FPGA Download Cable driver on the host computer.

Installation instructions for the Intel FPGA Download Cable driver for your operating system are available on the Intel website.

On the Intel website, navigate to the Cable and Adapter Drivers Information link to locate the table entry for your configuration and click the link to access the instructions.

3. Development Board Setup

The instructions in this chapter explain how to setup the Intel Stratix 10 GX Transceiver Signal Integrity Development Board.

3.1. Setting up the Development Board

To prepare and apply power to the board, perform the following steps:

1. The Intel Stratix 10 GX transceiver signal integrity development kit ships with its board switches preconfigured to support the design examples in the kit. If you suspect your board might not be correctly configured with the default settings, follow the instructions in the Factory Default Switch and Jumper Settings on page 10 to return the board to its factory settings before proceeding.
2. The development kit ships with design examples stored in the flash device. The POWER-ON slide switch (SW7) is provided to turn the board **ON** or **OFF**.

   Caution: When the power cord is plugged into connector **J103** of the Intel Stratix 10 transceiver signal integrity development kit, 12V_IN and 3.3V_STBY are present on to the board with switch **SW7** in the '**OFF**' position. These voltages are restricted to a small area of the board. When switch **SW7** is placed to '**ON**' position, all voltages planes have power at this point.
3. Set the POWER-ON switch **SW7** to the **ON** position. When power is supplied to the board, three green LEDs (**D29**, **D31** and **D32**) illuminate and an amber LED (**D36**) extinguishes indicating that the board has power. If the amber LED (**D36**) illuminates, it indicates that one or more power supply is incorrect.
4. **RESET** button (S12) is connected to the MAX V CPLD (MAX_RESETn pin) that is used for AvST configuration. When this button is pressed, the MAX V CPLD initiates a reloading of the stored image from the flash memory using AvST configuration mode. The image loaded right after power cycle or MAX V reset depends on FACTORY_LOAD settings.
   - **OFF(1)** - factory load
   - **ON (0)** - user defined load #1

   Page selection can be changed by the PGMSEL button (S10) when the board is powered on, and PGM_CONFIG (S11) is used to reconfigure FPGA with corresponding page which is indicated by PGM_LED0, PGM_LED1 or PGM_LED2.

   Caution: Use only the supplied power supply. Power regulation circuits on the board can get damaged by power supplies with greater voltage.

The MAX V CPLD device on the board contains a parallel flash loader II (PFL II) megafunction. After a POWER-ON or RESET (reconfiguration) event, the MAX V CPLD configures the Intel Stratix 10 FPGA in AvST mode with either factory design or user design depending on the setting of FACTORY_LOAD.

The development kit includes a MAX V CPLD design which contains the PFL II megafunction. The design resides in the <package dir>\examples\max5 directory. When configuration is complete, **LED D25** (CONF_DONE) illumintes signaling that the Intel Stratix 10 GX FPGA device is configured successfully. If the configuration fails, the **LED D23** (ERROR) illuminates.

3.2. Factory Default Switch and Jumper Settings

This section shows the factory switch settings for the Intel Stratix 10 GX transceiver signal integrity development kit.

Table 3. Factory Default Switch Settings

Switch	Board Label	Default Position	Function
SW10	MSEL1	2-3 Closed	MSEL setting=0
	MSEL2	5-6 Closed	MSEL setting=0
SW11	MSEL0	2-3 Closed	MSEL setting=0
SW3-1	Intel Stratix 10	OPEN/OFF	Enable Intel Stratix 10 in JTAG Chain
SW3-2	MAX V	OPEN/OFF	Enable MAX V in JTAG chain
SW3-3	FMC A	CLOSE/ON	Bypass FMC A in JTAG chain
SW3-4	FMC B	CLOSE/ON	Bypass FMC B in JTAG chain
S15-1	OFF = OSC	OPEN/OFF	Select Si570 clock source for U3
S15-2	ON = SMA	OPEN/OFF	Select Si570 clock source for U4
SW1-1	S0	OPEN/OFF	Frequency Select
SW1-2	S1	CLOSE/ON	Frequency Select
SW1-3	SS0	OPEN/OFF	Spread Spectrum Select
SW1-4	SS1	OPEN/OFF	Spread Spectrum Select
SW2-1	OFF=ISOLATE	CLOSE/ON	U15 (LTC2987) is enabled in I^2C topology
SW2-2	ON=FULL CHAIN	CLOSE/ON	U15 (LTC2987) is enabled in I^2C topology
S1-1	OFF=ISOLATE	CLOSE/ON	U5 and U6 (Si5341) is enabled in I^2C topology
S1-2	ON=FULL CHAIN	CLOSE/ON	U5 and U6 (Si5341) is enabled in I^2C topology
S14-1	VCCT	OPEN/OFF	Enable on-board VCCT regulator
S14-2	VCCH	OPEN/OFF	Enable on-board VCCH regulator
SW9-1	VCCRR	OPEN/OFF	Enable on-board VCCRR regulator
SW9-2	VCCRL	OPEN/OFF	Enable on-board VCCRL regulator

continued...

Switch	Board Label	Default Position	Function
SW9-3	VCCERAM	OPEN/OFF	Enable on-board VCCERAM regulator
SW9-4	VCC	OPEN/OFF	Enable on-board VCC regulator
SW8-1	MAX10_DIPSWITCH	OPEN/OFF	Power Intel MAX 10 user DIP Switch
SW8-2	FAN_ON	OPEN/OFF	FAN is not full speed
SW8-3	PWR_MGMT_SEL	OPEN/OFF	Select Linear Tech PWR MGMT solution
SW8-4	MAX10_BOOTSEL	OPEN/OFF	Power Intel MAX 10 boot select
SW6-1	FACTORY_LOAD	OPEN/OFF	Factory Load Control
SW6-2	MAX5_SWITCH2	OPEN/OFF	MAX V user DIPSwitch
SW6-3	MAX5_SWITCH0	OPEN/OFF	MAX V user DIPSwitch
SW6-4	MAX5_SWITCH1	OPEN/OFF	MAX V user DIPSwitch
SW4-1	S10_UNLOCK	OPEN/OFF	Stratix 10 User DIPSwitch
SW4-2	USER_DIP6	OPEN/OFF	Stratix 10 User DIPSwitch
SW4-3	USER_DIP5	OPEN/OFF	Stratix 10 User DIPSwitch
SW4-4	USER_DIP4	OPEN/OFF	Stratix 10 User DIPSwitch
SW5-1	USER_DIP3	OPEN/OFF	Stratix 10 User DIPSwitch
SW5-2	USER_DIP2	OPEN/OFF	Stratix 10 User DIPSwitch
SW5-3	USER_DIP1	OPEN/OFF	Stratix 10 User DIPSwitch
SW5-4	USER_DIP0	OPEN/OFF	Stratix 10 User DIPSwitch
SW7	SW7	OFF	On-board power switch

4. Board Components

4.1. Board Overview

This section provides an overview of the Intel Stratix 10 GX transceiver signal integrity development board including a block diagram of the board.

Figure 2. Stratix 10 GX Transceiver Signal Integrity Development Kit User Guide Block Diagram

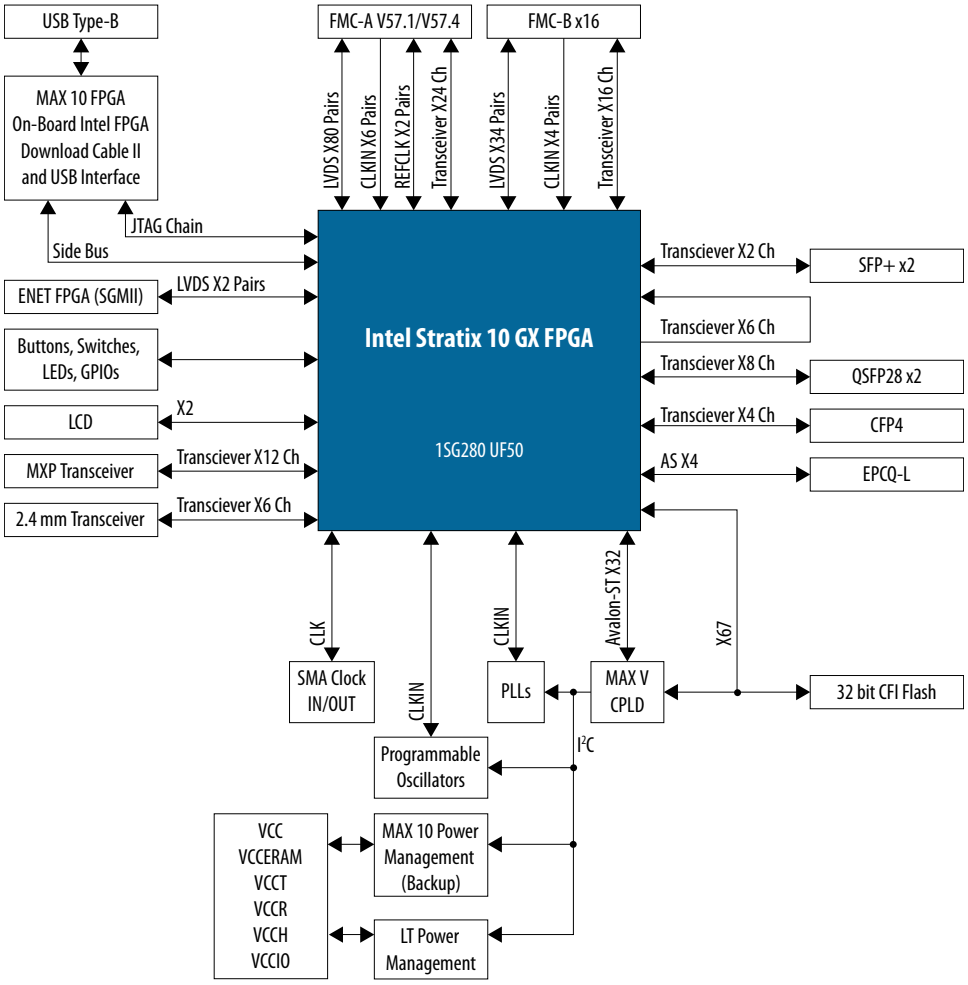
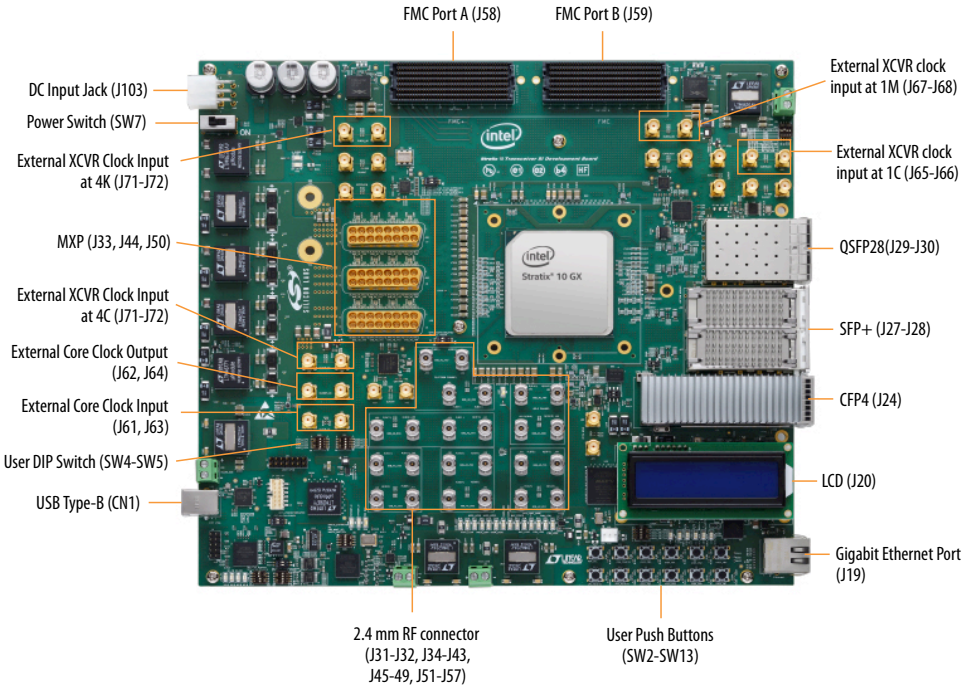


Figure 3. Intel Stratix 10 GX Transceiver Signal Integrity Development Kit Picture



Intel Stratix 10 GX Transceiver Signal Integrity Development Board Components

Table 4. Board Components Table

Board Reference	Type	Description
Featured Devices		
U43	FPGA	Intel Stratix 10 GX 280 F2397 FPGA
U20	CPLD	System MAX V CPLD (5M2210ZF256)
U97	FPGA	USB Intel MAX 10 FPGA (10M04SCU169)
U98	FPGA	PWR Intel MAX 10 FPGA (10M16SAU169)
General User Input and Output		
D12-D19	User LEDs (Green)	User LEDs (Green)
D20-D25	MAX V LEDs (Green)	MAX V LEDs (Green)
S2-S13	User Push Buttons	User Push Buttons
SW4-SW5	User DIP Switches	User DIP
SW6	MAX V DIP Switch	MAX V DIP Switch
J20	LCD Display Header	Connector for 16 Character x2 line LCD
Configuration, Status and Setup Elements		

continued...

Board Reference	Type	Description
J14	Intel FPGA Download Cable Programming Header	Header to interface external Intel FPGA Download Cable direct to FPGA (through USB Intel MAX 10)
D1-D2	Green LEDs	JTAG Transmit-Receive Activity
D3-D4	Green LEDs	System Console Transmit-Receive Activity
D36	Amber LEDs	System Power error indicator
D5-D6	Green LEDs	FMC cards present indicator
D7-D11	Ethernet LEDs	Ethernet LEDs (TX/RX/LINK)
Clock Circuits		
X2	50-MHz Oscillator	This 50-MHz oscillator is the clock source to clock buffer SL18860DC that provides three 50 MHz outputs to the FPGA and the MAX V CPLD
X1		This 50-MHz oscillator provides clock to the PWR Intel MAX 10 FPGA
SW1	Spread Spectrum/Frequency Selection Switch	SW1 selects frequency and spread spectrum percentages of clock buffer outputs ICS557-03.
Y1	Transceiver Dedicated Reference Clock/ Programmable Oscillator	Feeds REFCLKs on left side of the Intel Stratix 10 GX FPGA device and an LVDS trigger output at board reference J4/J5. The external input is available at board reference J2 and J3. The default frequency is 644.53125 MHz.
Y2		Feeds REFCLKs on right side of the Intel Stratix 10 GX FPGA device and an LVDS trigger output at board reference J8/J9. The external input is available at board reference J6 and J7. The default frequency is 706.25 MHz.
U3, U4, U5	Transceiver Dedicated Reference Clock/ Programmable PLL	Feeds REFCLKs on left side of the Intel Stratix 10 GX FPGA device and an LVDS trigger output at board reference J10/J11. The default frequencies are 625 MHz, 614.4 MHz, 100 MHz.
U6		Feeds REFCLKs on right side of the Intel Stratix 10 GX FPGA device and an LVDS trigger output at board reference J12/J13. The default frequencies are 625 MHz, 644.53125 MHz, 125 MHz.
J61, J63	External core clock input	SMA external input at `CLKIN_3C0`
J62, J64	External core clock output	SMA external output at `PLL_3C_CLKOUT0`
J65-J66	External transceiver clock input	SMA external input bank at 1C
J67-J68		SMA external input bank at 1M

continued...

Board Reference	Type	Description
J69-J70		SMA external input bank at 4C
J71-J72		SMA external input bank at 4K
X4	100-MHz Oscillator	This 100-MHz oscillator provides clock to the MAX V CPLD
Transceiver Interfaces		
J33, J44, J50	MXP connector	17 Gbps/28 Gbps, 4 channels MXP connectors
J31-J32 J34-J43 J45-J49 J51-J57	2.4 mm RF connector	17 Gbps/ 28 Gbps, 6 channels 2.4 mm RF connectors
J29-J30	SFP+ optical transceiver interface	17 Gbps/28 Gbps, 2 channels connected to SFP+ modules
J27-J28	QSFP28 optical transceiver interface	17 Gbps/28 Gbps, 8 channels connected to QSFP28 modules
J24	CFP4 optical transceiver interface	17 Gbps/ 28 Gbps, 4 channels connected to CFP4 module
J58-J59	FMC+ connector	17 Gbps/28 Gbps, 34 channels connected to FMC+ connectors
Memory Devices		
U21-U22	Flash Memory	Two 1-Gbit Micron PC28F00AP30BF CFI Flash device
Communication Ports		
J19	Gigabit Ethernet Port	RJ-45 connector which provides a 10/100/1000 Ethernet connection through a Marvell 88E1111 PHY
CN1	USB Type-B connector	Connects a type-B USB cable
Power Supply		
U15	LTM2987	Linear Technology power monitor device
U63-U64 U66-U67	LTM4677 3x LTM4650	Power regulators for VCC rail
U68	LTM4620	Power regulators for VCCERAM rail
U69	LTM4620	Power regulators for VCCH rail
U70	LTM4620	Power regulators for VCCRL rail
U71	LTM4620	Power regulators for VCCRR rail
U74	EN63A0	Power regulators for FMCA_VADJ rail
U78	EN63A0	Power regulators for FMCB_VADJ rail
U79	EN6337	Power regulators for 2.5V rail
U82	LTM4630A	Power regulators for 3.3V rail

4.2. Intel Stratix 10 GX FPGA

The development board features the Intel Stratix 10 GX FPGA (1SG280UF50).

For the Intel Stratix 10 GX Transceiver Signal Integrity Development Kit, there are two versions in production listed below.

Table 5. Development Kit Versions in Production

Board Ordering Part Number (OPN)	Device Ordering Part Number (OPN)
DK-SI-1SGX-L-A	1SG280LU2F50E2VG
DK-SI-1SGX-H-A	1SG280HU1F50E2VG

Intel Stratix 10 GX FPGA I/O Usage Summary

Table 6. Stratix 10 GX FPGA Pin Table

Signal Name/Function	I/O Count	Description
Configuration		
S10_JTAG_TCK/TDO/TDI/TMS	4	JTAG Configuration Pins
FPGA_MSEL[2:0]	2	Configuration input pins to set configuration scheme
FPGA_CONF_DONE	1	Configuration done pin
FPGA_nSTATUS	1	Configuration status pin
FPGA_INIT_DONE	1	Configuration pin to signify user mode
FPGAMSEL0	1	Configuration input pins to set configuration scheme and Chip select pin to EPCQL device
FPGA_nCONFIG	1	Configuration input pin to reset FPGA
FPGA_OSC_CLK_1	1	125 MHz Clock
FPGA_AS_CLK	1	Configuration Clock for AS configuration schemes
CPU_RESETn	1	Global reset signal
FPGA_CONFIG_D[31:0]	32	Configuration input pin that enables all IOs
FPGA_AS_DATA[3:0]	4	EPCQL data bus
FPGA_AVST_READY	1	SDM ready for AvST configuration scheme
FPGA_AVST_VALID	1	Data valid for AvST configuration scheme
FPGA_AVST_CLK	1	Configuration clock for AvST configuration scheme
FPGA_PR_DONE	1	Partial reconfiguration done pin
FPGA_PR_REQUEST	1	Partial reconfiguration request pin
FPGA_PR_ERROR	1	Partial reconfiguration error pin
NPERSTL, NPERSTR	4	Reset pin for PCIe HIP

continued...

Signal Name/Function	I/O Count	Description
FPGA_SDM10	1	SDM IO 10
FPGA_CvP_DONE	1	CvP configuration done pin
FPGA_SEU_ERR	1	SEU error indicate pin
VCC_SDA/VCC_SCL	2	SmartVID PMBus
VCC_ALERTn	1	SmartVID PMBus
Transceivers		
SFP0_TX_DS	1	SFP+ 0 TX disable control Pin
SFP0_RS[1:0]	2	SFP+ 0 Rate Select Control Pin
SFP0_MOD_ABS	1	SFP+ 0 Module Absent Status Pin
SFP0_RX_LOS	1	SFP+ 0
SFP0_TX_FLT	1	SFP+ 0 Transmitter Fault Status Pin
SFP0_SCL	1	SFP+ 0 Management Data Clock
SFP0_SDA	1	SFP+ 0 Management Data I/O Bi-Directional Data
SFP1_TX_DIS	1	SFP+ 1 TX disable control pin
SFP1_RS[1:0]	2	SFP+ 1 Rate Select Control Pin
SFP1_MOD_ABS	1	SFP+ 1 Module Absent Status Pin
SFP1_RX_LOS	1	SFP+ 1
SFP1_TX_FLT	1	SFP+ 1 Transmitter Fault Status Pin
SFP1_SCL	1	SFP+ 1 Management Data Clock
SFP1_SDA	1	SFP+ 1 Management Data I/O Bi-Directional Data
CFP4_MOD_LOPWR	1	CFP4 Module Low Power Mode
CFP4_MOD_RSTn	1	CFP4 Module Reset
CFP4_GLB_ALRMN	1	CFP4 Program Alarm bits
CFP4_PRTADR[2:0]	3	CFP4 MDIO Physical Port Address
CFP4_TX_DIS	1	CFP4 Transmitter Disable
CFP4_RX_LOS	1	CFP4 Receiver loss of signal
CFP4_MOD_ABS	1	CFP4 Module Absent
CFP4_MDC	1	CFP4 Management Data Clock
CFP4_MDIO	1	CFP4 Management Data I/O Bi-Directional Data
eQSFP_modselL0	1	QSFP28 0 model select
eQSFP_resetL0	1	QSFP28 0 Module Reset
eQSFP_LPmode0	1	QSFP28 0 Module Low Power Mode
eQSFP_modprsL0	1	QSFP28 0 Module Present

continued...

Signal Name/Function	I/O Count	Description
eQSFP_intl0	1	QSFP28 0 Module Interrupt
eQSFP_scl0	1	QSFP28 0 Management Data Clock
eQSFP_sda0	1	QSFP28 0 Management Data I/O Bi-Directional Data
eQSFP_modselL1	1	QSFP28 1 model select
eQSFP_resetL1	1	QSFP28 1 Module Reset
eQSFP_LPmode1	1	QSFP28 1 Module Low Power Mode
eQSFP_modprsL1	1	QSFP28 1 Module Present
eQSFP_intl1	1	QSFP28 1 Module Interrupt
eQSFP_scl1	1	QSFP28 1 Management Data Clock
eQSFP_sda1	1	QSFP28 1 Management Data I/O Bi-Directional Data
FALAp/n[33:0]	68	FMC A LA bank GPIOs
FAHAp/n[23:0]	48	FMC A HA bank GPIOs
FAHBp/n[21:0]	44	FMC A HB bank GPIOs
RZQ_2M	1	RZQ pin for bank 2M
RZQ_3K	1	RZQ pin for bank 3K
EXTA_SDA1V8	1	FMC A I^2C bus
EXTA_SCL1V8	1	FMC A I^2C bus
FAPRSNT1V8_N	1	FMC A present indicator
FACLKBIR1V8	1	FMC A clock direction control
FBLAp/n[33:0]	68	FMC B LA bank GPIOs
EXTB_SDA1V8	1	FMC B I^2C bus
EXTB_SCL1V8	1	FMC I^2C bus
FBPRSTN1V8_N	1	FMC B present indicator
USB		
USB_FULL	1	USB FIFO is full
USB_EMPTY	1	USB FIFO is empty
USB_RESETn	1	USB Reset
USB_OEn	1	USB Output Enable
USB_RDn	1	USB Read
USB_WRn	1	USB Write
USB_DATA[7:0]	8	USB Data Bus
USB_ADDR[1:0]	2	USB Address Bus
USB_SCL	1	USB Serial Clock

continued...

Signal Name/Function	I/O Count	Description
USB_SDA	1	USB Serial Data
Flash Memory		
FM_D[31:0]	32	Flash Data Bus
FM_A[26:1]	26	Flash Address Bus
FLASH_WEn	1	Flash Write Enable Strobe
FLASH_CEn0	1	Flash Chip Enable
FLASH_CEn1	1	Flash Chip Enable
FLASH_OEn	1	Flash Output Enable
FLASH_RDYBSYn0	1	Flash ready or busy
FLASH_RDYBSYn1	1	Flash ready or busy
FLASH_RESETn	1	Flash reset
FLASH_CLK	1	Flash clock
FLASH_ADVn	1	Flash address valid
MAX V CPLD		
MAX5_OEn	1	Output Enable
MAX5_CSn	1	Chip Select
MAX5_WEn	1	Write Enable
MAX5_CLK	1	Clock
MAX5_BEn[3:0]	4	Byte Enable
Switches, Buttons, LED		
USER_LED[7:0]	8	Light Emitting Diodes
USER_PB[7:0]	8	Push Buttons
USER_DIP[6:0]	7	DIP Switches
USER_IO[9:0]	10	Input/Output
S10_UNLOCK	1	FPGA Unlock Switch
Ethernet		
ENET_SGMII_TX_P/N	2	Ethernet SGMII Transmit Data
ENET_SGMII_RX_P/N	2	Ethernet SGMII Receive Data
ENET_RSTn	1	Reset
ENET_INTn	1	Interrupt
ENET_MDIO	1	Ethernet Management Data I/O
ENET_MDC	1	Ethernet Management Data Clock
Other Bus		

continued...

Signal Name/Function	I/O Count	Description
SPARE[20:1]	20	Spare bus between Intel Stratix 10 and MAX V
I2C_1V8_SCL	1	Intel Stratix 10 I^2C bus
I2C_1V8_SDA	1	Intel Stratix 10 I^2C bus
Temperature		
OVERTEMPn	1	Intel Stratix 10 over temperature indicator
TEMP_ALERTn	1	Intel Stratix 10 temperature alert indicator
Global Clocks		
CLK_50M_S10	1	50 MHz Global Clock Input
CLK_S10BOT_100M_p/n	2	100 MHz differential core clock for bottom banks
CLKIN_SMA_3C_p/n	2	Global Clock input from SMA
CLKOUT_SMA_3C_p/n	2	Dedicated Clock output to SMA
USB_FPGA_CLK	1	USB FPGA Clock
CLK_S10TOP_ADJ_p/n	2	Adjustable differential core clock for top banks
CLK_S10TOP_125M_p/n	2	125 MHz differential core clock for top banks
FACLKM2Cp/n0	2	FMC A clock input 0
FACLKM2Cp/n1	2	FMC A clock input 1
FBCLKM2Cp/n0	2	FMC B clock input 0
FBCLKM2Cp/n1	2	FMC B clock input 1
FACLKBIDIRp/n2	2	FMC A bidirectional clock 2
FACLKBIDIRp/n3	2	FMC A bidirectional clock 3
Transceiver Clocks		
CLK_CFP4_644_p/n	2	Differential top REFCLK input to the transceiver bank 1C
CLKIN_SMA_1C_p/n	2	Differential bottom REFCLK input to the transceiver bank 1C
CLK_QSFP0_644MT_p/n	2	Differential top REFCLK input to the transceiver bank 1D
CLK_QSFP0_644MB_p/n	2	Differential bottomREFCLK input to the transceiver bank 1D
CLK_GXBL1E_614MT_p/n	2	Differential top REFCLK input to the transceiver bank 1E
CLK_GXBL1E_614MB_p/n	2	Differential bottom REFCLK input to the transceiver bank 1E
CLK_GXBL1F_625M_p/n	2	Differential top REFCLK input to the transceiver bank 1F

continued...

Signal Name/Function	I/O Count	Description
CLK_SFP_644M_p/n	2	Differential top REFCLK input to the transceiver bank 1K
CLK_GXBL1K_614M_p/n	2	Differential bottom REFCLK input to the transceiver bank 1K
CLK_GXBK1L_625M_p/n	2	Differential top REFCLK input to the transceiver bank 1L
FBGBTCLKM2_Cp/n0	2	Differential top REFCLK input to the transceiver bank 1M
CLKIN_SMA_1M_p/n	2	Differential bottomREFCLK input to the transceiver bank 1M
CLK_FMCB_644M_p/n	2	Differential top REFCLK input to the transceiver bank 1N
FBGBTCLKM2_Cp/n1	2	Differential bottom REFCLK input to the transceiver bank 1N
CLK_SMA_706M_p/n	2	Differential top REFCLK input to the transceiver bank 4C
CLKIN_SMA_4C_p/n	2	Differential bottomREFCLK input to the transceiver bank 4C
CLK_MXP1_706M_p/n	2	Differential top REFCLK input to the transceiver bank 4D
CLK_GXBR4D_644M_p/n	2	Differential bottom REFCLK input to the transceiver bank 4D
CLK_MXP2_706M_p/n	2	Differential top REFCLK input to the transceiver bank 4E
CLK_GXBR4E_644M_p/n	2	Differential bottom REFCLK input to the transceiver bank 4E
CLK_MXP3_706M_p/n	2	Differential top REFCLK input to the transceiver bank 4F
CLK_GXB4F_644M_p/n	2	Differential bottomREFCLK input to the transceiver bank 4F
FAGBTCLKM2_Cp/n0	2	Differential top REFCLK input to the transceiver bank 4K
CLKIN_SMA_4K_p/n	2	Differential bottom REFCLK input to the transceiver bank 4K
FAGBTCLKM2_Cp/n1	2	Differential top REFCLK input to the transceiver bank 4L
CLK_GXBR4L_644M_p/n	2	Differential bottom REFCLK input to the transceiver bank 4L
FAGBTCLKM2_Cp/n2	2	Differential top REFCLK input to the transceiver bank 4M
CLK_GXBR4M_625M_p/n	2	Differential bottomREFCLK input to the transceiver bank 4M
FAGBTCLKM2_Cp/n3	2	Differential top REFCLK input to the transceiver bank 4N
CLK_FMCA_706M_p/n	2	Differential bottomREFCLK input to the transceiver bank 4N

4.3. MAX V CPLD System Controller

The Intel Stratix 10 GX transceiver signal integrity development kit consists of a MAX V CPLD (5M2210Z-F256), 256-pin FineLine BGA package. MAX V CPLD devices provide programmable solutions for applications such as FPGA reconfiguration from flash memory, I^2C chain to manage power consumption, core temperature, fan speed, clock frequency and remote update system. MAX V devices feature on-chip flash storage, internal oscillator and memory functionality. With up to 50% lower total power versus other CPLDs and requiring as few as one power supply, MAX V CPLDs can help you meet your low power design requirements.

The following list summarizes the features of MAX V CPLD devices:

- 2210 Logic Elements (LEs)
- 8192 bits of User Flash Memory
- 4 global clocks
- 1 internal oscillator
- 271 maximum user I/O pins
- Low-cost, low power and non-volatile CPLD architecture
- Fast propagation delays and clock-to-output times
- Single 1.8V external supply for device core
- Bus-friendly architecture including programmable slew rate, drive strength, bus-hold and programmable pull-up resistors

The table below lists the MAX V CPLD I/O signals.

Table 7. MAX V CPLD I/O Signals

Signal Name	Description
FA_A[26:1]	Flash Address Bus
FM_D[31:0]	Flash Data Bus
FLASH_CLK	Flash Clock
FLASH_RESETn	Flash Reset
FLASH_CEn[1:0]	Flash Chip Enable
FLASH_OEn	Flash Output Enable
FLASH_WEn	Flash Write Enable
FLASH_ADVn	Flash Address Valid
FLASH_RDYBSYn[1:0]	Flash Chip Ready/Busy
FPGA_CONFIG_D[31:0]	FPGA AvST configuration data bus
FPGA_INIT_DONE	FPGA initialization complete
FPGA_nSTATUS	FPGA status
FPGA_CONF_DONE	FPGA configuration complete
FPGA_nCONFIG	FPGA configuration control pin reset to FPGA
FPGA_ASCLK	FPGA AS configuration clock

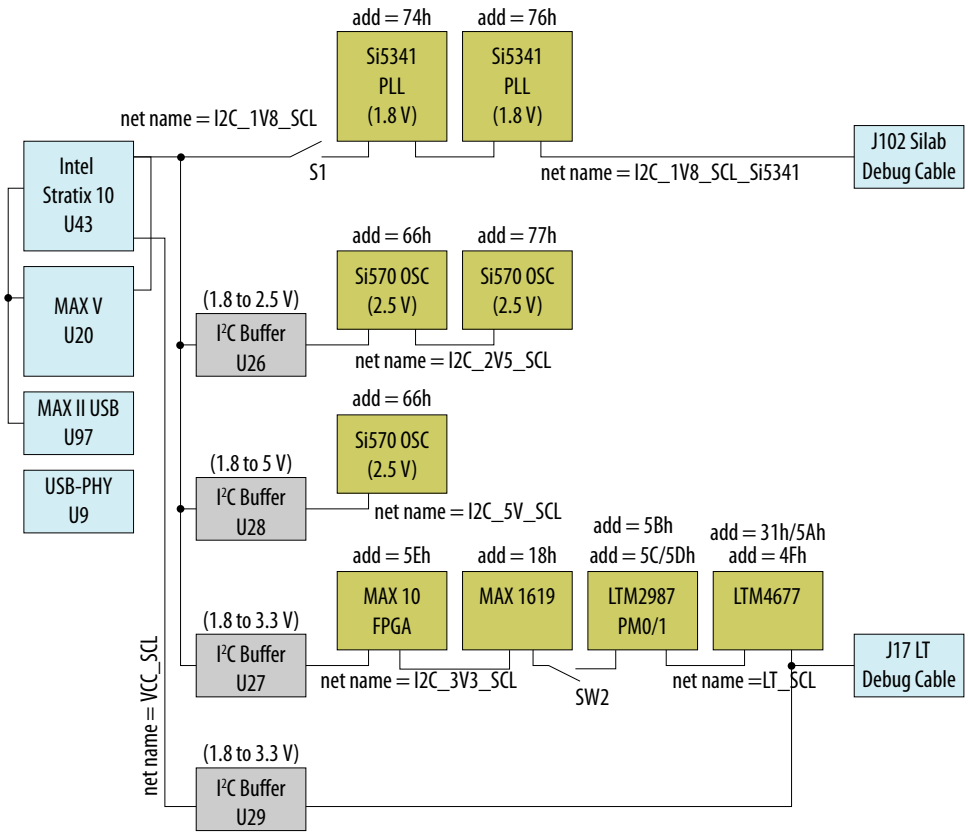
continued...

Signal Name	Description
FPGA_SEU_ERR	FPGA configuration SEU error
FPGA_CvP_DONE	FPGA CvP configuration done
FPGA_SDM	FPGA SDM IO10
FPGA_PR_REQUEST	FPGA partial reconfiguration request
FPGA_PR_DONE	FPGA partial reconfiguration done
FPGA_PR_ERROR	FPGA partial reconfiguration error
FPGA_MSEL[2:0]	FPGA configuration mode setting bits
FPGA_AVST_CLK	FPGA AvST configuration clock
FPGA_AVST_VALID	FPGA AvST configuration data valid
FPGA_AVST_READY	FPGA ready to receive data
I2C_1V8_SCL	MAX V I^2C bus
I2C_1V8_SDA	MAX V I^2C bus
FAPRSNT1V8_N	FMC A present indicator
FBPRSNT1V8_N	FMC B present indicator
SI5341_1_ENn	SI5341 1 ENABLE
SI5341_1_INTn	SI5341 1 interrupt indicators
SI5341_1_RSTn	SI5341 1 reset
SI5341_1_LOLn	SI5341 1 loss of clock indicators
SI5341_2_ENn	SI5341 2 ENABLE
SI5341_2_INTn	SI5341 2 interrupt indicators
SI5341_2_RSTn	SI5341 2 reset
SI5341_2_LOLn	SI5341 2 loss of clock indicators
EN_MASTER[1:0]	ENABLE specific I2C buffer
TEMP_ALERTn	FPGA temperature alert input
OVERTEMPn	FPGA over temperature input
OVERTEMP	Over temperature fan control
FAN_RPM	Fan speed control
USB_CFG[14:0]	Bus between USB Intel MAX 10 and MAX V
USB_MAX5_CLK	Clock from USB PHY chip
MAX_OSC_CLK_1	25MHz / 100 MHz / 125 MHz clock input
MAX5_JTAG_TCK	MAX V Test Clock
MAX5_JTAG_TMS	MAX V Test Mode Select
MAX5_JTAG_TDI	MAX V Test Data Input
MAX5_JTAG_TDO	MAX V Test Data Output

continued...

Signal Name	Description
FACTORY_LOAD	Factory image for configuration
MAX5_SWITCH [2:0]	System MAX V user DIP switch
PGM_SEL	Flash Memory program select pushbutton
PGM_CONFIG	Flash Memory program configuration pushbutton
MAX_RESETn	System MAX V reset pushbutton
CPU_RESETn	CPU reset pushbutton
PGM_LED[2:0]	Flash image program select indicators
MAXV_ERROR	Intel Stratix 10 configuration error indicator LED
MAXV_LOAD	Intel Stratix 10 configuration active indicator LED
MAXV_CONF_DONE	Intel Stratix 10 configuration done indicator LED
MAX5_BE_n[3:0]	Intel Stratix 10 and MAX V data path, byte enable
MAX5_OEn	Intel Stratix 10 and MAX V data path, output enable
MAX5_CSn	Intel Stratix 10 and MAX V data path, chip select
MAX5_WEn	Intel Stratix 10 and MAX V data path, write enable
MAX5_CLK	Intel Stratix 10 and MAX V data path, clock
SPARE[20:1]	Spare bus between MAX V and Intel Stratix 10
CLK_50M_MAX5	50 MHz clock input
FPGA_ASDATA[3:0]	Intel Stratix 10 AS configuration data
CLK_CONFIG	100 MHz clock input

Figure 4. I2C Block Diagram



4.4. FPGA Configuration

This section describes the FPGA, flash memory and MAX V CPLD System Controller device programming methods supported by the Intel Stratix 10 GX Transceiver Signal Integrity development kit.

Three configuration methods except AS mode are mostly used on the Intel Stratix 10 transceiver signal integrity development kit.

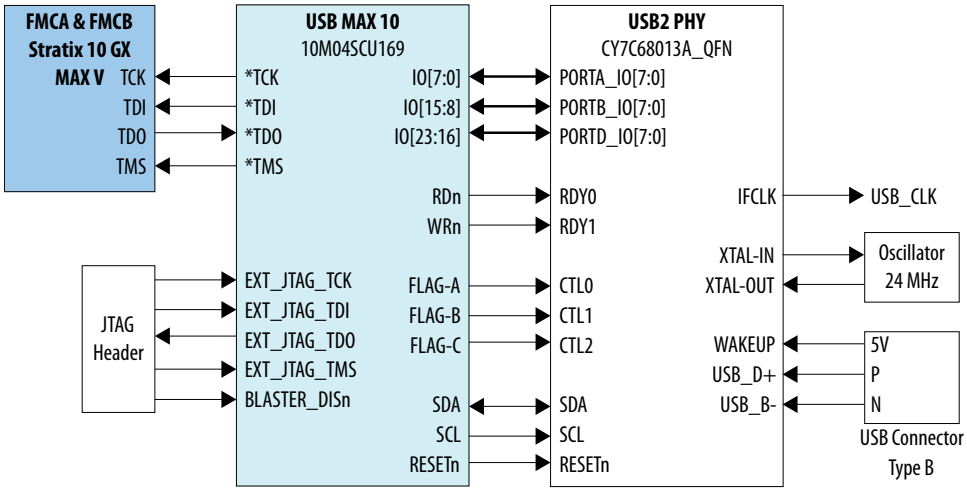
- Embedded Intel FPGA Download Cable II is the default method for configuring the FPGA at any time using the Intel Quartus Prime Programmer in JTAG mode with the supplied USB cable.
- MAX V configures the FPGA device via AvST mode using stored images from CFI flash devices either at power-up or pressing the MAX_RESETn/PGM_CONFIG push button.
- JTAG external header for debugging. Intel recommends that you use lower JTAG clock frequency value such as 16 MHz.

4.4.1. FPGA Programming over Embedded Intel FPGA Download Cable II

Embedded Intel FPGA Download Cable II is the default method for configuring the Intel Stratix 10 GX FPGA using the Intel Quartus Prime Programmer in the JTAG mode with the supplied USB cable.

The figure below shows the conceptual block diagram for the embedded Intel FPGA Download Cable II.

Figure 5. Intel FPGA Download Cable II Block Diagram



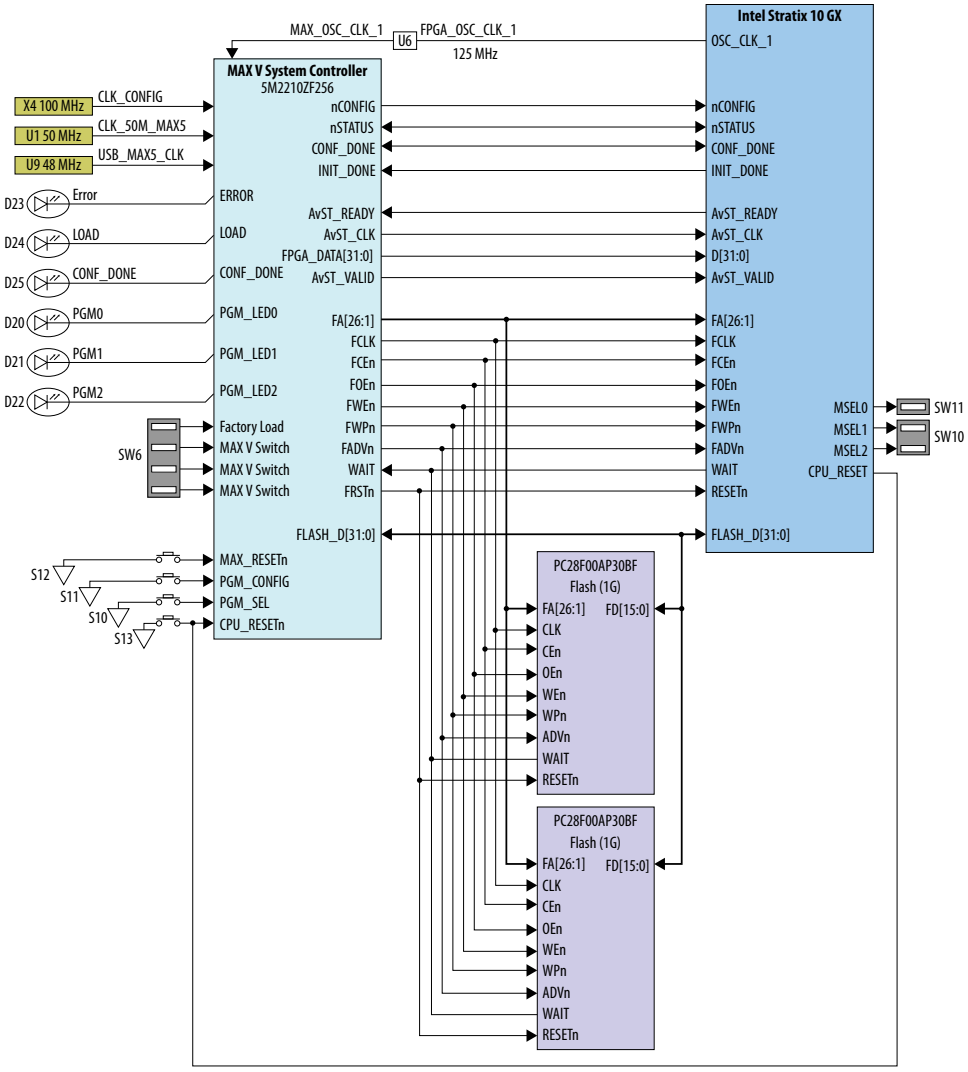
The embedded Intel FPGA Download Cable II core for USB-based configuration of the Intel Stratix 10 GX FPGA device is implemented using a Type-B USB connector, a CY7C68013A USB2 PHY device, and an Intel Intel MAX 10 10M04SCU169 FPGA. This will allow configuration of the Intel Stratix 10 GX FPGA device using a USB cable directly connected to a computer running Intel Quartus Prime software without requiring the external Intel FPGA Download Cable II dongle. This design will convert USB data to interface with the Intel Stratix 10 GX FPGA's dedicated JTAG port. Four LEDs are provided to indicate Intel FPGA Download Cable II activity. The embedded Intel FPGA Download Cable II is automatically disabled when an external Intel FPGA Download Cable II dongle is connected to the JTAG header.

4.4.2. FPGA Programming from Flash Memory

The figure below shows a detailed schematic block diagram for the MAX V + Flash AvSTx32 mode configuration implementation.

Note: Typical JTAG clock frequency for CFI Flash programming via PFL II core is 16 MHz. You may try it with a lower frequency such as 6 MHz if it fails with 16 MHz.

Figure 6. MAX V + Flash AvSTx32 Configuration Block Diagram



Once the FPGA is successfully initialized and in user mode, the CPLD will tri-state its Flash interface signals to avoid contention with the FPGA. The PGMSEL dipswitch (S10) is provided to select between two POF files (FACTORY and USER) stored on the Flash.

The Parallel Flash Loader II (PFL II) Megafunction is used to implement the AvSTx32 configuration in the MAX V CPLD. The PFL II Megafunction reads data from the flash and converts it to AvST format. This data is written into the Intel Stratix 10 GX FPGA device through dedicated AvST CLK and FPGA Config Data [31:0] pins at corresponding clock rate, such as 25 MHz, 50 MHz and 100 MHz.

Implementation will be done using an Intel MAX V 5M2210ZF256FBGA CPLD acting as the AvST download controller and two 1G Flash devices. The Flash will be Numonyx 1.8V core, 1.8V I/O 1Gigabit CFI NOR-type device (P/N: PC28F00AP30BF). The MAX V CPLD shares the CFI Flash interface with the Intel Stratix 10 GX FPGA. No arbitration is needed between MAX V CPLD and Intel Stratix 10 GX FPGA to access the Flash as the CPLD only has access prior to FPGA initialization.

After a POWER-ON or RESET (reconfiguration) event, the MAX V device shall configure the Intel Stratix 10 GX FPGA in the AvSTx32 mode with either the FACTORY POF or an USER DEFINED POF depnding on the FACTORY_LOAD setting.

The MSEL[2:0] pins indicate which configuration scheme is chosen. The manufacturing default condition is [000] for AvSTx32 scheme.

For different configuration modes, MSEL [2:0] signals must be set acccording to the table below:

Table 8. Support Configuration Modes for Stratix 10 Transceiver Signal Integrity Development Kit

Configuration Scheme	MSEL [2:0]
Avalon-ST (x32)	000
Avalon-ST (x16)	101
AS (Normal mode)	011
JTAG only	111
Not supported	Other Settings

4.4.3. FPGA Programming over External Intel FPGA Download Cable II

The JTAG chain allows programming of both the Intel Stratix 10 GX FPGA and MAX V CPLD devices using an external Intel FPGA Download Cable II dongle or the on-board Intel FPGA Download Cable II via the USB Interface Connector.

During board bring-up, and as a back-up in case the on-board Intel FPGA Download Cable II has a problem, the external Intel FPGA Download Cable II dongle can be used to program both the Intel Stratix 10 and MAX V CPLD via the Intel FPGA Download Cable II 2x5 pin 0.1" programming header (J14)

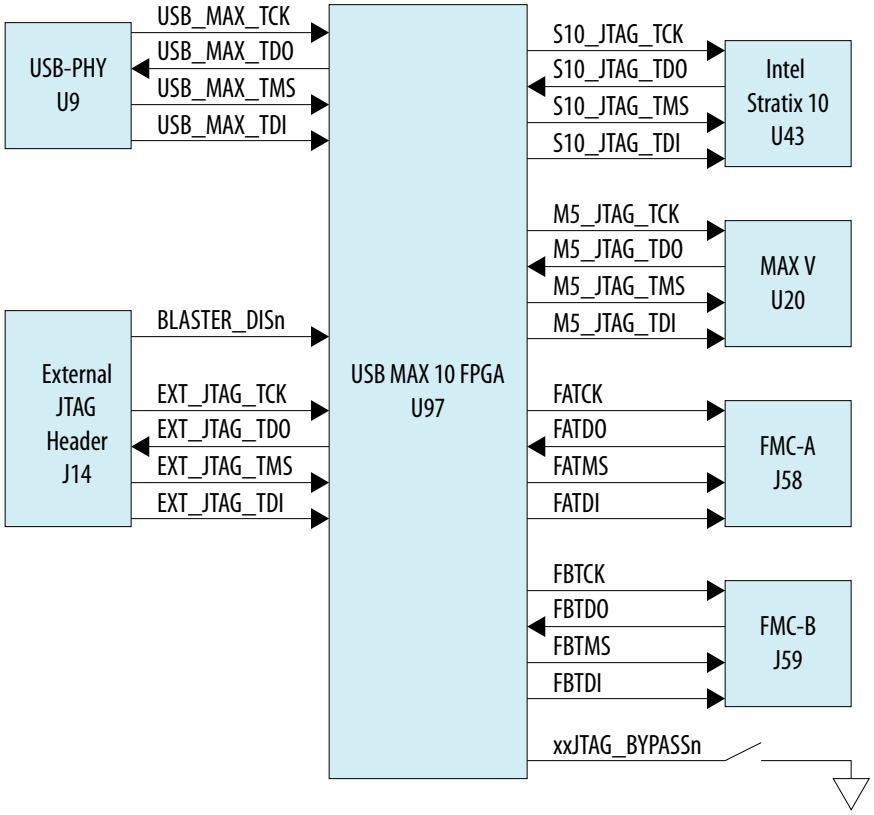
Another 2x5 pin 0.1" vertical non-shrouded header (J15) is provided on the board for programming the Intel MAX 10 FPGA for configuring the Intel FPGA Download Cable II circuitry. Once the Intel FPGA Download Cable II is configured and operational, the Intel FPGA Download Cable II can be used for subsequent programming of the Intel Stratix 10 GX FPGA and MAX V CPLD.

The Intel FPGA Download Cable II JTAG chain connects four JTAG nodes in the following order, with the option to bypass the Intel Stratix 10, MAX V, FMC A or FMC B by a dip switch SW3 setting as follows:

- Switch closed/ON: Corresponding JTAG node is bypassed.
- Switch open/OFF: Corresponding JTAG node is enabled in the JTAG chain.

Pin 2 of the J14 Header is used to disable the embedded Intel FPGA Download Cable II by connecting it to the embedded Intel FPGA Download Cable IIs low active disable pin with a pull-up resistor. Since Pin 2 from the mating Intel FPGA Download Cable II dongle is GND, when the dongle is connected into the JTAG header, the embedded Intel FPGA Download Cable II is disabled to avoid contention with the external Intel FPGA Download Cable II dongle.

Figure 7. JTAG Chain



4.5. Status Elements

The development board includes board-specific status LEDs and switches for enabling and configuring various features on the board, as well as 16 character x 2 line LCD for displaying board power and temperature measurements. This section describes these status elements.

Table 9. Board Specific LEDs

Board Reference	Signal Name	Description
D29	---	Green LED. Power 3.3V present.
D31	---	Green LED. Power 3.3V PRE present.
D32	---	Green LED. Power 12V present.
D5	FAPRSNT_N	Green LED. FMC A daughter card present.
D6	FBPRSNT_N	Green LED. FMC B daughter card present.
D36	ERR_LED_N	Amber LED. System Power error indicator.
D1	JTAG_RX	Green LED. JTAG receiver activity indicator.

continued...

Board Reference	Signal Name	Description
D2	JTAG_TX	Green LED. JTAG transmitter activity indicator.
D3	SC_RX	Green LED. System console receiver activity indicator.
D4	SC_TX	Green LED. System console transmittter activity indicator.
D7	ENET_LED_TX	Green LED. Blinks to indicate Ethernet PHY transmit activity.
D8	ENET_LED_RX	Green LED. Blinks to indicate Ethernet PHY activity.
D9	ENET_LED_LINK1000	Green LED. Illuminates to indicate Ethernet linked at 1000 Mbps connection speed.
D10	ENET_LED_LINK100	Green LED. Illuminates to indicate Ethernet linked at 100 Mbps connection speed.
D11	ENET_LED_LINK10	Green LED. Illuminates to indicate Ethernet linked at 10 Mbps connection speed.
D27	OVERTEMPn	Amber LED. Intel Stratix 10 over temperature indicator.

4.6. Setup Elements

This development board includes several different kinds of setup elements. This section describes the following setup elements:

- JTAG Chain Device removal switch
- Program Select pushbutton
- MAX V Reset pushbutton
- CPU Reset pushbutton

JTAG Chain Device Removal Switch

The JTAG chain connects the Intel Stratix 10 GX FPGA, the MAX V CPLD, FMC A and FMC B in a chain, with the option to selectively bypass each JTAG node by four dip switch setting.

Program Select Pushbutton

After a POWER-ON or RESET (reconfiguration) event, the MAX V configures the Intel Stratix 10 GX FPGA in the AvST mode with either the FACTORY POF or a USER-DEFINED POF depending on FACTORY_LOAD setting. The setting of the PGMSEL bit is selected by the PGMSEL pushbutton. Pressing this pushbutton and observing the program LEDs (FACTORY or USER) dictates the program selection. Then, the PGM_CONFIG pushbutton must be pressed to load the program.

MAX V Reset Pushbutton

This pushbutton is the development board's Master Reset. This pushbuttton is connected to the MAX V CPLD (MAX_RESETn pin) that is used for AvST configuration. When this button is pressed, the MAX V CPLD initiates a reloading of the stored image from flash memory using AvST configuration mode. The image that is reloaded depends on the PGMSEL setting.

CPU Reset Pushbutton

This pushbutton is the Nios II CPU Reset. This button is connected to a Intel Stratix 10 GX FPGA global signal input pin and can be used by Nios II implementations as a dedicated CPU Reset button. This button is also connected to the MAX V CPLD so that the FPGA device can be reset right after its configuration with AvST mode.

4.7. User Input-Output Components

This section describes the user I/O interface to the FPGA. The following I/O elements are described:

- User-defined pushbuttons
- User-defined DIP switches
- User-defined LEDs
- Character LCD

4.7.1. User-Defined Pushbuttons

The development kit includes 8 user-defined pushbuttons and 4 system pushbuttons that allow you to interact with the Intel Stratix 10 GX FPGA. When you press and hold down the pushbutton, the device pin is set to logic 0; when you release the pushbutton, the device pin is set to logic 1. There is no board-specific function for these general user pushbuttons.

The table below lists the pushbuttons, schematic signal names and their corresponding Intel Stratix 10 GX FPGA device pin numbers.

Table 10. User-Defined Pushbuttons

Board Reference	Schematic Signal Name	Description	Intel Stratix 10 Device Pin Number
S2	USER_PB0	User pushbutton	BG17
S3	USER_PB1	User pushbutton	BE17
S4	USER_PB2	User pushbutton	BH18
S5	USER_PB3	User pushbutton	BJ19
S6	USER_PB4	User pushbutton	BF17
S7	USER_PB5	User pushbutton	BH17
S8	USER_PB6	User pushbutton	BJ18
S9	USER_PB7	User pushbutton	BJ20
S10	PGM_SEL	System pushbutton	N/A

continued...

Board Reference	Schematic Signal Name	Description	Intel Stratix 10 Device Pin Number
S11	PGM_CONFIG	System pushbutton	N/A
S12	MAX_RESETn	System pushbutton	N/A
S13	CPU_RESETn	System pushbutton	AW10

4.7.2. User-Defined DIP Switch

Board reference SW4 and SW5 are two 4-pin DIP switches. The switches are user-defined and are provides additional FPGA input control. When the switch is in the OPEN position, a logic 1 is selected. When the switch is in the CLOSED or ON position, a logic 0 is selected. There is no board-specific function for these switches.

The table below lists the schematic signal names of each DIP switch and their corresponding Intel Stratix 10 GX FPGA pin numbers.

Table 11. User-Defined Switches

Board Reference	Schematic Signal Name	Intel Stratix 10 GX Device Pin Number
SW5.4	USER_DIP0	AV20
SW5.3	USER_DIP1	AV21
SW5.2	USER_DIP2	AT19
SW5.1	USER_DIP3	BE19
SW4.4	USER_DIP4	BB18
SW4.3	USER_DIP5	BC18
SW4.2	USER_DIP6	BD18
SW4.1	S10_UNLOCK	BG18

4.7.3. User-Defined LEDs

The development board includes 8 user-defined LEDs. Board references D12 through D19 are user LEDs that allow status and debugging signals to be driven to the LEDs from the designs loaded into the Intel Stratix 10 GX FPGA device. The LEDs illuminate when a logic 0 is driven and turns off when a logic 1 is driven. There is no board-specific function for these LEDs.

The table below lists the user-defined schematic signal names and their corresponding Intel Stratix 10 GX FPGA device pin numbers.

Table 12. User-Defined LEDs

Board Reference	Schematic Signal Name	Intel Stratix 10 Device Pin Number
D12	USER_LED0	BC21
D13	USER_LED1	BC20
D14	USER_LED2	BA20
D15	USER_LED3	BA21

continued...

Board Reference	Schematic Signal Name	Intel Stratix 10 Device Pin Number
D16	USER_LED4	BD21
D17	USER_LED5	BB20
D18	USER_LED6	AW21
D19	USER_LED7	AY21

4.7.4. Character LCD

A 16 character x 2 line LCD display is connected to the Intel Stratix 10 GX FPGA device to display board information and IP address. The LCD module used is New Haven - NHD-0216K3Z-NSW-BBW-V3. This LCD module will be mounted to the Intel Stratix 10 GX transceiver signal integrity development board using a 1x10 vertical male 0.1" header on the left side of the module and three plastic standoffs. This mounting scheme allows low profile (less than 0.5 inches in height) components to be placed underneath the LCD module, preserving board real-estate.

The table below summarizes the LCD pin assignments. This signal names and directions are relative to the Intel Stratix 10 GX FPGA.

Table 13. LCD Pin Assignments and Schematic Signal Names

Board Reference	Schematic Signal Name	Description
7	I2C_5V_SCL	I^2C serial clock
8	I2C_5V_SDA	I^2C serial data

4.8. Clock Circuits

4.8.1. Transceiver Dedicated Clocks

Dedicated clocking scheme that is implemented on the Intel Stratix 10 GX transceiver signal integrity development board allows four different protocols to run simultaneously by the Intel Stratix 10 GX FPGA.

Four differential clock sources are provided from an I^2C programmable VCO oscillator or PLL to the dedicated REFCLK input pins of transceiver blocks on both sides of the FPGA. The default frequencies for these two oscillators and PLLs at startup are:

- 644.53125 MHz (Y1 left side xcvrs and U6 right side xcvrs)
- 706.25 MHz (Y2 right side xcvrs)
- 625 MHz (U5 left side xcvrs and U6 right side xcvrs)
- 614.4 MHz (U5 left side xcvrs)

The default frequencies can be overridden and a different frequency can be programmed into the oscillators and PLLs for support of other protocols.

Note: Programmed frequencies are lost upon a board power down. Oscillator and PLL frequencies return to their default frequency upon power up.

Each oscillator or PLL provides a differential LVDS trigger output to SMA connectors for scope or other lab equipment triggering purposes.

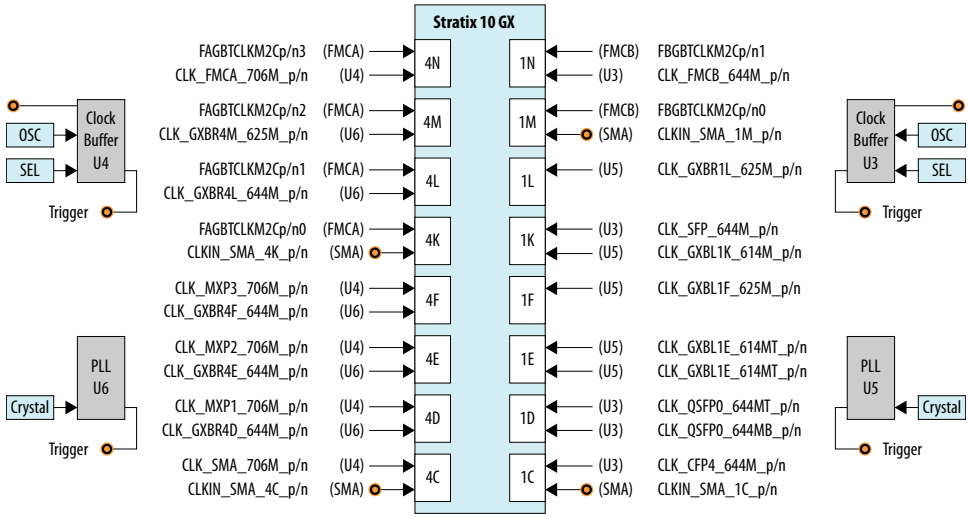
In addition to the two oscillators and PLLs, each sides have two dedicated differential REFCLK input from a pair of SMA connectors to allow use of lab equipment clock generators as the transceiver clock source.

The four inputs below connect directly to the transceiver clock inputs:

- J65/J66 SMA connectors direct connection to REFCLK_GXB1C block
- J67/J68 SMA connectors direct connection to REFCLK_GXB1M block
- J69/J70 SMA connectors direct connection to REFCLK_GXB4C block
- J71/J72 SMA connectors direct connection to REFCLK_GXB4K block

The figure below shows the dedicated transceiver clocks that are implemented on the Intel Stratix 10 GX FPGA development kit.

Figure 8. Transceiver Dedicated Clocks



4.8.2. General-Purpose Clocks

In addtion to transceiver dedicated clocks, five other clock sources are provided to the FPGA Global CLK inputs for general FPGA design as shown in the figure below.

The usage of these clocks is as follows:

- 50 MHz oscillator through an SL18860 buffer for Nios II applications. USB_FPGA_CLK drives from on-board Intel FPGA Download Cable circuit.
- 25 MHz crystal supplied to an ICS557-03 Spread Spectrum differential clock buffer. The available frequencies and down spread percentages available from the spread spectrum buffer as shown in the table below.
- External differential clock source from SMA connectors. Dedicated differential output clock to SMA connectors.
- Three clock outputs are provided from two Si5341 PLLs:
  - `CLK_S10_BOT_100M: 100 MHz LVDS standard`
  - `CLK_S10_TOP_125M: 125 MHz LVDS standard`
  - `FPGA_OSC_CLK_1: 125 MHz 1.8V CMOS standard`
- Another clock source is clock from FMC daughter cards.

Figure 9. FPGA Clocks

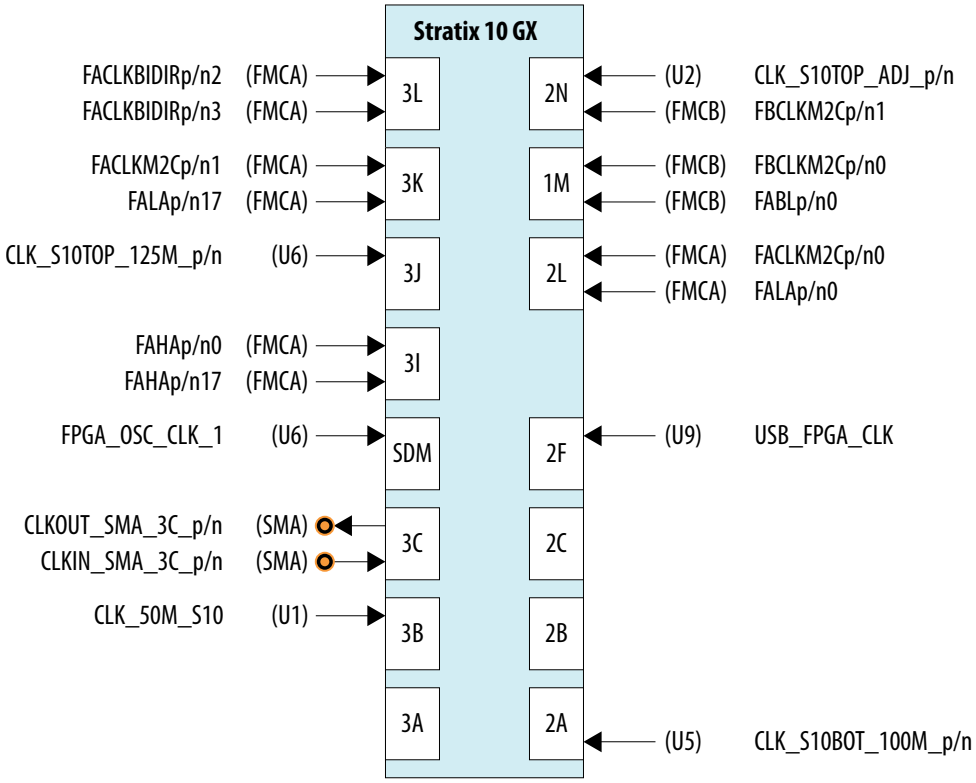


Table 14. Spread Spectrum Clock Settings and Frequencies

Spread Spectrum Buffer (Inputs)		Output Clock Select (MHz)	Spread (%)
SS1/S1	**SS0/S0**		
0	0	25 (Default)	Center+/-0.25

continued...

Spread Spectrum Buffer (Inputs)		Output Clock Select (MHz)	Spread (%)
0	1	100	Down -0.5
1	0	125	Down -0.75
1	1	200	No Spread

4.8.3. Embedded Intel FPGA Download Cable II Clock

A 24 MHz crystal is dedicated for the embedded Intel FPGA Download Cable II circuit. The crystal is used to clock the Cypress CY7C68013A USB2 PHY device.

4.9. Transceiver Channels

The Intel Stratix 10 GX transceiver signal integrity development kit dedicates 78 channels from both the left and right sides of the device. Transceiver channels are allocated as shown in the table below.

Table 15. Stratix 10 GX FPGA Transceiver Channels

Transceiver Channel	Data Rate	Number of Channels
2.4 mm RF Platinum channel	17.4 Gbps or 28.3 Gbps (applies to GXT channels only)	1
2.4 mm RF Gold channel	17.4 Gbps or 28.3 Gbps (applies to GXT channels only)	1
2.4 mm RF channels	17.4 Gbps or 28.3 Gbps (applies to GXT channels only)	4
MXP connector 0	17.4 Gbps or 28.3 Gbps (applies to GXT channels only)	4
MXP connector 1	17.4 Gbps or 28.3 Gbps (applies to GXT channels only)	4
MXP connector 2	17.4 Gbps or 28.3 Gbps (applies to GXT channels only)	4
CFP4 Optical Interface	17.4 Gbps or 28.3 Gbps (applies to GXT channels only)	4
QSFP28 0 Optical Interface	17.4 Gbps or 28.3 Gbps (applies to GXT channels only)	4
QSFP28 1 Optical Interface	17.4 Gbps or 28.3 Gbps (applies to GXT channels only)	4
SFP+ 0 Optical Interface	14 Gbps	1
SFP+ 1 Optical Interface	14 Gbps	1
FMC A Interface	17.4 Gbps or 28.3 Gbps (applies to GXT channels only)	24
FMC B Interface	17.4 Gbps or 28.3 Gbps (applies to GXT channels only)	16
External loopback Interface	17.4 Gbps or 28.3 Gbps (applies to GXT channels only)	6

Figure 10. Stratix 10 GX FPGA Transceiver Usage Block Diagram

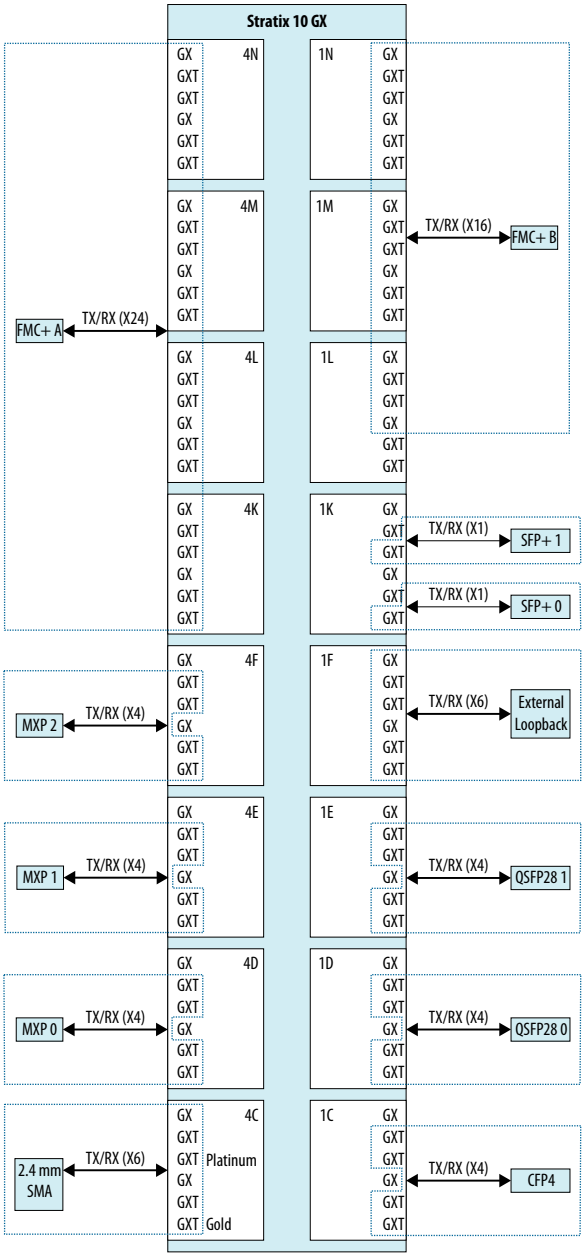


Table 16. 2.4 mm RF Interface

Schematic Signal Name	Stratix 10 FPGA Pin Number	Description
GXB_4C_TXp/n[5:0]	Positive pin location increases from index 0: BJ4, BF5, BG3, BE3, BF1, BC3	2.4 mm RF GXB Transmitter
GXBR_4C_RXp/n[5:0]	Positive pin location increases from index 0: BH9, BJ7, BG7, BE7, BC7, BD5	2.4 mm RF GXB Receiver

Table 17. MXP Interface

Schematic Signal Name	Stratix 10 FPGA Pin Number	Description
GXBL_4D_TXp/n[1:0][4:3]	Positive pin location increases from index 0: BD1, BA3, AW3, AY1	MXP 1 GXB Transmitter
GXBL_4D_RXp/n[1:0][4:3]	Positive pin location increases from index 0: BA7, BB5, AY5, AU7	MXP 1 GXB Receiver
GXBL_4E_TXp/n[1:0][4:3]	Positive pin location increases from index 0: AV1, AR3, AP1, AN3	MXP 2 GXB Transmitter
GXBL_4E_RXp/n[1:0][4:3]	Positive pin location increases from index 0: AR7, AT5, AN7, AM5	MXP 2 GXB Receiver
GXBL_4F_TXp/n[1:0][4:3]	Positive pin location increases from index 0: AK1, AL3, AJ3, AF1	MXP 3 GXB Transmitter
GXBL_4F_RXp/n[1:0][4:3]	Positive pin location increases from index 0: AL7, AH5, AF5, AG7	MXP 3 GXB Receiver

Figure 11. MXP connector pin function mapping

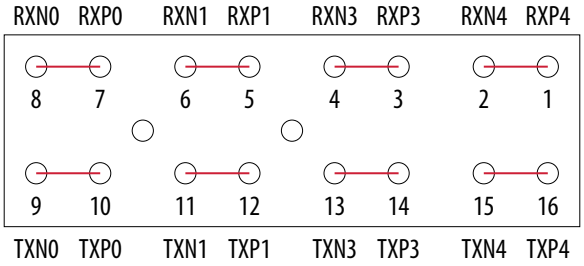


Table 18. Optical Modules Interface

Schematic Signal Name	Intel Stratix 10 FPGA Pin Number	Description
GXBL_1C_TXp/n[1:0][4:3]	Positive pin location increases from index 0: BJ46, BF45, BE47, BF49	CFP4 GXB Transmitter
GXBL_1C_RXp/n[1:0][4:3]	Positive pin location increases from index 0: BH41, BJ43, BE43, BC43	CFP4 GXB Receiver
GXBL_1D_TXp/n[1:0][4:3]	Positive pin location increases from index 0: BD49, BA47, AW47, AY49	QSFP28 0 GXB Transmitter
GXBL_1D_RXp/n[1:0][4:3]	Positive pin location increases from index 0: BA43, BB45, AY45, AU43	QSFP28 0 GXB Receiver
GXBL_1E_TXp/n[1:0][4:3]	Positive pin location increases from index 0: AV49, AR47, AP49, AN47	QSFP28 1 GXB Transmitter
GXBL_1E_RXp/n[1:0][4:3]	Positive pin location increases from index 0: AR43, AT45, AN43, AM45	QSFP28 1 GXB Receiver
GXBL_1K_TXp/n 0/3	Positive pin location increases from index 0: AE47, AA47	SFP+ 0/1 GXB Transmitter
GXBL_1K_RXp/n 0/3	Positive pin location increases from index 0: AC43, AB45	SFP+ 0/1 GXB Receiver

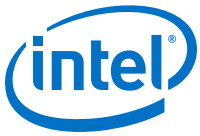


Table 19. FMC Interface

Schematic Signal Name	Intel Stratix 10 FPGA Pin Number	Description
FAC2Mp/n[23:0]	Positive pin location increases from index 0: AE3, AC3, AD1, AA3, AB1, W3, Y1, V1, U3, T1, P1, R3, M1, N3, K1, L3, H1, J3, F1, G3, D1, E3, C3, B5	FMC A GXB Transmitter
FAM2Cp/n[23:0]	Positive pin location increases from index 0: AC7, AD5, AA7, AB5, W7, Y5, V5, U7, T5, P5, R7, M5, N7, K5, L7, H5, J7, F5, G7, D5, E7, C7, A7, B9	FMC A GXB Receiver
FBC2Mp/n[15:0]	Positive pin location increases from index 0: U47, T49, P49, R47, M49, N47, K49, L47, H49, J47, F49, G47, D49, E47, C47, B45	FMC B GXB Transmitter
FBM2Cp/n[15:0]	Positive pin location increases from index 0: T45, P45, R43, M45, N43, K45, L43, H45, J43, F45, G43, D45, E43, C43, A43, B41	FMC B GXB Receiver

Table 20. External Loopback Interface

Schematic Signal Name	Intel Stratix 10 FPGA Pin Number	Description
GXBL_1F_TXp/n[5:0]	Positive pin location increases from index 0: AK49, AL47, AH49, AJ47, AF49, AG47	External loopback GXB Transmitter
GXBL_1F_RXp/n[5:0]	Positive pin location increases from index 0: AL43, AH45, AJ43, AF45, AG43, AE43	External loopback GXB Receiver

4.10. Communication Ports

The Intel Stratix 10 GX transceiver signal integrity development board supports a 10/100/1000 BASE-T Ethernet connection using a Marvell 88E1111 PHY device and the Intel Triple-Speed Ethernet Megacore MAC function. The device is an auto-negotiating Ethernet PHY with an SGMII interface to the FPGA.

The Intel Stratix 10 GX FPGA device can communicate with the LVDS interfaces at up to 1.25 Gbps. The MAC function is provided in the FPGA for typical networking applications. The Marvell 88E1111 PHY uses 2.5 V and 1.2 V power rails and requires a 25-MHz reference clock driven from a dedicated oscillator. It interfaces to an RJ-45 connector with internal magnetics that are used for driving copper lines with Ethernet traffic.

Table 21. Ethernet PHY Pin Assignments

Schematic Signal Name	Marvell 88E1111 (U23) PHY Pin Number	Description
ENET_LED_LINK1000	60/73	1000 Mb link LED
ENET_LED_LINK100	74	100 Mb link LED
ENET_LED_LINK10	59/76	10 Mb link LED
ENET_LED_TX	68	TX data active LED
ENET_LED_RX	69	RX data active LED

continued...

Schematic Signal Name	Marvell 88E1111 (U23) PHY Pin Number	Description
ENET_SGMII_TX_P	82	SGMII transmit
ENET_SGMII_TX_N	81	SGMII transmit
ENET_SGMII_RX_P	77	SGMII receive
ENET_SGMII_RX_N	75	SGMII receive
ENET_XTAL_25MHZ	55	25 MHz clock
ENET_T_INTn	23	Management bus interrrupt
ENET_RSET	30	Device reset
MDIO_T	24	Management bus data input/output
MDC_T	25	Management bus data clock
MDI_P0	29	Management bus data
MDI_N0	31	Management bus data
MDI_P1	33	Management bus data
MDI_N1	34	Management bus data
MDI_P2	39	Management bus data
MDI_N2	41	Management bus data
MDI_P3	42	Management bus data
MDI_N3	43	Management bus data

4.11. Flash Memory

The development board has two 1-Gbit CFI compatible synchronous flash device for non-voltaile storage of the FPGA configuration data, board information, test application data and user code space.

Two flash devices are implemented to achieve a 32-bit wide data bus at 16 bits each per device. The target device is a Micron PC28F00AP30BF CFI Flash device. Both MAX V CPLD and Intel Stratix 10 GX FPGA can access this Flash device.

MAX V CPLD accesses are for AvST configuration of the FPGA at power-on and board reset events. It uses the PFL Megafunction. Intel Stratix 10 GX FPGA access to the flash memory's user space is done by Nios II for the BUP application. The flash is wired for WORD mode operation to support AvSTx32 download directly.

The table below shows the memory map for the on-board flash. This memory provides non-volatile storage for two FPGA bit-streams as well as various settings for data used for the Board Update Portal (BUP) image and on-board devices such as PFL II configuration bits.

Table 22. Flash Memory Map

Block Description	Size	Address
Board Test System	512 KB	0x09F4.0000 - 09FB.FFFF
User Software	14,336 KB	0x0914.0000 - 09F3.FFFF
Factory Software	8,192 KB	0x0894.0000 - 0913.FFFF
zipfs	8,192 KB	0x0814.0000 -0893.FFFF
User Hardware 2	44,032 KB	0x0564.0000 - 0813.FFFF
User Hardware 1	44,032 KB	0x02B4.0000 - 0563.FFFF
Factory Hardware	44,032 KB	0x0004.0000 - 02B3.FFFF
PFL Option Bits	64 KB	0x0003.0000 - 0003.FFFF
Board Information	64 KB	0x0002.0000 - 0002.FFFF
Ethernet Option Bits	64 KB	0x0001.0000 - 0001.FFFF
User Design Reset	64 KB	0x0000.0000 - 0000.FFFF

Each FPGA bit-stream can be a maximum of 254.25 Mbits (or less than 32 MB) for the Intel Stratix 10 GX FPGA device. The remaining area is designated as RESERVED flash area for storage of the BUP image and PFL configuration settings, software binaries and other data relevant to the FPGA design.

Table 23. Flash Memory Pin Assignments Table

Flash Memory Device Pin Number (U33/U34)	Schematic Signal Name	Description	Intel Stratix 10 Device Pin Number
A1 (U33/U34)	FM_A1	Address Bus	BB30
B1 (U33/U34)	FM_A2	Address Bus	BF31
C1 (U33/U34)	FM_A3	Address Bus	BG32
D1 (U33/U34)	FM_A4	Address Bus	BC35
D2 (U33/U34)	FM_A5	Address Bus	BG29
A2 (U33/U34)	FM_A6	Address Bus	BG30
C2 (U33/U34)	FM_A7	Address Bus	BH28
A3 (U33/U34)	FM_A8	Address Bus	BH31
B3 (U33/U34)	FM_A9	Address Bus	BF29
C3 (U33/U34)	FM_A10	Address Bus	BH32
D3 (U33/U34)	FM_A11	Address Bus	BD29
C4 (U33/U34)	FM_A12	Address Bus	BC36
A5 (U33/U34)	FM_A13	Address Bus	BA31
B5 (U33/U34)	FM_A14	Address Bus	BJ29
C5 (U33/U34)	FM_A15	Address Bus	BJ30
D7 (U33/U34)	FM_A16	Address Bus	BA32

continued...

Flash Memory Device Pin Number (U33/U34)	Schematic Signal Name	Description	Intel Stratix 10 Device Pin Number
D8 (U33/U34)	FM_A17	Address Bus	BE28
A7 (U33/U34)	FM_A18	Address Bus	AU30
B7 (U33/U34)	FM_A19	Address Bus	AT30
C7 (U33/U34)	FM_A20	Address Bus	BJ28
C8 (U33/U34)	FM_A21	Address Bus	BG28
A8 (U33/U34)	FM_A22	Address Bus	BE29
G1 (U33/U34)	FM_A23	Address Bus	BD36
H8 (U33/U34)	FM_A24	Address Bus	BH30
B6 (U33/U34)	FM_A25	Address Bus	BC31
B8 (U33/U34)	FM_A26	Address Bus	BC31
F2 (U33)	FM_D0	Data Bus	AV33
E2 (U33)	FM_D1	Data Bus	BC33
G3 (U33)	FM_D2	Data Bus	BD33
E4 (U33)	FM_D3	Data Bus	BJ33
E5 (U33)	FM_D4	Data Bus	BF35
G5 (U33)	FM_D5	Data Bus	AT32
G6 (U33)	FM_D6	Data Bus	BB34
H7 (U33)	FM_D7	Data Bus	BD34
E1 (U33)	FM_D8	Data Bus	AU33
E3 (U33)	FM_D9	Data Bus	AY34
F3 (U33)	FM_D10	Data Bus	BB35
F4 (U33)	FM_D11	Data Bus	BD35
F5 (U33)	FM_D12	Data Bus	BA34
H5 (U33)	FM_D13	Data Bus	BB33
G7 (U33)	FM_D14	Data Bus	AV32
E7 (U33)	FM_D15	Data Bus	BF34
F2 (U34)	FM_D16	Data Bus	AW35
E2 (U34)	FM_D17	Data Bus	BF36
G3 (U34)	FM_D18	Data Bus	AW34
E4 (U34)	FM_D19	Data Bus	BG34
E5 (U34)	FM_D20	Data Bus	BG35
G5 (U34)	FM_D21	Data Bus	BA36
G6 (U34)	FM_D22	Data Bus	AT34
H7 (U34)	FM_D23	Data Bus	AR32

continued...

Flash Memory Device Pin Number (U33/U34)	Schematic Signal Name	Description	Intel Stratix 10 Device Pin Number
E1 (U34)	FM_D24	Data Bus	AU32
E3 (U34)	FM_D25	Data Bus	BJ34
F3 (U34)	FM_D26	Data Bus	BH35
F4 (U34)	FM_D27	Data Bus	AV35
F5 (U34)	FM_D28	Data Bus	AY36
H5 (U34)	FM_D29	Data Bus	AU35
G7 (U34)	FM_D30	Data Bus	AR31
E7 (U34)	FM_D31	Data Bus	AT35
E6 (U33/U44)	FLASH_CLK	Clock	BB29
D4 (U33/U34)	FLASH_RESETn	Reset	BF32
B4 (U33)	FLASH_CEn0	Chip Enable 0	BE32
B4 (U34)	FLASH_CEn1	Chip Enable 1	BF30
F8 (U33/U34)	FLASH_OEn	Output Enable	BC30
G8 (U33/U34)	FLASH_WEn	Write Enable	BE36
F6 (U33/U34)	FLASH_ADVn	Address Valid	BD30
C6 (U33/U34)	FLASH_WPn	Write Protect	N/A
F7 (U33)	FLASH_RDYBSYn0	Ready/Busy	BJ31
F7 (U34)	FLASH_RDYBSYn1	Ready/Busy	AT29

5. System Power

5.1. Power Guidelines

Intel Stratix 10 GX transceiver signal integrity development kits can be powered by either Intel provided 240 W brick or a standard ATX power supply which provides more than 240 W power.

Use Intel provided 24-pin to 6-pin adapter cable to hook up ATX power supply's 24-pin ATX output with Intel Stratix 10 transceiver signal integrity development kit's J103 connector. Do not plug an ATX power supply 6-pin connector into J103 connector directly.

You can supply power for VCC, VCCERAM, VCCRL, VCCRR, VCCT and VCCH rails with external equipment by following the two steps outlined below for such kind of application:

1. Turn OFF corresponding on-board regulators via SW9 or S14 dipswitch before board power up.
2. Supply power with banana jacks (J92, J94) or power terminations (J19, J86, J89, J91, J83). Manage the power-up and power-down sequence for on-board regulators and external equipments with necessary tools (LTpowerplay).

5.2. Power Supply

Power supply for this development kit is provided through an external laptop style DC power brick connected to a 6-pin ATX power connector. The input voltage is in the range of 12V +/- 5%. This DC voltage is then stepped down to the various power rails used by the components on the development board.

Important: The power rails on the development board have the option to be supplied from an external source through a banana jack or power terminal connectors by first disabling corresponding power regulator using SW9/S14 DIP Switch.

Table 24. Power per Device on the Development Board

Device	Voltage Name	Voltage Value (Volts)	Note
Intel Stratix 10 GX FPGA The device can either be 1SG280LU2F50E2VG (L-Tile version) or 1SG280HU2F50E2VG (H-Tile version).	S10_VCC	0.85/VID	Core and periphery power
	S10_VCCRL	1.12/1.03	Left XCVR RX path
	S10_VCCRR	1.12/1.03	Right XCVR RX path
	S10_VCCT	1.12/1.03	XCVR TX path
	S10_VCCERAM	0.9	Memory and PLL digital power

continued...

Device	Voltage Name	Voltage Value (Volts)	Note
	S10_VCCH	1.8	XCVR and PLL analog power
	1.8V	1.8	I/O voltage and I/O pre-drivers
	2.4V	2.4	VCCFUSEWR power
	FMCA_VADJ	1.8/1.5/1.35/1.2	I/O Voltage
	FMCB_VADJ	1.8/1.5/1.35/1.2	I/O Voltage
USB Intel MAX 10 (10M04SCU169)	3.3V_PRE	3.3	Core, PLL and VCCIO
	1.8V_PRE	1.8	VCCIO for Intel Stratix 10 Interface
PWR Intel MAX 10 (10M16SAU169)	3.3V_STBY	3.3	Intel Power Management Chip
MAX V (EPM2210F256)	1.8V	1.8	System Controller
Flash (PC28F00AP30BFx2)	1.8V	1.8	CFI Flash
USB PHY (CY7C68103)	3.3V_PRE	3.3	USB PHY
Ethernet PHY (88E1111)	2.5V	2.5	Ethernet PHY
Power Monitor (LTM2987)	12V_IN	12	Linear Tech Power Management Chip
Clock Buffer (SL18860DC)	1.8V	1.8	Core Clock Buffer
SS Clock Generator (ICS557)	3.3V	3.3	Spread Spectrum / Clock Select capability to core clock
Programmable Oscillator (Si570x2) Clock Buffer (Si533311x2)	2.5V	2.5	Transceiver Reference Clock Buffers
Programmable PLL (Si5341x2)	1.8V	1.8	Transceiver Reference Clock and Core Clock
	3.3V	3.3	
Power Measurement (LTC2418)	5V	5	Measure current in Intel power management solution
DAC (DAC7578)	3.3V_STBY	3.3	Trim voltage in Intel power management solution
CFP4 Module	3.3V	3.3	CFP4 Module
QSFP28 Modules	3.3V	3.3	QSFP28 Modules
SFP+ Modules	3.3V	3.3	SFP+ Modules

5.3. Power Management

Two power management solutions are provided in the Intel Stratix 10 GX Transceiver Signal Integrity Development Kit:

- Linear Tech LTM2987
- Intel power Intel MAX 10 logic

You can select either of the aforementioned power management solutions by using Sw8-3.

LTM2987 or power Intel MAX 10 devices are capabale of measuring the voltage, measuring the current, trimming the voltage and sequencing the order at power on and power off. Voltages can be trimmed upto +/- 10%. Communication to these devices is through I^2C interface. A Linear Technology power monitor application known as LTPowerPlay is utilized to measure, trim and observe each voltage rail's condition.

Table 25. Functions supported by the two Power Management Solutions

Rail Name	LT/Intel Voltage Monitor	LT/Intel Current Monitor	LT Voltage Trim	Intel Voltage Trim	LT/Intel PWR Sequence Control
VCC	Y	-	-	-	Y
VCCRL	Y	Y	Y	N*	Y
VCCRR	Y	Y	Y	N*	Y
VCCT	Y	Y	Y	N*	Y
VCCH	Y	Y	Y	N*	Y
VCCERAM	Y	Y	Y	N*	Y
1.8V	Y	Y	Y	N*	Y
3.3V	Y	N	N	N	Y
2.5V	Y	N	N	N	Y
12V	Y	N	-	-	Y

Note: *: Default not supported, request for an example design if you want this feature.

5.4. Power Distribution System

The figure shows the power distribution system of the Intel Stratix 10 GX transceiver signal integrity development kit.

Figure 12. Power Distribution System (Power Tree)

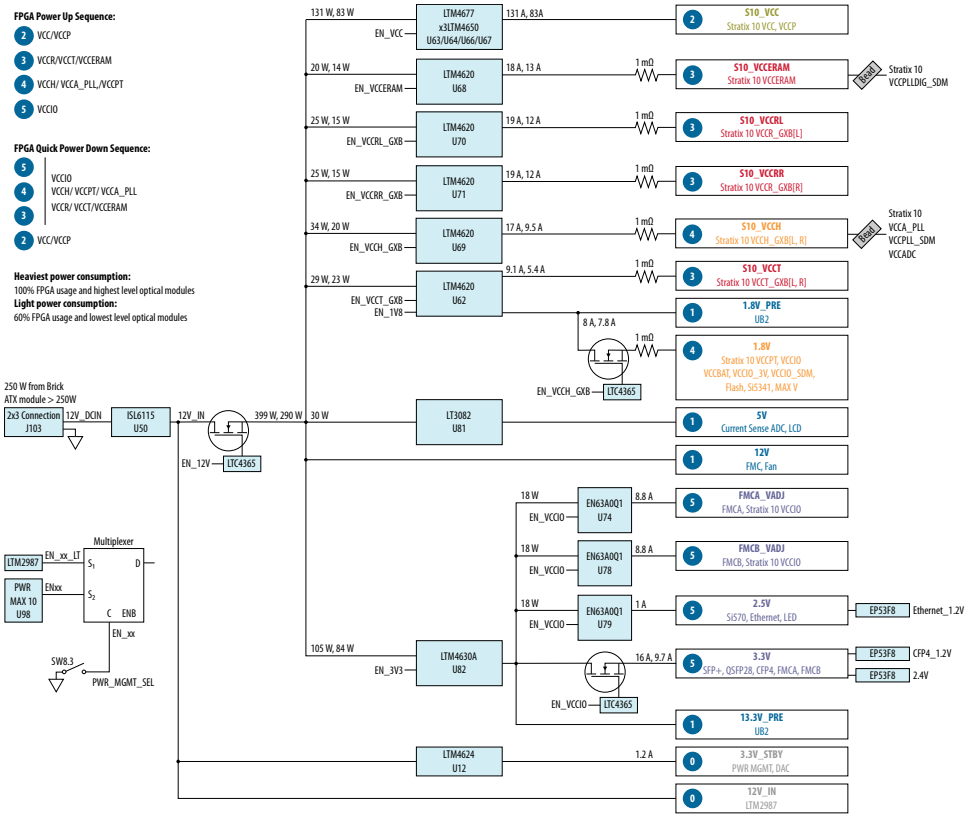
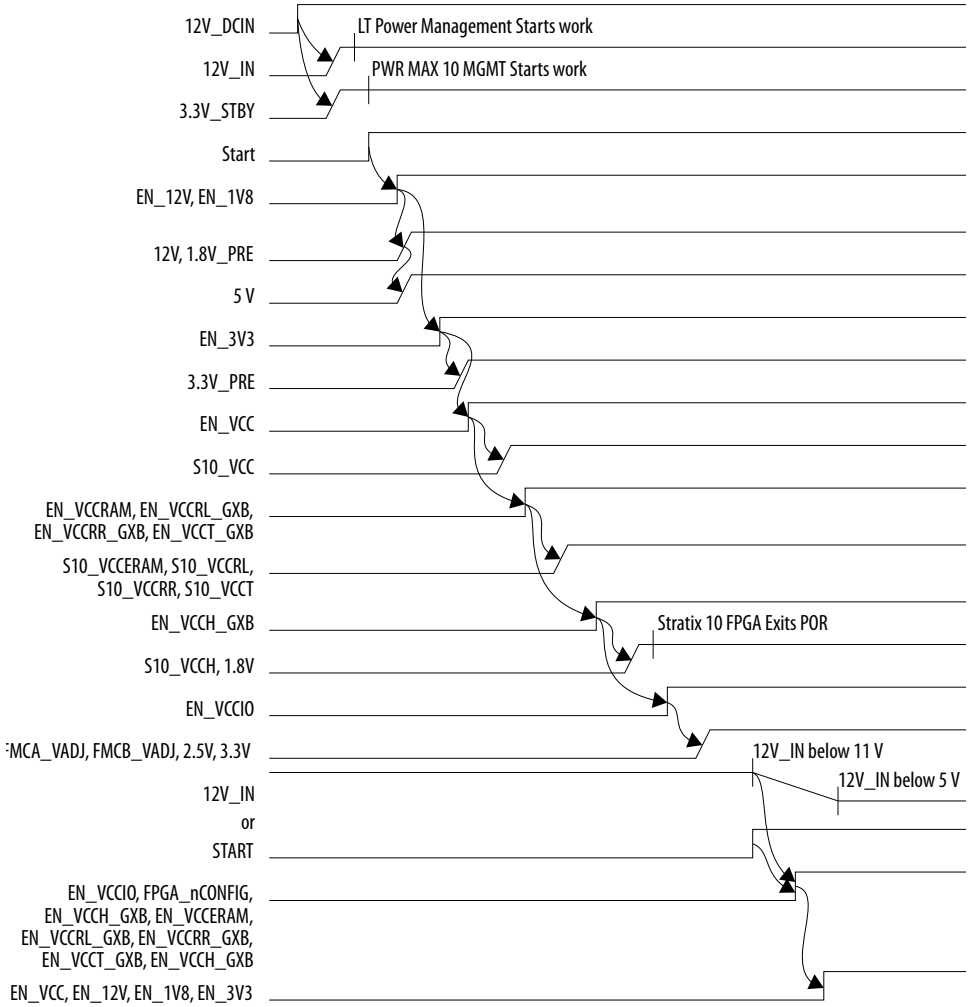


Figure 13. Power Sequence Waveforms



5.5. Thermal Limitations and Protection Guidelines

With 25C ambient temperature and 50C printed circuit board (PCB) temperature, you must ensure that your FPGA designs do not consume more than 200 W with the liquid cooling solution.

MAX1619 chip is connected to the Intel Stratix 10 GX FPGA internal temperature diode to continuously monitor FPGA die temperature. In the meantime, a dedicated FPGA TSD real-time monitor solution under `~\ip\onchip_sensors\` is added to each transceiver example design to monitor the temperatures of both FPGA core and each transceiver tile. Based on the data from both MAX1619 and FPGA, MAX V will run fan at its maximum speed whenever any temperature is over 60C or immediately power off the board whenever any temperature is over 100C. Remember to unplug the power supply when the board is powered off after the temperature crosses 100C. Plug the power supply back again to ensure that the board can be normally turned on/off again.

6. Board Test System

The Intel Stratix 10 GX Transceiver Signal Integrity Developement Kit includes a design example and an application called the Board Test System (BTS) to test the functionality of this board. The BTS provides an easy-to-use interface to alter functional settings and observe results. You can use the BTS to test board components, modify functional parameters, observe performance and measure power usage.

While using the BTS, you reconfigure the FPGA several times with test designs specific to the functionality that you are testing. The BTS is also useful as a reference for designing systems. The BTS communicates over the JTAG bus to a test design running in the Intel Stratix 10 GX FPGA device. The figure below shows the Graphical User Interface (GUI) for a board that is in factory confiuration.

Figure 14. BTS GUI

Figure 15. About BTS

6.1. Preparing the Board

Several designs are provided to test the major board features. Each design provides data for one or more tabs in the BTS. The Configure Menu identifies the appropriate design to download to the FPGA for each tab.

After successful FPGA configuration, the appropriate tab appears and allows you to exercise the related board features. Highlights appear in the board picture around the corresponding components.

The BTS shares the JTAG bus with other applications like Nios II debugger and the Signal Tap II Embedded Logic Analyzer. As the Intel Quartus Prime Programmer uses most of the bandwidth of the JTAG bus, other applications using the JTAG bus might time out. Be sure to close the other applications before attempting to reconfigure the FPGA using the Intel Quartus Prime Programmer.

6.2. Running the Board Test System

Before you begin

The BTS relies on the Intel Quartus Prime software's specific library. Before running the BTS, open the Intel Quartus Prime software to automatically set the enviromment variable `$QUARTUS_ROOTDIR`. The BTS uses this environment variable to locate the Intel Quartus Prime library. The version of Intel Quartus Prime software set in the `$QUARTUS_ROOTDIR` environment variable should be newer than version 17.0. For example, the Development Kit Installer version 17.0IR3 requires that the Intel Quartus Prime software 17.0IR1 or later version to be installed.

Also, to ensure that the FPGA is configured successfully, you should install the latest Intel Quartus Prime software that can support the silicon on the development kit. For this board, Intel recommends you install Intel Quartus Prime version `17.1ir2.b50`.

Please refer to the `README.txt` file under `examples\board_test_system` directory.

To run the BTS

1. Navigate to the `<package dir>\examples\board_test_system` directory and run the `BoardTestSystem.exe` application.
2. A GUI appears, displaying the application tab corresponding to the design running in the FPGA. If the design loaded in the FPGA is not supported by the BTS GUI, you will receive a message prompting you to configure your board with a valid BTS design. Refer to the Configure Menu for information on configuring your board.

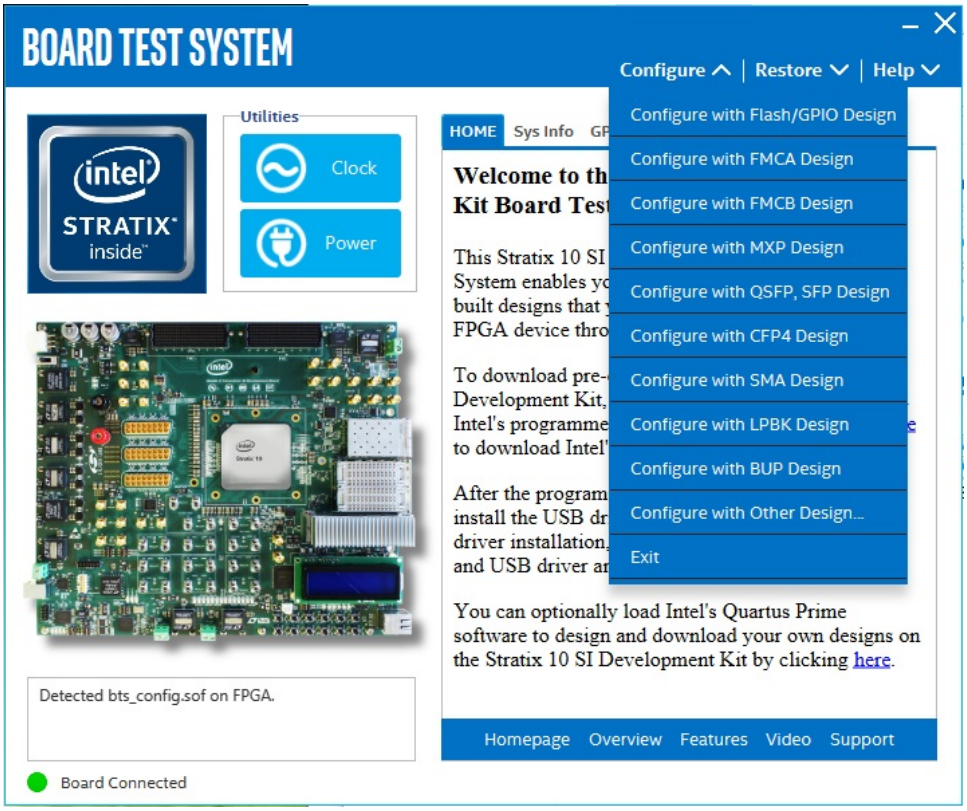
6.3. Using the Board Test System

This section describes each control in the Board Test System.

6.3.1. The Configure Menu

Use the Configure Menu to select the design you want to use. Each design example tests different functionality that corresponds to one or more application tabs.

Figure 16. The Configure Menu



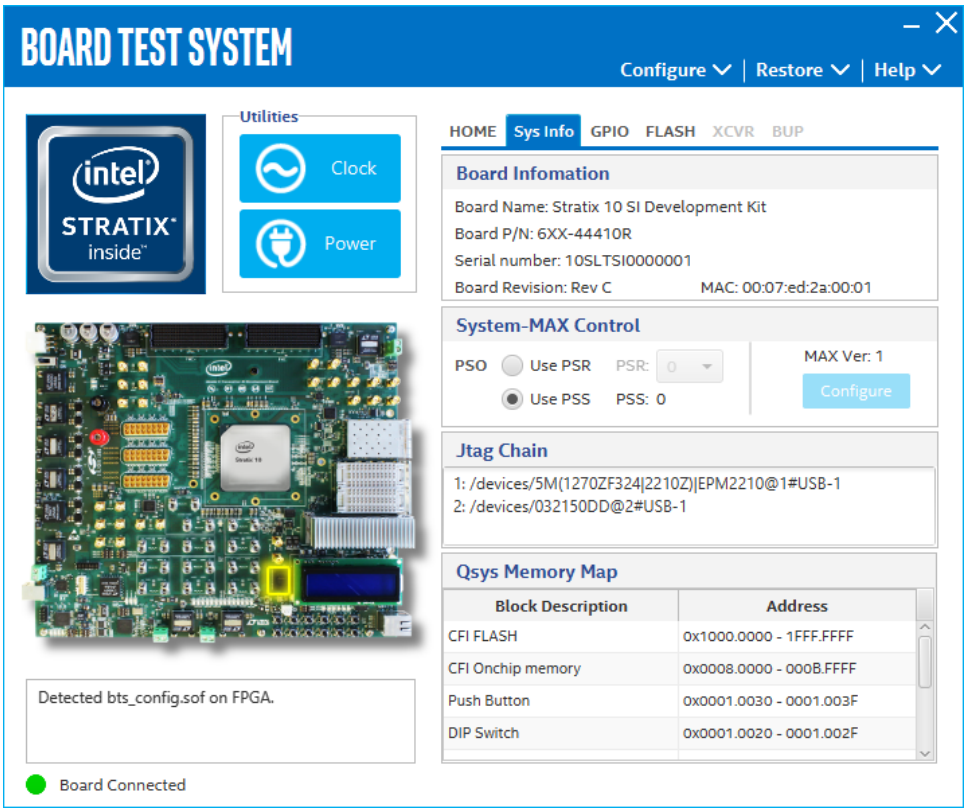
To configure the FPGA with a test system design, perform the following steps:

- On the Configure Menu, click the configure command that corresponds to the functionality you wish to test.
- In the dialog box that appears, click Configure to download the corresponding design's SRAM Object File (.sof) to the FPGA. The download process usually takes less than a minute.
- When configuration finishes, the design begins running in the FPGA. The corresponding GUI application tabs that interface with the design are now enabled. If you use the Intel Quartus Prime Programmer for configuration, rather than the BTS GUI, you may need to restart the GUI.

6.3.2. The System Info Tab

The System Info tab shows information about the board's current configuration. The tab displays system-MAX V control setting, the board's MAC address, and other details stored on the board.

Figure 17. The System Info Tab



The following sections describe the controls on the System Info tab.

Board Information

The Board Information control displays static information about your board.

- Board Name: Indicates the official name of the board given by the BTS.
- Board P/N: Indicates the part number of the board.
- Serial Number: Indicates the serial number of the board.
- Board Revision: Indicates the revision of the board.
- MAC: Indicates the MAC address of the board.

System-MAX Control

The MAX V register control allows you to view and change the current MAX V register values as described in the table below. Change to the register values with the GUI take effect immediately.

Table 26. MAX V Registers

MAX V Register Values	Description
`Configure`	Resets the system and reloads the FPGA with a design from flash memory based on the other MAX V register values.
`PSO`	Sets the MAX V PSO register
`PSR`	Sets the MAX V PSR register. Allows PSR to determine the page of flash memory to use for FPGA reconfiguration. The numerical values in the list corrresponds to the page of flash memory to load during the FPGA reconfiguration.
`PSS`	Displays the MAX V PSS register value. Allows the PSS to determine the page of flash memory to use for FPGA reconfiguration.
`MAX Ver`	Indicates the version of MAX V code currently running on the board.The MAX V code resides in the `<package dir>\examples\max5` directory. Newer revisions of this code may be available on the Stratix 10 Transceiver Signal Integrity Development Kit link on the Intel website.

JTAG Chain

The JTAG chain control shows all the devices currently in the JTAG chain.

Note: When switch SW 3-2 (`MAX  BYPASS`) is set to 1, the JTAG chain includes the MAX V device. When set to 0, the MAX V device is removed from the JTAG chain. System MAX and FPGA should all be in the JTAG chain when running the BTS GUI.

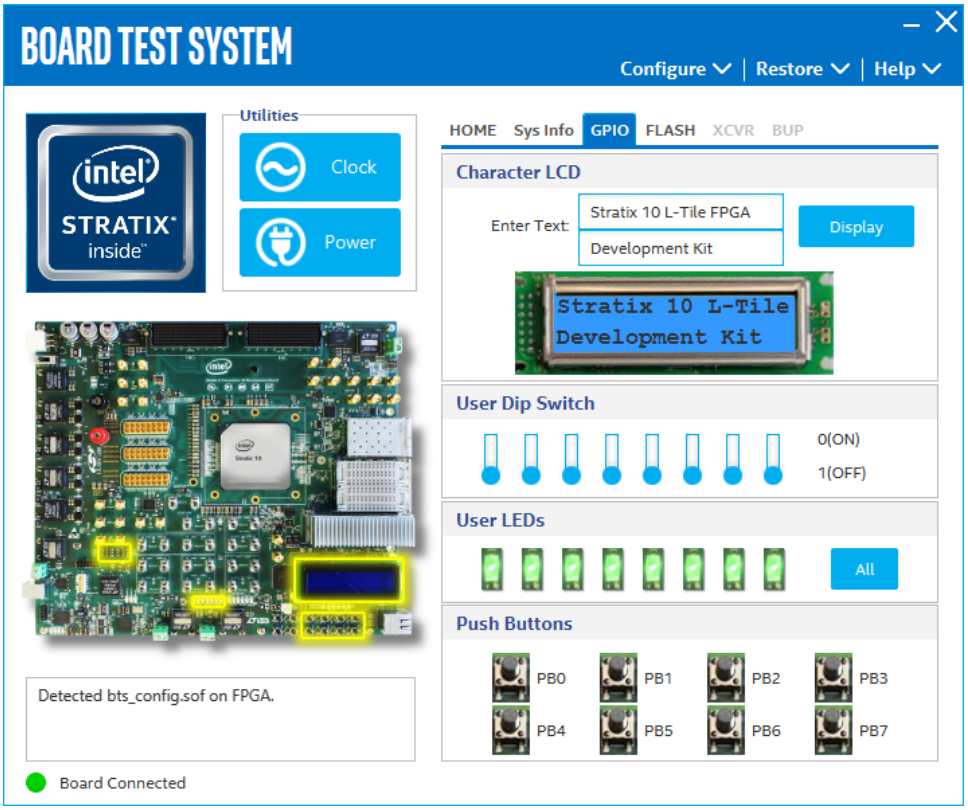
Platform Designer (Standard) Memory Map

The Platform Designer (Standard) memory map control shows the memory map of `bts_config.sof` design running on your board. This can be visible when `bts_config.sof` design is running on board.

6.3.3. The GPIO Tab

The GPIO Tab allows you to interact with all the genral purpose user I/O components on your board. You can write to the character LCD, read DIP switch settings, turn LEDs on or off and detect push button presses.

Figure 18. The GPIO Tab



The following sections describe the controls on the GPIO tab.

Character LCD

The Character LCD controls allow you to display text strings on the character LCD on your board. Type text in the text boxes and then click Display. If you exceed the 16 character display limit on either line, a warning message appears.

User DIP Swicthes

The read-only User DIP switches control displays the current positions of the switches in the user DIP switch bank (SW2 and SW6). Change the switches on the board to see the graphical display change.

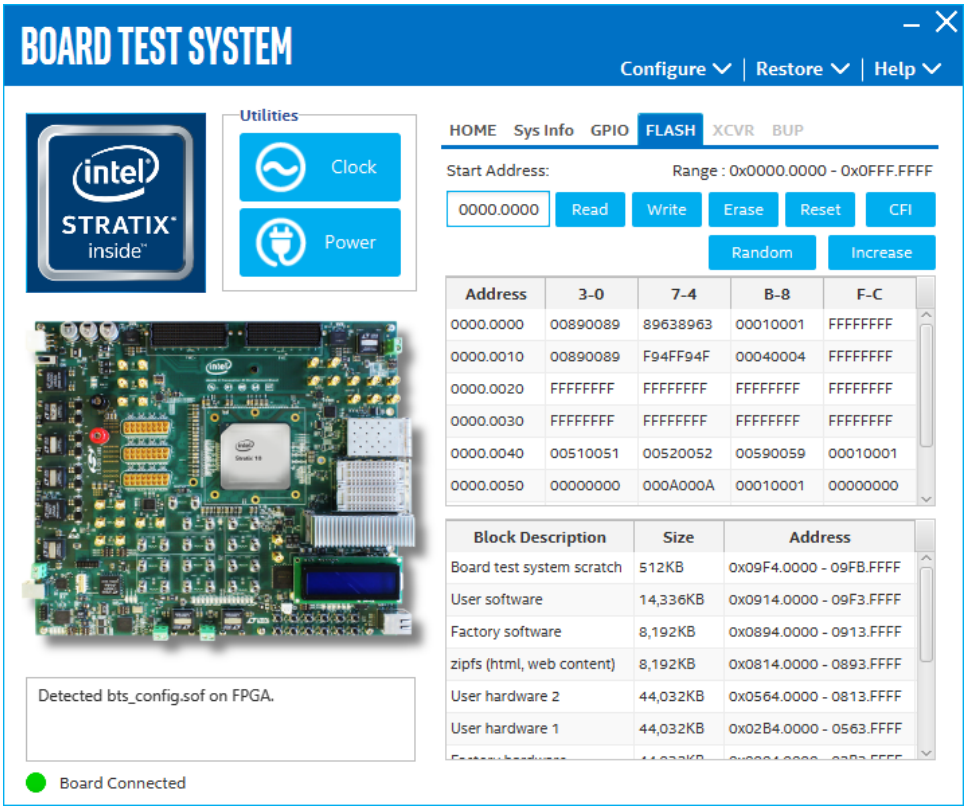
User LEDs

The User LEDs control displays the current state of the user LEDs. Toggle the LED buttons to turn the board LEDs on and off.

6.3.4. The Flash Tab

The Flash tab allows you to read and write flash memory on your board.

Figure 19. The Flash Tab



The following sections describe the controls on the Flash tab.

Read

The Read control reads the flash memory on your board. To see the flash memory contents, type a starting address in the text box and click **Read**. Values starting at the specified address appear in the table. The flash memory sits at the base address of `0x1000.0000`. To see flash memory contents, type the address above the base and values starting at this address are displayed. Valid entries are `0x0000.0000` through `0x0FFF.FF80`.

Note: If you enter an address outside of `0x0000.0000` to `0x0FFF.FFFF` flash memory address space, a warning message identifies the valid flash memory address range.

Write

The Write control writes the flash memory on your board. To update the flash memory contents, change values in the table and click **Write**. The application writes the new values to flash memory and then reads the values back to guarantee that the graphical display accurately reflects the memory contents.

Note: To prevent overwriting the dedicated portions of the flash memory, the application limits the writable flash memory address range to `0x0FF80000`- `0x0FFFFF80` (which corresponds to address range `0x0000.0000-0x00080000` in the uppermost portion of the user software memory block).

Increase

Start an increase data pattern to test flash memory.

Random

Starts a random data pattern to test flash memory.

CFI

The CFI Query control updates the memory table, displaying the CFI ROM table contents from the flash memory

Reset

The Reset control executes the flash memory's reset command and updates the memory table diaplayed on the Flash tab.

Erase

When erasing flash memory contents should read FFFFFFFF, which is limited to a scratch page in the upper 512K block.

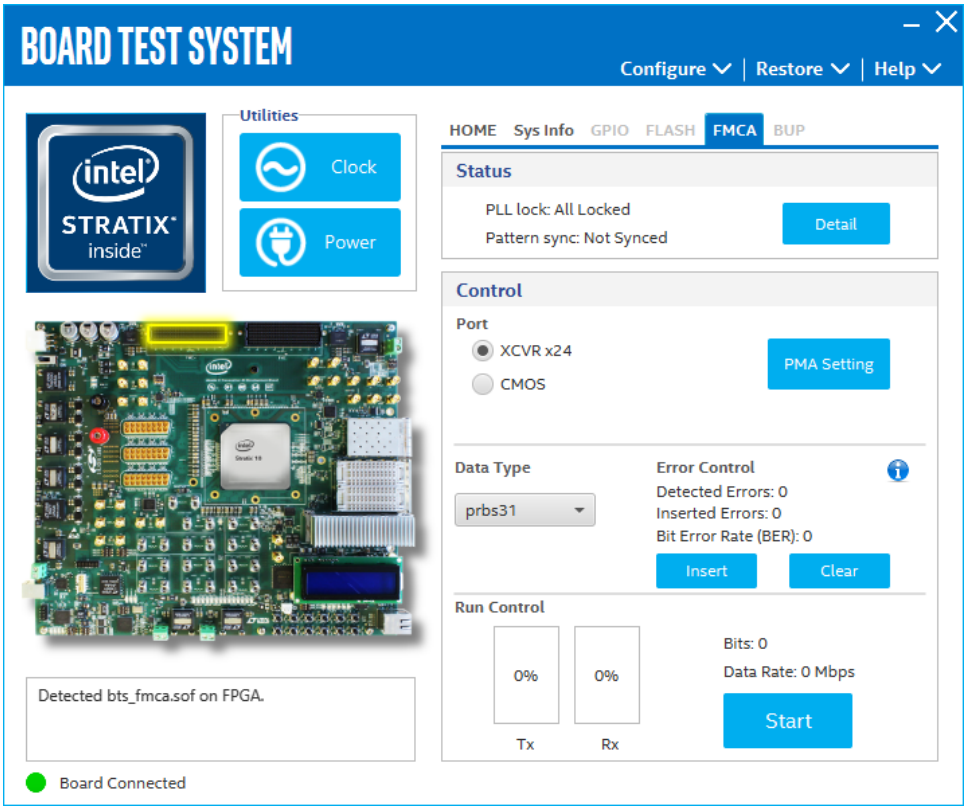
Flash Memory Map

Displays the flash memory map for the Intel Stratix 10 Transceiver Signal Integrity Development Kit.

6.3.5. The FMCA Tab

This tab allows you to perform loopback tests on the FMCA port.

Figure 20. The FMCA tab

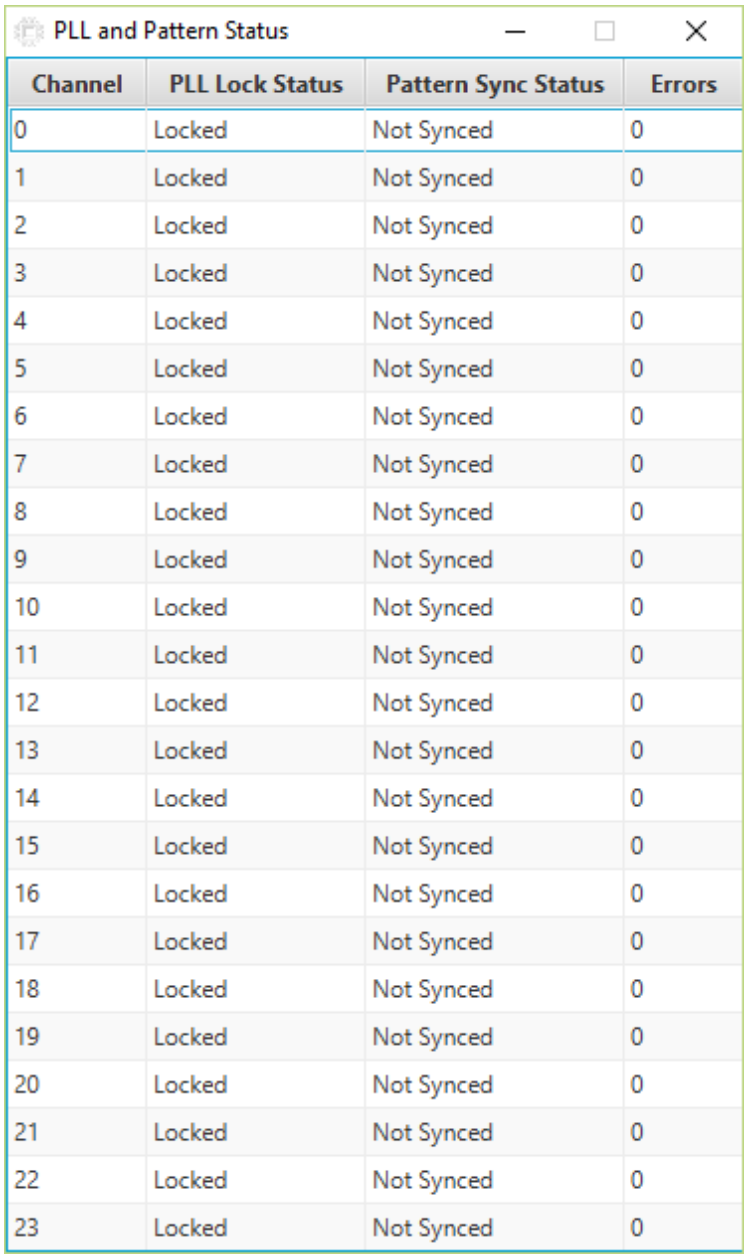


The following sections describe the controls on the FMCA tab.

Status

Displays the following status information during a loopback test:

- PLL Lock: Shows the PLL locked or unlocked state.
- Pattern Sync: Shows the pattern synced or not synced state. The pattern is considered synced when the start of the data sequence is detected.
- Details: Shows the PLL lock and pattern status:



Channel	PLL Lock Status	Pattern Sync Status	Errors
0	Locked	Not Synced	0
1	Locked	Not Synced	0
2	Locked	Not Synced	0
3	Locked	Not Synced	0
4	Locked	Not Synced	0
5	Locked	Not Synced	0
6	Locked	Not Synced	0
7	Locked	Not Synced	0
8	Locked	Not Synced	0
9	Locked	Not Synced	0
10	Locked	Not Synced	0
11	Locked	Not Synced	0
12	Locked	Not Synced	0
13	Locked	Not Synced	0
14	Locked	Not Synced	0
15	Locked	Not Synced	0
16	Locked	Not Synced	0
17	Locked	Not Synced	0
18	Locked	Not Synced	0
19	Locked	Not Synced	0
20	Locked	Not Synced	0
21	Locked	Not Synced	0
22	Locked	Not Synced	0
23	Locked	Not Synced	0

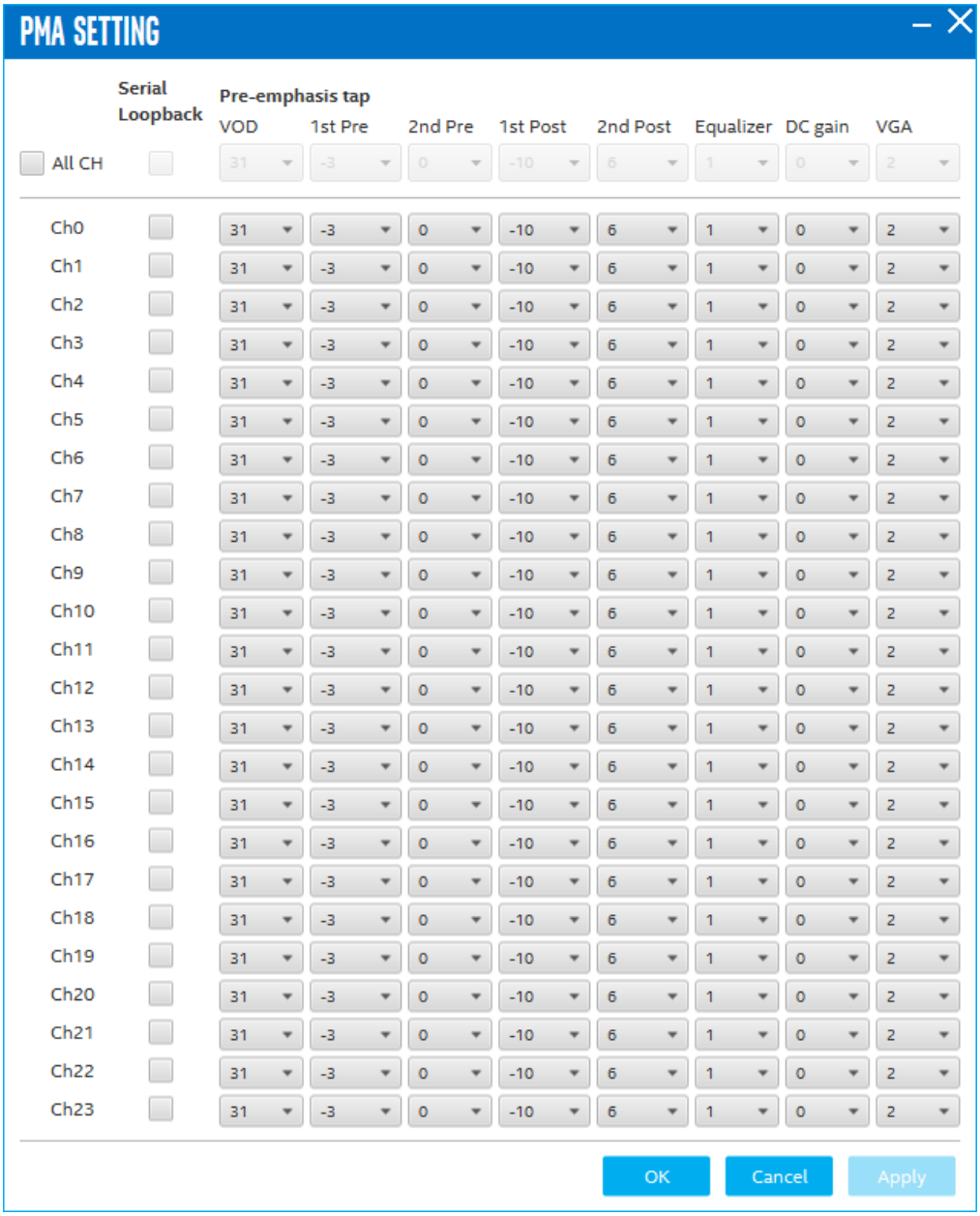
Port

Allows you to specify which interface to test. The following port tests are available: XCVR and CMOS

PMA Setting

Allows you to make changes to the PMA parameters that affect the active transceiver interface. The following settings are available for analysis:

- Serial Loopback: Routes signals between the transmitter and the receiver.
- VOD: Specifies the voltage output differential of the transmitter buffer.
- Pre-emphasis tap:
  - 1st pre: Specifies the amount of pre-emphasis on the pre-tap of the transmitter buffer.
  - 2nd pre (L-Tile): Specifies the amount of pre-emphasis on the second pre-tap of the transmitter buffer.
  - 1st post: Specifies the amount of pre-emphasis on the first post tap of the transmitter buffer.
  - 2nd post (L-Tile): Specifies the amount of pre-emphasis on the second post-tap of the transmitter buffer.
- Equalizer: Specifies the AC gain setting for the receiver equalizer in four stage mode.
- DC gain: Specifies the DC gain setting for the receiver equalizer in four stage mode.
- VGA: Specifies the VGA gain value.



Data Type

Specifies the type of data contained in the transactions. The following data types are available for analysis.

- PRBS 7: Selects pseudo-random 7-bit sequences.
- PRBS 15: Selects pseudo-random 15-bit sequences.
- PRBS 23: Selects pseudo-random 23-bit sequences.

- PRBS 31: Selects pseudo-random 31-bit sequences.
- HF: Selects highest frequency divide-by-2 data pattern 10101010.
- LF: Selects lowest frequency divide-by-33 data pattern.

Error Control

Displays data errors detected during analysis and allows you to insert errors:

- Detected errors: Displays the number of data errors detected in the hardware.
- Inserted errors: Displays the number of errors inserted into the transmit data stream.
- Insert: Inserts a one-word error into the transmit data stream each time you click the button. Insert is enabled only during transaction performance analysis.
- Clear: Resets the Detected errors and Inserted errors counters to zeroes.

Run Control

TX and RX performance bars: Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve.

Start: This control initiates the loopback tests.

Data Rate (H-Tile): Displays the XCVR type and data rate of each channel.

Figure 21. FMCA Data Rate

Data Rate

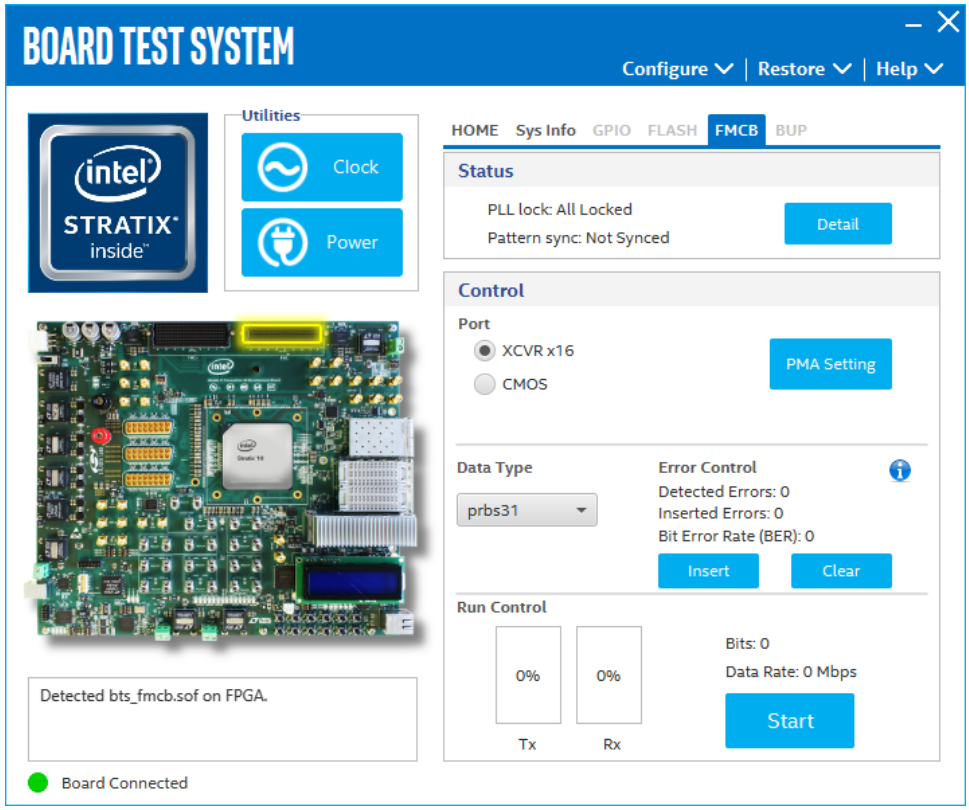
Channel	XCVR Type	Frequency
0	GXT	28035.52 Mbps
1	GXT	28035.84 Mbps
2	GX	12245.44 Mbps
3	GXT	28035.84 Mbps
4	GXT	28035.52 Mbps
5	GX	12245.44 Mbps
6	GXT	28035.84 Mbps
7	GXT	28035.84 Mbps
8	GX	12245.44 Mbps
9	GXT	28035.84 Mbps
10	GXT	28035.84 Mbps
11	GX	12245.44 Mbps
12	GXT	28036.80 Mbps
13	GXT	28036.80 Mbps
14	GX	12246.08 Mbps
15	GXT	28037.12 Mbps
16	GXT	28036.80 Mbps
17	GX	12245.76 Mbps
18	GXT	28037.12 Mbps
19	GXT	28036.80 Mbps
20	GX	12245.76 Mbps
21	GXT	28037.12 Mbps
22	GXT	28037.12 Mbps
23	GX	12246.08 Mbps

Tx (Mbps) and Rx (Mbps): Show the number of bytes of data analyzed per second.

6.3.6. The FMCB Tab

The FMCB tab allows you to perform loopback tests on the FMCB port.

Figure 22. The FMCB tab

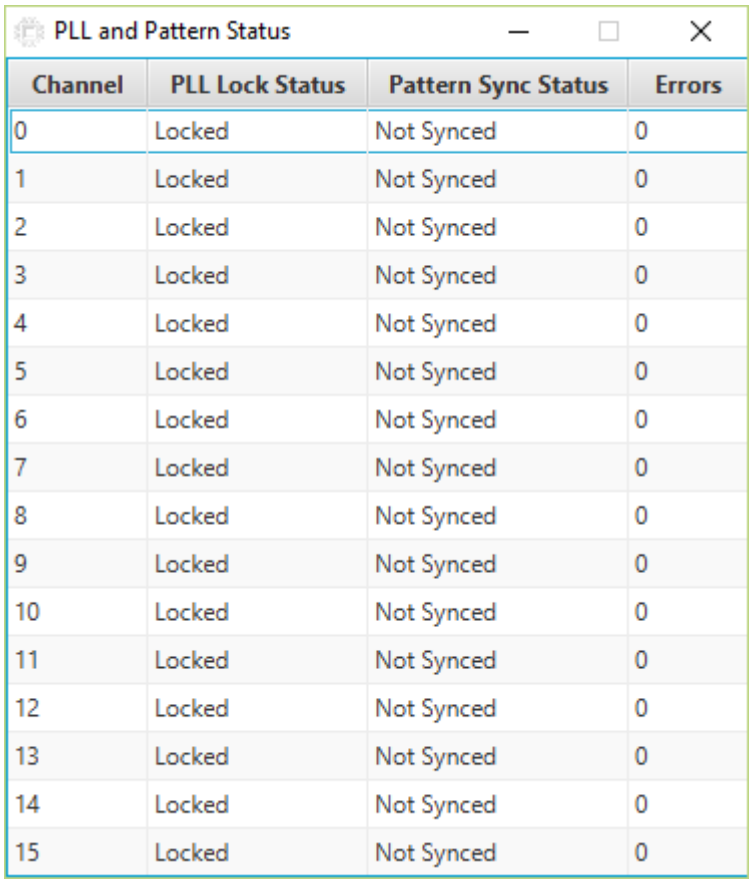


The following sections describe the controls on the FMCB tab.

Status

Displays the following status information during a loopback test:

- PLL Lock: Shows the PLL locked or unlocked state.
- Pattern Sync: Shows the pattern synced or not synced state. The pattern is considered synced when the start of the data sequence is detected.
- Details: Shows the PLL lock and pattern status:



Channel	PLL Lock Status	Pattern Sync Status	Errors
0	Locked	Not Synced	0
1	Locked	Not Synced	0
2	Locked	Not Synced	0
3	Locked	Not Synced	0
4	Locked	Not Synced	0
5	Locked	Not Synced	0
6	Locked	Not Synced	0
7	Locked	Not Synced	0
8	Locked	Not Synced	0
9	Locked	Not Synced	0
10	Locked	Not Synced	0
11	Locked	Not Synced	0
12	Locked	Not Synced	0
13	Locked	Not Synced	0
14	Locked	Not Synced	0
15	Locked	Not Synced	0

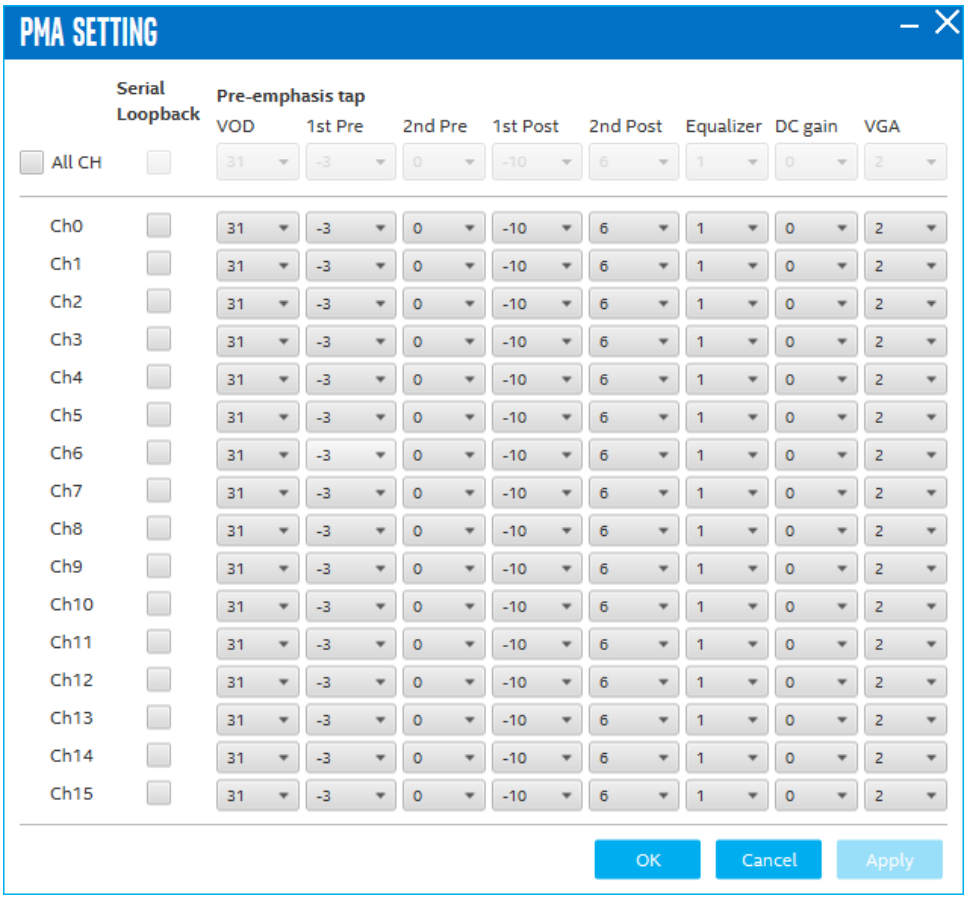
Port

Allows you to specify which interface to test. The following port tests are available: XCVR and CMOS

PMA Setting

Allows you to make changes to the PMA parameters that affect the active transceiver interface. The following settings are available for analysis:

- Serial Loopback: Routes signals between the transmitter and the receiver.
- VOD: Specifies the voltage output differential of the transmitter buffer.
- Pre-emphasis tap:
  - 1st pre: Specifies the amount of pre-emphasis on the pre-tap of the transmitter buffer.
  - 2nd pre (L-Tile): Specifies the amount of pre-emphasis on the second pre-tap of the transmitter buffer.
  - 1st post: Specifies the amount of pre-emphasis on the first post tap of the transmitter buffer.
  - 2nd post (L-Tile): Specifies the amount of pre-emphasis on the second post-tap of the transmitter buffer.
- Equalizer: Specifies the AC gain setting for the receiver equalizer in four stage mode.
- DC gain: Specifies the DC gain setting for the receiver equalizer in four stage mode.
- VGA: Specifies the VGA gain value.



Data Type

Specifies the type of data contained in the transactions. The following data types are available for analysis.

- PRBS 7: Selects pseudo-random 7-bit sequences.
- PRBS 15: Selects pseudo-random 15-bit sequences.
- PRBS 23: Selects pseudo-random 23-bit sequences.
- PRBS 31: Selects pseudo-random 31-bit sequences.
- HF: Selects highest frequency divide-by-2 data pattern 10101010.
- LF: Selects lowest frequency divide-by-33 data pattern.

Error Control

Displays data errors detected during analysis and allows you to insert errors:

- Detected errors: Displays the number of data errors detected in the hardware.
- Inserted errors: Displays the number of errors inserted into the transmit data stream.
- Insert: Inserts a one-word error into the transmit data stream each time you click the button. Insert is enabled only during transaction performance analysis.
- Clear: Resets the Detected errors and Inserted errors counters to zeroes.

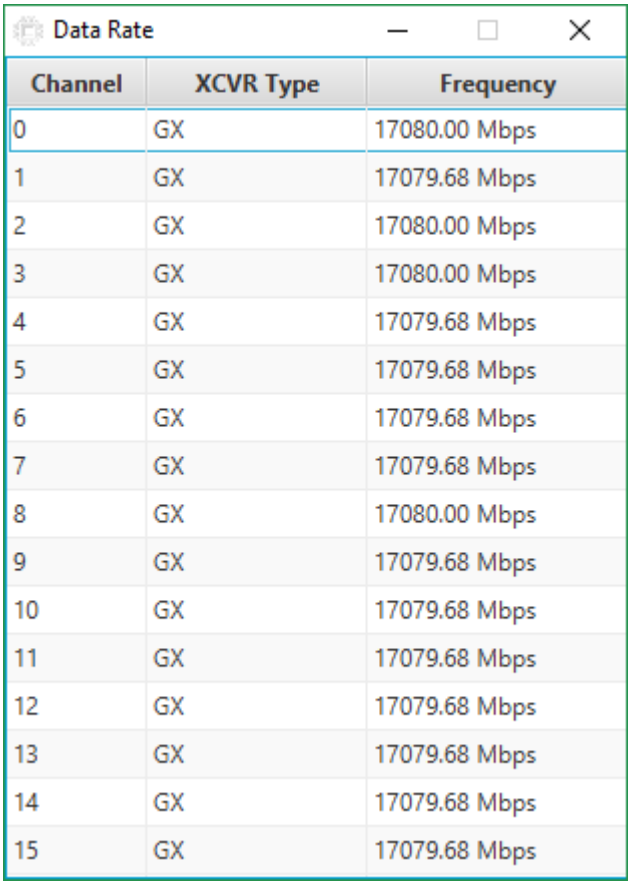
Run Control

TX and RX performance bars: Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve.

Start: This control initiates the loopback tests.

Data Rate (H-Tile): Displays the XCVR type and data rate of each channel.

Figure 23. FMCB Data Rate



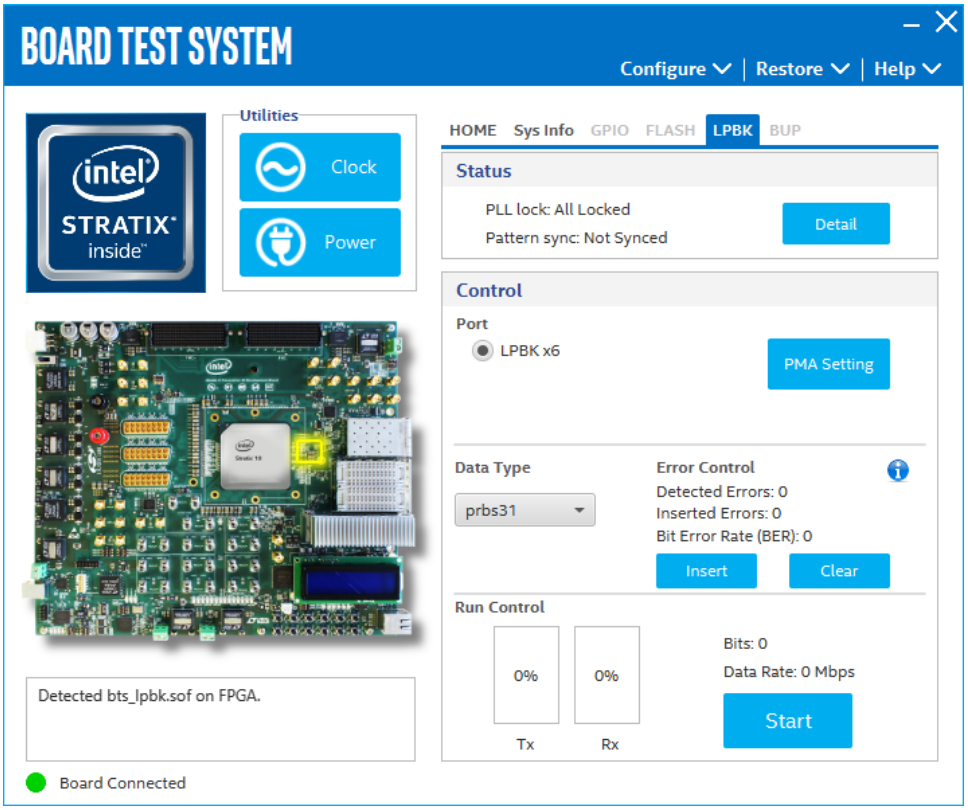
Channel	XCVR Type	Frequency
0	GX	17080.00 Mbps
1	GX	17079.68 Mbps
2	GX	17080.00 Mbps
3	GX	17080.00 Mbps
4	GX	17079.68 Mbps
5	GX	17079.68 Mbps
6	GX	17079.68 Mbps
7	GX	17079.68 Mbps
8	GX	17080.00 Mbps
9	GX	17079.68 Mbps
10	GX	17079.68 Mbps
11	GX	17079.68 Mbps
12	GX	17079.68 Mbps
13	GX	17079.68 Mbps
14	GX	17079.68 Mbps
15	GX	17079.68 Mbps

Tx (Mbps) and Rx (Mbps): Show the number of bytes of data analyzed per second.

6.3.7. The LPBK Tab

The LPBK tab allows you to perform on-board loopback tests.

Figure 24. The LPBK Tab

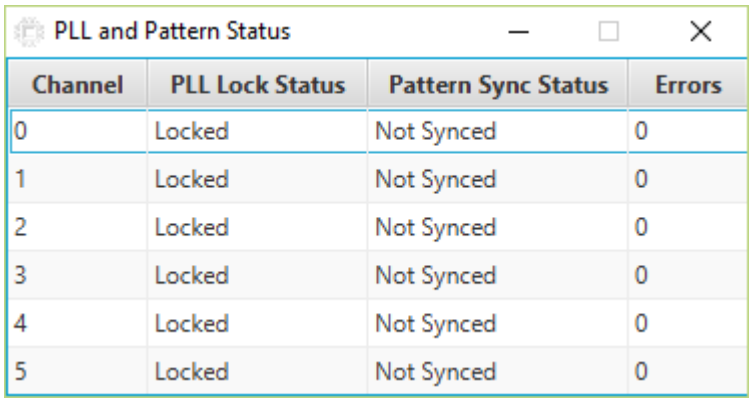


The following sections describe controls on the LPBK tab.

Status

Displays the following status information during a loopback test:

- PLL Lock: Shows the PLL locked or unlocked state.
- Pattern Sync: Shows the pattern synced or not synced state. The pattern is considered synced when the start of the data sequence is detected.
- Details: Shows the PLL lock and pattern status:



Channel	PLL Lock Status	Pattern Sync Status	Errors
0	Locked	Not Synced	0
1	Locked	Not Synced	0
2	Locked	Not Synced	0
3	Locked	Not Synced	0
4	Locked	Not Synced	0
5	Locked	Not Synced	0

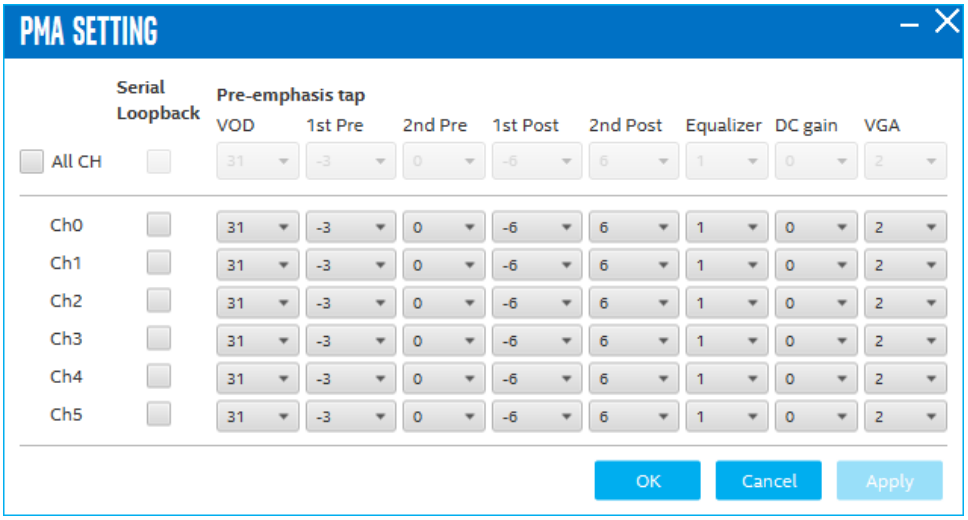
Port

Allows you to specify which interface to test. The following port tests are available: LPBKx6

PMA Setting

Allows you to make changes to the PMA parameters that affect the active transceiver interface. The following settings are available for analysis:

- Serial Loopback: Routes signals between the transmitter and the receiver.
- VOD: Specifies the voltage output differential of the transmitter buffer.
- Pre-emphasis tap:
  - 1st pre: Specifies the amount of pre-emphasis on the pre-tap of the transmitter buffer.
  - 2nd pre (L-Tile): Specifies the amount of pre-emphasis on the second pre-tap of the transmitter buffer.
  - 1st post: Specifies the amount of pre-emphasis on the first post tap of the transmitter buffer.
  - 2nd post (L-Tile): Specifies the amount of pre-emphasis on the second post-tap of the transmitter buffer.
- Equalizer: Specifies the AC gain setting for the receiver equalizer in four stage mode.
- DC gain: Specifies the DC gain setting for the receiver equalizer in four stage mode.
- VGA: Specifies the VGA gain value.



Data Type

Specifies the type of data contained in the transactions. The following data types are available for analysis.

- PRBS 7: Selects pseudo-random 7-bit sequences.
- PRBS 15: Selects pseudo-random 15-bit sequences.
- PRBS 23: Selects pseudo-random 23-bit sequences.
- PRBS 31: Selects pseudo-random 31-bit sequences.
- HF: Selects highest frequency divide-by-2 data pattern 10101010.
- LF: Selects lowest frequency divide-by-33 data pattern.

Error Control

Displays data errors detected during analysis and allows you to insert errors:

- Detected errors: Displays the number of data errors detected in the hardware.
- Inserted errors: Displays the number of errors inserted into the transmit data stream.
- Insert: Inserts a one-word error into the transmit data stream each time you click the button. Insert is enabled only during transaction performance analysis.
- Clear: Resets the Detected errors and Inserted errors counters to zeroes.

Run Control

TX and RX performance bars: Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve.

Start: This control initiates the loopback tests.

Data Rate (H-Tile): Displays the XCVR type and data rate of each channel.

Figure 25. LPBK Data Rate

Data Rate

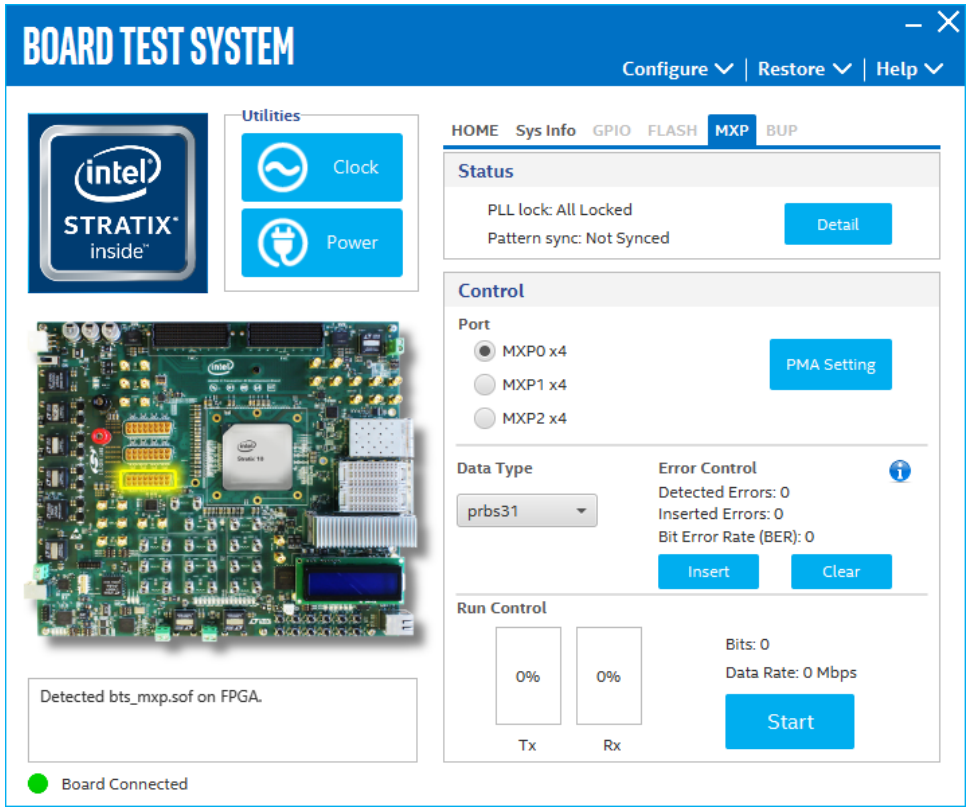
Channel	XCVR Type	Frequency
0	GXT	28124.16 Mbps
1	GXT	28124.03 Mbps
2	GX	17186.94 Mbps
3	GXT	28124.16 Mbps
4	GXT	28124.16 Mbps
5	GX	17186.94 Mbps

Tx (Mbps) and Rx (Mbps): Show the number of bytes of data analyzed per second.

6.3.8. The MXP Tab

The MXP tab allows you to perform loopback tests on the MXP port.

Figure 26. The MXP Tab

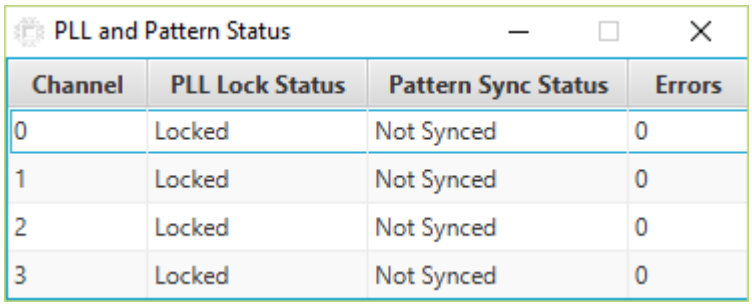


The following sections describe the controls on the MXP tab.

Status

Displays the following status information during a loopback test:

- PLL Lock: Shows the PLL locked or unlocked state.
- Pattern Sync: Shows the pattern synced or not synced state. The pattern is considered synced when the start of the data sequence is detected.
- Details: Shows the PLL lock and pattern status:



Channel	PLL Lock Status	Pattern Sync Status	Errors
0	Locked	Not Synced	0
1	Locked	Not Synced	0
2	Locked	Not Synced	0
3	Locked	Not Synced	0

Port

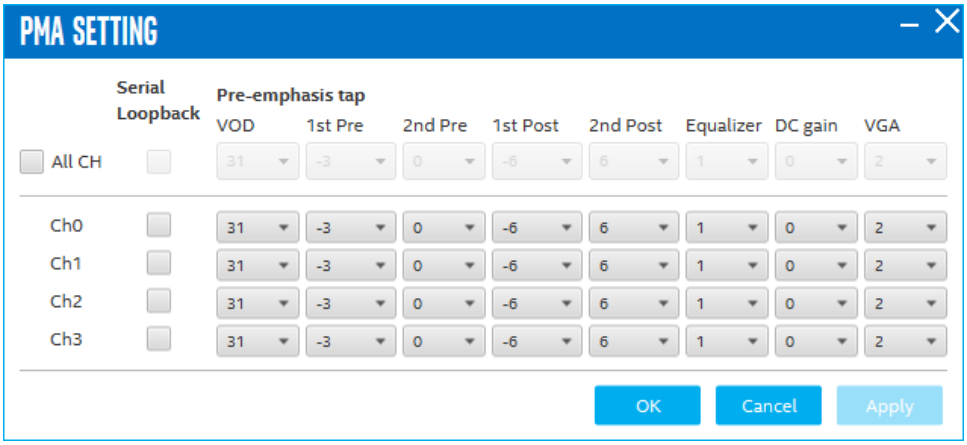
Allows you to specify which interface to test. The following port tests are available:

- MXP0 x4
- MXP1 x4
- MXP2 x4

PMA Setting

Allows you to make changes to the PMA parameters that affect the active transceiver interface. The following settings are available for analysis:

- Serial Loopback: Routes signals between the transmitter and the receiver.
- VOD: Specifies the voltage output differential of the transmitter buffer.
- Pre-emphasis tap:
  - 1st pre: Specifies the amount of pre-emphasis on the pre-tap of the transmitter buffer.
  - 2nd pre (L-Tile): Specifies the amount of pre-emphasis on the second pre-tap of the transmitter buffer.
  - 1st post: Specifies the amount of pre-emphasis on the first post tap of the transmitter buffer.
  - 2nd post (L-Tile): Specifies the amount of pre-emphasis on the second post-tap of the transmitter buffer.
- Equalizer: Specifies the AC gain setting for the receiver equalizer in four stage mode.
- DC gain: Specifies the DC gain setting for the receiver equalizer in four stage mode.
- VGA: Specifies the VGA gain value.



Data Type

Specifies the type of data contained in the transactions. The following data types are available for analysis.

- PRBS 7: Selects pseudo-random 7-bit sequences.
- PRBS 15: Selects pseudo-random 15-bit sequences.
- PRBS 23: Selects pseudo-random 23-bit sequences.
- PRBS 31: Selects pseudo-random 31-bit sequences.
- HF: Selects highest frequency divide-by-2 data pattern 10101010.
- LF: Selects lowest frequency divide-by-33 data pattern.

Error Control

Displays data errors detected during analysis and allows you to insert errors:

- Detected errors: Displays the number of data errors detected in the hardware.
- Inserted errors: Displays the number of errors inserted into the transmit data stream.
- Insert: Inserts a one-word error into the transmit data stream each time you click the button. Insert is enabled only during transaction performance analysis.
- Clear: Resets the Detected errors and Inserted errors counters to zeroes.

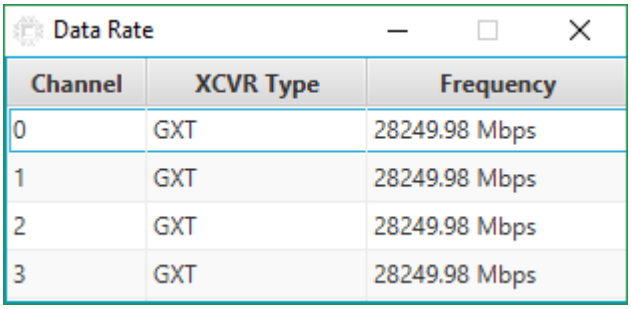
Run Control

TX and RX performance bars: Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve.

Start: This control initiates the loopback tests.

Data Rate (H-Tile): Displays the XCVR type and data rate of each channel.

Figure 27. MXP Data Rate

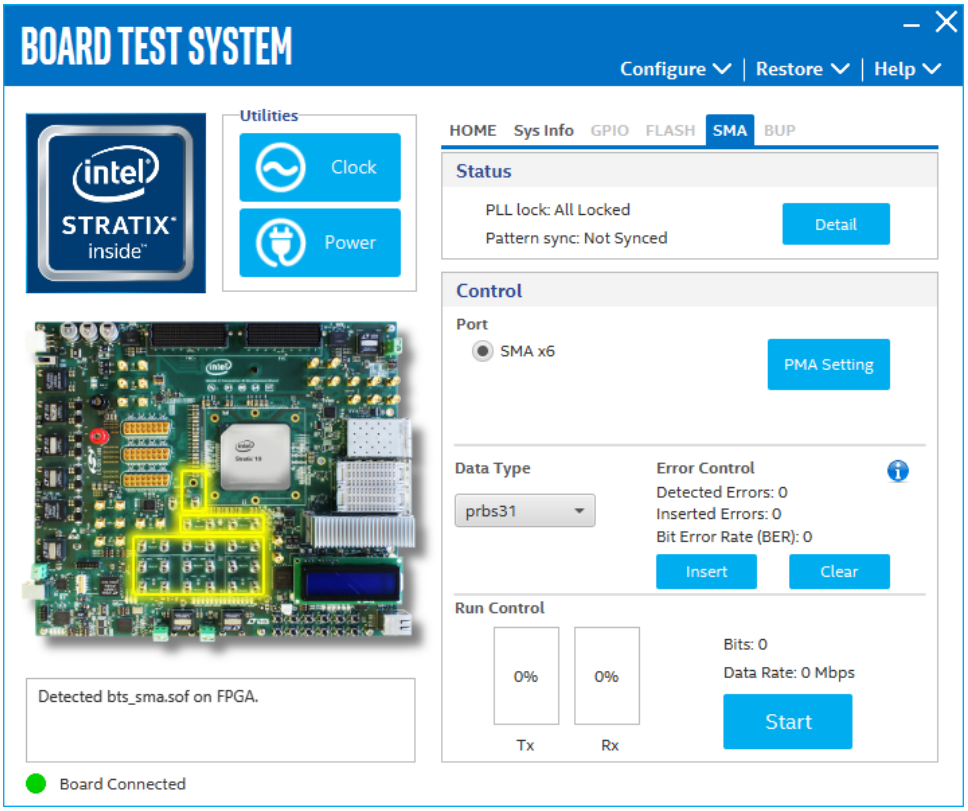


Tx (Mbps) and Rx (Mbps): Show the number of bytes of data analyzed per second.

6.3.9. The SMA Tab

The SMA tab allows you to perform loopback tests on the SMA port.

Figure 28. The SMA Tab

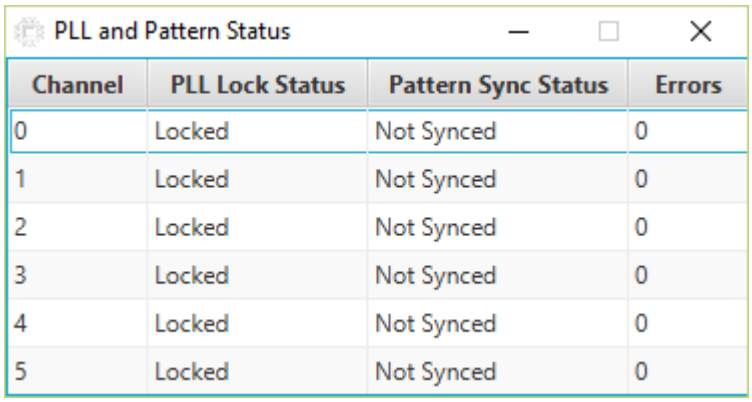


The following sections describe the controls on the SMA tab.

Status

Displays the following status information during a loopback test:

- PLL Lock: Shows the PLL locked or unlocked state.
- Pattern Sync: Shows the pattern synced or not synced state. The pattern is considered synced when the start of the data sequence is detected.
- Details: Shows the PLL lock and pattern status:



Channel	PLL Lock Status	Pattern Sync Status	Errors
0	Locked	Not Synced	0
1	Locked	Not Synced	0
2	Locked	Not Synced	0
3	Locked	Not Synced	0
4	Locked	Not Synced	0
5	Locked	Not Synced	0

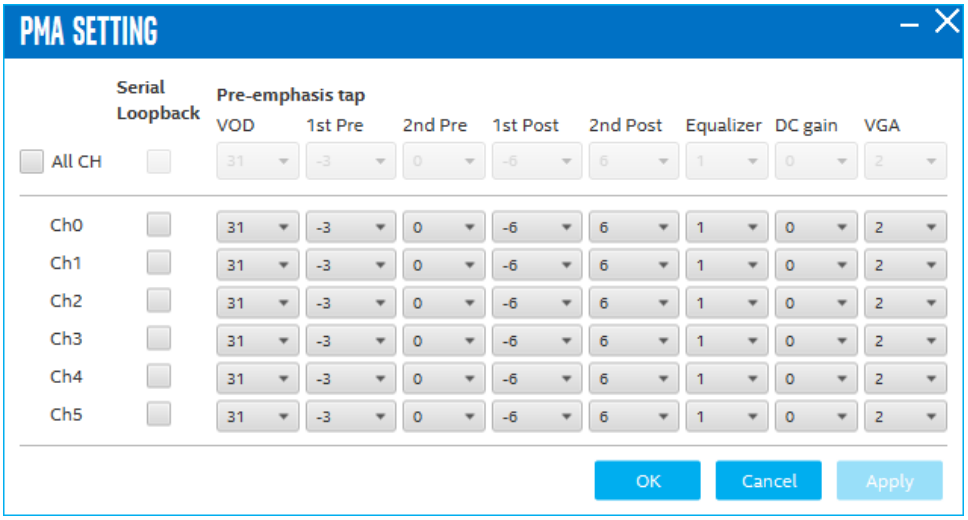
Port

Allows you to specify which interface to test. The following port tests are available: SMAx6

PMA Setting

Allows you to make changes to the PMA parameters that affect the active transceiver interface. The following settings are available for analysis:

- Serial Loopback: Routes signals between the transmitter and the receiver.
- VOD: Specifies the voltage output differential of the transmitter buffer.
- Pre-emphasis tap:
  - 1st pre: Specifies the amount of pre-emphasis on the pre-tap of the transmitter buffer.
  - 2nd pre (L-Tile): Specifies the amount of pre-emphasis on the second pre-tap of the transmitter buffer.
  - 1st post: Specifies the amount of pre-emphasis on the first post tap of the transmitter buffer.
  - 2nd post (L-Tile): Specifies the amount of pre-emphasis on the second post-tap of the transmitter buffer.
- Equalizer: Specifies the AC gain setting for the receiver equalizer in four stage mode.
- DC gain: Specifies the DC gain setting for the receiver equalizer in four stage mode.
- VGA: Specifies the VGA gain value.



Data Type

Specifies the type of data contained in the transactions. The following data types are available for analysis.

- PRBS 7: Selects pseudo-random 7-bit sequences.
- PRBS 15: Selects pseudo-random 15-bit sequences.
- PRBS 23: Selects pseudo-random 23-bit sequences.
- PRBS 31: Selects pseudo-random 31-bit sequences.
- HF: Selects highest frequency divide-by-2 data pattern 10101010.
- LF: Selects lowest frequency divide-by-33 data pattern.

Error Control

Displays data errors detected during analysis and allows you to insert errors:

- Detected errors: Displays the number of data errors detected in the hardware.
- Inserted errors: Displays the number of errors inserted into the transmit data stream.
- Insert: Inserts a one-word error into the transmit data stream each time you click the button. Insert is enabled only during transaction performance analysis.
- Clear: Resets the Detected errors and Inserted errors counters to zeroes.

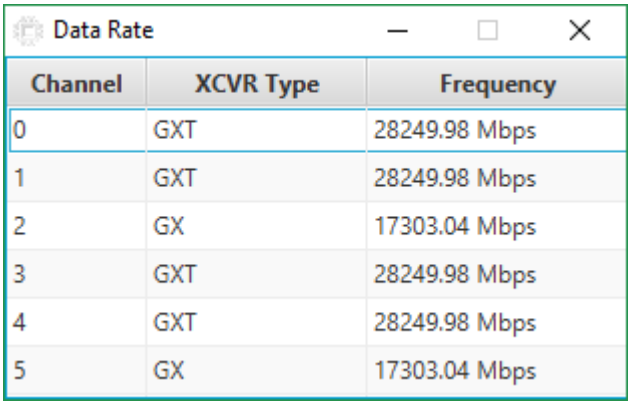
Run Control

TX and RX performance bars: Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve.

Start: This control initiates the loopback tests.

Data Rate (H-Tile): Displays the XCVR type and data rate of each channel.

Figure 29. SMA Data Rate

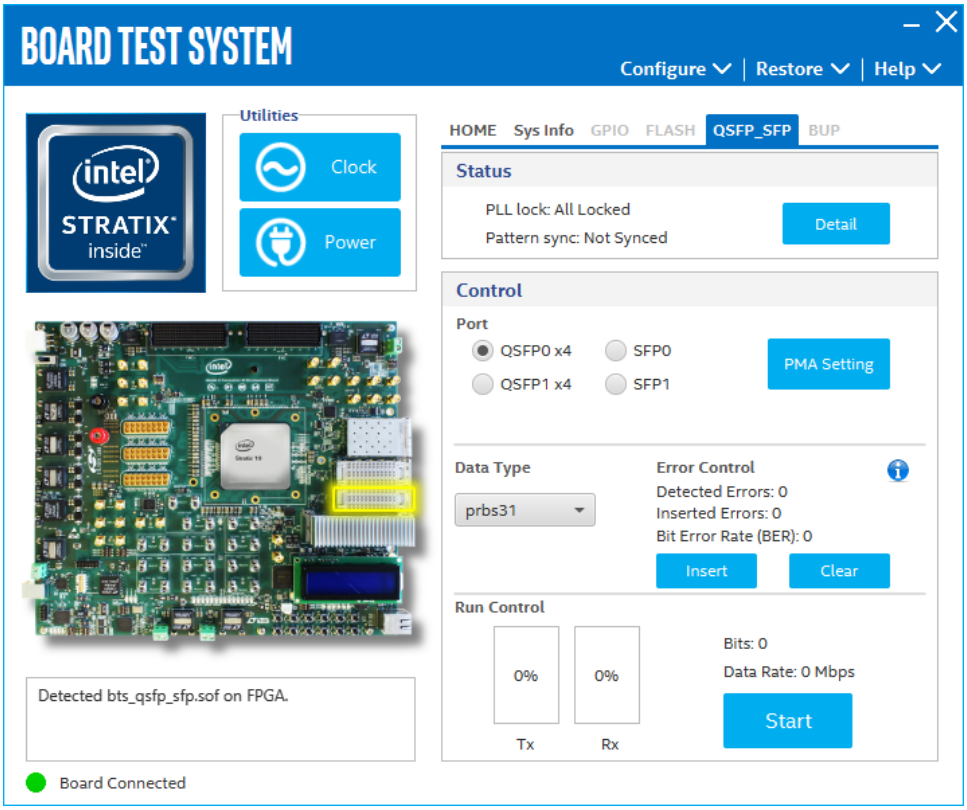


Tx (Mbps) and Rx (Mbps): Show the number of bytes of data analyzed per second.

6.3.10. The QSFP and SFP+ Tab

The QSFP and SFP+ Tab allows you to run transceivers QSFP and SFP+ loopback tests on your board. You can run the test using either electrical loopback modules or optical fiber modules.

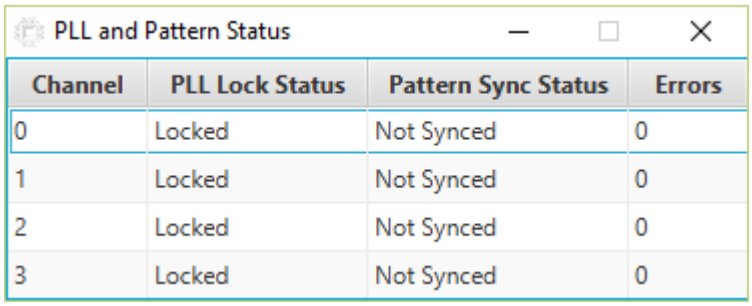
Figure 30. The QSFP and SFP+ Tab



Status

The Status control displays the following status information during the loopback test:

- PLL lock: Shows the PLL locked or unlocked state
- Pattern Sync: Shows the pattern synced or not state. The pattern is considered synced when the start of the data sequence is detected.
- Details: Shows the PLL lock and pattern sync status.



Channel	PLL Lock Status	Pattern Sync Status	Errors
0	Locked	Not Synced	0
1	Locked	Not Synced	0
2	Locked	Not Synced	0
3	Locked	Not Synced	0

Port

Use the following controls to select an interface to apply PMA settings, data type and error control:

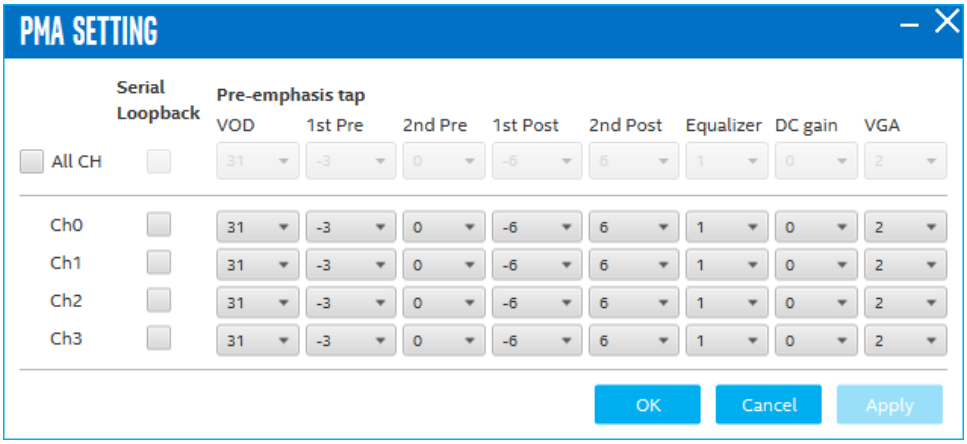
- QSFP0 x4
- QSFP1 x4
- SFP0
- SFP1

PMA Setting

Allows you to make changes to the PMA parameters that affect the active transceiver interface. The following settings are available for analysis:

1. Serial Loopback: Routes signals between the transmitter and the receiver.
2. VOD: Specifies the voltage output differential of the transmitter buffer.
3. Pre-emphasis tap:
   - 1st pre: Specifies the amount of pre-emphasis on the pre-tap of the transmitter buffer.
   - 2nd pre (L-Tile): Specifies the amount of pre-emphasis on the second pre-tap of the transmitter buffer.
   - 1st post: Specifies the amount of pre-emphasis on the first post tap of the trasnmitter buffer.
   - 2nd post (L-Tile): Specifies the amount of pre-emphasis on the second post tap of the transmitter buffer.
4. Equalizer: Specifies the AC gain setting for the receiver equalizer in four stage mode.
5. DC Gain: Specifies the DC Gain setting for the receiver equalizer in four stage mode.
6. VGA: Specifies the VGA gain value.

Figure 31. PMA Setting



Data Type

The Data Type control specifies the type of data pattern contained in the transactions. Select the following available data types for analysis:

- PRBS: pseudo-random 7-bit sequences (default)
- PRBS15: pseudo-random 15-bit sequences
- PRBS23: pseudo-random 23-bit sequences
- PRBS31: pseudo-random 31-bit sequences
- HF: highest frequency divide-by-2 data pattern `10101010`
- LF: lowest frequency divide by 33 data pattern

Settings Hf and LF are for transmit observation only and are not intended for use in the receiver data detection circuits.

Error Control

This control displays data errors detected during analysis and allows you to insert errors:

- Detected Errors: Displays the number of data errors detected in the received bit stream.
- Inserted Errrors: Displays the number of errors inserted into the transmit data stream.
- Insert Error: Insert a one-word error into the transmit data stream each time you click the button. Insert Error is only enabled during transaction performance analysis.
- Clear: Resets the Detected Errors counter and Inserted Errors counter to zeros.

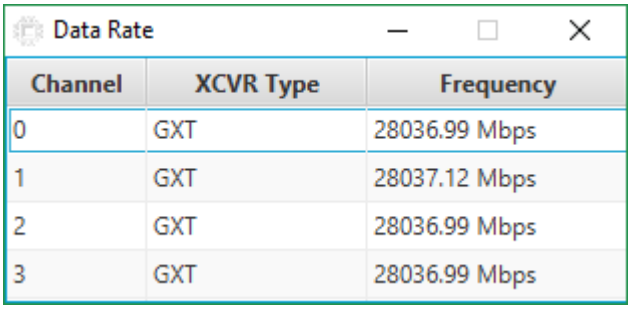
Run Control

TX and RX performance bars: Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve.

Start: This control initiates the loopback tests.

Data Rate (H-Tile): Displays the XCVR type and data rate of each channel.

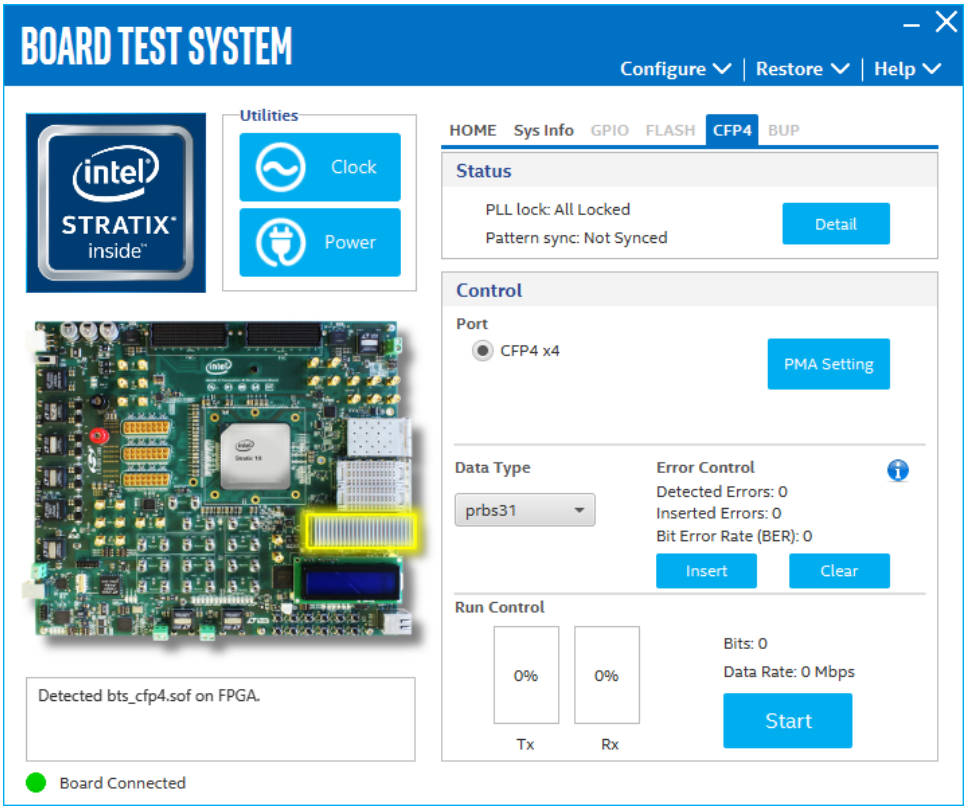
Figure 32. QSFP and SFP+ Data Rate



Tx (Mbps) and Rx (Mbps): Show the number of bytes of data analyzed per second.

6.3.11. The CFP4 Tab

Figure 33. The CFP4 Tab

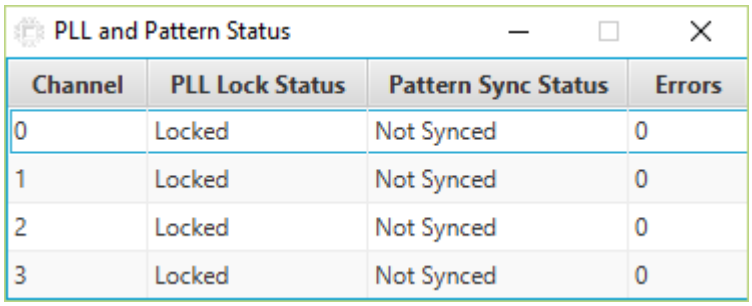


The following sections describe controls on the CFP4 tab.

Status

The Status control displays the following status information during the loopback test:

- PLL lock: Shows the PLL locked or unlocked state
- Pattern Sync: Shows the pattern synced or not state. The pattern is considered synced when the start of the data sequence is detected.
- Details: Shows the PLL lock and pattern sync status.



Channel	PLL Lock Status	Pattern Sync Status	Errors
0	Locked	Not Synced	0
1	Locked	Not Synced	0
2	Locked	Not Synced	0
3	Locked	Not Synced	0

Port

Use the following controls to select an interface to apply PMA settings, data type and error control:

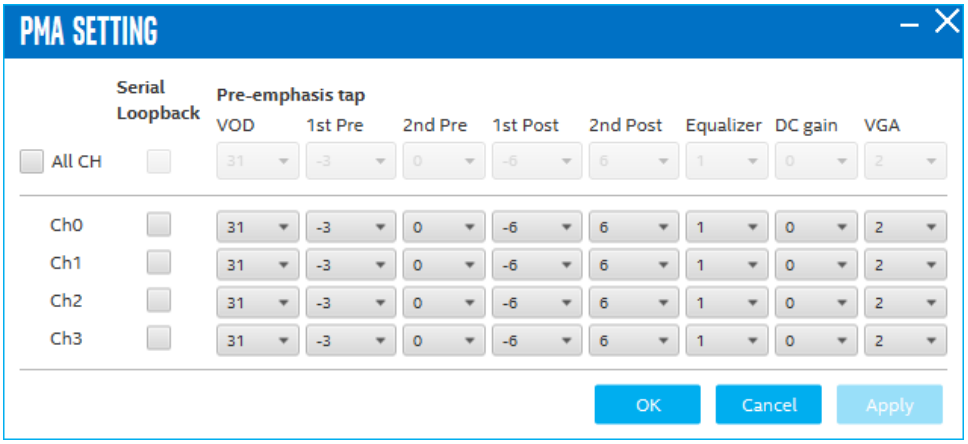
- CFP4 x4

PMA Setting

Allows you to make changes to the PMA parameters that affect the active transceiver interface. The following settings are available for analysis:

1. Serial Loopback: Routes signals between the transmitter and the receiver.
2. VOD: Specifies the voltage output differential of the transmitter buffer.
3. Pre-emphasis tap:
   - 1st pre: Specifies the amount of pre-emphasis on the pre-tap of the transmitter buffer.
   - 2nd pre: Specifies the amount of pre-emphasis on the second pre-tap of the transmitter buffer.
   - 1st post: Specifies the amount of pre-emphasis on the first post tap of the trasnmitter buffer.
   - 2nd post: Specifies the amount of pre-emphasis on the second post tap of the transmitter buffer.
4. Equalizer: Specifies the AC gain setting for the receiver equalizer in four stage mode.
5. DC Gain: Specifies the DC Gain setting for the receiver equalizer in four stage mode.
6. VGA: Specifies the VGA gain value.

Figure 34. PMA Setting



Data Type

The Data Type control specifies the type of data pattern contained in the transactions. Select the following available data types for analysis:

- PRBS: pseudo-random 7-bit sequences (default)
- PRBS15: pseudo-random 15-bit sequences
- PRBS23: pseudo-random 23-bit sequences
- PRBS31: pseudo-random 31-bit sequences
- HF: highest frequency divide-by-2 data pattern `10101010`
- LF: lowest frequency divide by 33 data pattern

Settings Hf and LF are for transmit observation only and are not intended for use in the receiver data detection circuits.

Error Control

This control displays data errors detected during analysis and allows you to insert errors:

- Detected Errors: Displays the number of data errors detected in the received bit stream.
- Inserted Errrors: Displays the number of errors inserted into the transmit data stream.
- Insert Error: Insert a one-word error into the transmit data stream each time you click the button. Insert Error is only enabled during transaction performance analysis.
- Clear: Resets the Detected Errors counter and Inserted Errors counter to zeros.

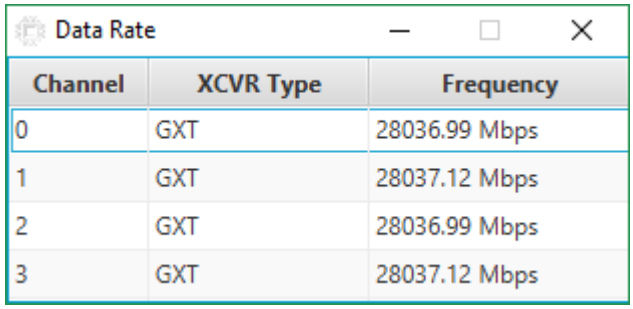
Run Control

TX and RX performance bars: Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve.

Start: This control initiates the loopback tests.

Data Rate (H-Tile): Displays the XCVR type and data rate of each channel.

Figure 35. CFP4 Data Rate



Tx (Mbps) and Rx (Mbps): Show the number of bytes of data analyzed per second.

6.3.12. Power Monitor

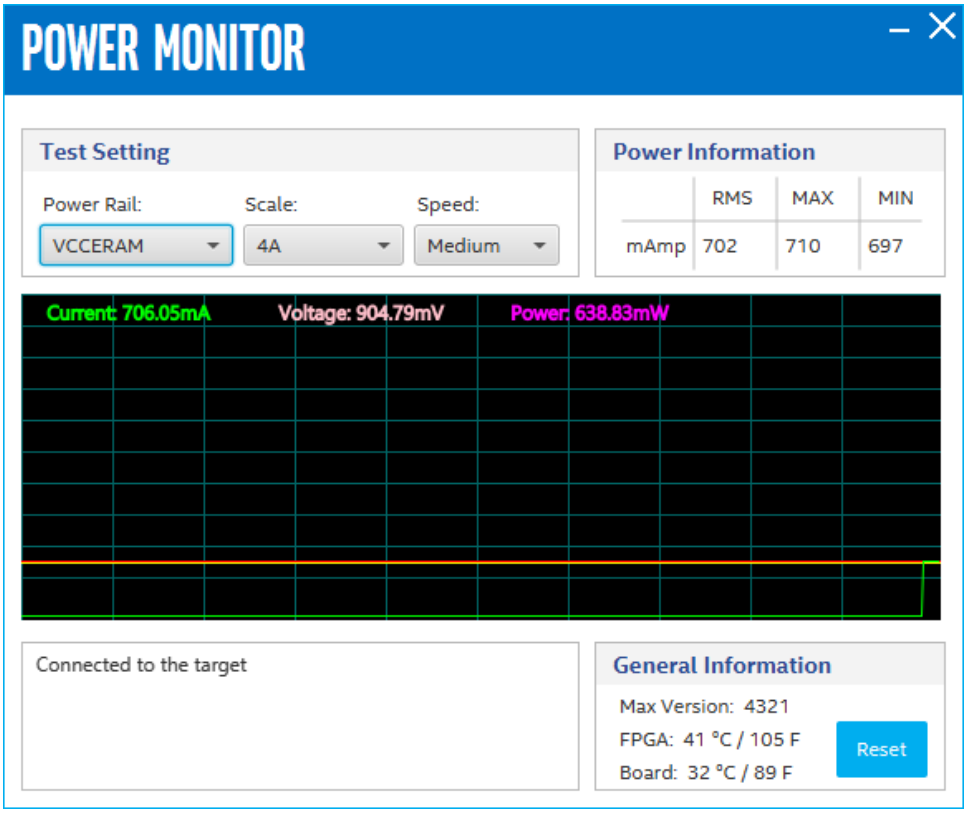
The Power Monitor measures and reports current power information and communicates with the MAX V device on the board through the JTAG bus. A power monitor cicruit attached to the device allows you to measure the power that the FPGA is consuming.

To start the application, click the Power Monitor icon in the BTS. You can also run the Power Monitor as a stand-alone application. The `PowerMonitor.exe` resides in the `<package dir>\examples\board_test_system` directory.

Note: You cannot run the stand-alone power application and BTS at the same time. Also, you cannot run power and clock interface at the same time.

Note: Intel recommends to remove R494 resistor from the board if VCC total current is less than 36 A. Reserve R494 if VCC total current is larger than 36 A.

Figure 36. The Power Monitor



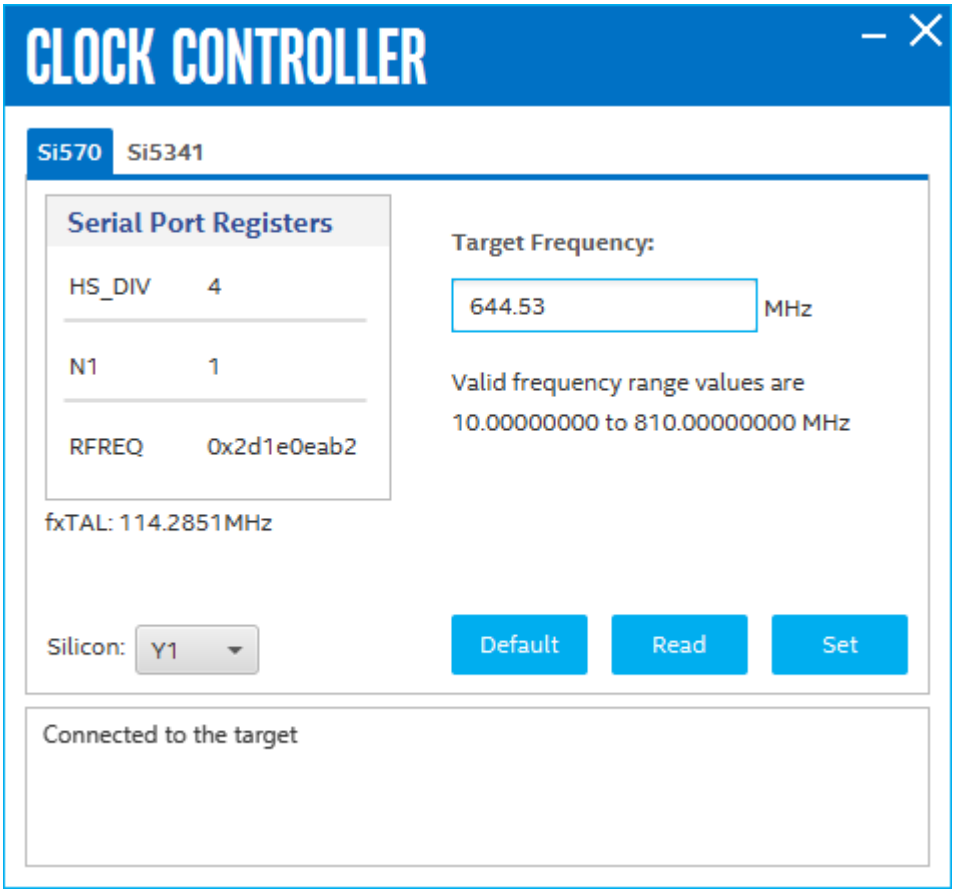
6.3.13. Clock Controller

The Clock Controller application sets the Si570 programmable oscillators to any frequency between 10 MHz and 945 MHz and select frequencies to 1400 MHz. The oscillator drives a 2-to-6 buffer that drives a copy of the clock to all transceiver blocks of the FPGA.

The Clock Control applications runs as a stand-alone application. `ClockControl.exe` resides in the `<package dir>\examples\board_test_system` directory.

The Clock Control communicates with the MAX V device on the board throught the JTAG bus. The Si570 programmable oscillator is connected to the MAX V device through a 2-wire serial bus.

Figure 37. Clock Controller



The following sections describe the Clock Control controls

Serial Port Registers

The Serial Port Registers control shows the current values from the Si570 registers.

Note: For more information about the Si570 registers, refer to the Si570/Si571 data sheet available on the Silicon Labs website (www.silabs.com).

fXTAL

The fXTAL control shows the calculated internal fixed-frequency crystal, based on the serial port register values.

Note: For more information about the fXTAL value and how it is calculated, refer to the Si570/Si571 data sheet available on the Silicon Labs website (www.silabs.com)

Target Frequency

The Target frequency control allows you to specify the frequency of the clock. Legal values are between 10 MHz and 945 MHz and select frequencies to 1400 MHz. For example, 421.31259873 is possible within 100 parts per million (ppm). The Target Frequency control works in conjunction with the Set New Frequency Control.

Reset Si570

The clear control sets the Si570 programmable oscillator to the default frequency as follows:

- Y3 = 644.53125 MHz
- Y4 = 706.25 MHz
- Y5 = 625 MHz
- Y6 = 875 MHz

Set New Frequency

The Set New Frequency control sets the Si570 programmable oscillator frequency to the value in the Target frequency control. Frequency changes might take several milliseconds to take effect. You might see glitches on the clock during this time.

Note: Intel recommends resetting the FPGA logic after changing frequencies

7. Board Update Portal

The Intel Stratix 10 GX Transceiver Signal Integrity Development Kit ships with the Board Update Portal design example stored in the factory portion of the flash memory on the board. The design consists of a Nios II embedded processor, an Ethernet MAC and an HTML web server.

When you power up the board with the **SW6.1** FACTORY_LOAD to **OFF(1)** position, Intel Stratix 10 GX FPGA configures with the Board Update Portal design example. The design can obtain an IP address from any DHCP server and serve a webpage from the flash on your board to any host computer on the same network. The webpage allows you to upload a new FPGA design to the user portion of flash memory and provides links to useful information on the Intel website, including kit-specific links and design resources.

After successfully updating the user flash memory, you can load the user design from flash memory into the FPGA by setting **SW6.1** to **ON(0)** position and power cycle the board. The source code for the Board Update Portal resides in the `<package dir>\examples\board_update_portal` directory.

7.1. Connecting to the Board Update Portal

Before you begin

This section provides instructions to connect to the Board Update Portal webpage. Before you proceed, ensure that you have the following:

- A PC with a connection to a working Ethernet port on a DHCP enabled network.
- A separate working Ethernet port connected to the same network for the board.
- The Ethernet, power cables and development board that are included in the kit.

Connecting to the Board Update Portal

To connect to the Board Update Portal webpage, please perform the following steps:

1. Install the latest Intel software tools, including Intel Quartus Prime software, Nios II processor and IP blocks.
2. Set **SW6.1** to **OFF(1)** position with the board powered down.
3. Attach the Ethernet cable from the board to your LAN.
4. Power up the board. The board connects to the LAN's gateway router and obtains an IP address. The LCD on the board displays the IP address.
5. Launch a web browser on a PC that is connected to the same network and enter the IP address from the LCD into the web browser's address bar. The Board Update Portal webpage appears in the web browser

You can click the Stratix 10 GX Transceiver Signal Integrity Development Kit on the Board Update Portal to access the development kit's home page for documentation updates and additional new designs.

You can also navigate directly to the Stratix 10 GX Transceiver Signal Integrity Development Kit link on the Intel website to determine if you have the latest kit software.

7.2. Using the Board Update Portal

The Board Update Portal allows you to write new designs to the user portion of flash memory.

Hardware designs must be in the (`.bin`) format which can be found in the package or created on your own.

Software designs must be in the Nios II Flash Programmer File (**.flash**) format.

To create your own hardware designs, perform these steps:

1. From the **Start** menu, open **Nios II Command Shell**.
2. In the **Nios II Command Shell**, navigate to the `build_hw.sh` file and type

```
sh build_hw.sh yourfile_hw.sof 1
```

To upload a design over the network into the user portion of flash memory on your board, perform the following steps:

1. Perform the steps in "Connecting to the Board Update Portal on page 87" to access the Board Update Portal webpage.
2. In the `Hardware File Name` field, specify the **.bin** file that you either downloaded from the Intel website or created on your own.
3. If there is a software component to the design, specify it in the same manner using the `Software File Name` field; otherwise leave the `Software Field Name` blank.
4. Click **Upload**. The progress bar indicates the completion percentage. The file takes a few seconds to upload.
5. Set **SW6.1** to **ON(0)** position to configure the FPGA with the new design after flash memory upload process is complete.

A. Additional Information

A.1. Safety and Regulatory Information

ENGINEERING DEVELOPMENT PRODUCT - NOT FOR RESALE OR LEASE

This development kit is intended for laboratory development and engineering use only.

This development kit is designed to allow:

- Product developers and system engineers to evaluate electronic components, circuits, or software associated with the development kit to determine whether to incorporate such items in a finished product.
- Software developers to write software applications for use with the end product.

This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required Federal Communications Commission (FCC) equipment authorizations are first obtained.

Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference.

Unless the assembled kit is designed to operate under Part 15, Part 18 or Part 95 of the United States Code of Federal Regulations (CFR) Title 47, the operator of the kit must operate under the authority of an FCC licenseholder or must secure an experimental authorization under Part 5 of the United States CFR Title 47.

Safety Assessment and CE mark requirements have been completed, however, other certifications that may be required for installation and operation in your region have not been obtained.

A.1.1. Safety Warnings

Power Supply Hazardous Voltage

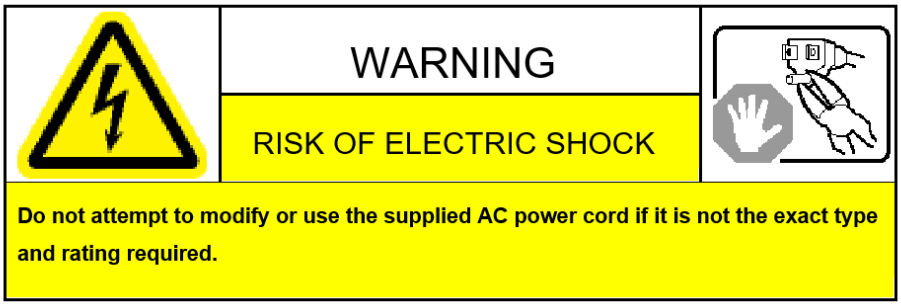
AC mains voltages are present within the power supply assembly. No user serviceable parts are present inside the power supply.

Power Connect and Disconnect

The AC power supply cord is the primary disconnect device from mains (AC power) and used to remove all DC power from the board/system. The socket outlet must be installed near the equipment and must be readily accessible.

System Grounding (Earthing)

To avoid shock, you must ensure that the power cord is connected to a properly wired and grounded receptacle. Ensure that any equipment to which this product will be attached is also connected to properly wired and grounded receptacles.



Power Cord Requirements

The connector that plugs into the wall outlet must be a grounding-type male plug designed for use in your region. It must have marks showing certification by an agency in your region. The connector that plugs into the AC receptacle on the power supply must be an IEC 320, sheet C13, female connector. If the power cord supplied with the system does not meet requirements for use in your region, discard the cord and do not use it with adapters.

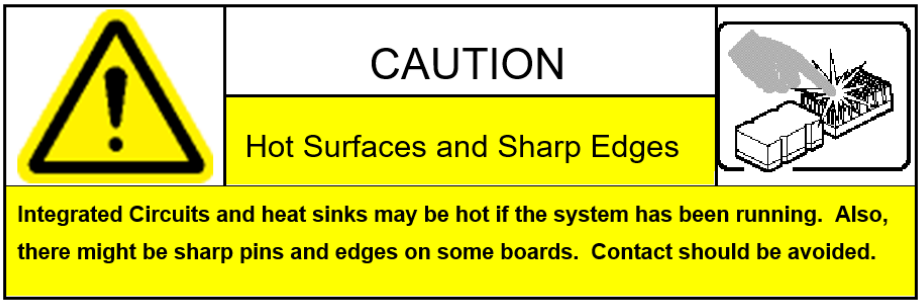
Lightning/Electrical Storm

Do not connect/disconnect any cables or perform installation/maintenance of this product during an electrical storm.

Risk of Fire

To reduce the risk of fire, keep all flammable materials a safe distance away from the boards and power supply. You must configure the development kit on a flame retardant surface.

A.1.2. Safety Cautions



Caution: Hot Surfaces and Sharp Edges. Integrated Circuits and heat sinks may be hot if the system has been running. Also, there might be sharp edges on some boards. Contact should be avoided.

Thermal and Mechanical Injury

Certain components such as heat sinks, power regulators, and processors may be hot. Heatsink fans are not guarded. Power supply fan may be accessible through guard. Care should be taken to avoid contact with these components.

Cooling Requirements

Maintain a minimum clearance area of 5 centimeters (2 inches) around the isde, front and back of the board for cooling purposes. Do not block power supply ventilation holes and fan.

Electro-Magnetic Interference (EMI)

This equipment has not been tested for compliance with emission limits of FCC and similar international regulations. Use of this equipment in a residential location is prohibited. This equipment generates, uses and can radiate radio frequency energy which may result in harmful interference to radio communications. If this equipment does cause harmful interfence to radio or television reception, which can be determined by turning the equipment on and off, the user is required to take measures to eliminate this interference.

Telecommunications Port Restrictions

The wireline telecommunications ports (modem, xDSL, T1/E1) on this product must not be connected to the Public Switched Telecommunication Network (PSTN) as it might result in disruption of the network. No formal telecommunication certification to FCC, R&TTE Directive, or other national requirements have been obatined.

Electrostatic Discharge (ESD) Warning

A properly grounded ESD wrist strap must be worn during operation/installation of the boards, connection of cables, or during installation or removal of daughter cards. Failure to use wrist straps can damage components within the system.

Attention: Please return this product to Intel for proper disposition. If it is not returned, refer to local environmental regulations for proper recycling. Do not dispose of this product in unsorted municipal waste.

A.2. Compliance and Conformity Information

CE EMI Conformity Caution

This development board is delivered conforming to relevant standards mandated by Directive 2004/108/EC. Because of the nature of programmable logic devices, it is possible for the user to modify the development kit in such a way as to generate electromagnetic interference (EMI) that exceeds the limits established for this equipment. Any EMI caused as a result of modifications to the delivered material is the responsibility of the user of this development kit.

CE

B. Revision History

B.1. User Guide Revision History

Document Version	Changes
2019.07.24	Sections Updated: • Overview on page 4 • Installing the Development Board on page 6 • Board Overview on page 12 • Intel Stratix 10 GX FPGA on page 16 • Power Supply on page 44 All occurences of USB-Blaster have been renamed to Intel FPGA Download Cable II throughout this document

Table 27. Intel Stratix 10 GX Transceiver Signal Integrity Development Kit User Guide Revision History

Version	Description
2017.10.11	Reorganized Revision History as a separate Appendix chapter.
2017.08.10	H-Tile Updates completed
2017.04.17	ES Release

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- *Специальные условия для постоянных клиентов.*
- *Подбор аналогов.*
- *Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.*

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- *Тестирование поставляемой продукции.*
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