Ultralow Distortion, High Speed, 0.95 nV/√Hz Voltage Noise Op Amp

Data Sheet

AD8099

FEATURES

Ultralow noise: 0.95 nV/√Hz, 2.6 pA/√Hz
Ultralow distortion
- **2nd harmonic R_L = 1 kΩ , G = +2**
  - **−92 dB at 10 MHz**
- **3rd harmonic R_L = 1 kΩ , G = +2**
  - **−105 dB at 10 MHz**

High speed
- **Gain bandwidth product (GBWP): 3.8 GHz**
- **−3 dB bandwidth**
  - **700 MHz (G = +2)**
  - **550 MHz (G = +10)**
- **Slew rate**
  - **475 V/µs (G = +2)**
  - **1350 V/µs (G = +10)**

New pinout
Custom external compensation, gain range −1, +2 to +10
Supply current: 15 mA
Offset voltage: 0.5 mV max
Wide supply voltage range: 5 V to 12 V

APPLICATIONS

Preamplifiers
Receivers
Instrumentation
Filters
Intermediate frequency (IF) and baseband amplifiers
Analog-to-digital drivers
Digital-to-analog converter (DAC) buffers
Optical electronics

GENERAL DESCRIPTION

The AD8099 is an ultralow noise (0.95 nV/√Hz) and distortion (−92 dBc at 10 MHz) voltage feedback op amp, the combination of which makes it ideal for 16- and 18-bit systems. The AD8099 features a new, highly linear, low noise input stage that increases the full power bandwidth (FPBW) at low gains with high slew rates. The Analog Devices, Inc., proprietary next generation extra fast complimentary bipolar (XFCB) process enables such high performance amplifiers with relatively low power.

The AD8099 features external compensation, which lets the user set the gain bandwidth product. External compensation allows gains from +2 to +10 with minimal trade-off in bandwidth. The AD8099 also features an extremely high slew rate of 1350 V/µs, giving the designer flexibility to use the entire dynamic range without trading off bandwidth or distortion. The AD8099 settles to 0.1% in 18 ns and recovers from overdrive in 50 ns.

CONNECTION DIAGRAMS

Figure 1. 8-Lead LFCSP (CP-8-13)

Figure 2. 8-Lead SOIC-EP (RD-8-1)

The AD8099 drives 100 Ω loads at breakthrough performance levels with only 15 mA of supply current. With the wide supply voltage range (5 V to 12 V), low offset voltage (0.1 mV typ), wide bandwidth (700 MHz for G = +2), and a GBWP up to 3.8 GHz, the AD8099 is designed to work in a wide variety of applications.

The AD8099 is available in a 3 mm × 3 mm lead frame chip scale package (LFCSP) with a new pinout that is specifically optimized for high performance, high speed amplifiers. The new LFCSP and pinout enable the breakthrough performance that previously was not achievable with amplifiers. The AD8099 is rated to work over the extended industrial temperature range, −40°C to +125°C.

Figure 3. Harmonic Distortion vs. Frequency and Gain (SOIC)

Rev. E
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REVISION HISTORY

7/2016—Rev. D to Rev. E

Changed CP-8-2 to CP-8-13 ... Throughout
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8/2013—Rev. C to Rev. D

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1/2013—Rev. B to Rev. C

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6/2004—Rev. A to Rev. B

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1/2004—Rev. 0 to Rev. A

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11/2003—Revision 0: Initial Version

SPECIFICATIONS

SPECIFICATIONS WITH ±5 V SUPPLY

T_A = 25°C, G = +2, R_L = 1 kΩ to ground, unless otherwise noted. Refer to Figure 60 through Figure 66 for component values and gain configurations.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	G = +5, V_{OUT} = 0.2 V p-p	450	510		MHz
	G = +5, V_{OUT} = 2 V p-p	205	235		MHz
Bandwidth for 0.1 dB Flatness (SOIC/LFCSP)	G = +2, V_{OUT} = 0.2 V p-p		34/25		MHz
Slew Rate	G = +10, V_{OUT} = 6 V Step	1120	1350		V/µs
	G = +2, V_{OUT} = 2 V Step	435	470		V/µs
Settling Time to 0.1%	G = +2, V_{OUT} = 2 V Step		18		ns
NOISE/DISTORTION PERFORMANCE					
Harmonic Distortion (dBc) HD2/HD3	f_C = 500 kHz, V_{OUT} = 2 V p-p, G = +10		−102/−111		dBc
	f_C = 10 MHz, V_{OUT} = 2 V p-p, G = +10		−84/−92		dBc
Input Voltage Noise	f = 100 kHz		0.95		nV/√Hz
Input Current Noise	f = 100 kHz, $\overline{\text{DISABLE}}$ pin floating		2.6		pA/√Hz
	f = 100 kHz, $\overline{\text{DISABLE}}$ pin = $+V_S$		5.2		pA/√Hz
DC PERFORMANCE					
Input Offset Voltage			0.1	0.5	mV
Input Offset Voltage Drift			2.3		µV/°C
Input Bias Current	$\overline{\text{DISABLE}}$ pin floating		−6	−13	µA
	$\overline{\text{DISABLE}}$ pin = $+V_S$		−0.1	−2	µA
Input Bias Current Drift			3		nA/°C
Input Bias Offset Current			0.06	1	µA
Open-Loop Gain		82	85		dB
INPUT CHARACTERISTICS					
Input Resistance	Differential mode		4		kΩ
	Common mode		10		MΩ
Input Capacitance			2		pF
Input Common-Mode Voltage Range			−3.7 to +3.7		V
Common-Mode Rejection Ratio	V_{CM} = ±2.5 V	98	105		dB
$\overline{\text{DISABLE}}$ PIN					
$\overline{\text{DISABLE}}$ Input Voltage	Output disabled		<2.4		V
Turn-Off Time	50% of $\overline{\text{DISABLE}}$ to < 10% of final V_{OUT}, V_{IN} = 0.5 V, G = +2		105		ns
Turn-On Time	50% of $\overline{\text{DISABLE}}$ to < 10% of final V_{OUT}, V_{IN} = 0.5 V, G = +2		39		ns
Enable Pin Leakage Current	$\overline{\text{DISABLE}}$ = +5 V		17	21	µA
$\overline{\text{DISABLE}}$ Pin Leakage Current	$\overline{\text{DISABLE}}$ = −5 V		35	44	µA
OUTPUT CHARACTERISTICS					
Output Overdrive Recovery Time (Rise/Fall)	V_{IN} = −2.5 V to +2.5 V, G =+2		30/50		ns
Output Voltage Swing	R_L = 100 Ω	−3.4 to +3.5	−3.6 to +3.7		V
	R_L = 1 kΩ	−3.7 to +3.7	−3.8 to +3.8		V
Short-Circuit Current	Sinking and sourcing		131/178		mA
Off Isolation	f = 1 MHz, $\overline{\text{DISABLE}}$ = low		−61		dB
POWER SUPPLY					
Operating Range			±5	±6	V
Quiescent Current			15	16	mA
Quiescent Current (Disabled)	$\overline{\text{DISABLE}}$ = Low		1.7	2	mA
Positive Power Supply Rejection Ratio	$+V_S$ = 4 V to 6 V, $-V_S$ = −5 V (input referred)	85	91		dB
Negative Power Supply Rejection Ratio	$+V_S$ = 5 V, $-V_S$ = −6 V to −4 V (input referred)	86	94		dB

SPECIFICATIONS WITH +5 V SUPPLY

V_S = 5 V at T_A = 25°C, G = +2, R_L = 1 kΩ to midsupply, unless otherwise noted. Refer to Figure 60 through Figure 66 for component values and gain configurations.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	G = +5, V_{OUT} = 0.2 V p-p	415	440		MHz
	G = +5, V_{OUT} = 2 V p-p	165	210		MHz
Bandwidth for 0.1 dB Flatness (SOIC/LFCSP)	G = +2, V_{OUT} = 0.2 V p-p		33/23		MHz
Slew Rate	G = +10, V_{OUT} = 2 V Step	630	715		V/µs
	G = +2, V_{OUT} = 2 V Step	340	365		V/µs
Settling Time to 0.1%	G = +2, V_{OUT} = 2 V Step		18		ns
NOISE/DISTORTION PERFORMANCE					
Harmonic Distortion (dBc) HD2/HD3	f_C = 500 kHz, V_{OUT} = 1 V p-p, G = +10		−82/−94		dBc
	f_C = 10 MHz, V_{OUT} = 1 V p-p, G = +10		−80/−75		dBc
Input Voltage Noise	f = 100 kHz		0.95		nV/√Hz
Input Current Noise	f = 100 kHz, $\overline{\text{DISABLE}}$ pin floating		2.6		pA/√Hz
	f = 100 kHz, $\overline{\text{DISABLE}}$ pin = $+V_S$		5.2		pA/√HZ
DC PERFORMANCE					
Input Offset Voltage			0.1	0.5	mV
Input Offset Voltage Drift			2.5		µV/°C
Input Bias Current	$\overline{\text{DISABLE}}$ pin floating		−6.2	−13	µA
	$\overline{\text{DISABLE}}$ pin = $+V_S$		−0.2	−2	µA
Input Bias Offset Current			0.05	1	µA
Input Bias Offset Current Drift			2.4		nA/°C
Open-Loop Gain	V_{OUT} = 1 V to 4 V	76	81		dB
INPUT CHARACTERISTICS					
Input Resistance	Differential mode		4		kΩ
	Common mode		10		MΩ
Input Capacitance			2		pF
Input Common-Mode Voltage Range			1.3 to 3.7		V
Common-Mode Rejection Ratio	V_{CM} = 2 V to 3 V	88	105		dB
$\overline{\text{DISABLE}}$ PIN					
$\overline{\text{DISABLE}}$ Input Voltage	Output disabled		<2.4		V
Turn-Off Time	50% of $\overline{\text{DISABLE}}$ to <10% of Final V_{OUT}, V_{IN} = 0.5 V, G = +2		105		ns
Turn-On Time	50% of $\overline{\text{DISABLE}}$ to <10% of Final V_{OUT}, V_{IN} = 0.5 V, G = +2		61		ns
Enable Pin Leakage Current	$\overline{\text{DISABLE}}$ = 5 V		16	21	µA
$\overline{\text{DISABLE}}$ Pin Leakage Current	$\overline{\text{DISABLE}}$ = 0 V		33	44	µA
OUTPUT CHARACTERISTICS					
Overdrive Recovery Time (Rise/Fall)	V_{IN} = 0 to 2.5 V, G = +2		50/70		ns
Output Voltage Swing	R_L = 100 Ω	1.5 to 3.5	1.2 to 3.8		V
	R_L = 1 kΩ	1.2 to 3.8	1.2 to 3.8		V
Short-Circuit Current	Sinking and Sourcing		60/80		mA
Off Isolation	f = 1 MHz, $\overline{\text{DISABLE}}$ = Low		−61		dB
POWER SUPPLY					
Operating Range			±5	±6	V
Quiescent Current			14.5	15.4	mA
Quiescent Current (Disabled)	$\overline{\text{DISABLE}}$ = Low		1.4	1.7	mA
Positive Power Supply Rejection Ratio	$+V_S$ = 4.5 V to 5.5 V, $-V_S$ = 0 V (input referred)	84	89		dB
Negative Power Supply Rejection Ratio	$+V_S$ =5 V, $-V_S$= −0.5 V to +0.5 V (input referred)	84	90		dB

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	12.6 V
Power Dissipation	See Figure 4
Differential Input Voltage	±1.8 V
Differential Input Current	±10mA
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +125°C
Lead Temperature (Soldering 10 sec)	300°C
Junction Temperature	150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation in the AD8099 package is limited by the associated rise in junction temperature (T_J) on the die. The plastic encapsulating the die locally reaches the junction temperature. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit may change the stresses that the package exerts on the die, permanently shifting the parametric performance of the AD8099. Exceeding a junction temperature of 150°C for an extended period can result in changes in silicon devices, potentially causing failure.

The still-air thermal properties of the package and PCB (θ_{JA}), the ambient temperature (T_A), and the total power dissipated in the package (P_D) determine the junction temperature of the die. The junction temperature can be calculated as

$$T_J = T_A + \left(P_D \times \theta_{JA}\right)$$

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive for all outputs. The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S). Assuming the load (R_L) is referenced to midsupply, the total drive power is $V_S/2 \times I_{OUT}$, some of which is dissipated in the package and some in the load ($V_{OUT} \times I_{OUT}$).

The difference between the total drive power and the load power is the drive power dissipated in the package.

$$P_D = \textit{Quiescent Power} + (\textit{Total Drive Power} - \textit{Load Power})$$

$$P_D = \left(V_S \times I_S\right) + \left(\frac{V_S}{2} \times \frac{V_{OUT}}{R_L}\right) - \frac{V_{OUT}^{\ 2}}{R_L}$$

RMS output voltages should be considered. If R_L is referenced to V_S−, as in single-supply operation, then the total drive power is $V_S \times I_{OUT}$. If the rms signal levels are indeterminate, consider the worst case, when $V_{OUT} = V_S/4$ for R_L to midsupply:

$$P_D = \left(V_S \times I_S\right) + \frac{\left(V_S/4\right)^2}{R_L}$$

In single-supply operation with R_L referenced to V_S−, worst case is $V_{OUT} = V_S/2$.

Airflow increases heat dissipation, effectively reducing θ_{JA}. Also, more metal directly in contact with the package leads from metal traces, through holes, ground, and power planes reduce the θ_{JA}. Soldering the exposed paddle to the ground plane significantly reduces the overall thermal resistance of the package. Take care to minimize parasitic capacitances at the input leads of high speed op amps, as discussed in the PCB Layout section.

Figure 4 shows the maximum safe power dissipation in the package versus the ambient temperature for the exposed paddle (EPAD) SOIC-8 (70°C/W), and LFCSP (70°C/W), packages on a JEDEC standard 4-layer board. θ_{JA} values are approximations.

Figure 4. Maximum Power Dissipation

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

Default conditions: V_S = ±5 V, T_A = 25°C, R_L = 1 kΩ tied to ground unless otherwise noted. Refer to Figure 63 through Figure 66 for component values and gain configurations.

Figure 5. Small Signal Frequency Response for Various Gains (SOIC)

Figure 8. Small Signal Frequency Response for Various Gains (LFCSP)

Figure 6. Small Signal Frequency Response for Various Load Resistors

Figure 9. Small Signal Frequency Response for Various Supply Voltages

Figure 7. Small Signal Frequency Response for Various Temperatures (SOIC)

Figure 10. Small Signal Frequency Response for Various Temperatures (LFCSP)

Figure 11. Small Signal Frequency Response for Various Capacitive Loads

Figure 14. Open Loop Frequency Response

Figure 12. Large Signal Frequency Response for Various Gains (SOIC)

Figure 15. Large Signal Frequency Response for Various Gains (LFCSP)

Figure 13. 0.1 dB Flatness (SOIC)

Figure 16. 0.1 dB Flatness (LFCSP)

Figure 17. Large Signal Frequency Response for Various Load Resistances

Figure 20. Large Signal Frequency Response for Various Supply Voltages

Figure 18. Input Impedance vs. Frequency

Figure 21. Off Isolation vs. Frequency

Figure 19. Output Impedance vs. Frequency for Various Gains

Figure 22. Harmonic Distortion vs. Frequency

Figure 23. Harmonic Distortion vs. Frequency (SOIC)

Figure 24. Harmonic Distortion vs. Frequency (SOIC)

Figure 25. Harmonic Distortion vs. Frequency (SOIC)

Figure 26. Harmonic Distortion vs. Frequency (LFCSP)

Figure 27. Harmonic Distortion vs. Frequency (LFCSP)

Figure 28. Harmonic Distortion vs. Frequency (LFCSP)

Figure 29. Harmonic Distortion vs. Frequency and Supply Voltage (SOIC)

Figure 30. Harmonic Distortion vs. Output Amplitude (SOIC)

Figure 31. Harmonic Distortion vs. Output Amplitude (SOIC)

Figure 32. Harmonic Distortion vs. Frequency for Various Supplies (LFCSP

Figure 33. Harmonic Distortion vs. Output Amplitude (LFCSP)

Figure 34. Harmonic Distortion vs. Output Amplitude (LFCSP)

Figure 35. Small Signal Transient Response for Various Capacitive Loads (SOIC)

Figure 36. Small Signal Transient Response for Various Supply Voltages

Figure 37. Output Overdrive Recovery for Various Resistive Loads

Figure 38. Small Signal Transient Response for Various Capacitive Loads (LFCSP)

Figure 39. Small Signal Transient Response for Various Supply Voltages

Figure 40. Disable/Enable Switching Speed

Figure 41. Large Signal Transient Response vs. Supply Voltage (LFCSP)

Figure 42. Large Signal Transient Response vs. Supply Voltage (SOIC)

Figure 43. Large Signal Transient Response for Various Supply Voltages and Load Resistances (SOIC and LFCSP)

Figure 44. Short Term Settling Time (LFCSP)

Figure 45. Short Term Settling Time (SOIC)

Figure 46. Long Term Settling Time

Figure 47. Common-Mode Rejection vs. Frequency

Figure 50. Power Supply Rejection vs. Frequency

Figure 48. Input Current Noise vs. Frequency ($\overline{DISABLE}$ = Open)

Figure 51. Input Current Noise vs. Frequency ($\overline{DISABLE}$ = +V_S)

Figure 49. Input Voltage Noise vs. Frequency

Figure 52. Input Offset Voltage Distribution

Figure 53. Input Offset Voltage vs. Temperature

Figure 54. Input Bias Current vs. Temperature ($\overline{DISABLE}$ Pin Floating)

Figure 55. Output Saturation Voltage vs. Temperature

Figure 56. Supply Current vs. Temperature

Figure 57. Input Bias Current vs. Temperature ($\overline{DISABLE}$ Pin = $+V_S$)

THEORY OF OPERATION

The AD8099 is a voltage feedback op amp that employs a new highly linear low noise input stage. With this input stage, the AD8099 can achieve better than 90 dB distortion for a 2 V p-p, 10 MHz output signal with an input referred voltage noise of less than 1 nV/√Hz. This noise level and distortion performance has been previously achievable only with fully uncompensated amplifiers. The AD8099 achieves this level of performance for gains as low as +2. This new input stage also triples the achievable slew rate for comparably compensated 1 nV/√Hz amplifiers.

The simplified AD8099 topology is shown in Figure 58. The amplifier is a single gain stage with a unity gain output buffer fabricated in the Analog Devices extra fast complimentary bipolar (XFCB) process. The AD8099 has 85 dB of open-loop gain and maintains precision specifications such as CMRR, PSRR, V_{OS}, and $\Delta V_{OS}/\Delta T$ to levels that are normally associated with topologies having two or more gain stages.

Figure 58. AD8099 Topology

The AD8099 can be externally compensated down to a gain of 2 through the use of an RC network. Above gains of 15, no external compensation network is required. To realize the full gain bandwidth product of the AD8099, no PCB trace should be connected to or within close proximity of the external compensation pin for the lowest possible capacitance.

External compensation allows the user to optimize the closed-loop response for minimal peaking while increasing the gain bandwidth product in higher gains, lowering distortion errors that are normally more prominent with internally compensated parts in higher gains. For a fixed gain bandwidth, wideband distortion products would normally increase by 6 dB going from a closed-loop gain of 2 to 4. Increasing the gain bandwidth product of the AD8099 eliminates this effect with increasing closed-loop gain.

The AD8099 is available in both a SOIC and an LFCSP, each of which has a thermal pad for lower operating temperature. To help avoid this pad in board layout, both packages have an extra output pin on the opposite side of the package for ease in connecting a feedback network to the inputs. The secondary output pin also isolates the interaction of any capacitive load on the output and self-inductance of the package and bond wire from the feedback loop. While using the secondary output for feedback, inductance in the primary output now helps to isolate capacitive loads from the output impedance of the amplifier. Since the SOIC has greater inductance in its output, the SOIC drives capacitive loads better than the LFCSP. Using the primary output for feedback with both packages results in the LFCSP driving capacitive load better than the SOIC.

The LFCSP and SOIC pinouts are identical, except for the rotation of all pins counterclockwise by one pin on the LFCSP. This isolates the inputs from the negative power supply pin, removing a mutually inductive coupling that is most prominent while driving heavy loads. For this reason, the LFCSP second harmonic, while driving a heavy load, is significantly better than that of the SOIC.

A three-state input pin is provided on the AD8099 for a high impedance power-down and an optional input bias current cancellation circuit. The high impedance output allows several AD8099 devices to drive the same ADC or output line time interleaved. Pulling the $\overline{\text{DISABLE}}$ pin low activates the high impedance state. See Table 5 for threshold levels. When the $\overline{\text{DISABLE}}$ pin is left floating, the AD8099 operates normally. With the $\overline{\text{DISABLE}}$ pin pulled within 0.7 V of the positive supply, an optional input bias current cancellation circuit is turned on, which lowers the input bias current to less than 200 nA. In this mode, the user can drive the AD8099 with a high dc source impedance and still maintain minimal output referred offset without having to use impedance matching techniques. In addition, the AD8099 can be ac-coupled while setting the bias point on the input with a high dc impedance network. The input bias current cancellation circuit doubles the input referred current noise, but this effect is minimal as long as wideband impedance is kept low (see Figure 48 and Figure 51).

A pair of internally connected diodes limits the differential voltage between the noninverting input and the inverting input of the AD8099. Each set of diodes has two series diodes, which are connected in anti-parallel. This limits the differential voltage between the inputs to approximately ±1.8 V. All of the AD8099 pins are ESD protected with voltage limiting diodes connected between both rails. The protection diodes can handle 5 mA of steady state current. Currents should be limited to 5 mA or less through the use of a series limiting resistor.

APPLICATIONS INFORMATION

USING THE AD8099

The AD8099 offers unrivaled noise and distortion performance in low signal gain configurations. In low gain configurations (less than 15), the AD8099 requires external compensation. The amount of gain and performance needed determines the compensation network.

Understanding the subtleties of the AD8099 gives the user insight on how to exact its peak performance. Use the component values and circuit configurations shown in the Applications Information section as starting points for designs. Specific circuit applications dictate the final configuration and value of the components.

CIRCUIT COMPONENTS

The circuit components are referenced in Figure 59, the recommended noninverting circuit schematic for the AD8099. See Table 4 for typical component values and performance data.

Figure 59. Wideband Noninverting Gain Configuration (SOIC)

R_F and R_G—The feedback resistor and the gain set resistor determine the noise gain of the amplifier; typical R_F values range from 250 Ω to 499 Ω.

C_F—Creates a zero in the loop response to compensate the pole created by the input capacitance (including stray capacitance) and the feedback resistor, R_F. C_F helps reduce high frequency peaking and ringing in the closed-loop response. The typical range is 0.5 pF to 1.5 pF for the evaluation circuits used here.

R1—This resistor terminates the input of the amplifier to the source resistance of the signal source, typically 50 Ω. (This is application specific and not always required.)

R_S—Many high speed amplifiers in low gain configurations require that the input stage be terminated into a nominal impedance to maintain stability. The value of R_S should be kept to 50 Ω or lower to maintain low noise performance. At higher gains, R_S may be reduced or even eliminated. Typical range is 0 Ω to 50 Ω.

C_C—The compensation capacitor decreases the open-loop gain at higher frequencies where the phase is degrading. By decreasing the open-loop gain here, the phase margin is increased and the amplifier is stabilized. Typical range is 0 pF to 5 pF. The value of C_C is gain dependent.

R_C—The series lead inductance of the package and the compensation capacitance (C_C) forms a series resonant circuit. R_C dampens this resonance and prevents oscillations. The recommended value of R_C is 50 Ω for a closed-loop gain of 2. This resistor introduces a zero in the open-loop response and must be kept low so that this zero occurs at a higher frequency. The purpose of the compensation network is to decrease the open-loop gain. If the resistance becomes too large, the gain is reduced to the resistor value, and not necessarily to 0 Ω, which is what a single capacitor would do over frequency. Typical value range is 0 Ω to 50 Ω.

C1—To lower the impedance of R_C, C1 is placed in parallel with R_C. C1 is not required, but greatly reduces peaking at low closed-loop gains. The typical value range is 0 pF to 2 pF.

C2 and C3—Bypass capacitors are connected between both supplies for optimum distortion and PSRR performance. These capacitors should be placed as close as possible to the supply pins of the amplifier. For C3 and C5, a 0508 case size should be used. The 0508 case size offers reduced inductance and better frequency response.

C4 and C2—Electrolytic bypass capacitors.

RECOMMENDED VALUES

Table 4. Recommended Values and AD8099 Performance

Gain	Package	Feedback Network Values				Compensation Network Values			–3 dB SS Bandwidth (MHz)	Slew Rate (V/µs)	Peaking (dB)	Output Noise (AD8099 Only) (nV/√Hz)	Total Output Noise Including Resistors (nV/√Hz)
		R_F	R_G	R_S	C_F	R_C	C_C	C1					
–1, 2	SOIC	250	250	50	1.5	50	4	1.5	440/700	515	0.3/3.1	2.1	4
2	LFCSP	250	250	50	0.5	50	5	2	700	475	3.2	2.1	4
–1	LFCSP	250	250	50	1.0	50	5	2	420	475	0.8	2.1	4
5	LFCSP/SOIC	499	124	20	0.5	50	1	0	510	735	1.4	4.9	8.6
10	LFCSP/SOIC	499	54	0	0	0	0.5	0	550	1350	0.8	9.6	13.3
20	LFCSP/SOIC	499	26	0	0	0	0	0	160	1450	0	19	23.3

CIRCUIT CONFIGURATIONS

Figure 60 through Figure 66 show typical schematics for the AD8099 in various gain configurations. Table 4 data was collected using the schematics shown in Figure 60 through Figure 66. Resistor R1, as shown in Figure 60 through Figure 66, is the test equipment termination resistor. R1 is not required for normal operation, but is shown in the schematics for completeness.

Figure 60. Amplifier Configuration for SOIC Package, Gain = –1

Figure 61. Amplifier Configuration for SOIC Package, Gain = +2

Figure 62. Amplifier Configuration for LFCSP, Gain = –1

Figure 63. Amplifier Configuration for LFCSP, Gain = +2

Figure 64. Amplifier Configuration for LFCSP and SOIC Package, Gain = +5

Figure 65. Amplifier Configuration for LFCSP and SOIC Packages, Gain = +10

Figure 66. Amplifier Configuration for LFCSP and SOIC Packages, Gain = +20

PERFORMANCE vs. COMPONENT VALUES

The influence that each component has on the AD8099 frequency response can be seen in Figure 68 to Figure 73. In Figure 68 to Figure 73, all component values are held constant, except for the individual component shown, which is varied. For example, in the R_S performance plot (Figure 69), all components are held constant except R_S, which is varied from 0 Ω to 50 Ω. Figure 69 clearly indicates that R_S has a major influence on the peaking and the bandwidth of the AD8099.

Figure 67. Complete Noninverting Amplifier Configuration for SOIC Package with Compensation Network

Figure 68. Frequency Response for Various Values of R_F and R_G

Figure 69. Frequency Response for Various Values of R_S

Figure 70. Frequency Response for Various Values of R_C

Figure 71. Frequency Response for Various Values of C_F

Figure 72. Frequency Response for Various Values of C1

Figure 73. Frequency Response for Various Values of C_C

TOTAL OUTPUT NOISE CALCULATIONS AND DESIGN

To analyze the noise performance of an amplifier circuit, the individual noise sources must be identified. A user must then determine if the source has a significant contribution to overall noise performance of the amplifier. To simplify the noise calculations, this data sheet works with noise spectral densities rather than actual voltages to leave bandwidth out of the expressions (noise spectral density, which is generally expressed in nV/√Hz, is equivalent to the noise in a 1 Hz bandwidth).

The noise model shown in Figure 74 has six individual noise sources: the Johnson noise of the three resistors, the op amp voltage noise, and the current noise in each input of the amplifier. Each noise source has its own contribution to the noise at the output. Noise is generally specified referred to input (RTI), but it is often simpler to calculate the noise referred to the output (RTO) and then divide by the noise gain to obtain the RTI noise.

All resistors have a Johnson noise of $\sqrt{(4kBTR)}$, where k is Boltzmann's Constant (1.38×10^{-23} J/K), T is the absolute temperature in Kelvin, B is the bandwidth in Hz, and R is the resistance in ohms. A simple relationship, which is easy to remember, is that a 50 Ω resistor generates a Johnson noise of 1 nV√Hz at 25°C. The AD8099 amplifier has roughly the same equivalent noise as a 50 Ω resistor.

◆ RTI NOISE = $\sqrt{V_N^2 + 4kTR3 + 4kTR1\left[\frac{R2}{R1 + R2}\right]^2 + I_{N+}^2R3^2 + I_{N-}^2\left[\frac{R1 \times R2}{R1 + R2}\right]^2 + 4kTR2\left[\frac{R1}{R1 + R2}\right]^2}$

◆ RTO NOISE = NG × RTI NOISE

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Figure 74. Op Amp Noise Analysis Model

In applications where noise sensitivity is critical, care must be taken not to introduce other significant noise sources to the amplifier. Each resistor is a noise source. Attention to design, layout, and component selection is critical to maintain low noise performance. A summary of noise performance for the amplifier and associated resistors can be seen in Table 4.

INPUT BIAS CURRENT AND DC OFFSET

In high noise gain configurations, the effects of output offset voltage can be significant, even with low input bias currents and input offset voltages. Figure 75 shows a comprehensive offset voltage model, which can be used to determine the referred to output (RTO) offset voltage of the amplifier or referred to input (RTI) offset voltage.

◆ OFFSET (RTO) = $V_{OS}\left[1 + \frac{R2}{R1}\right] + I_{B+} \times R3\left[1 + \frac{R2}{R1}\right] - I_{B-} \times R2$

◆ OFFSET (RTI) = $V_{OS} + I_{B+} \times R3 - I_{B-}\left[\frac{R1 \times R2}{R1 + R2}\right]$

FOR BIAS CURRENT CANCELLATION:

OFFSET (RTI) = V_{OS} IF $I_{B+} = I_{B-}$ AND R3 = $\left[\frac{R1 \times R2}{R1 + R2}\right]$

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Figure 75. Op Amp Total Offset Voltage Model

For RTO calculations, the input offset voltage and the voltage generated by the bias current flowing through R3 are multiplied by the noise gain of the amplifier. The voltage generated by I_{B-} through R2 is summed together with the previous offset voltages to arrive at a final output offset voltage. The offset voltage can also be referred to the input (RTI) by dividing the calculated output offset voltage by the noise gain.

As seen in Figure 75, if I_{B+} and I_{B-} are the same and R3 equals the parallel combination of R1 and R2, then the RTI offset voltage can be reduced to only V_{OS}. This is a common method used to reduce output offset voltage. Keeping resistances low helps to minimize offset error voltage and keeps the voltage noise low.

$\overline{\text{DISABLE}}$ PIN AND INPUT BIAS CANCELLATION

The AD8099 $\overline{\text{DISABLE}}$ pin performs three functions; enable, disable, and reduction of the input bias current. When the $\overline{\text{DISABLE}}$ pin is brought to within 0.7 V of the positive supply, the input bias current is reduced by an approximate factor of 60. However, the input current noise doubles to 5.2 pA/√Hz. Table 5 outlines the $\overline{\text{DISABLE}}$ pin functionality.

Table 5. $\overline{\text{DISABLE}}$ Pin Truth Table

Supply Voltage	±5 V	+5 V
Disable	−5 to +2.4	0 to 2.4
Enable	Open	Open
Low Input Bias Current	4.3 to 5	4.3 to 5

Figure 76. ADC Driver

16-BIT ADC DRIVER

Ultralow noise and distortion performance make the AD8099 an ideal ADC driver. Even though the AD8099 is not unity-gain stable, it can be configured to produce a net gain of +1 amplifier, as shown in Figure 76. This is achieved by combining a gain of +2 and a gain of −1 for a net gain of +1. The input range of the ADC is 0 V to 2.5 V.

Table 6 shows the performance data of the AD8099 and the AD7667, a 1 MSPS 16-bit ADC.

Table 6. ADC Driver Performance, f_C = 20 kHz, V_{OUT} = 2.24 V p-p

Parameter	Measurement (dB)
Second Harmonic Distortion	−111.4
Third Harmonic Distortion	−103.2
THD	−101.4
SFDR	102.2
SNR	88.1

CIRCUIT CONSIDERATIONS

Optimizing the performance of the AD8099 requires attention to detail in layout and signal routing of the board. Power supply bypassing, parasitic capacitance, and component selection all contribute to the overall performance of the amplifier. The AD8099 features an exposed paddle on the backs of both the LFCSP and SOIC packages. The exposed paddle provides a low thermal resistive path to the ground plane. For best performance, solder the exposed paddle to the ground plane.

PCB Layout

The compensation network is determined by the amplifier gain requirements. For lower gains, the layout and component placement are more critical. For higher gains, there are fewer compensation components, which results in a less complex layout.

Parasitics

The area surrounding the compensation pin is very sensitive to parasitic capacitance. To realize the full gain bandwidth product of the AD8099, there should be no trace connected to or within close proximity of the external compensation pin for the lowest possible capacitance. When compensation is required, the traces to the compensation pin, the negative supply, and the interconnect between components (C_C, C1, and R_C in Figure 59) should be made as wide as possible to minimize inductance.

All ground and power planes under the pins of the AD8099 should be cleared of copper to prevent parasitic capacitance between the input and output pins to ground. A single mounting pad on a SOIC footprint can add as much as 0.2 pF of capacitance to ground as a result of not clearing the ground or power plane under the AD8099 pins. Parasitic capacitance can cause peaking and instability, and should be minimized to ensure proper operation.

The new pinout of the AD8099 reduces the distance between the output and the inverting input of the amplifier. This helps to minimize the parasitic inductance and capacitance of the feedback path, which, in turn, reduces ringing and second harmonic distortion.

Grounding

When possible, ground and power planes should be used. Ground and power planes reduce the resistance and inductance of the power supply feeds and ground returns. If multiple planes are used, they should be stitched together with multiple vias. The returns for the input, output terminations, bypass capacitors, and R_G should all be kept as close to the AD8099 as possible. Ground vias should be placed at the very end of the component mounting pad to provide a solid ground return. The output load ground and the bypass capacitor grounds should be returned to a common point on the ground plane to minimize parasitic inductance and improve distortion performance. The AD8099 packages feature an exposed paddle. For optimum performance, solder this paddle to ground. For more information on PCB layout and design considerations, refer to section 7-2 of the 2002 Analog Devices Op Amp Applications book.

Power Supply Bypassing

The AD8099 power supply bypassing has been optimized for each gain configuration as shown in Figure 60 through Figure 66 in the Circuit Configurations section. The values shown should be used when possible. Bypassing is critical for stability, frequency response, distortion, and PSRR performance. The 0.1 µF capacitors shown in Figure 60 through Figure 66 should be as close to the supply pins of the AD8099 as possible and the electrolytic capacitors beside them.

Component Selection

Smaller components less than 1206 SMT case size, offer smaller mounting pads, which have fewer parasitics and allow for a more compact layout. It is critical for optimum performance that high quality, tight tolerance (where critical), and low drift components be used. For example, tight tolerance and low drift is critical in the selection of the feedback capacitor used in Figure 60. The feedback compensation capacitor in Figure 60 is 1.5 pF. This capacitor should be specified with NPO material. NPO material typically has a ±30 ppm/°C change over −55°C to +125°C temperature range. For a 100°C change, this results in a 4.5 fF change in capacitance, compared to an X7R material, which results in a 0.23 pF change, a 15% change from the nominal value. This can introduce excessive peaking, as shown in Figure 71.

DESIGN TOOLS AND TECHNICAL SUPPORT

Analog Devices is committed to the design process by providing technical support and online design tools. Analog Devices offers technical support via evaluation boards, sample ICs, SPICE models, interactive evaluation tools, application notes, phone and email support—all available at www.analog.com.

OUTLINE DIMENSIONS

Figure 77. 8-Lead Standard Small Outline Package with Exposed Pad [SOIC_N_EP]
Narrow Body
(RD-8-1)
Dimensions shown in millimeters

Figure 78. 8-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 mm Package Height
(CP-8-13)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding	Ordering Quantity
AD8099ARDZ	−40°C to +125°C	8-Lead SOIC_N_EP	RD-8-1		98
AD8099ARDZ-REEL	−40°C to +125°C	8-Lead SOIC_N_EP	RD-8-1		2,500
AD8099ARDZ-REEL7	−40°C to +125°C	8-Lead SOIC_N_EP	RD-8-1		1,000
AD8099ACPZ-R2	−40°C to +125°C	8-Lead LFCSP	CP-8-13	HDB	250
AD8099ACPZ-REEL	−40°C to +125°C	8-Lead LFCSP	CP-8-13	HDB	5,000
AD8099ACPZ-REEL7	−40°C to +125°C	8-Lead LFCSP	CP-8-13	HDB	1,500

[1] Z = RoHS Compliant Part.

NOTES

NOTES

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