

MAX9860

16-Bit Mono Audio Voice Codec

General Description

The MAX9860 is a low-power, voiceband, mono audio codec designed to provide a complete audio solution for wireless voice headsets and other mono voice audio devices. Using an on-chip bridge-tied load mono head-phone amplifier, the MAX9860 can output 30mW into a 32Ω earpiece while operating from a single 1.8V power supply. Very low power consumption makes it an ideal choice for battery-powered applications.

The MAX9860's flexible clocking circuitry utilizes common system clock frequencies ranging from 10MHz to 60MHz, eliminating the need for an external PLL and multiple crystal oscillators. Both the ADC and DAC support sample rates of 8kHz to 48kHz in either synchronous or asynchronous operation. Both master and slave timing modes are supported.

Two differential microphone inputs are available with a user-programmable preamplifier and programmable gain amplifier. Automatic gain control with selectable attack/release times and signal threshold allows maximum dynamic range. A noise gate with selectable threshold provides a means to quiet the channel when no signal is present. Both the DAC and ADC digital filters provide full attenuation for out-of-band signals as well as a 5th order GSM-compliant digital highpass filter. A digital side tone mixer provides loopback of the microphones/ADC signal to the DAC/headphone output.

Serial DAC and ADC data is transferred over a flexible digital I²S-compatible interface that also supports TDM mode. Mode settings, volume control, and shutdown are programmed through a 2-wire, I²C-compatible interface.

The MAX9860 is fully specified over the -40°C to +85°C extended temperature range and is available in a low-profile, 4mm x 4mm, 24-pin thin QFN package.

Applications

Audio Headsets

- Portable Navigation Device
- Mobile Phones
- Smart Phones
- VoIP Phones
- Audio Accessories

Pin Configuration and Typical Operating Circuit appear at end of data sheet.

Features

- ♦ 1.8V Single-Supply Operation
- Digital Highpass Elliptical Filters with Notch for 217Hz (GSM)
- Mono 30mW BTL Headphone Amplifier
- Dual Low-Noise Microphone Inputs
- Automatic Microphone Gain Control and Noise Gate
- ♦ 90dB DAC DR (f_S = 48kHz)
- 81dB ADC DR (fs = 48kHz)
- Supports Master Clock Frequencies from 10MHz to 60MHz
- Supports Sample Rates from 8kHz to 48kHz
- ♦ Flexible Digital Audio Interface
- Clickless/Popless Operation
- ♦ 2-Wire, I²C-Compatible Control Interface
- Available in 24-Pin, Thin QFN, 4mm x 4mm x 0.8mm Package

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX9860ETG+	-40°C to +85°C	24 TQFN-EP*

+Denotes a lead-free/RoHS-compliant package.

*EP = Exposed pad.

_Simplified Block Diagram



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to AGND.)	
DVDDIO, SDA, SCL, IRQ	0.3V to +3.6V
AVDD, DVDD	0.3V to +2V
AGND, DGND, MICGND	0.3V to +0.3V
OUTP, OUTN, PREG, REF, MICBIAS	0.3V to (V _{AVDD} + 0.3V)
MICLP, MICLN, MICRP, MICRN, REG	60.3V to (VPREG + 0.3V)
MCLK, LRCLK, BCLK,	
SDOUT, SDIN	0.3V to (V _{DVDDIO} + 0.3V)

Continuous Power Dissipation ($T_A = +70^{\circ}C$)	
24-Pin TQFN (derate 27.8mW/°C above +7	'0°С,
multilayer board)	2222mW
Operating Temperature Range	40°C to +85°C
Storage Temperature Range	65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C
Soldering Temperature (reflow)	+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

TQFN

Junction-to-Ambient Thermal Resistance (θ _{JA})......36°C/W Junction-to-Case Thermal Resistance (θ _{JC})......3°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to <u>www.maximintegrated.com/thermal-tutorial</u>.

ELECTRICAL CHARACTERISTICS

 $(V_{AVDD} = V_{DVDD} = V_{DVDDIO} = +1.8V, R_L = \infty$, headphone load (R_L) connected between OUTP and OUTN, $C_{REF} = 2.2\mu$ F, $C_{MICBIAS} = C_{PREG} = C_{REG} = 1\mu$ F, $A_{VPRE} = +20$ dB, $A_{VMICPGA} = 0$ dB, $f_{MCLK} = 13$ MHz, $f_{LRCLK} = 8$ kHz, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^{\circ}$ C.) (Note 2)

PARAMETER	SYMBOL	CONDITIO	NS	MIN	ТҮР	MAX	UNITS
		AVDD (inferred from HP of	utput PSRR)	1.7	1.8	1.9	
Supply Voltage Range		DVDD (inferred from code tests)	c performance	1.7	1.8	1.9	V
		DVDDIO		1.7	1.8	3.6	
		DAC playback mode	AVDD		1.46	2.2	
		(48kHz)	DVDD		1.05	1.6	
		Full operation	AVDD		4.08	5.7	
Total Supply Current		8kHz mono ADC + DAC	DVDD		0.78	1.0	
(Note 3)	IAVDD+DVDD	Full operation	AVDD		6.17	9.0	MA
		8kHz stereo ADC + DAC	DVDD		0.8	1.2	-
	Stereo	Stereo ADC only (48kHz)	AVDD		5.38	8.0	
			DVDD		1.68	2.2	
			AVDD		0.56	5	
Shutdown Supply Current	ISHDN	$T_A = +25^{\circ}C$	DVDD + DVDDIO		1.65	5	μA
Shutdown to Full Operation					10		ms
DAC (Note 4)							
Gain Error					±1	±5	%
Dynamic Range (Note 5)	DR	+0dB volume setting, $f_S = 8$ at headphone output, $T_A =$	3kHz, measured = +25°C	84	90		dB
DAC Full-Scale Output			_		1		V _{RMS}
DAC Path Phase Delay		f = 1kHz, 0dBFS, HP filter disabled_digital	f _S = 8kHz		1.2		ms
		input to analog output	f _S = 16kHz		0.59		1110
Total Harmonic Distortion + Noise	THD+N	$f = 1$ kHz, $f_{MCLK} = 12.288$ M $f_{LRCLK} = 48$ kHz	MHz,		-87		dB

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ELECTRICAL CHARACTERISTICS (continued)

 $(V_{AVDD} = V_{DVDD} = V_{DVDDIO} = +1.8V, R_L = \infty, headphone load (R_L) connected between OUTP and OUTN, C_{REF} = 2.2\mu F, C_{MICBIAS} = C_{REG} = 1\mu F, A_{VPRE} = +20dB, A_{VMICPGA} = 0dB, f_{MCLK} = 13MHz, f_{LRCLK} = 8kHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)$

PARAMETER	SYMBOL	CONDITIONS	MIN TYP MAX	UNITS	
Dower Supply Dejection Datio		$f = 1 kHz$, $V_{RIPPLE} = 100 mV_{P-P}$, $A_{VPGA} = 0 dB$	94	dD	
Power-Supply nejection natio	ronn	$f = 10kHz, V_{RIPPLE} = 100mV_{P-P}, A_{VPGA} = 0dB$	71	uв	
DAC LOWPASS DIGITAL FILTER					
Passband Cutoff	fplp	With respect to f_S within ripple; $f_S = 8kHz$ to $48kHz$	0.448 x fs	Hz	
		-3dB cutoff	0.451	fs	
Passband Ripple		f < f _{PLP}	±0.1	dB	
Stopband Cutoff	fSLP	With respect to f_S ; $f_S = 8kHz$ to $48kHz$	0.476 x fs	Hz	
Stopband Attenuation		$f > f_{SLP}, f = 20Hz$ to 20kHz	75	dB	
DAC HIGHPASS DIGITAL FILTER				_	
		DVFLT = 0x1 (elliptical for 16kHz GSM)	0.0161 x fs		
	fdнppb	DVFLT = 0x2 (500Hz Butterworth for 16kHz)	0.0312 x fs	Hz	
5th Order Passband Cutoff (-3dB from Peak, I ² C Register Programmable) (Note 6)		DVFLT = 0x3 (elliptical for 8kHz GSM)	0.0321 x fs		
Frogrammable) (Note 0)		DVFLT = 0x4 (500Hz Butterworth for 8kHz)	0.0625 x fs		
		DVFLT = 0x5 (200Hz Butterworth for 48kHz)	0.0042 x fs		
		DVFLT = 0x1 (elliptical for 16kHz GSM)	0.0139 x fs		
		DVFLT = 0x2 (500Hz Butterworth for 16kHz)	0.0156 x fs		
5th Order Stopband Cutoff (-30dB from Peak, I ² C Register Programmable) (Note 6)	f DHPSB	DVFLT = 0x3 (elliptical for 8kHz GSM)	0.0279 x fs	Hz	
		DVFLT = 0x4 (500Hz Butterworth for 8kHz)	0.0312 x fs		
		DVFLT = 0x5 (200Hz Butterworth for 48kHz)	0.0021 x fs	1	
DC Blocking	DCAtten	DVFLT ≠ 0x0	90	dB	
ADC					
Full-Scale Input Voltage	0dBFS	Differential MIC Input, A _{VPRE} = 0dB, A _{VPGA} = 0dB	1	Vp-p	
Channel Gain Mismatch			±0.3	%	

ELECTRICAL CHARACTERISTICS (continued)

 $(V_{AVDD} = V_{DVDD} = V_{DVDDIO} = +1.8V, R_L = \infty, headphone load (R_L) connected between OUTP and OUTN, C_{REF} = 2.2\mu F, C_{MICBIAS} = C_{REG} = 1\mu F, A_{VPRE} = +20dB, A_{VMICPGA} = 0dB, f_{MCLK} = 13MHz, f_{LRCLK} = 8kHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)$

PARAMETER	SYMBOL	CONDITIONS		MIN	ТҮР	МАХ	UNITS
Dynamic Range (Note 5)	DR	$f_S = 8kHz, A_{VPRE} = 0dB,$ DR A-weighted from 20Hz to $f_S/2$			81		dB
		$f_S = 48$ kHz, A _{VPRE} = 0dB, 1	A = +25°C	75	83		
		f = 1kHz, 0dBFS, HP filter	f _S = 8kHz		1.2		
ADC Phase Delay		digital output	f _S = 16kHz		0.61		ms
Total Harmonic Distortion	THD	$f = 1kHz$, $f_S = 48kHz$, $T_A =$	+25°C	-70	-75		dB
Dower Curply Dejection Datio		$f = 1kHz, V_{RIPPLE} = 100mV$ AVPGA = 0dB	Р-Р,		82		dD
Power-supply rejection Ratio	PORK	$f = 10kHz$, $V_{RIPPLE} = 100mV_{P-P}$, $A_{VPGA} = 0dB$		76			dB
Channel Crosstalk		Driven channel at -1dBFS, 1	= 1kHz		-92		dB
ADC LOWPASS DIGITAL FILTER							-
Passband Cutoff	fplp	With respect to f_S within rip $f_S = 8$ kHz to 48kHz	ple;		0.445 x f _S		Hz
		-3dB cutoff			0.449		fs
Passband Ripple		f < f _{PLP}			±0.1		dB
Stopband Cutoff	fSLP	With respect to f_S ; $f_S = 8kH$	z to 48kHz		0.469 x f _S		Hz
Stopband Attenuation		f > f _{SLP}			74		dB
ADC HIGHPASS DIGITAL FILTER	2						
		AVFLT = $0x1$ (elliptical for 1	6kHz GSM)		0.0161 x f _S		
		AVFLT = 0x2 (500Hz Butterworth for 16kHz)		0.0312 x fs			
5th Order Passband Cutoff (-3dB from Peak, I ² C Register	fahppb	AVFLT = 0x3 (elliptical for 8kHz GSM)			0.0321 x f _S		Hz
		AVFLT = 0x4 (500Hz Butterworth for 8kHz)			0.0625 x fs		
		AVFLT = 0x5 (200Hz Butterworth for 48kl	Hz)		0.0042 x fs		

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ELECTRICAL CHARACTERISTICS (continued)

 $(V_{AVDD} = V_{DVDD} = V_{DVDDIO} = +1.8V, R_L = \infty, headphone load (R_L) connected between OUTP and OUTN, C_{REF} = 2.2\mu F, C_{MICBIAS} = C_{REG} = 1\mu F, A_{VPRE} = +20dB, A_{VMICPGA} = 0dB, f_{MCLK} = 13MHz, f_{LRCLK} = 8kHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)$

PARAMETER	SYMBOL	CONDITIO	NS	MIN	ТҮР	МАХ	UNITS
		AVFLT = 0x1 (elliptical for 16kHz GSM)			0.0139 x f _S		
		AVFLT = 0x2 (500Hz Butterworth for 16	<hz)< td=""><td></td><td>0.0156 x f_S</td><td></td><td></td></hz)<>		0.0156 x f _S		
5th Order Stopband Cutoff (-30dB from peak, I ² C Register Programmable) (Note 6)	f AHPSB	AVFLT = 0x3 (elliptical for 8kHz GSM)			0.0279 x f _S		Hz
		AVFLT = 0x4 (500Hz Butterworth for 8kł	Hz)		0.0312 x f _S		
		AVFLT = 0x5 (200Hz Butterworth for 48	<hz)< td=""><td></td><td>0.0021 x f_S</td><td></td><td></td></hz)<>		0.0021 x f _S		
DC Blocking	DCATTEN	AVFLT ≠ 0x0			90		dB
CLOCKING							
MCLK Input Frequency		MCLK is not required to be or related to the desired L	e synchronous RCLK data rate	10		60	MHz
MCLK Duty Cycle				40	50	60	%
Maximum MCLK Input Jitter		For guaranteed performar	nce limits		100		psrms
LRCLK Data Rate Frequency				8		48	kHz
LRCLK PLL Lock Time					12	25	ms
LRCLK Acceptable Jitter for Maintaining PLL Lock					±20		ns
MONO HEADPHONE AMPLIFIER							
	Bour	$f = 1$ kHz, THD+N ≤ 1 % $R_L = 16\Omega$		30	50		m\\/
	POUI	$T_A = +25^{\circ}C$	$R_L = 32\Omega$		33		TIIVV
Total Harmonia Distartian - Naisa		$R_L=32\Omega,P_{OUT}=25mW,$	f = 1kHz		0.05		0/
Total Harmonic Distortion + Noise		$R_L = 16\Omega$, $P_{OUT} = 25mW$,	f = 1kHz		0.08		70
Dynamic Range (Note 5)	DR	+0dB volume setting, DAC f _S = 8kHz to 48kHz	C input at		90		dB
		V _{AVDD} = 1.7V to 1.9V		60	84		
Power-Supply Rejection Ratio	PSRR	$V_{RIPPLE} = 100 m V_{P-P}, f = 2$	217Hz		86		dB
		$V_{\text{RIPPLE}} = 100 \text{mV}_{\text{P-P}}, f = 20 \text{kHz}$			71		
Output Offset Voltage	Vos	VOUTP - VOUTN, TA =+25°	С			± 3.5	mV
Capacitive Drive Capability		No sustained oscillations	$R_{L} = 32\Omega$ $R_{I} = \infty$		500 100		pF
Click-and-Pop Level		Peak voltage into/out of sh A-weighted	nutdown, 32sps,		-70		dBV

ELECTRICAL CHARACTERISTICS (continued)

 $(V_{AVDD} = V_{DVDD} = V_{DVDDIO} = +1.8V, R_L = \infty, headphone load (R_L) connected between OUTP and OUTN, C_{REF} = 2.2\mu F, C_{MICBIAS} = C_{PREG} = C_{REG} = 1\mu F, A_{VPRE} = +20dB, A_{VMICPGA} = 0dB, f_{MCLK} = 13MHz, f_{LRCLK} = 8kHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)$

PARAMETER	SYMBOL	CONDITIONS		MIN	ТҮР	MAX	UNITS
MICROPHONE AMPLIFIER							
			PAM = 00		Off		
Dreemenlifier Cain	A	Τ	PAM = 01	-0.5	0	+0.5	
Preampillier Gain	AVPRE	$IA = +25^{\circ}C$	PAM = 10	19	20	21	uв
			PAM = 11	29	30	31	1
	A	PGAM = 0x14-0x1F			0		-10
MIC PGA Gain	AVMICPGA	PGAM = 0x00			+20		aв
MIC PGA Gain Step Size					1		dB
Common-Mode Rejection Ratio	CMRR	$V_{IN} = 100 \text{mV}_{P-P}$ at 217Hz			50		dB
MIC Input Resistance	RIN_MIC	All gain settings, measured MICLN/MICRN	at	30	50		kΩ
MIC Input Bias Voltage				0.7	0.8	0.9	V
	Ē	$A_{VPRE} = 0dB, A_{VMICPGA} = V_{IN} = 1V_{P-P}, f = 1kHz$	0dB,		-75		dB
Iotal Harmonic Distortion + Noise	THD+N	AVPRE = $+30$ dB, AVMICPGA = 0dB, VIN = 31 mVP-P, f = 1kHz			-66		dB
		V _{AVDD} = 1.7V to 1.9V		60	95		dB
MIC Power-Supply Rejection	PSRR	VRIPPLE = 100mV at 1kHz, input referred			82		dB
Ralio		VRIPPLE = 100mV at 10kHz	, input referred		76		dB
MICROPHONE BIAS							·
MICBIAS Output Voltage	VMICBIAS	$I_{LOAD} = 1$ mA, $T_A = +25$ °C		1.5	1.55	1.6	V
Load Regulation		$I_{LOAD} = 1 mA$ to $2 mA$			0.2	10	mV
MICRIAS Line Ripple Rejection		VRIPPLE = 100mVP-P at 217	Hz		82		dB
	LNN	VRIPPLE = 100mVP-P at 10k	Hz		81		dB
MICBIAS Noise Voltage		A-weighted			9.5		μV _{RMS}
AUTOMATIC GAIN CONTROL							
AGC Hold Duration		AGCHLD[1:0] setting range	e, FREQ ≠ 0	50		400	ms
AGC Attack Time		AGCATK[1:0] setting range	e, FREQ ≠ 0	3		200	ms
AGC Release Time		AGCRLS[2:0] setting range	, FREQ ≠ 0	0.078		10	S
AGC Threshold Level		AGCSTH[3:0] setting range	e, FREQ ≠ 0	-3		-18	dB
NOISE GATE							
NG Attack and Release Time					0.5		S
NG Threshold Level				-72		-16	dB
Noise Gate Threshold Step Size					4		dB
NG Attenuation				0		12	dB
DIGITAL SIDETONE							
Sidetone Gain Adjust	DVST	2dB steps	-	-60		0	dB
Sidetone Phase Delay	PDI Y	MIC input to headphone output $f = 1 \text{ kHz}$ HP filter	8kHz		2.2		ms
		disabled	16kHz		1.1		

DIGITAL AUDIO INTERFACE ELECTRICAL CHARACTERISTICS

 $(V_{DVDD} = V_{DVDDIO} = 1.8V$, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BCLK Cycle Time	t BCLKS	Slave operation	75			ns
BCLK High Time	t BCLKH	Slave operation	30			ns
BCLK Low Time	t BCLKL	Slave operation	30			ns
BCLK or LRCLK Rise and Fall Time	t _R , t _F	Master operation		7		ns
SDIN or LRCLK to BCLK Rising Setup Time	tsu	ABCI = DBCI = 0	25			ns
SDIN or LRCLK to BCLK Falling Setup Time	tsu	ABCI = DBCI = 1	25			ns
SDIN or LRCLK to BCLK Rising Hold Time	thd	ABCI = DBCI = 0	0			ns
SDIN or LRCLK to BCLK Falling Hold Time	thd	ABCI = DBCI = 1	0			ns
SDOUT Delay Time from BCLK Rising Edge	tDLY	$ABCI = DBCI = 0, C_L = 30pF$	0		40	ns

I²C INTERFACE ELECTRICAL CHARACTERISTICS

 $(V_{DVDD} = V_{DVDDIO} = 1.8V$, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	ТҮР	MAX	UNITS
Serial-Clock Frequency	fscl		0		400	kHz
Bus Free Time Between STOP and START Conditions	^t BUF		1.3			μs
Hold Time (Repeated) START Condition	thd,sta		0.6			μs
SCL Pulse Width Low	tLOW		1.3			μs
SCL Pulse Width High	thigh		0.6			μs
Setup Time for a Repeated START Condition	tsu,sta		0.6			μs
Data Hold Time	thd,dat		0		900	ns
Data Setup Time	tsu,dat		100			ns
SDA and SCL Receiving Rise Time	t _R	C _B is in pF	20 + 0.10	Св	300	ns
SDA and SCL Receiving Fall Time	tF	C _B is in pF	20 + 0.10	CB	300	ns

I²C INTERFACE ELECTRICAL CHARACTERISTICS (continued)

 $(V_{DVDD} = V_{DVDDIO} = 1.8V$, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	ТҮР	MAX	UNITS
SDA Transmitting Fall Time	tF	C _B is in pF	20 + 0.1C	В	250	ns
Setup Time for STOP Condition	tsu,sto		0.6			μs
Bus Capacitance	CB				400	рF
Pulse Width of Suppressed Spike	tsp		0		50	ns
DIGITAL INPUTS (LRCLK, BCLK,	SDIN, MCL	<)				
Input Voltage High	VIH		0.7 x V _{DVDDIO}	1		V
Input Voltage Low	VIL			(× V _D	D.3 IVDDIO	V
MCLK Input Voltage High			1.4			V
MCLK Input Voltage Low					0.4	V
Input Leakage Current	I _{IH} , I _{IL}	$T_A = +25^{\circ}C$	-1		+1	μA
Input Capacitance				3		рF
DIGITAL INPUTS (SCL, SDA)						
Input Voltage High	VIH		0.7 x V _{DVDD}			V
Input Voltage Low	VIL			x	0.3 V _{DVDD}	V
Input Hysteresis				200		mV
Input Leakage Current	I _{IH} , I _{IL}	$T_A = +25^{\circ}C$	-1		+1	μΑ
Input Capacitance				3		рF
CMOS DIGITAL OUTPUTS (BCLK	K, LRCLK, SE	DOUT)				
Output Low Voltage	Vol	I _{OL} = 3mA			0.4	V
Output High Voltage	V _{OH}	I _{OL} = 3mA	V _{DVDDIO} - 0.4			V
OPEN-DRAIN DIGITAL OUTPUTS	(SDA, IRQ)	·				
Output High Leakage Current	Юн	$V_{OUT} = V_{DVDDIO}, T_A = +25^{\circ}C$	-1		+1	μA
Output Low Voltage	Vol	I _{OL} = 3mA			0.4	V

Note 2: All devices are 100% production tested at room temperature. All temperature limits are guaranteed by design.

Note 3: Supply current measurements taken with no applied signal at microphone inputs. A digital zero audio signal used for all digital serial audio inputs. Headphone outputs are loaded as stated in the global conditions.

Note 4: DAC performance is measured at headphone outputs.

Note 5: ADC, DAC, and headphone amplifier dynamic ranges are measured using the EIAJ method. -60dBV 1kHz input signal, A-weighted and normalized to 0dBFS.

Note 6: Notch for GSM filters occurs at 217Hz.

Typical Operating Characteristics

 $(V_{AVDD} = +1.8V, V_{DVDD} = V_{DVDDIO} = +1.8V, R_L = \infty$, headphone load (R_L) connected between OUTP and OUTN, $C_{REF} = 2.2\mu F$, $C_{PREG} = C_{REG} = 1\mu F$, $C_{MICBIAS} = 1\mu F$ AVMICPGA = 0dB, AVPRE = +20dB, f_{MCLK} = 13MHz, T_A = +25°C, unless otherwise noted.)



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Typical Operating Characteristics (continued)

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 $(V_{AVDD} = +1.8V, V_{DVDD} = V_{DVDDIO} = +1.8V, R_L = \infty$, headphone load (R_L) connected between OUTP and OUTN, $C_{REF} = 2.2\mu$ F, $C_{PREG} = C_{REG} = 1\mu$ F, $C_{MICBIAS} = 1\mu$ F AVMICPGA = 0dB, AVPRE = +20dB, f_{MCLK} = 13MHz, T_A = +25°C, unless otherwise noted.)



Typical Operating Characteristics (continued)

(V_{AVDD} = +1.8V, V_{DVDD} = V_{DVDDIO} = +1.8V, R_L = ∞, headphone load (R_L) connected between OUTP and OUTN, C_{REF} = 2.2µF, CPREG = CREG = 1µF, CMICBIAS = 1µF AVMICPGA = 0dB, AVPRE = +20dB, fMCLK = 13MHz, TA = +25°C, unless otherwise noted.)



0.001

10

20

30

MCLK FREQUENCY (MHz)

40

50

60

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50

60

40

-100

-110

-120

10

20

30

MCLK FREQUENCY (MHz)

f_{LRCLK} = 8kHz

0

-10

-20

-30

-40

-50

-60

-70

-80

-90

-100

-80

-60

INPUT AMPLITUDE (dBV)

-40

-20

OUTPUT AMPLITUDE (dBFS)

Pin Description

PIN	NAME	FUNCTION
1	MICBIAS	Microphone Bias. +1.55V microphone bias for internal and/or external microphone. An external resistor from 2.2k Ω to 470 Ω should be used to set the microphone current. Bypass to MICGND with a 1µF capacitor.
2	REG	Internal Bias. PREG/2 voltage reference. Bypass to AGND with a 1µF capacitor (+0.8V).
3	PREG	Positive Internal Regulated Supply. Bypass to AGND with a 1µF capacitor (+1.6V).
4	REF	Converter Reference (1.23V). Bypass to AGND with a 2.2µF capacitor.
5	AGND	Analog Ground
6	AVDD	Analog Power Supply. Bypass to AGND with 10µF and 0.1µF capacitors.
7	OUTP	Positive Headphone Output
8	OUTN	Negative Headphone Output
9	SDA	I ² C Serial-Data Input/Output
10	SCL	I ² C Serial-Data Clock
11	DVDDIO	Digital Interface Power Supply. Supply for digital audio interface. Bypass to DGND with a 1µF capacitor.
12	DGND	Digital Ground
13	DVDD	Digital Core Power Supply. Bypass to DGND with a 1µF capacitor.
14	MCLK	Master Clock Input
15	SDOUT	Serial Audio Interface ADC Data Output
16	SDIN	Serial Audio Interface DAC Data Input
17	LRCLK	Serial Audio Interface Left/Right Clock
18	BCLK	Serial Audio Interface Bit Clock
19	ĪRQ	Interrupt Request. $\overline{\text{IRQ}}$ is an active-low open drain output. Pull up to DVDDIO with a 10k Ω resistor.
20	MICRN	Negative Right Microphone Input. AC-couple to low-side of microphone or connect to negative signal. AC-couple to ground for single-ended operation.
21	MICRP	Positive Right Microphone Input. AC-couple to high-side of microphone or connect to positive signal. AC-couple the signal for single-ended operation.
22	MICLN	Negative Left Microphone Input. AC-couple to low-side of microphone or connect to negative signal. AC-couple to ground for single-ended operation.
23	MICLP	Positive Left Microphone Input. AC-couple to high-side of microphone or connect to positive signal. AC-couple the signal for single-ended operation.
24	MICGND	MICBIAS Ground. Connect to AGND.
_	EP	Exposed Pad. Connect to AGND.

Detailed Description

The MAX9860 low-power, voiceband, mono audio codec provides a complete audio solution for wireless voice headsets and other mono audio devices.

The mono playback path accepts digital audio over a flexible digital audio interface compatible with I²S, TDM, and left-justified audio signals. An oversampling sigmadelta DAC converts an incoming digital data stream to analog audio and outputs through the mono bridge-tied load headphone amplifier.

The stereo record path has two microphone inputs with selectable gain. The microphones are powered by an integrated microphone bias. An oversampling sigmadelta ADC converts the microphone signals and outputs the digital bit stream over the digital audio interface.

The record path includes automatic gain control (AGC) to optimize the signal level and a noise gate to reduce idle noise. The automatic gain control monitors the outputs of the ADC and makes constant adjustments to the input gain to reduce the dynamic range of the incoming microphone signal by up to 20dB. The noise gate corrects for the increase in noise typically associated with AGC by lowering the gain when there is no audio signal.

Integrated digital filtering provides a range of notch and highpass filters for both the playback and record paths

to limit undesirable low-frequency signals and GSM transmission noise. The digital filtering provides attenuation of out-of-band energy by up to 76dB, eliminating audible aliasing. A digital sidetone function allows audio from the record path to be summed into the playback path after digital filtering.

The MAX9860's flexible clock circuitry utilizes a programmable clock divider and a digital PLL to allow the DAC and ADC to operate at maximum dynamic range for all combinations of master clock (MCLK) and sample rate (LRCLK). Any master clock between 10MHz to 60MHz is supported as are all sample rates from 8kHz to 48kHz. Master and slave mode are supported for maximum flexibility.

I²C Registers

The MAX9860 audio codec is completely controlled through software using an I²C interface. The power-on default setting is software shutdown, requiring that the internal registers be programmed to activate the device. See Table 1 for the device's complete register map.

I²C Slave Address

The MAX9860 responds to the slave address 0x20 for all write commands and 0x21 for all read operations.

Table 1. I²C Register Map

REGISTER	B7	B6	B5	E	B4	B3	B2	В	1	B0	REGISTER ADDRESS	POR	R/W
STATUS/INTERRUPT													
Interrupt Status	CLD	SLD	ULK		0	0	0	0)	0	0x00		R
Microphone NG/AGC Readback		NG					AG	С			0x01	_	R
Interrupt Enable	ICLD	ISLD	IULK	<u> </u>	0	0	0	0)	0	0x02	0x00	R/W
CLOCK CONTROL													
System Clock	0	0	F	PSCLK	<	0	FI	REQ		16KHZ	0x03	0x00	R/W
Stereo Audio Clock Control High	PLL					NHI					0x04	0x00	R/W
Stereo Audio Clock Control Low					۱	NLO					0x05	0x00	R/W
DIGITAL AUDIO INTE	RACE												
Interface	MAS	WCI	DB	CII	DDLY	HIZ	TD	М	0	0	0x06	0x00	R/W
Interface	0	0	AB	CI /	ADLY	ST			BSE	L	0x07	0x00	R/W
DIGITAL FILTERING													
Voice Filter		А	VFLT			DVFLT				0x08	0x00	R/W	
DIGITAL LEVEL CON	TROL												
DAC Attenuation					[DVA					0x09	0x00	R/W
ADC Output Levels		A	DCRL					ADC	LL		0x0A	0x00	R/W
DAC Gain and	0		DVG			DVST				0x0B	0x00	R/W	
MICROPHONE LEVEL								^ N /			0,400	0,00	
	0		PAIVI				PG	AIVI			UXUC	000	H/VV
RESERVED	0			0	0	0			0	0		0.4	0
						UXUD	UXU	,0					
Microphone ACC					۸۵	CATK		1		OVOE	0,00		
	AGUSHC AGCHLS					AGCATK AGCHLD			AGCHLD	UXUE	0,00		
Noise Gate, Microphone AGC	ANTH					AGCTH			0x0F	0x00	R/W		
POWER MANAGEME	Т												
System Shutdown	SHDN	0	0	0)	DACEN	0	ADC	LEN	ADCREN	0x10	0x00	R/W

Status/Interrupt

Status registers 0x00 and 0x01 are read-only registers that report the status of various device functions. The status register bits are cleared upon a read operation of the status register and are set the next time the event occurs. Register 0x02 determines whether or not the status flags in register 0x00 simultaneously sets IRQ high.

Table 2. Status/Interrupt Registers

REGISTER ADDRESS	B7	B6	B5	B4	B3	B2	B1	B0
0x00	CLD	SLD	ULK	0	0	0	0	0
0x01	0x01 NG AGC							
0x02	ICLD	ISLD	IULK	0	0	0	0	0

BITS	FUNCTION							
CLD	Clip Detect Flag. Indicates that a signal has become clipped in the ADC or DAC digital signal paths. CLD also indicates that the AGC function, when enabled, has set the microphone PGA to 0dB and no further gain reduction is possible.							
SLD	Slew Level Detect Flag. When volume or gain changes are made, the slewing circuitry smoothly steps through all intermediate settings. When SLD is set high, all slewing has completed and the volume or gain is at its final value.							
ULK	Digital PLL Unlock Flag. Indicates that the digital audio PLL for the ADC or DAC has become unlocked and digital signal data is not reliable. When beginning operation in master mode, this flag goes high and can be cleared by reading the status register.							
	Noise Gate Attenuation. When the noise gate is enabled these bits indicate the current noise gate attenuation.							
	Code	Attenuation						
	000	0dB						
	001	1dB						
NG	010	2dB						
NG	011	3dB						
	100	6dB						
	101	8dB						
	110	10dB						
	111	12dB						
AGC	AGC Gain. When the AGC is enabled these bits indicate the AGC control indicated by these bits correspond to the levels defined for the PGAM b	blled level to the MIC preamp. The levels its described in register 0x0C.						

MAX9860

16-Bit Mono Audio Voice Codec

Clock Control

The MAX9860 can work with a master clock (MCLK) supplied from any system clock within the range of 10MHz to 60MHz. Internally, the MAX9860 requires a 10MHz to 20MHz clock so a prescaler divides by 1, 2, or 4 to create the internal clock (PCLK). PCLK is used to clock all portions of the MAX9860.

The MAX9860 is capable of supporting any sample rate from 8kHz to 48kHz, including all common sample rates (8kHz, 16kHz, 24kHz, 32kHz, 44.1kHz, 48kHz). To accommodate a wide range of system architectures, the MAX9860 supports three main clocking modes:

Normal Mode: This mode uses a 15-bit clock divider coefficient to set the sample rate relative to the

prescaled MCLK input (PCLK). This allows high flexibility in both the MCLK and LRCLK frequencies and can be used in either master or slave mode.

Exact Integer Mode: Common MCLK frequencies (12MHz, 13MHz, and 19.2MHz) can be programmed to operate in exact integer mode for both 8kHz and 16kHz sample rates. In these modes, the MCLK and LRCLK rates are selected by using the FREQ and 16KHZ bits instead of the NHI, NLO, and PLL control bits.

PLL Mode: When operating in slave mode, a PLL can be enabled to lock onto externally generated LRCLK signals that are asynchronously related to PCLK.

Table 3. Clock Control Registers

REGISTER ADDRESS	B7	B6	B5	B4	B3	B2	B1	B0
0x03	0	0	0 PSCLK		0	FREQ		16KHZ
0x04	PLL	NHI						
0x05				NI	_0			

BITS	FUNCTION
	MCLK Prescaler
	Divides MCLK down to generate a PCLK between 10MHz and 20MHz.
PSCLK[1:0]	00 = Disable clock for low-power shutdown.
	01 = Select if MCLK is between 10MHz and 20MHz.
	10 = Select if MCLK is between 20MHz and 40MHz.
	11 = Select if MCLK is greater than 40MHz.
	Integer Clock Mode
	Enables exact integer mode for three predefined PCLK frequencies. Exact integer mode is normally
	Interfued for master mode, but can be enabled in slave mode in the externally supplied LNOLN exactly
	matches the frequency specified in each mode.
FREQ[1:0]	00 = Normal operation (configure clocking with the PLL, NHI, and NLO bits).
	01 = Select when PCLK is 12MHz (LRCLK = PCLK/1500 or PCLK/750).
	10 = Select when PCLK is 13MHz (LRCLK = PCLK/1625 or PCLK/812.5).
	11 = Select when PCLK is 19.2MHz (LRCLK = PCLK/2400 or PCLK/1200).
	When FREQ \neq 00, the PLL, NHI, and NLO bits are unused.
	16kHz Mode
	When FREQ ≠ 00:
	0 = LRCLK is exactly 8kHz.
16KHZ	1 = LHCLK is exactly 16kHz.
	When $FREQ = 00$, 16KHZ is used to set the AGC clock rate:
	$0 = Use when LRCLK \leq 24kHz.$
	1 = Use when LRCLK > 24kHz.

Table 3. Clock Control Registers (continued)

BITS	FUNCTION
	PLL Enable 0 = (Valid for slave and master mode)—The frequency of LRCLK is set by the NHI and NLO divider bits. Set PLL = 0 in slave mode only if the externally generated LRCLK can be exactly selected using the LRCLK divider.
PLL	 1 = (Valid for slave mode only)—Used when the audio master generates an LRCLK not selectable using the LRCLK divider. A digital PLL locks on to the externally supplied LRCLK signal regardless of the MCLK frequency.
	Rapid Lock Mode To enable rapid lock mode set NHI and NLO to the nearest desired ratio and set NLO[0] = 1 (Register 0x05, bit 0) before setting the PLL mode bit.
NHI and NLO	LRCLK Divider NHI and NLO control a 15-bit clock divider (N). When the PLL = 0 and FREQ = 00, the frequency of LRCLK is determined by the clock divider. See Table 4 for common N values.
	$ N = (65,536 \times 96 \times f_{LRCLK})/f_{PCLK} $ $ f_{LRCLK} = LRCLK frequency $ $ f_{PCLK} = prescaled MCLK internal clock frequency (PCLK) $

Table 4. Common N Values

	LRCLK (kHz)								
MCLK (MHz)	PSCLK	8	16	32	44.1	48			
11.2896	01	116A	22D4	45A9	6000	687D			
12	01	1062	20C5	4189	5A51	624E			
12.288	01	1000	2000	4000	5833	6000			
13	01	F20	1E3F	3C7F	535F	5ABE			
19.2	01	A3D	147B	28F6	3873	3D71			
24	10	1062	20C5	4189	5A51	624E			
26	10	F20	1E3F	3C7F	535F	5ABE			
27	10	E90	1D21	3A41	5048	5762			

Note: Values in bold italics are exact integers that provide maximum full-scale performance.

MAX9860

16-Bit Mono Audio Voice Codec

Digital Audio Interface

The MAX9860's digital audio interface supports a wide range of operating modes to ensure maximum compatibility. See Figures 1 through 4 for timing diagrams. In master mode, the MAX9860 outputs LRCLK and BCLK, while in slave mode, they are inputs. When operating in master mode, BCLK can be configured in a number of ways to ensure compatibility with other audio devices.

Table 5. Digital Audio Interface Registers

REGISTER ADDRESS	B7	B6	B5	B4	B3	B2	B1	B0
0x06	MAS	WCI	DBCI	DDLY	HIZ	TDM	0	0
0x07	0	0	ABCI	ADLY	ST	BSEL		

BITS	FUNCTION
MAS	Master Mode 0 = The MAX9860 operates in slave mode with LRCLK and BCLK configured as inputs. 1 = The MAX9860 operates in master mode with LRCLK and BCLK configured as outputs.
WCI	LRCLK Invert 0 = Left-channel data is input and output while LRCLK is low. 1 = Right-channel data is input and output while LRCLK is low. WCl is ignored when TDM = 1
DBCI	 DAC BCLK Invert (must be set to ABCI) In master and slave mode: 0 = SDIN is latched into the part on the rising edge of BCLK. 1 = SDIN is latched into the part on the falling edge of BCLK. In master mode: 0 = LRCLK changes state following the rising edge of BCLK. 1 = LRCLK changes state following the falling edge of BCLK.
DDLY	 DAC Delay Mode 0 = SDIN data is latched on the first BCLK edge following an LRCLK edge. 1 = SDIN data is assumed to be delayed one BCLK cycle so that it is latched on the 2nd BCLK edge following an LRCLK edge (I²S-compatible mode). DDLY is ignored when TDM = 1.
HIZ	 SDOUT High-Impedance Mode 0 = SDOUT is set either high or low after all data bits have been transferred out of the part. 1 = SDOUT goes to a high-impedance state after all data bits have been transferred out of the part, allowing SDOUT to be shared by other devices. Use HIZ only when TDM = 1.
TDM	 TDM Mode Select 0 = LRCLK signal polarity indicates left and right audio. 1 = LRCLK is a framing pulse which transitions polarity to indicate the start of a frame of audio data consisting of multiple channels. When operating in TDM mode the left channel is output immediately following the frame sync pulse. If right-channel data is being transmitted, the 2nd channel of data immediately follows the 1st channel data.
ABCI	ADC BCLK Invert (must be set to DBCI) 0 = SDOUT is valid on the rising edge of BCLK and transitions immediately after the rising edge. 1 = SDOUT is valid on the falling edge of BCLK and transitions immediately after the falling edge.

Table 5. Digital Audio Interface Registers (continued)

BITS	FUNCTION
ADLY	 ADC Delay Mode 0 = SDOUT data is valid on the first BCLK edge following an LRCLK edge. 1 = SDOUT data is delayed one BCLK cycle so that it is valid on the 2nd BCLK edge following an LRCLK edge (I²S-compatible mode). ADLY is ignored when TDM = 1.
ST	 Stereo Enable 0 = The interface transmits and receives only one channel of data. If right record path is enabled, no data from this channel is transmitted. 1 = The interface operates in stereo. The left and right incoming data are summed to mono and then routed to the DAC. The summed data is divided by 2 to prevent overload. Both the left and right record signals are transmitted.
BSEL	BCLK Select Configures BCLK when operating in master mode. BSEL has no effect in slave mode. Set BSEL = 010, unless sharing the bus with multiple devices. 000 = Off 001 = 64x LRCLK (192x internal clock divided by 3) 010 = 48x LRCLK (192x internal clock divided by 4) 011 = Reserved for future use. 100 = PCLK/2 101 = PCLK/4 110 = PCLK/8 111 = PCLK/16

MAX9860

16-Bit Mono Audio Voice Codec



Figure 1. Digital Audio Interface Audio Master Mode Examples



Figure 2. Digital Audio Interface Voice Master Mode Examples

MAX9860

16-Bit Mono Audio Voice Codec



Figure 3. Digital Audio Interface Audio Slave Mode Examples



Figure 4. Digital Audio Interface Voice Slave Mode Examples

Digital Filtering The MAX9860 incorporates selecable highpass and notch filters for both the playback and record paths. Each filter is valid for a specific sample rate.

Table 6. Digital Filter Registers

REGISTER ADDRESS	B7	B6	B5	B4	B3	B2	B1	B0
0x08	AVFLT					DV	FLT	

BITS	FUNCTION
AVFLT	ADC Voice Filter Frequency Select. See Table 7.
DVFLT	DAC Voice Filter Frequency Select. See Table 7.

Table 7. Digital Filters

CODE	FILTER TYPE	SAMPLE RATE	DESCRIPTION
0x0	—		Disabled
0x1	Elliptical	16kHz	Elliptical highpass with 217Hz notch
0x2	Butterworth	16kHz	500Hz Butterworth highpass
0x3	Elliptical	8kHz	Elliptical highpass with 217Hz notch
0x4	Butterworth	8kHz	500Hz Butterworth highpass
0x5	Butterworth	48kHz	200Hz Butterworth highpass
0x6 to 0xF	—	_	Reserved

Digital Level Control

The MAX9860 includes digital gain adjustment for the playback and record paths. Independent gain

adjustment is provided for the two record channels. Sidetone gain adjustment is also provided to set the sidetone level relative to the playback level.

Table 8. Digital Level Control Registers

REGISTER ADDRESS	B7	B6	B5	B4	B3	B2	B1	B0
0x09		DVA						
0x0A		ADCRL ADCLL						
0x0B	0	0 DVG DVST						

BITS			FUNCT	ΓΙΟΝ		
	DAC Level Adjus	t				
	Adjusts the digita	al audio level befo	ore being converted	by the DAC. The I	east significant b	oit of DVA is
	always 0.		I			
	CODE	GAIN	CODE	GAIN	CODE	GAIN
	0x00	+3	0x40	-29	0x80	-61
	0x02	+2	0x42	-30	0x82	-62
	0x04	+1	0x44	-31	0x84	-63
	0x06	0	0x46	-32	0x86	-64
	0x08	-1	0x48	-33	0x88	-65
	0x0A	-2	0x4A	-34	0x8A	-66
	0x0C	-3	0x4C	-35	0x8C	-67
	0x0E	-4	0x4E	-36	0x8E	-68
	0x10	-5	0x50	-37	0x90	-69
	0x12	-6	0x52	-38	0x92	-70
	0x14	-7	0x54	-39	0x94	-71
	0x16	-8	0x56	-40	0x96	-72
	0x18	-9	0x58	-41	0x98	-73
	0x1A	-10	0x5A	-42	0x9A	-74
	0x1C	-11	0x5C	-43	0x9C	-75
	0x1E	-12	0x5E	-44	0x9E	-76
	0x20	-13	0x60	-45	0xA0	-77
	0x22	-14	0x62	-46	0xA2	-78
	0x24	-15	0x64	-47	0xA4	-79
	0x26	-16	0x66	-48	0xA6	-80
	0x28	-17	0x68	-49	0xA8	-81
	0x2A	-18	0x6A	-50	0xAA	-82
	0x2C	-19	0x6C	-51	0xAC	-83
	0x2E	-20	0x6E	-52	0xAE	-84
	0x30	-21	0x70	-53	0xB0	-85
	0x32	-22	0x72	-54	0xB2	-86
	0x34	-23	0x74	-55	0xB4	-87
	0x36	-24	0x76	-56	0xB6	-88
	0x38	-25	0x78	-57	0xB8	-89
	0x3A	-26	0x7A	-58	0xBA	-90
	0x3C	-27	0x7C	-59	≥ 0xBC	MUTE
	0x3E	-28	0x7E	-60	—	

Table 8. Digital Level Control Registers (continued)

BITS			FUNCTION		
	Left and Right AD	C Output Level			
	Adjusts the digital a	udio level output by	the ADCs.		
	CODE	GAIN	_		
	0x0	+3	_		
	0x1	+2	_		
	0x2	+1			
	0x3	0	_		
	0x4	-1			
	0x5	-2			
ADCRL/ADCLL	0x6	-3	_		
	0x7	-4			
	0x8	-5			
	0x9	-6			
	0xA	-7			
	0xB	-8			
	0xC	-8			
	0xD	-10			
	0xE	-11			
	0xF	-12			
	DAC Gain				
	The gain set by DV	G adds to the level s	set by DVA.		
	CODE	GAIN			
DVG	00	0			
	01	+6	_		
	10	+12			
	11	+18			
	Sidetone				
	Sets the level of left	ADC output mixed	into the DAC.	-	1
	CODE	GAIN	CODE	GAIN	_
	0x00	Disabled	0x10	-30	4
	0x01	0	0x11	-32	4
	0x02	-2	0x12	-34	
	0x03	-4	0x13	-36	_
	0x04	-6	0x14	-38	
	0x05	-8	0x15	-40	4
DVST	0x06	-10	0x16	-42	
	0x07	-12	0x17	-44	
	0x08	-14	0x18	-46	
	0x09	-16	0x19	-48	4
	0x0A	-18	0x1A	-50	4
	0x0B	-20	0x1B	-52	4
	0x0C	-22	0x1C	-54	4
	0x0D	-24	0x1D	-56	4
	0x0E	-26	0x1E	-58	4
	0x0F	-28	0x1F	-60	

Microphone Inputs

The MAX9860 provides two differential microphone inputs and a low-noise 1.55V microphone bias for powering the microphones. In typical applications, the left microphone is used to record a voice signal and the right microphone is used to record a background noise signal. In applications that require only one microphone, use the left microphone input and disable the right ADC. The microphone signals are amplified by two stages of gain and then routed to the ADCs. The first stage offers selectable 0dB, 20dB, or 30dB settings. The second stage is a programmable gain amplifier (PGA) adjustable from 0dB to 20dB in 1dB steps. Zero-crossing detection is included on the PGA to minimize zipper noise while making gain changes. See Figure 5 for a detailed diagram of the microphone input structure.



Figure 5. Microphone Input Block Diagram

Table 9. Microphone Input Register

REGISTER ADDRESS	B7	B6	B5	B4	B3	B2	B1	B0
0x0C	0	PA	PAM PGAM					

BITS	FUNCTION							
	Left and Right Microphone Preamp Gain							
	CODE	GAIN (dB)						
	00	Disabled						
PAM	01	0						
	10	+20						
	11	+30						
	Note: Selecting 00	disables the microph	none inputs and mici	ophone bias automat	tically.			
	Left and Right Microphone PGA							
	CODE	GAIN (dB)	CODE	GAIN (dB)				
	0x00	+20	0x0B	+9				
	0x01	+19	0x0C	+8				
	0x02	+18	0x0D	+7				
	0x03	+17	0x0E	+6				
PGAM	0x04	+16	0x0F	+5				
	0x05	+15	0x10	+4				
	0x06	+14	0x11	+3				
	0x07	+13	0x12	+2				
	0x08	+12	0x13	+1				
	0x09	+11	≥0x14	0				
	0x0A	+10	—	—				
	Note: When AGC i	s enabled, the AGC c	controller overrides th	nese settings.				

Automatic Gain Control (AGC) and Noise Gate

The MAX9860 includes AGC on both microphone inputs. AGC is enabled by setting the hold time through AGCHLD. AGC dynamically controls the analog PGA microphone input gain to hold the level constant over a 20dB input range, enhancing the voice path operation for various use conditions. When AGC is enabled, it monitors the signal level at the output of the ADC and then makes gain adjustments by controlling the analog microphone PGA. When AGC is enabled, PGAM is not user programmable. Since AGC increases the level of all signals below a user-defined threshold, the noise floor effectively is increased by 20dB. To counteract this, a noise gate is included to reduce the gain at low levels. Unlike typical noise gates that completely silence the output below a threshold, the noise gate in the MAX9860 reduces the gain for signals below the defined level. As the signal level becomes further below the threshold, the gain is further reduced. The Automatic Gain Control Thresholds and Noise Gate Thresholds graphs in the *Typical Operating Characteristics* show the resulting steady-state transfer curves when AGC and the noise gate are enabled.

Table 10. AGC and Noise Gate Registers

REGISTER ADDRESS	B7	B6	B5	B4	B3	B2	B1	B0
0x0E	AGCSRC		AGCRLS			ATK	AGCHLD	
0x0F		ANTH				AG	СТН	

BITS	FUNCTION							
	AGC/Noise Gate S	ignal Source Select						
AGCSRC	0 = The left ADC ou	0 = The left ADC output is used by the AGC and noise gate.						
	1 = The sum of the	1 = The sum of the left and right ADC outputs is used by the AGC and noise gate.						
	AGC Release Time	AGC Release Time						
	Time taken by the A	GC circuit to increas	e the gain from minimum to maximum.					
	CODE	TIME						
	000	78ms						
	001	156ms						
AGCRLS	010	312ms						
	011	625ms						
	100	1.25s						
	101	2.5s						
	110	5s						
	111	10s						
	AGC Attack Time							
	The time constant o	f the AGC gain reduc	ction curve.					
	CODE	TIME (ms)						
AGCATK	00	3						
	01	12						
	10	50						
	11	200						
	AGC Hold Time							
	Time the AGC circu	it waits before begini	ning to increase gain when a signal below the threshold is					
	detected.							
	CODE	TIME (ms)						
	00	AGC disabled						
	01	50						
	10	100						
	11	400						

Table 10. AGC and Noise Gate Registers (continued)

BITS			FUNCTION					
	Noise Gate Thresh The signal level at v	old which the noise gate	begins reducing the	gain. When the signa	al level is above the			
	decreases the gain	by 1dB for every 2dl	dently from AGC. Wh	the threshold.	PGAM must be set to			
	+20dB (indicating a small signal is present) for the noise gate to attenuate. For microphone signals, use the noise gate and AGC simultaneously with ANTH set between -16dB							
	and -28dB.		ANTH[2.0]					
		LEVEL (UBFS)			T T			
	0x0	Disabled	0x8	-44				
	UXI	-72	0x9	-40				
	0x2	-68	UXA	-36				
	0x3	-64	0xB	-32				
	0x4	-60	0xC	-28				
	0x5	-56	0xD	-24				
	0x6	-52	0xE	-20				
	0x7	-48	0xF	-16				
	AGC Signal Thresh The target output si gain. The signal lev	h old gnal level. When the el is measured after <i>i</i>	signal level is below ADCRL and ADCLL :	the threshold, the A0 are applied to the AD	GC increases the OC output.			
	ANTH[3:0]	LEVEL (dBFS)	ANTH[3:0]	LEVEL (dBFS)				
	0x0	-3	0x8	-11				
	0x1	-4	0x9	-12				
AGCTH	0x2	-5	0xA	-13				
	0x3	-6	0xB	-14				
	0x4	-7	0xC	-15				
	0x5	-8	0xD	-16				
	0x6	-9	0xE	-17				
	0x7	-10	0xF	-18				

Power Management

The MAX9860 includes complete power management control to minimize power usage. The DAC and both

ADCs can be independently enabled so that only the required circuitry is active.

Table 11. Power Management Register

REGISTER ADDRESS	B7	B6	B5	B4	B3	B2	B1	B0		
0x10	SHDN	0	0	0	DACEN	0	ADCLEN	ADCREN		
BITS		FUNCTION								
SHDN	Active-Low 9 0 = MAX9860 1 = MAX9860 When SHDN	Active-Low Software Shutdown) = MAX9860 is in full shutdown. = MAX9860 is powered on. When SHDN = 0. All register settings are preserved and the I ² C interface remains active.								
DACEN	DAC Enable 0 = DAC disa 1 = DAC ena	DAC Enable 0 = DAC disabled. 1 = DAC enabled.								
ADCLEN/ADCREN	ADC Left/Right Enable 0 = Left/right ADC disabled. 1 = Left/right ADC enabled. The left ADC must be enabled when using the right ADC.									

Revision Code

The MAX9860 includes a revision code to allow easy identification of the device revision. The current revision code is 0x40.

Table 12. Revision Code Register

ADDR	B7	B6	B5	B4	B3	B2	B1	B0
0xFF				RI	ΞV			

I²C Serial Interface

The MAX9860 features an I²C/SMBus[™]-compatible, 2-wire serial interface consisting of a serial-data line (SDA) and a serial-clock line (SCL). SDA and SCL facilitate communication between the MAX9860 and the master at clock rates up to 400kHz. Figure 6 shows the 2-wire interface timing diagram. The master generates SCL and initiates data transfer on the bus. The master device writes data to the MAX9860 by transmitting the proper slave address followed by the register address and then the data word. Each transmit sequence is framed by a START (S) or REPEATED START (Sr) condition and a STOP (P) condition. Each word transmitted to the MAX9860 is 8 bits long and is followed by an acknowledge clock pulse. A master reading data from the MAX9860 transmits the proper slave address followed by a series of nine SCL pulses. The MAX9860

transmits data on SDA in sync with the master-generated SCL pulses. The master acknowledges receipt of each byte of data. Each read sequence is framed by a START or REPEATED START condition, a not acknowledge, and a STOP condition. SDA operates as both an input and an open-drain output. A pullup resistor, typically greater than 500 Ω , is required on SDA. SCL operates only as an input. A pullup resistor, typically greater than 500 Ω , is required on SCL if there are multiple masters on the bus, or if the single master has an opendrain SCL output. Series resistors in line with SDA and SCL are optional. Series resistors protect the digital inputs of the MAX9860 from high voltage spikes on the bus lines, and minimize crosstalk and undershoot of the bus signals.



Figure 6. 2-Wire Interface Timing Diagram

Bit Transfer

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are control signals (see the *START and STOP Conditions* section).

START and STOP Conditions

SDA and SCL idle high when the bus is not in use. A master initiates communication by issuing a START (S) condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP (P) condition is a low-tohigh transition on SDA while SCL is high (Figure 7). A START condition from the master signals the beginning of a transmission to the MAX9860. The master terminates transmission, and frees the bus, by issuing a STOP condition. The bus remains active if a REPEATED START (Sr) condition is generated instead of a STOP condition.

Early STOP Conditions

The MAX9860 recognizes a STOP condition at any point during data transmission except if the STOP condition occurs in the same high pulse as a START condition. For proper operation, do not send a STOP condition during the same SCL high pulse as the START condition.

Slave Address

The slave address is defined as the seven most significant bits (MSBs) followed by the read/write bit. For the MAX9860, the seven most significant bits are 0010000. Setting the read/write bit to 1 (slave address = 0x21) configures the MAX9860 for read mode. Setting the read/write bit to 0 (slave address = 0x20) configures the MAX9860 for write mode. The address is the first byte of information sent to the MAX9860 after the START condition.

Acknowledge

The acknowledge bit (ACK) is a clocked 9th bit that the MAX9860 uses to handshake receipt each byte of data when in write mode (see Figure 8). The MAX9860 pulls down SDA during the entire master-generated 9th clock pulse if the previous byte is successfully received. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master retries communication. The master pulls down SDA during the 9th clock cycle to acknowledge receipt of data when the MAX9860 is in read mode. An acknowledge is sent by the master after each read byte to allow data transfer to continue. A not acknowledge is sent when the master reads the final byte of data from the MAX9860, followed by a STOP condition.

Write Data Format

A write to the MAX9860 includes transmission of a START condition, the slave address with the R/W bit set to 0, one byte of data to configure the internal register address pointer, one or more bytes of data, and a STOP condition. Figure 9 illustrates the proper frame format for writing one byte of data to the MAX9860. Figure 10 illustrates the frame format for writing n bytes of data to the MAX9860.

The slave address with the R/\overline{W} bit set to 0 indicates that the master intends to write data to the MAX9860. The MAX9860 acknowledges receipt of the address byte during the master-generated 9th SCL pulse.

The second byte transmitted from the master configures the MAX9860's internal register address pointer. The pointer tells the MAX9860 where to write the next byte of data. An acknowledge pulse is sent by the MAX9860 upon receipt of the address pointer data.



Figure 7. START (S), STOP (P), and REPEATED START (Sr) Conditions



Figure 8. Acknowledge



Figure 9. Writing One Byte of Data to the MAX9860

The third byte sent to the MAX9860 contains the data that is written to the chosen register. An acknowledge pulse from the MAX9860 signals receipt of the data byte. The address pointer autoincrements to the next register address after each received data byte. This autoincrement feature allows a master to write to sequential registers within one continuous frame. Figure 10 illustrates how to write to multiple registers with one frame. The master signals the end of transmission by issuing a STOP condition. Register addresses greater than 0x10 are reserved. Do not write to these addresses.

Read Data Format

Send the slave address with the R/W bit set to 1 to initiate a read operation. The MAX9860 acknowledges receipt of its slave address by pulling SDA low during the 9th SCL clock pulse. A START command followed by a read command resets the address pointer to register 0x00.

The first byte transmitted from the MAX9860 is the contents of register 0x00. Transmitted data is valid on the rising edge of SCL. The address pointer autoincrements after each read data byte. This autoincrement







Figure 12. Reading N Bytes of Data from the MAX9860

feature allows all registers to be read sequentially within one continuous frame. A STOP (P) condition can be issued after any number of read data bytes. If a STOP condition is issued followed by another read operation, the first data byte to be read is from register 0x00.

The address pointer can be preset to a specific register before a read command is issued. The master presets the address pointer by first sending the MAX9860's slave address with the R/W bit set to 0 followed by the register address. A REPEATED START (Sr) condition is then sent followed by the slave address with the R/W bit set to 1. The MAX9860 then transmits the contents of the specified register. The address pointer autoincrements after transmitting the first byte.

The master acknowledges receipt of each read byte during the acknowledge clock pulse. The master must acknowledge all correctly received bytes except the last byte. The final byte must be followed by a not acknowledge from the master and then a STOP condition. Figure 11 illustrates the frame format for reading one byte from the MAX9860. Figure 12 illustrates the frame format for reading multiple bytes from the MAX9860.



Pin Configuration

Route microphone signals from the microphone to the MAX9860 as a differential pair, ensuring that the positive and negative signals follow the same path as closely as possible with equal trace length. When using single-ended microphones or other single-ended audio sources, AC ground the negative microphone input signal as near to the audio source as possible and then treat the positive and negative traces as differential pairs.

The MAX9860 thin QFN package features an exposed thermal pad on its underside. This pad lowers the package's thermal resistance by providing a direct heat conduction path from the die to the PCB. Connect the exposed thermal pad to AGND.

An evaluation kit (EV kit) is available to provide an example layout for the MAX9860. The EV kit allows quick setup of the MAX9860 and includes easy-to-use software allowing all internal registers to be controlled.

Applications Information

Proper layout and grounding are essential for optimum performance. When designing a PCB for the MAX9860, partition the circuitry so that the analog sections of the MAX9860 are separated from the digital sections. This ensures that the analog audio traces do not need to be routed near digital traces.

Use a large continuous ground plane on a dedicated layer of the PCB to minimize loop areas. Connect AGND, DGND, and MICGND directly to the ground plane using the shortest trace length possible. Proper grounding improves audio performance, minimizes crosstalk between channels, and prevents any digital noise from coupling into the analog audio signal.

Ground the bypass capacitors on REG, PREG, and REF directly to the ground plane with minimum trace length. Also be sure to minimize the path length to AGND and MICGND. Bypass AVDD directly to AGND. Bypass MICBIAS directly to MICGND.

Connect all digital I/O termination to the ground plane with minimum path length to DGND. Bypass DVDD and DVDDIO directly to DGND.



Functional Diagram/Typical Operating Circuit

Package Information

For the latest package outline information and land patterns (footprints), go to <u>www.maximintegrated.com/packages</u>. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE	PACKAGE	OUTLINE NO.	LAND
TYPE	CODE		PATTERN NO.
24 TQFN-EP	T2444+4	<u>21-0139</u>	<u>90-0022</u>

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/08	Initial release	—
1	9/09	Corrected error in Table 11	32
2	2/12	Removed V _{OS} typical spec and updated max spec	5



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38

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