General Description

The MAX20317 is an I²C controllable, universal 3.5mmØ accessory management IC. The device provides a universal jack interface solution, as well as a compact solution for the power management and interface control of a powered accessory, such as an active noise cancelling (ANC) headset.

The MAX20317 automatically measures headset impedance with a high precision, triple current source 8 bit ADC. After impedance detection, the device also detects when a headset is in a CTIA or OMTP configuration and automatically configures the SLEEVE and RING2 terminals to correctly connect the microphone and ground lines.

When a boost supply is applied, the MAX20317 can detect the presence of an ANC headset. When the ANC headset is detected and enabled, a button-press monitoring circuit activates and flags button presses by detecting the voltage drop across a sense resistor.

The MAX20317 provides a power line communication tool to a headset to exchange the data with the host device.

The MAX20317 has the two separate ground sense inputs from the SLEEVE and RING2 terminals of the connector to provide a high ground isolation to the audio codec.

The MAX20317 is available in a space-saving, 20-bump, 0.4mm pitch, 1.65mm x 2.05mm wafer-level package (WLP) and operates over the -40°C to +85°C extended temperature range.

Applications

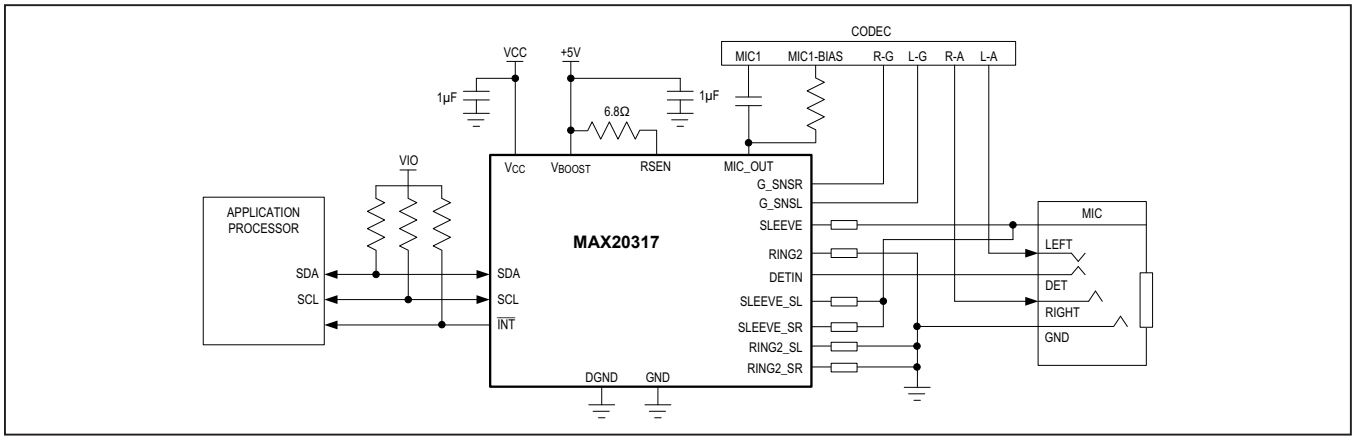
- Smart Phones
- Phablet
- Tablet PCs
- Notebook PCs

Benefits and Features

- Allows Wide Range of Applications by Supporting Universal 3.5mm Jack Types
  - Auto-Configuration for CTIA and OMTP Headsets
  - Supports MEMS Microphone
  - 50mΩ Ground Switch
- Enables Long Utilization of Accessories by Supplying Power Through 3.5mm Jack
  - Powered Accessory/Headset Detection
  - Bypass Switch to Power Accessories such as ANC Headsets
  - Programmable Button Detection in Powered Accessory Mode
- Empowers New Path in Data Communication to Accessories
  - Power Line Communication by 3.5mm Jack
  - Bidirectional Digital Data Communication in Power Mode
  - Allow Emergence of New Accessory Types
- Provides Comfortable Sounds by Introducing Automatic Volume Adjustment
  - Adaptive Volume Control Based on Precision Headset Impedance
  - False Insertion Detection
- Saves Board Space with Small Form Factor
  - 1.65mm x 2.05mm 4 x 5 Array 20 Bump 0.4mm Pitch WLP

***Ordering Information* appears at end of data sheet.**

Typical Application Circuit



Absolute Maximum Ratings

All voltages are referred to GND unless otherwise noted
V_{CC}, SCL, SDA, $\overline{INT}$ .....-0.3V to +6V
V_{BOOST}, RSEN .....-0.3V to +12V
MIC_OUT .....-0.3V to V_{CC} + 0.3V
DETIN.....-3V to V_{CC} + 0.3V
SLEEVE, SLEEVE_SL, SLEEVE_SR,
RING2, RING2_SL, RING2_SR .....-0.3V to +6V
G_SNSL, G_SNSR .....-0.3V to +0.3V
Continuous Current into V_{BOOST}, RSEN,
MIC_OUT, RING2, SLEEVE.....±200mA
Continuous Current into Any Other Terminal .....±100mA
Continuous Power Dissipation (Multilayer Board)
(Derate 18.02mW/°C above +70°C).....1441.6mW
Operating Temperature Range..... -40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Soldering Temperature (Reflow).....+260°C

Package Thermal Characteristics (Note 1)

WLP
Junction-to-Ambient Thermal Resistance,
Four Layer Board (θ_{JA}) .....55.49°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{CC} = +3.0V to +5.5V, V_{BOOST} = 0V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC}						
Supply Voltage Range	V_{CC}		3		5.5	V
V_{CC} POR	V_{CCPOR}		0.9	1.7	2.45	V
V_{CC} Supply Current	I_{VCC}	V_{CC} = +3.5V, DETIN = 1		2	5	µA
		BYPASS (0x08[2]) = 0, DETIN = 0		10	15	
		V_{CC} = +3.5V, BYPASS (0x08[2]) = 1, DETIN = 0, I_{VBOOST} = 30mA		0.1	0.2	mA
Bypass Supply Voltage Range	V_{BOOST}				5.5	V
DETIN						
DETIN Pullup Current	I_{DETIN_PU}			4.5		µA
DETIN Detection Threshold			1/3 x V_{CC}	1/2 x V_{CC}	2/3 x V_{CC}	V
DETIN Current Source	I_{DETIN}	SET_IDET (0x0B[5:4]) = 01	95	100	105	µA
		SET_IDET (0x0B[5:4]) = 10	1.05	1.1	1.15	mA
		SET_IDET (0x0B[5:4]) = 11	5.25	5.5	5.75	

Electrical Characteristics (continued)

(V_{CC} = +3.0V to +5.5V, V_{BOOST} = 0V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BYPASS SWITCH						
Output Shutdown R_{SEN} Drop	V_{SH}	V_{BOOST} = 5.0V	1.28	1.36	1.44	V
Bypass Switch R_{ON}	R_{BYPASS}	V_{CC} = 4.2V, V_{BOOST} = 5.0V, I_{BYPASS} = 150mA		1	1.5	Ω
Off Isolation to SLEEVE		V_{RSEN} = 5V ± 50mV, f = 20Hz to 20kHz		-90		dB
SLEEVE, RING2 (GND MUX SWITCH)						
Ground MUX Switch R_{ON}	R_{GMP}	V_{CC} = 3.5V		50	85	mΩ
Ground MUX Switch Bandwidth		R_{SOURCE} = R_{LOAD} = 50Ω		300		MHz
Ground Switch PSRR	$PSRR_{GNDSW}$	V_{CC} = 3.5V, R_{SOURCE} = 50Ω, f = 217Hz		-96		dB
Ground Bypass Switch THD		100mV_{Pk-Pk}, DC bias = 0V, f = 20Hz to 20KHz, R_{SOURCE} = R_{LOAD} = 50Ω		0.002		%
SLEEVE, RING2 (MIC MUX SWITCH)						
MIC Switch Turn-On Time				5		µs
MIC Switch Turn-Off Time				4		µs
MIC Switch R_{ON}	R_{MIC}	V_{CC} = 3.5V, I = 10mA		1	2	Ω
MIC Switch Bandwidth		R_{SOURCE} = R_{LOAD} = 50Ω		25		MHz
MIC Switch PSRR		V_{CC} = 3.5V, R_{SOURCE} = 50Ω, f = 217Hz		-90		dB
MIC Switch Isolation				-90		dB
V_{BOOST}, RSEN (ANC DETECTION)						
ANC Headset Detection Accuracy		Using 6.8Ω External Sense for ANC detection, range from 1.5 to 5mA (ADC2_HL(0x0B[2])) = 1. Thresholds I²C Programmable by HSDET_VAL	-3		+3	%
Button Press Current Measurement Accuracy		Using 6.8Ω External Sense, range from 5mA to 200mA (ADC2_HL(0x0B[2])) = 0. Thresholds I²C Programmable by HSDET_VAL	-3		+3	%
ANC Button Detection Interrupt Falling Edge Threshold	V_{COM_DET}	COM_THRS[1:0](0x08[1:0]) = 00	87	88	89	%V_{BOOST}
		COM_THRS[1:0] (0x08[1:0]) = 01	89	90	91	%V_{BOOST}
		COM_THRS[1:0] (0x08[1:0]) = 10	91	92	93	%V_{BOOST}
		COM_THRS[1:0] (0x08[1:0]) = 11	93	94	95	%V_{BOOST}
BOOST OVP OVLO Threshold	V_{BOOST_OVLO}	V_{BOOST} slew rate ≤ 1V/µs	5.6	5.75	5.94	V

Electrical Characteristics (continued)

(V_{CC} = +3.0V to +5.5V, V_{BOOST} = 0V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GROUND SENSE SWITCH (G_SNSR/G_SNSL)						
G_SNS Switch Turn-On Time				50		µs
G_SNS Switch Turn-Off Time				3		µs
G_SNS Switch R_{ON}		I_{LOAD} = 10mA		0.8	1.5	Ω
G_SNS Switch Bandwidth		R_{SOURCE} = R_{LOAD} = 50Ω, C_{LOAD} = 10pF		300		MHz
G_SNS Switch PSRR		V_{CC} = 3.3V, R_{SOURCE} = R_{LOAD} = 50Ω, f = 217Hz, V_{IN} = 3.3V ±0.1V		-90		dB
G_SNS Switch Cross talk		V_{CC} = 3.3V, R_{SOURCE} = R_{LOAD} = 50Ω, f = 20Hz to 20kHz, V_{MIC} = ±150mV		-90		dB
DIGITAL SIGNALS (SDA, SCL, $\overline{INT}$)						
Input Logic-High	V_{IH}		1.4			V
Input Logic-Low	V_{IL}				0.4	V
Input Leakage Current			-1		1	µA
Output Logic-High Leakage Current (Open-Drain)	I_{OH_LKG}	V_{IO} = 5V			1	µA
Output Logic-Low	V_{OL}	I_{SINK} = 4mA			0.4	V
POWER LINE COMMUNICATION						
PLC Logic-High		V_{BOOST} = 5V, Low is V_{RSENSE} below V_{COM_DET}			V_{COM_DET}	V
PLC Logic-Low		V_{BOOST} = 5V, High is V_{RSENSE} above V_{COM_DET}	V_{COM_DET}			V
Time Unit	t_{UNIT}	I^2C Programmable (24/30µs) Inferred from 1µs clock		24/30		µs
TX Logic 0	$t_{TXLOGIC0}$		90		110	% t_{UNIT}
TX Logic 1	$t_{TXLOGIC1}$	Period for low and high	40		60	% t_{UNIT}
RX Logic 0	$t_{RXLOGIC0}$		85		115	% t_{UNIT}
RX Logic 1	$t_{RXLOGIC1}$	Period for low and high	35		65	% t_{UNIT}
PLC TX Current Sink	I_{PLC}	PLC_SINK (0x18[6]) = 0	90	100	110	mA
		PLC_SINK(0x18[6]) = 1	70	80	90	mA

Electrical Characteristics (continued)

(V_{CC} = +3.0V to +5.5V, V_{BOOST} = 0V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.5V, T_A = +25°C.) (Note 2)

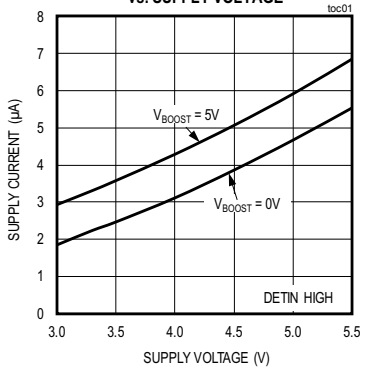
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC						
DETIN Debounce Time	t_{DIDEB}	DETIN Falling Edge, DET_DEBOUNCE (0x08[6]) = 0		115		ms
		DETIN Falling Edge, DET_DEBOUNCE (0x08[6]) = 1		300		
SEND/END Debounce Time	t_{SEDEB}	I²C selectable: 20/30/40/50ms		30		ms
I_{DETIN} Rise Time	$t_{IDETINR}$	Rising		50		ms
I_{DETIN} Fall Time	$t_{IDETINF}$	Falling		50		ms
I²C TIMING						
I²C Serial Clock Frequency	f_{SCL}			400		kHz
ESD PROTECTION						
DETIN		Human Body Model		±15		kV
SLEEVE, RING2, SLEEVE_SR, SLEEVE_SL, RING2_SR, RING2_SL		Human Body Model		±10		kV
All Other Pins		Human Body Model		±2		kV
THERMAL PROTECTION						
Thermal Shutdown	T_{SHDN}	Low to high		130		°C
Thermal Hysteresis	T_{HYST}	High to low		20		°C

Note 2: All devices are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design.

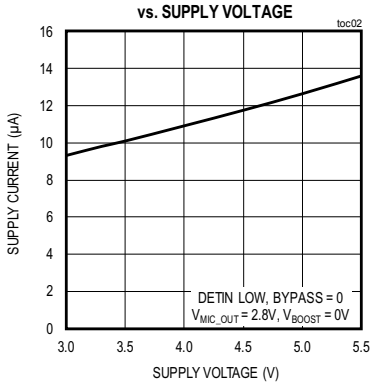
Typical Operating Characteristics

(V_{CC} = +3.5V, R_{SEN} = 6.8Ω, T_A = +25°C unless otherwise noted.)

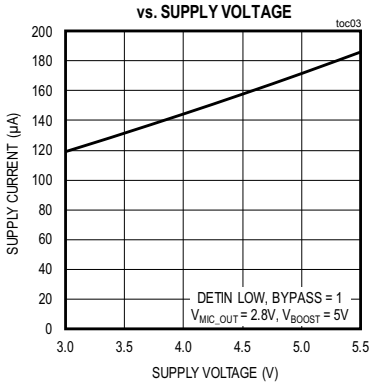
SUPPLY CURRENT vs. SUPPLY VOLTAGE



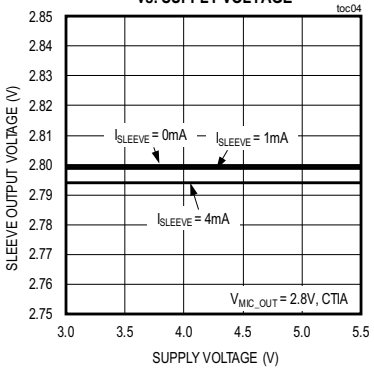
SUPPLY CURRENT vs. SUPPLY VOLTAGE



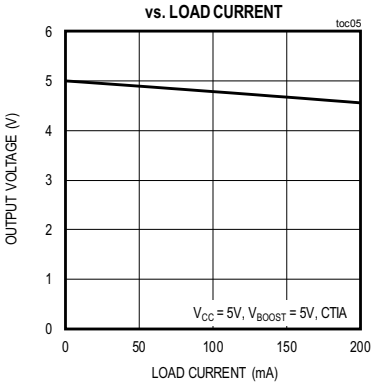
SUPPLY CURRENT vs. SUPPLY VOLTAGE



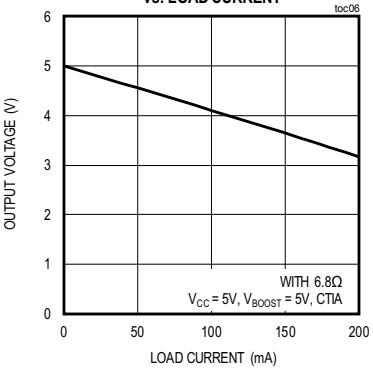
SLEEVE OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



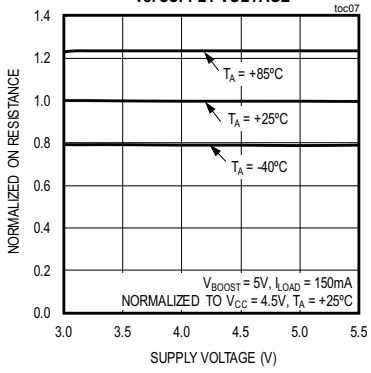
BYPASS SWITCH OUTPUT VOLTAGE vs. LOAD CURRENT



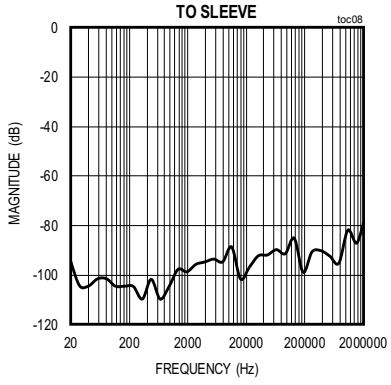
BYPASS SWITCH OUTPUT VOLTAGE vs. LOAD CURRENT



BYPASS SWITCH NORMALIZED ON-RESISTANCE vs. SUPPLY VOLTAGE



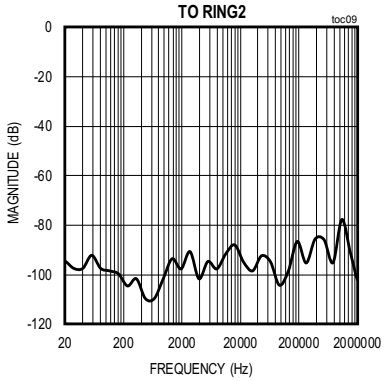
BYPASS SWITCH OFF-ISOLATION TO SLEEVE



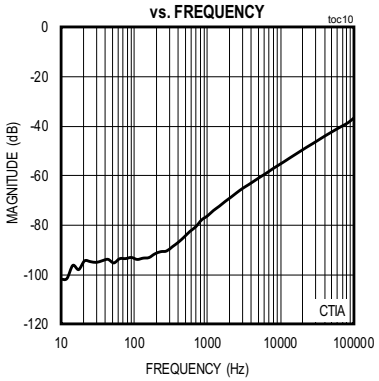
Typical Operating Characteristics (continued)

(V_{CC} = +3.5V, R_{SEN} = 6.8Ω, T_A = +25°C unless otherwise noted.)

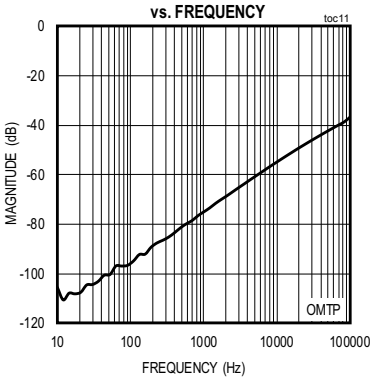
BYPASS SWITCH OFF-ISOLATION TO RING2



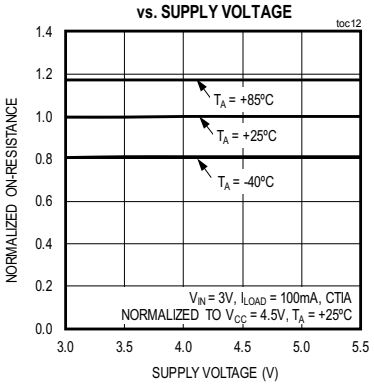
MIC MUX PSRR vs. FREQUENCY



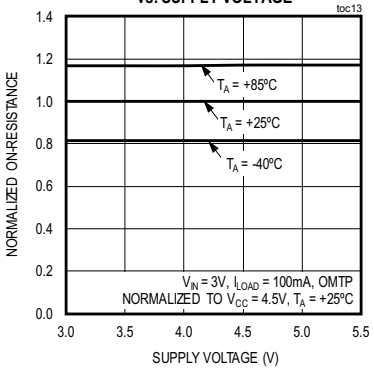
MIC MUX PSRR vs. FREQUENCY



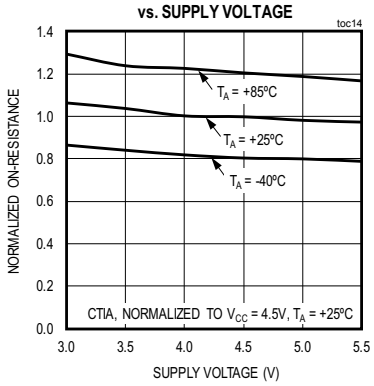
MIC MUX NORMALIZED ON-RESISTANCE vs. SUPPLY VOLTAGE



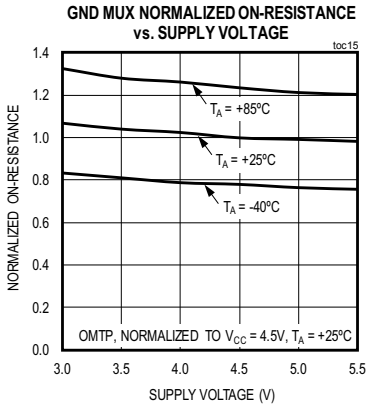
MIC MUX NORMALIZED ON-RESISTANCE vs. SUPPLY VOLTAGE



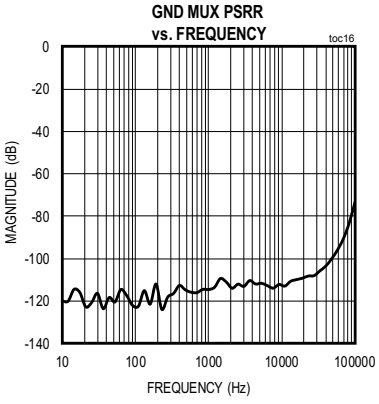
GND MUX NORMALIZED ON-RESISTANCE vs. SUPPLY VOLTAGE



GND MUX NORMALIZED ON-RESISTANCE vs. SUPPLY VOLTAGE



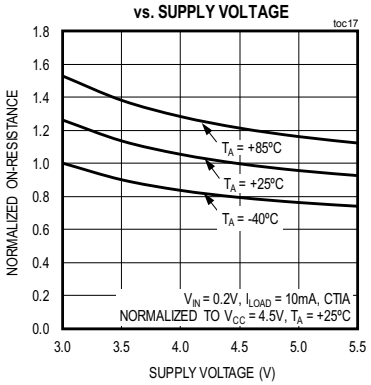
GND MUX PSRR vs. FREQUENCY



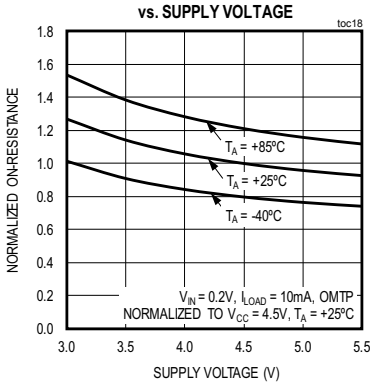
Typical Operating Characteristics (continued)

(V_{CC} = +3.5V, R_{SEN} = 6.8Ω, T_A = +25°C unless otherwise noted.)

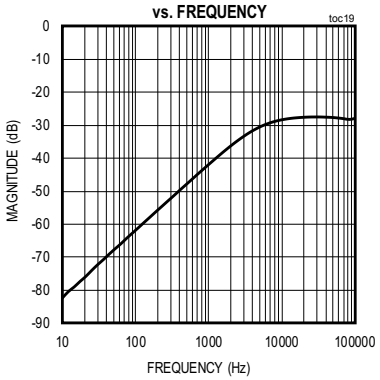
GND SENSE NORMALIZED ON-RESISTANCE vs. SUPPLY VOLTAGE



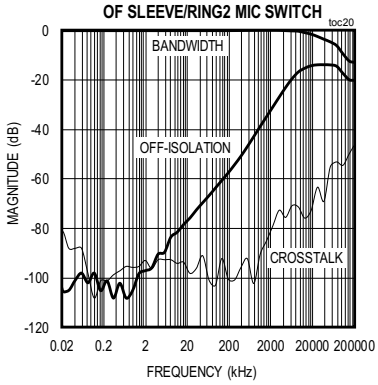
GND SENSE NORMALIZED ON-RESISTANCE vs. SUPPLY VOLTAGE



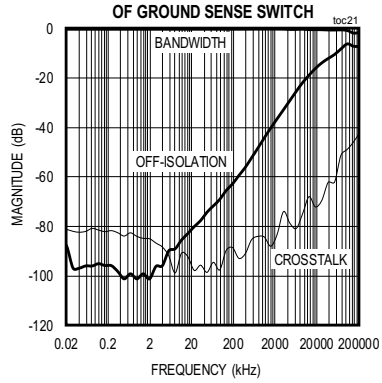
GND SENSE PSRR vs. FREQUENCY



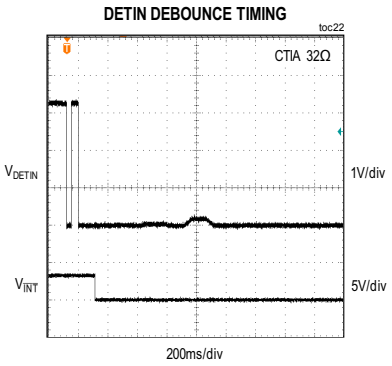
BANDWIDTH, OFF-ISOLATION, CROSSTALK OF SLEEVE/RING2 MIC SWITCH



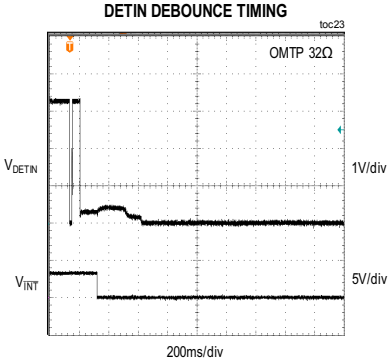
BANDWIDTH, OFF-ISOLATION, CROSSTALK OF GROUND SENSE SWITCH



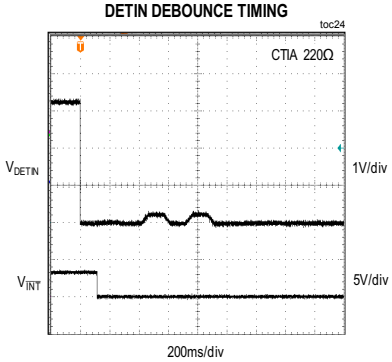
DETIN DEBOUNCE TIMING



DETIN DEBOUNCE TIMING



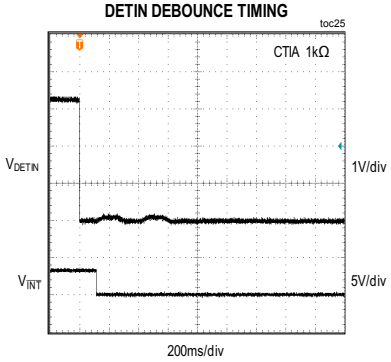
DETIN DEBOUNCE TIMING



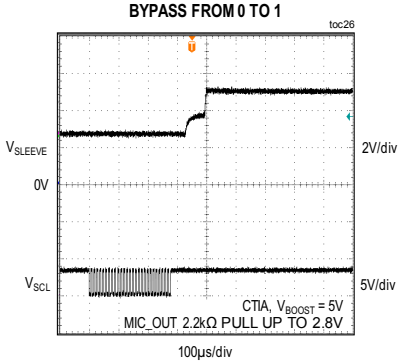
Typical Operating Characteristics (continued)

(V_{CC} = +3.5V, R_{SEN} = 6.8Ω, T_A = +25°C unless otherwise noted.)

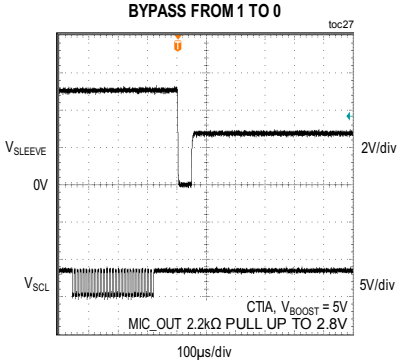
DETIN DEBOUNCE TIMING



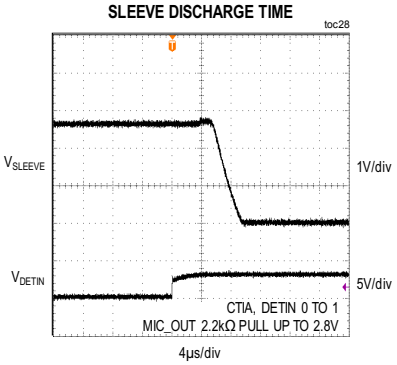
SLEEVE WAVEFORM BYPASS FROM 0 TO 1



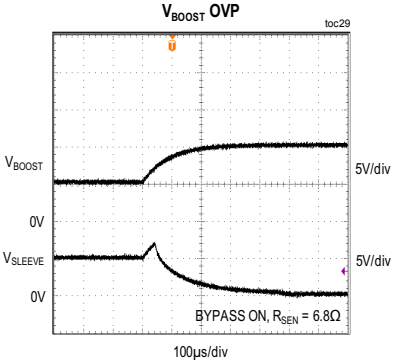
SLEEVE WAVEFORM BYPASS FROM 1 TO 0



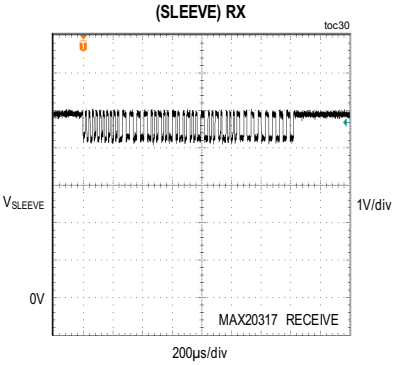
SLEEVE DISCHARGE TIME



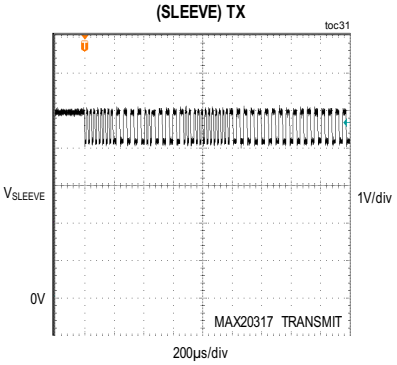
VBOOST OVP



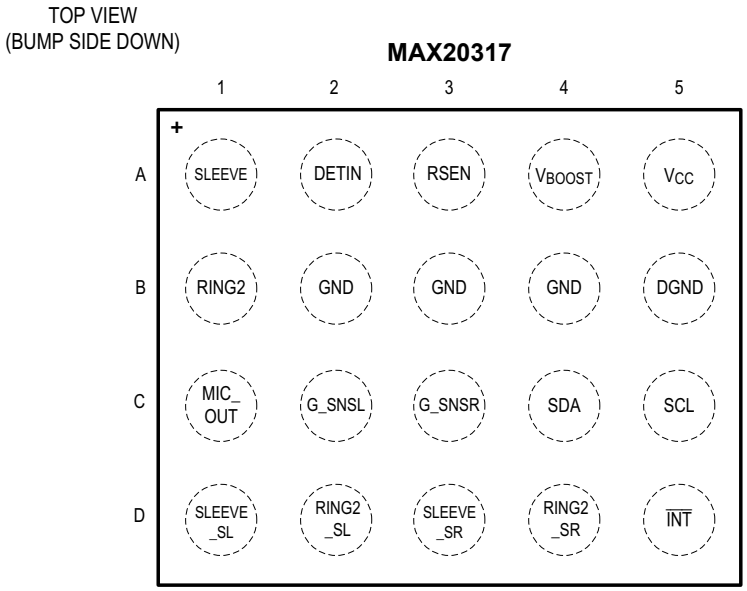
PLC COMMUNICATION (SLEEVE) RX



PLC COMMUNICATION (SLEEVE) TX



Bump Configuration



WLP
(2.05mm x 1.65mm)

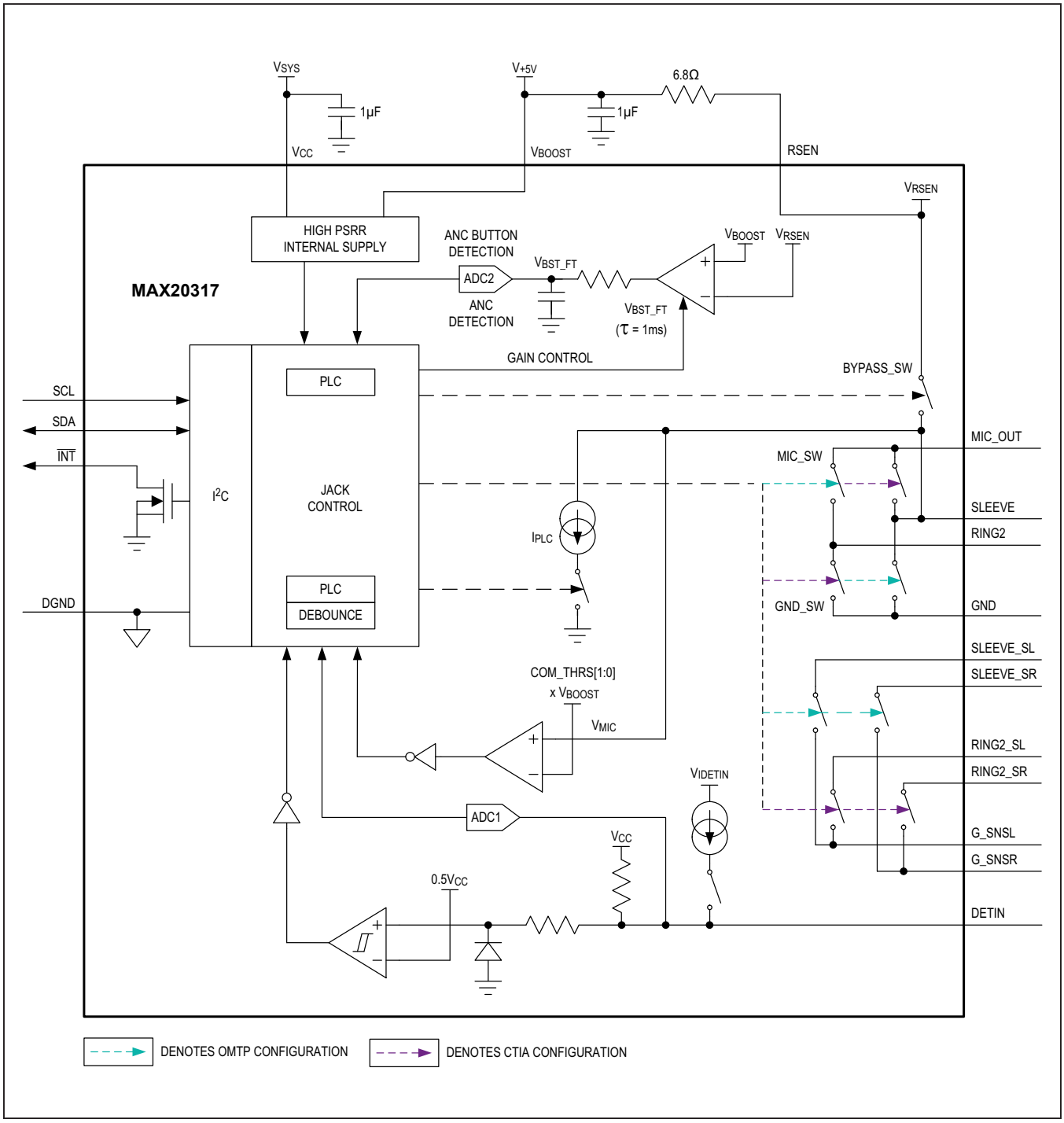
Bump Descriptions

BUMP	NAME	FUNCTION
A1	SLEEVE	Jack Sleeve Pin Contact
A2	DETIN	Jack Insertion Detection Input. An internal comparator monitors DETIN for jack insertion/ removal events.
A3	RSEN	RSEN connection for Bypass mode
A4	V_{BOOST}	Supply Voltage Input for Bypass Mode. Bypass V_{BOOST} to ground with a 1µF ceramic capacitor as close as possible to the device.
A5	V_{CC}	Supply Voltage Input. Bypass V_{CC} to ground with a 1µF decoupling capacitor as close as possible to the device.

Bump Descriptions (continued)

BUMP	NAME	FUNCTION
B1	RING2	Jack Ring2 Pin Connection
B2, B3, B4	GND	Ground. Connect all GND and DGND pins together.
B5	DGND	Digital Ground. Connect all GND and DGND pins together.
C1	MIC_OUT	Microphone to Phone Codec Output
C2	G_SNSL	Left Ground Reference Sense. G_SNSL is a ground reference prior to the ground switch to obtain a high ground isolation for the audio codec.
C3	G_SNSR	Right Ground Reference Sense. G_SNSL is a ground reference prior to the ground switch to obtain a high ground isolation for the audio codec.
C4	SDA	I^2C Data Line
C5	SCL	I^2C Clock
D1	SLEEVE_SL	Jack Sleeve Kelvin Pin Contact for Left Audio Line
D2	RING2_SL	Jack Ring2 Kelvin Pin Contact for Left Audio Line
D3	SLEEVE_SR	Jack Sleeve Kelvin Pin Contact for Right Audio Line
D4	RING2_SR	Jack Ring2 Kelvin Pin Contact for Right Audio Line
D5	$\overline{INT}$	I^2C Active-Low, Open-Drain Interrupt Output. Connect $\overline{INT}$ to an external pullup resistor.

Block Diagram



Detailed Description

The MAX20317 supports both CTIA and OMTP headsets. The advanced method used to detect the headset type provides error free connections to ground and the microphone line. Manual control allows for future expansion of accessory types and functions.

In addition to detecting the jack configuration, the MAX20317 also reliably detects ANC headsets and headset button press events. A built-in, low offset 8-bit ADC provides a precise method of detecting an ANC headset and button presses in ANC music mode. These functions are handled automatically by the device, but can also be controlled manually.

For both ANC and normal headsets, the MAX20317 measures the impedance of the speaker. High precision current sources and an 8-bit ADC permit high accuracy sensing of low impedance headsets, even distinguishing between 16Ω and 32Ω speakers. This is useful in dynamic volume scaling applications.

The MAX20317 features power-line communication (PLC) for accessories powered by the microphone line. Data transmits above audio frequencies to prevent interference with the audio signal to the headset. This permits accessories to communicate with the device while a system is in music mode.

After the startup process is complete and the DEVICE_READY bit (0x03[2]) is set, the MAX20317 enters normal operation. During this stage, an external controller and CODEC can confirm the jack type, either 3P or 4P, to enable or disable a MIC bias, detect the presence of an ANC headset, and communicate with accessories or use the headset microphone. The full system flowchart is shown in Figure 1, while Figure 2 details the jack detection process when a headset is connected.

Impedance Detection

When the MAX20317 detects the presence of a headset, it can measure the headset impedance. DETIN applies a current, I_{DETIN}, to the left channel of the 3.5mm jack and reads the resulting DC voltage with ADC1. This measurement occurs automatically when DET goes low after a DETIN debounce period or triggers manually upon receipt of an I^2C command while DET = 0. The start condition is set with ADC_CTRL[1:0] (0x0A[3:2]).

Automatic impedance measurements begin when a headset insertion event forces DET low. The MIC and GND switches close in a CTIA configuration. If the OPEN_DETECT bit (0x09[4]) is HIGH, I_{DETIN} is set to 100µA for a high-impedance measurement. If the voltage measured by ADC1 is less than the value saved in HIHS_VAL (register 0x0E), or if OPEN_DETECT is low, a low impedance measurement is performed with I_{DETIN} = 1.1mA. If the voltage is still too low, the low-impedance measurement is repeated with I_{DETIN} = 5.5mA. This automatic process is illustrated in Figure 3.

Alternatively, the MAX20317 can measure impedance only upon receipt of an I^2C command. Setting ADC1_CTRL[1:0] to 01 or 10 causes the impedance measurement to trigger when FORCE_ADC1_START (0x0B[1]) goes high. The I_{DETIN} value for manual impedance measurements is set by SET_IDET[1:0] (0x0B[5:4]). After an automatic measurement, SET_IDET[1:0] equals the last I_{DETIN} value used in the impedance check, but it can be forced to any value for manual tests.

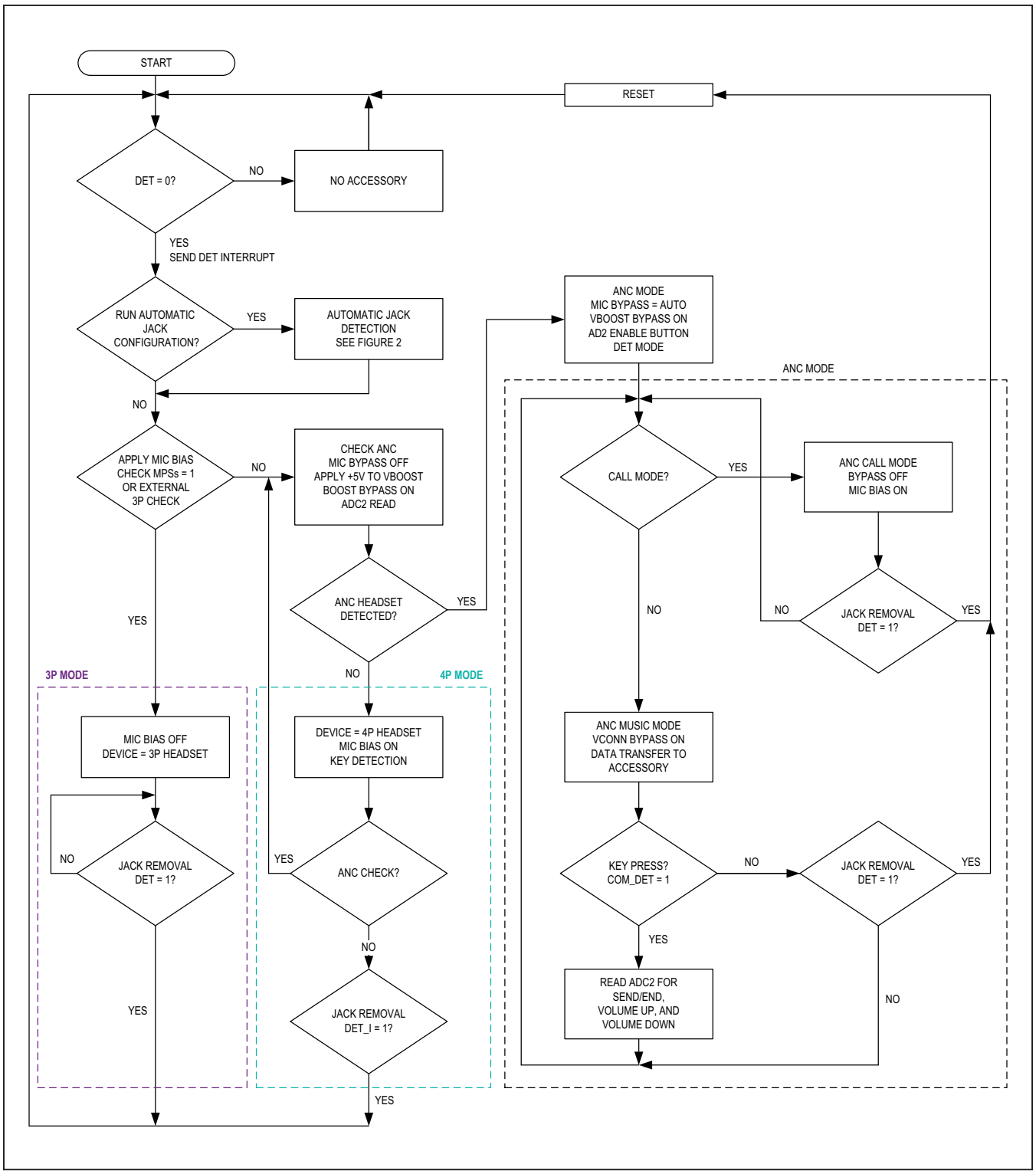


Figure 1. Full operation of the MAX20317

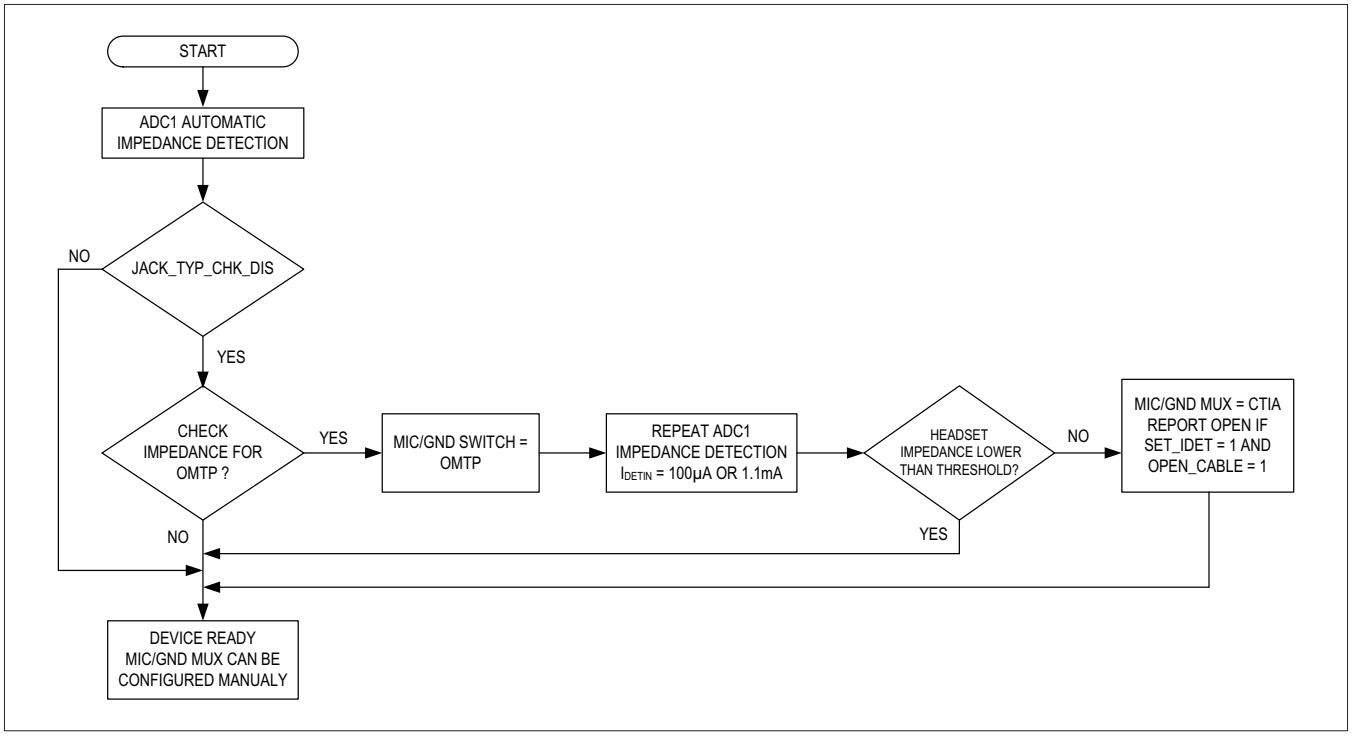


Figure 2. Automatic Jack Detection

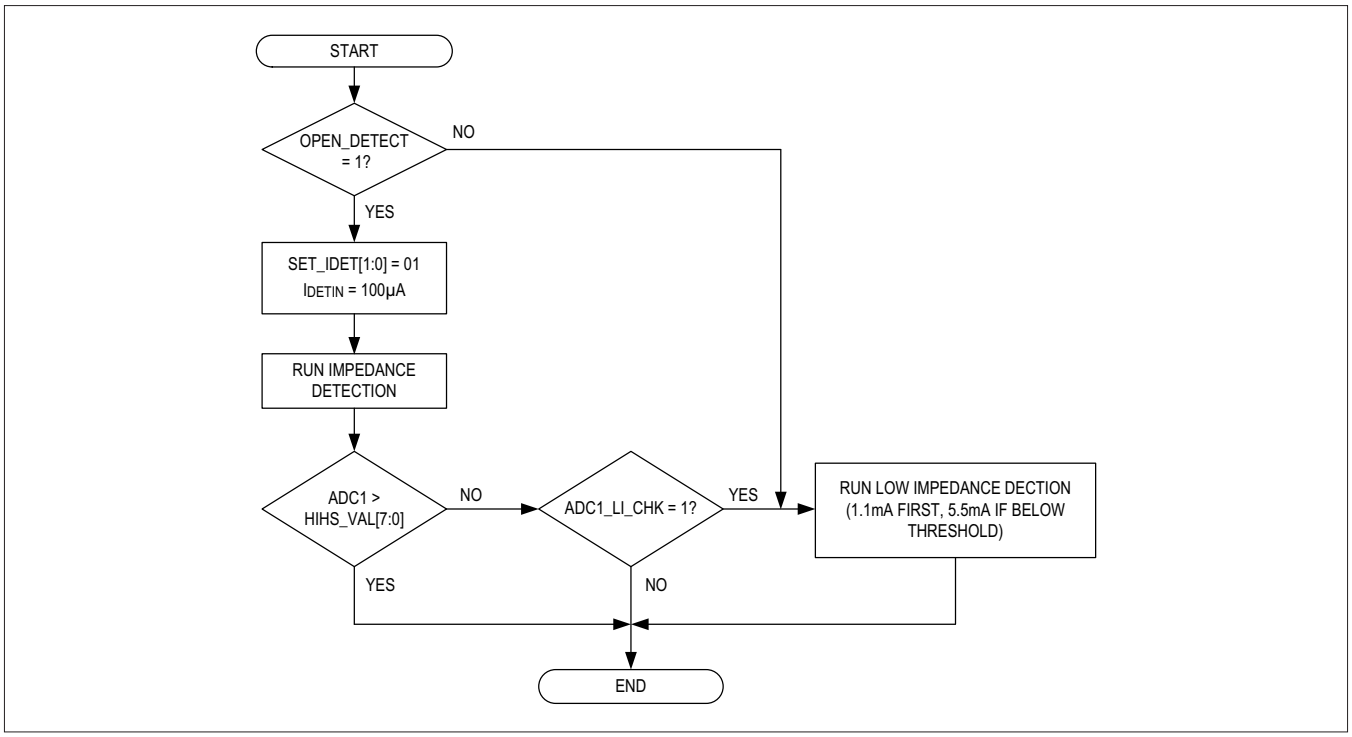


Figure 3. ADC1 Automatic Impedance Detection

CTIA/OMTP Detection

The impedance measurement process is also used to identify a jack as CTIA or OMTP. When JACK_TYP_CHK_DIS = 0 (0x0A[6]), CTIA/OMTP detection begins after an automatic impedance measurement. This second measurement keeps the last value of I_{DETIN}, either 100µA or 1.1mA, and measures the L-channel impedance with the MIC and GND MUX switches closed in OMTP mode. If the voltage measured by ADC1 is less than the threshold defined in OMTP_VAL (register 0x0F) when testing a low-impedance headset, or HIHS_VAL for high-impedance headsets, the MIC and GND MUX switches remain configured for OMTP. Otherwise, the switches connect in the CTIA configuration. Automatic jack detection is disabled when ADC1 is controlled manually or when JACK_TYP_CHK_DIS = 1 and the MIC and GND switches must be set by FORCE_MG_SW[1:0] (0x09[1:0]) and MANUAL_MG_SW (0x09[5]).

Open Cable Check

If OPEN_DETECT = 1 (0x09[4], the MAX20317 performs an open cable check after determining the jack type. If a high-impedance measurement exceeds the HIHS_VAL threshold, the cable is considered open and the OPEN_CABLE flag (0x03[4]) is set. This feature helps ensure that a there is a clean connection to a real headset when DET goes LOW after the DETIN debounce period.

ANC Headset Detection

The MAX20317 identifies ANC headsets by measuring the current drawn through an external resistor connected to RSEN. If there is +5V present on V_{BOOST}, an automatic measurement launches when the bypass switch closes. An internal, high-gain differential amplifier measures the current through the sense resistor and is read by ADC2. If the current is higher than HSDET_VAL (register 0x10), the headset is considered to be ANC and the ANC_HS bit (0x05[7]) is set. ANC headset detection is only compatible with CTIA headsets.

ANC Current Sense

The MAX20317 automatically detects ANC button presses while in BYPASS mode through the current sense resistor. When a button is pressed, the microphone voltage drops, triggering a COM_DET interrupt. This also triggers an automatic ADC2 conversion. The ADC2 conversion continues as long as the microphone voltage is below the COM_DET threshold set by COM_THRS[1:0] (0x08[1:0]).

Pop-Up Noise Suppression

In order to prevent any pop-up noise, SLEEVE and RING2 are discharged immediately after a headset is unplugged.

Microphone Short Protection

Overcurrent protection on RSEN protects the MAX20317 from drawing too much current through the sense resistor. When the voltage drop across the sense resistor exceeds V_{SH} for longer than the time set in tSHO_DEB[1:0] (0x0D[1:0]), the MPSs bit (0x04[4]) is set and triggers an interrupt. The MAX20317 exits bypass mode and resets BYPASS to “0.” The device also exits bypass mode if an overvoltage condition occurs on V_{BOOST}.

Power Line Communication

A one-wire accessory Power-Line-Communication Protocol (PLC) enables communication between a master device and a single accessory device over the microphone power line. The protocol allows the master to configure, control, and read the status of the attached accessory. When the accessory is powered, power line communication takes place over the microphone using biphase mark code (BMC).

The PLC can be implemented on any single power line between two devices. Error checking, including parity and checksum, is included in the protocol to validate all data transferred between devices. The protocol is defined by a physical layer, which describes the physical communication protocol, and the logical layer that includes high-level commands and handshakes. Figure 4 and Figure 5 show the process of sending and receiving PLC data, respectively. The MAX20317 supports physical data transfer between the master device and slave accessory. The meaning of the data contained in each individual accessory must be defined by the manufacturer of the master device.

SLEEVE and RING2 Ground Sense

Because audio systems require high levels of isolation between audio channels, the MAX20317 incorporates separate ground sense connections for SLEEVE and RING2. These ground sense contacts provide channel isolation with a Kelvin contact, especially when an EMC filter is included between the 3.5mm jack and the MAX20317. Individual left- and right-channel ground sense outputs provide separate return paths for SLEEVE and RING2.

I²C Interface

The MAX20317 uses the two-wire I²C interface to communicate with a host application processor. The configuration settings and status information provided through this interface are detailed in the register descriptions (Tables 2 – 31). MAX20317 uses the seven-bit slave address 0b0010101 (0x2A for writes, 0x2B for reads).

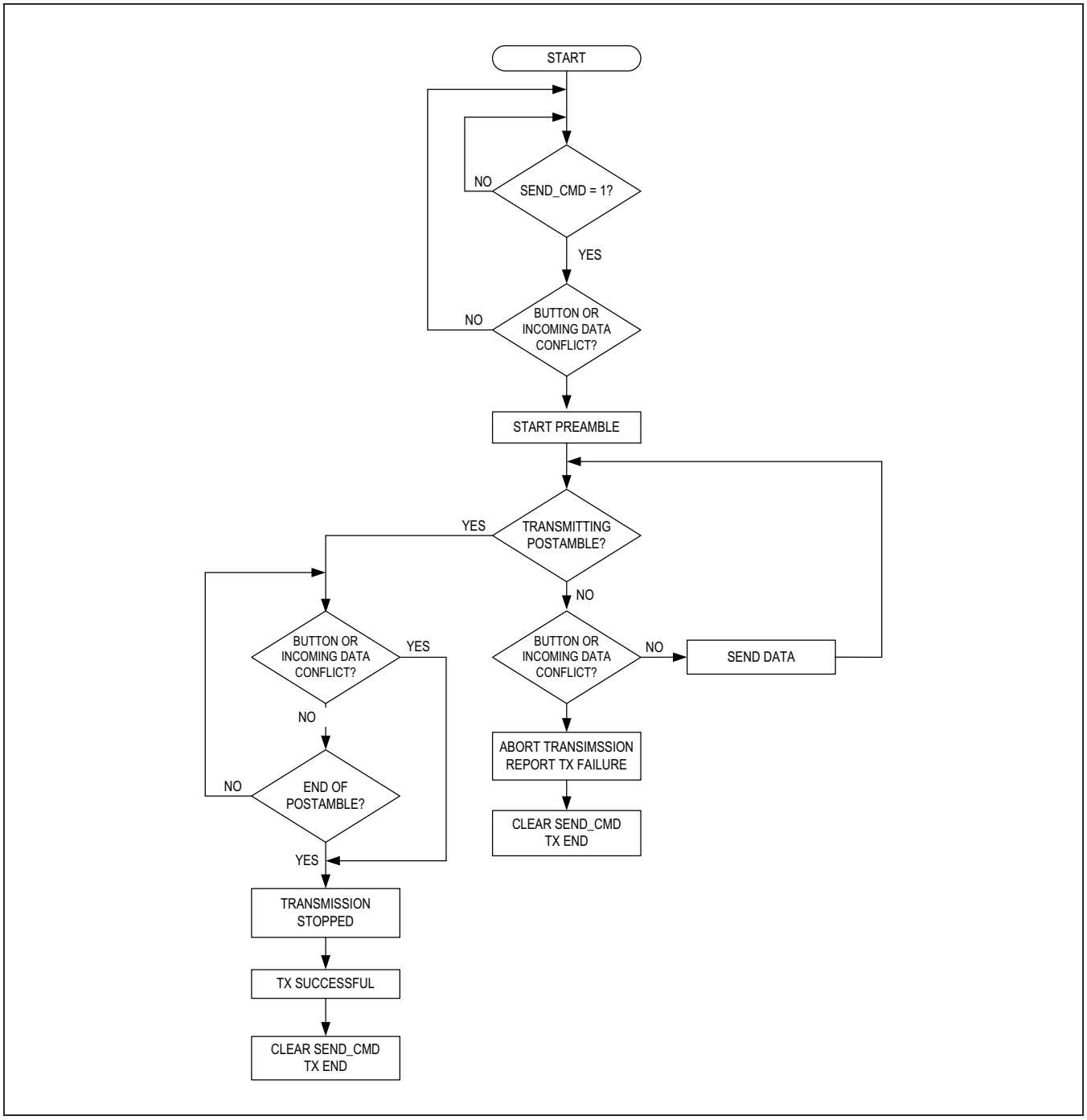


Figure 4. PLC TX Process

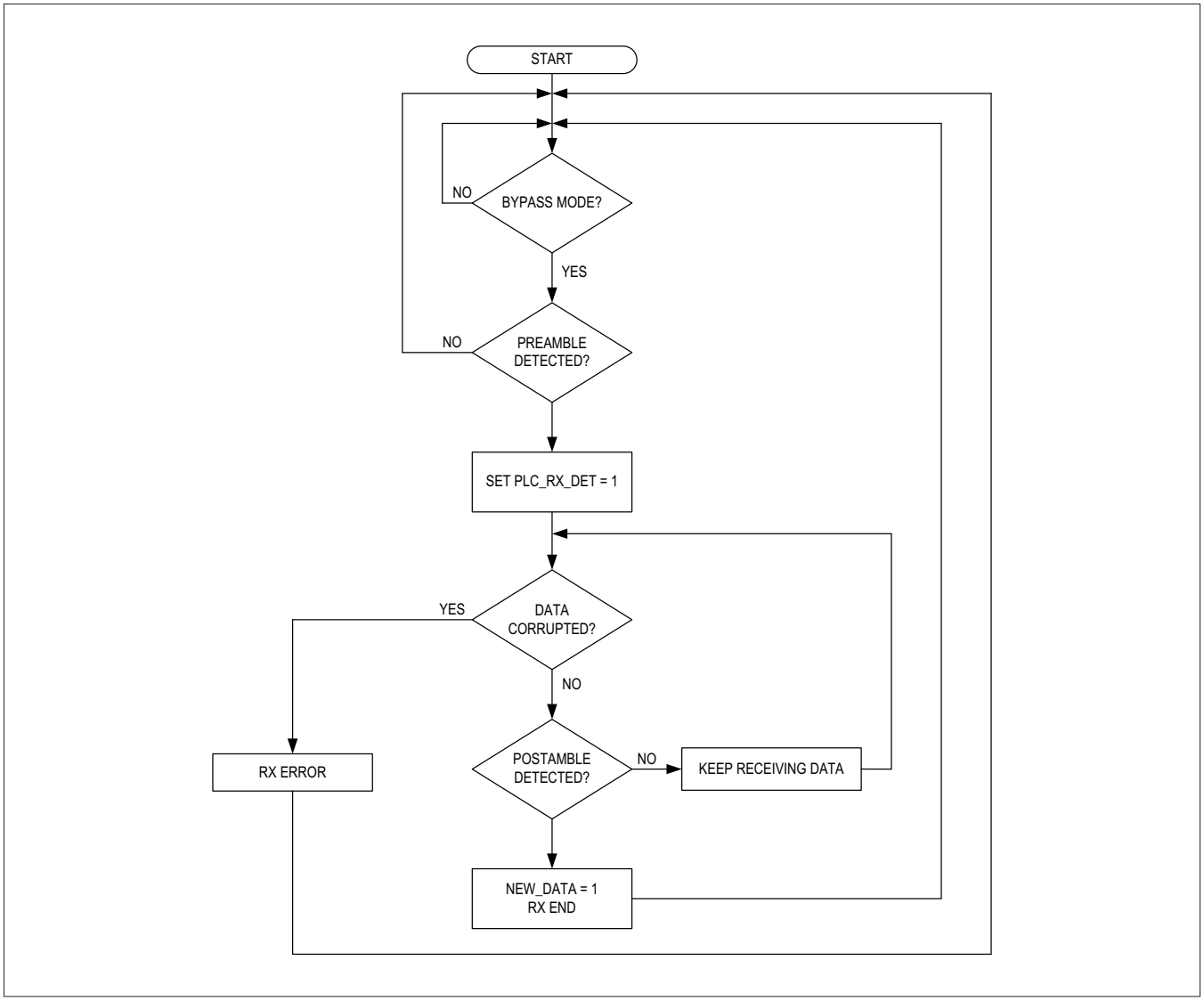


Figure 5. PLC RX Process

Applications Information

I²C Serial Interface

The I²C serial interface is used to configure the device. Figure 6 shows the I²C timing diagram.

Serial Addressing

When in I²C mode, the device operates as a slave device that sends and receives data through an I²C-compatible 2-wire interface. The interface uses a serial data line (SDA) and a serial-clock line (SCL) to achieve bidirectional communication between master(s) and slave(s). A master (typically a microcontroller) initiates all data transfers to and from the MAX20317 and generates the SCL clock that synchronizes the data transfer. The SDA line operates as both an input and an open drain output. A pullup resistor is required on SDA. The SCL line operates only as an input. A pullup resistor is required on SCL if there are multiple masters on the 2-wire interface, or if the master in a single-master system has an open drain SCL output. Each transmission consists of a START condition sent by a master, followed by the MAX20317 7-bit slave address plus R/W bit, a register address byte, one or more data bytes, and finally a STOP condition.

Start and Stop Conditions

Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a START (S) condition by transitioning SDA from high to low while SCL is high (Figure 7). When the master has finished communicating with the slave, it issues a STOP (P) condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission.

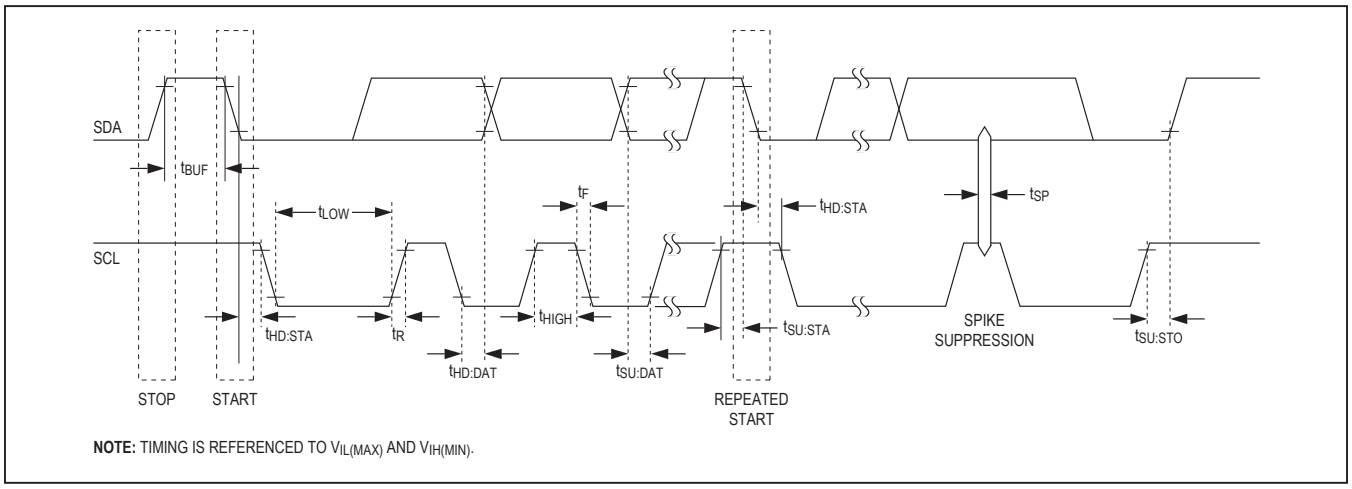


Figure 6. I²C Timing Diagram

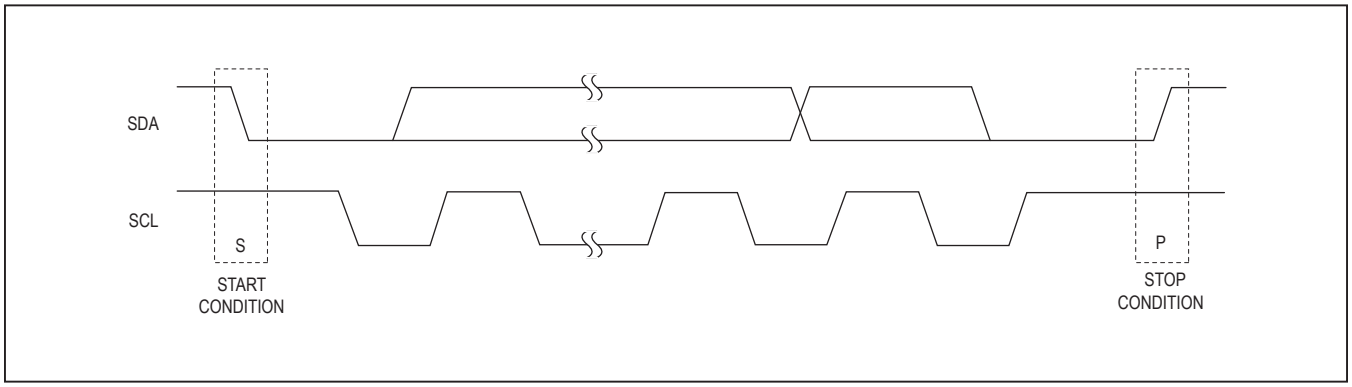


Figure 7. Start and Stop Conditions

Bit Transfer

One data bit is transferred during each clock pulse (Figure 8). The data on SDA must remain stable while SCL is high.

Acknowledge

The acknowledge bit is a clocked 9th bit (Figure 9), which the recipient uses to handshake receipt of each byte of data. Thus, each byte transferred effectively requires 9 bits. The master generates the 9th clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse. The SDA line is stable low during the high period of the clock pulse. When the master is transmitting to the MAX20317, it generates the acknowledge bit because the device is the recipient. When the device is transmitting to the master, the master generates the acknowledge bit because the master is the recipient. If the device does not pull SDA low, a not acknowledge is indicated.

Slave Address

The device has a 7-bit slave address. The bit following a 7-bit slave address is the R/$\overline{W}$ bit, which is low for a write command and high for a read command. The slave address for the device is 0b00101011 for read commands and 0b00101010 for write commands. This is summarized in Table 1.

Table 1. I²C Slave Addresses

ADDRESS FORMAT	VALUE	
	HEX	BINARY
7-BIT SLAVE ADDRESS	0x15	001 0101
WRITE ADDRESS	0x2A	0010 1010
READ ADDRESS	0x2B	0010 1011

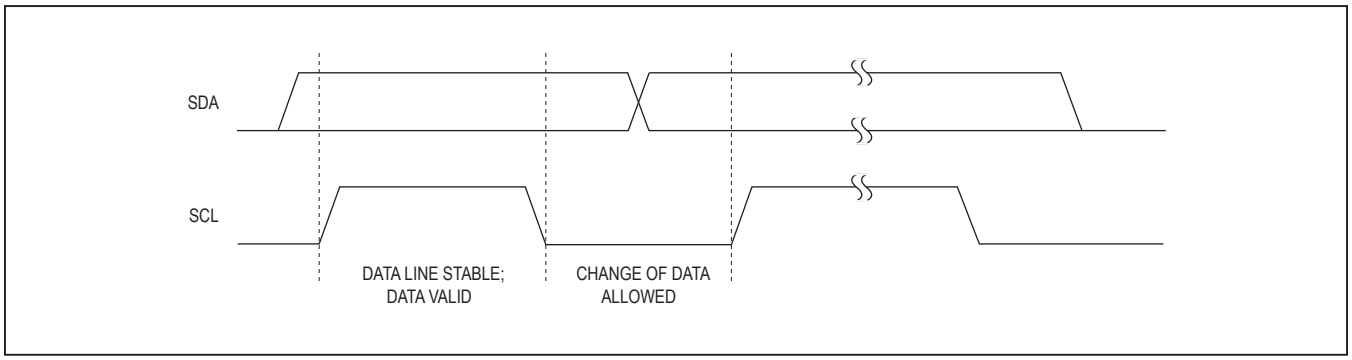


Figure 8. Bit Transfer

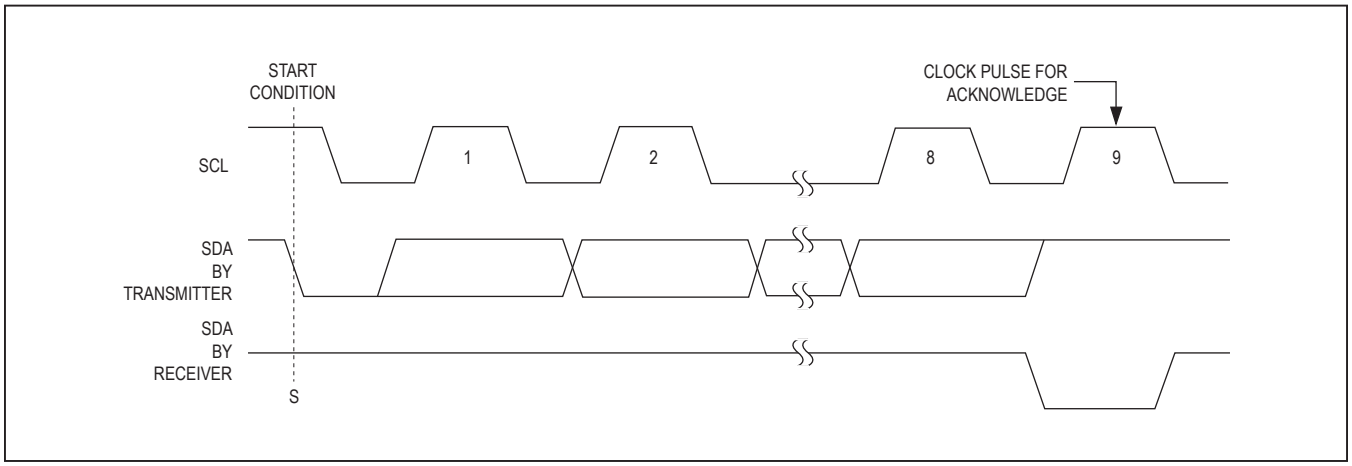


Figure 9. Acknowledge

Bus Reset

The MAX20317 resets the bus with the I2C start condition for reads. When the R/$\overline{W}$ bit is set to 1, the MAX20317 transmits data to the master, thus the master is reading from the device.

Format for Writing

A write to the MAX20317 comprises the transmission of the slave address with the R/$\overline{W}$ bit set to zero, followed by at least 1 byte of information. The first byte of information is the register address or command byte. The register address determines which register of the device is to be written by the next byte, if received. If a STOP (P) condition is detected after the register address is received, then the device takes no further action beyond storing the register address. Any bytes received after the register address are data bytes. The first data byte goes into the register selected by the register address and subsequent data bytes go into subsequent registers (Figure 10). If multiple data bytes are transmitted before a STOP condition, these bytes are stored in subsequent registers because the register addresses auto-increments (Figure 11).

Format for Reading

The MAX20317 is read using the internally stored register address as an address pointer, the same way the stored register address is used as an address pointer for a write. The pointer auto-increments after each data byte is read using the same rules as for a write. Thus, a read is initiated by first configuring the register address by performing a write (Figure 12). The master can now read consecutive bytes from the device, with the first data byte being read from the register addressed pointed by the previously written register address (Figure 13). Once the master sends a NACK, the MAX20317 stop sending valid data.

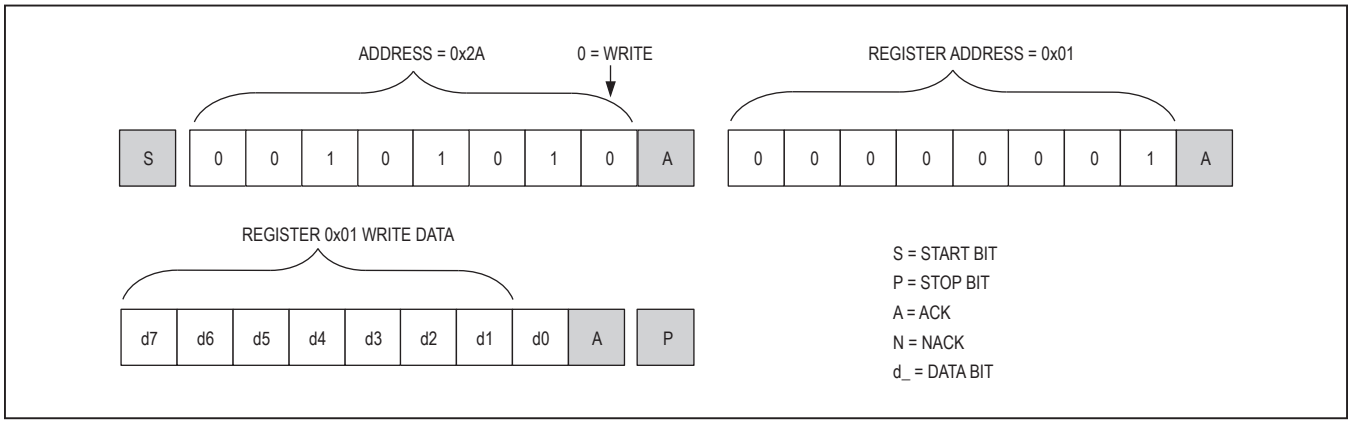


Figure 10. Format for I2C Write

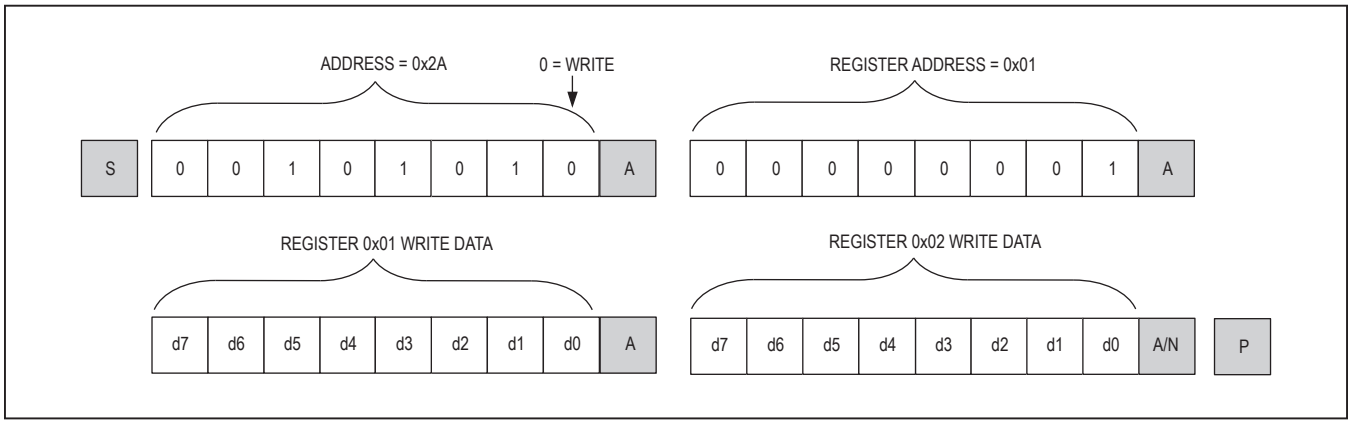


Figure 11. Format for Writing to Multiple Registers

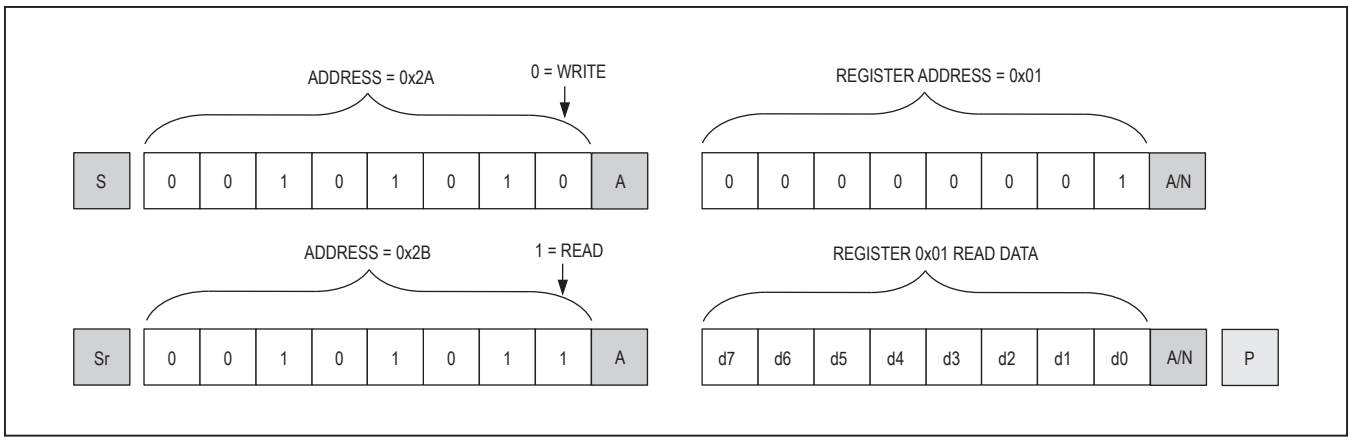


Figure 12. Format for Reads (Repeated Start)

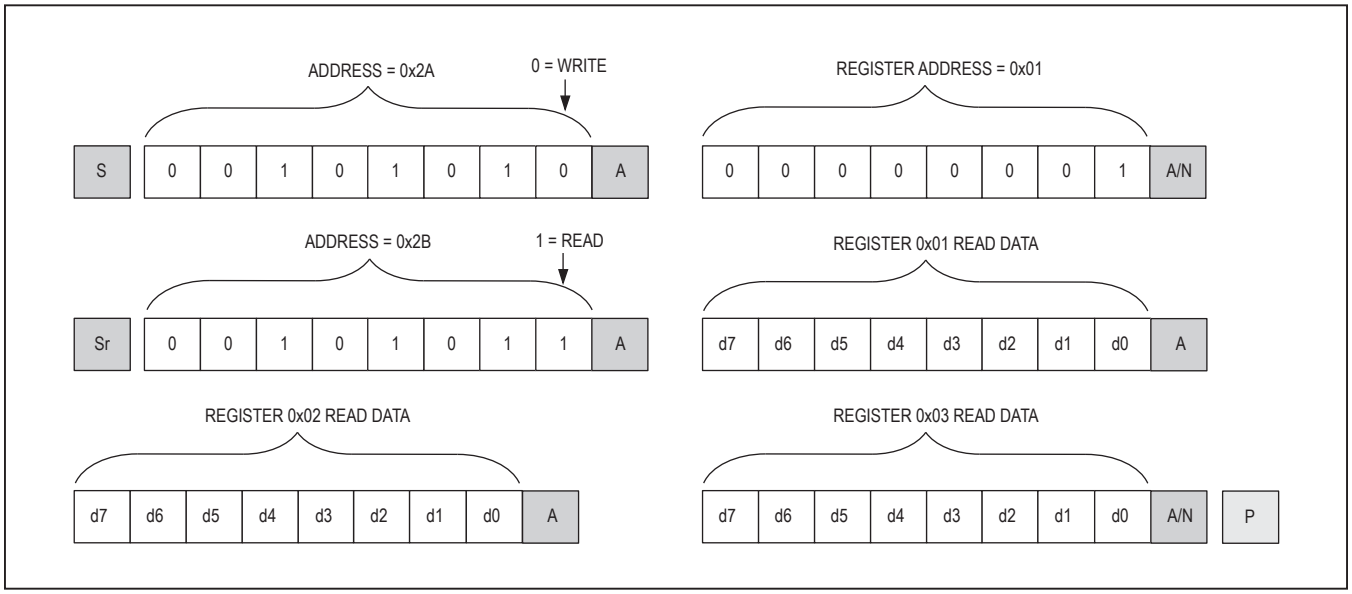


Figure 13. Format for Reading Multiple Registers

Power Line Communication

Physical Structure

In biphase mark code, high and low bits are defined by state transitions. In the MAX20317, the PLC code comprises a time unit and the low and high states of the MIC line. The time unit, t_{UNIT} defines the interval of time in which a bit is determined to be either 0 or 1. By default, t_{UNIT} = 24µs, but setting the FREQ bit (0x18[4]) HIGH increases t_{UNIT} to 30µs. A bit is considered 0 if no MIC state transition occurs during t_{UNIT}. If there is a state change, either high to low or low to high, the bit is 1.

When the MIC line is above the V_{COM_DET} threshold, a low state is recorded. Conversely, a high state is recorded when the MIC line is below the V_{COM_DET} threshold. For example, MIC line transitions and their corresponding logic values and BMC bits are shown in Figure 14.

Transmission Format

A valid PLC packet comprises a preamble, two data bytes, checksum, and postamble. The preamble is eight consecutive 1 bits. After a successful preamble, data transfer takes place until an error condition occurs or the end of transmission is reached.

Each byte of data begins with a 0 bit to indicate the start condition followed by one byte of data. A parity and stop bit are transmitted at the end of each byte. The stop bit is always 1. If parity is disabled, a parity bit of 1 will be sent, but ignored by the device.

Following the data bytes, a checksum is transmitted. The checksum is generated as NOT(DATA1 + DATA2). Transmission will end with the checksum unless the postamble is enabled. The postamble transmits 0 for a duration of 50ms. A typical data packet is shown in Figure 15.

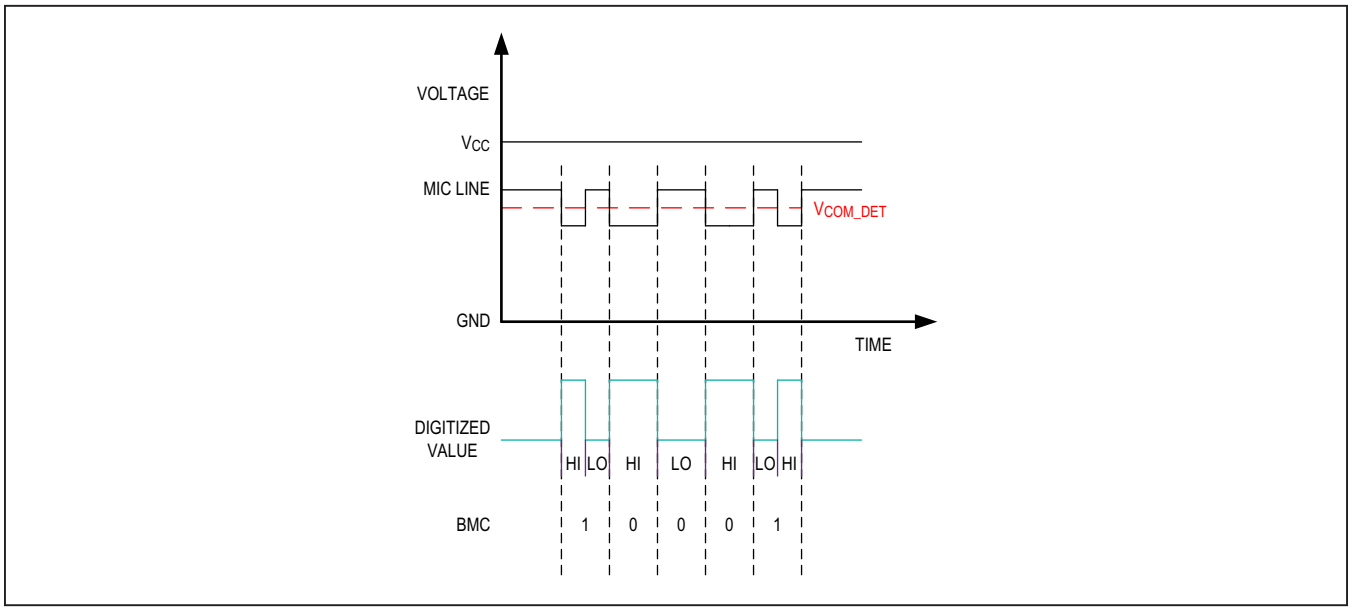


Figure 14. Determination of PLC Data Bit

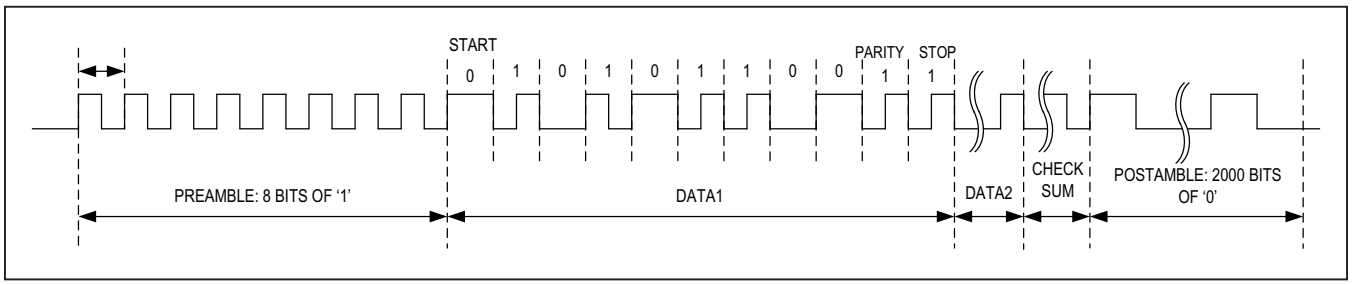


Figure 15. Sample PLC Data Packet

I²C Register Map

ADDRESS	NAME	R/W	B7	B6	B5	B4	B3	B2	B1	B0
0x00	DEVICE_ID	R	CHIP_ID[3:0]				CHIP_REV[3:0]			
0x01	ADC1_VAL	R	ADC1_VAL[7:0]							
0x02	ADC2_VAL	R	ADC2_VAL[7:0]							
0x03	STATUS1	R	IDET_LVL[1:0]		COM_DET	OPEN_ CABLE	JACK_ TYPE	DEVICE_ RDY	EOC1	EOC2
0x04	STATUS2	R	VOL_UP	VOL_ DOWN	VBOOST_ OV	MPSs	MIC_IN	SWD	DET	DETIN
0x05	STATUS3	R	ANC_HS	THT_CMP	SAR_CMP	V94_CMP	–	–	–	VOL_RFU
0x06	IRQ	R/C	SWDi	EOCi	COM_DETi	MPS/ VBOOST_ OVi	MIC_INi	DEVICE_ RDYi	DETi	DETINi
0x07	MASK	R/W	SWDm	EOCm	COM_ DETm	MPS/ VBOOST_ OVm	MIC_INm	DEVICE_ RDYm	DETm	DETINm
0x08	CONTROL1	R/W	–	DET_ DEBOUNCE	DETIN_ OVERRIDE	MIC_OUT_ DELAY	–	BYPASS	COM_THRS[1:0]	
0x09	CONTROL2	R/W	MANUAL_ G_SNS	MANUAL_ MIC_SW	MANUAL_ MG_SW	OPEN_ DETECT	FORCE_ G_SNS	FORCE_ MIC_SW	FORCE_MG_SW[1:0]	
0x0A	ADC_ CONTROL1	R/W	IDET_FLAT	JACK_TYP_ CHK_DIS	–	ADC1_ LI_CHK	ADC1_CTL[1:0]		ADC2_CTL[1:0]	
0x0B	ADC_ CONTROL2	R/W	–	–	SET_IDET[1:0]		–	ADC2_HL	FORCE_ ADC1_ START	FORCE_ ADC2_ START
0x0C	TIMING CONTROL	R/W	ADC1_AVG#[1:0]		ADC2_AVG#[1:0]		tANCDET_DEB[1:0]		tANCBPD_DEB[1:0]	

I²C Register Map (continued)

ADDRESS	NAME	R/W	B7	B6	B5	B4	B3	B2	B1	B0
0x0D	SHORT CURRENT CONTROL	R/W	FU[5:0]						tSHO_DEB[1:0]	
0x0E	HIHS_VAL	R/W	HIHS_VAL[7:0]							
0x0F	OMTP_VAL	R/W	OMTP_VAL[7:0]							
0x10	HSDET_VAL	R/W	HSDET_VAL[7:0]							
0x11	VOL0_TH	R/W	VOL0[7:0]							
0x12	VOL1_TH	R/W	VOL1[7:0]							
0x13	VOL2_TH	R/W	VOL2[7:0]							
0x14	VOL3_TH	R/W	VOL3[7:0]							
0x15	PLC_STAT	R	–	–	PLC_ TX_ERR	PLC_ TX_OK	PLC_TXP	PLC_ RX_ERR	NEW_DATA	PLC_ RX_DET
0x16	PLC_IRQ	R/C	–	–	PLC_ TX_ERRi	PLC_ TX_OKi	PLC_TXPi	PLC_ RX_ERRi	NEW_DATAi	PLC_ RX_DETi
0x17	PLC_MASK	R/W	–	–	PLC_ TX_ERRm	PLC_ TX_OKm	PLC_TXPm	PLC_ RX_ERRm	NEW_ DATAm	PLC_ RX_DETm
0x18	PLC_CON1	R/W	–	PLC_SINK	POS_ AM_DIS	FREQ	PARITY[1:0]		–	SEND_ CMD
0x19	ACC_ID	R	ACC_ID[3:0]				ACC_CAT[3:0]			
0x1A	ACC_DB1	R	ACC_DB1[7:0]							
0x1B	ACC_DB2	R	ACC_DB2[7:0]							
0x1C	ACC_ADD	R/W	ACC_ADD[7:0]							
0x1D	ACC_DATA	R/W	ACC_DAT[7:0]							

Table 2. DEVICE_ID Register (0x00)

ADDRESS	0x00							
MODE	Read Only							
BIT	7	6	5	4	3	2	1	0
NAME	CHIP_ID[3:0]				CHIP_REV[3:0]			
RESET	0	0	0	1	0	0	0	0
CHIP_ID [3:0]	Chip ID Shows information about the version of MAX20317							
CHIP_REV [3:0]	Chip Revision Shows information about the revision of MAX20317							

Table 3. ADC1_VAL Register (0x01)

ADDRESS	0x01							
MODE	Read Only							
BIT	7	6	5	4	3	2	1	0
NAME	ADC1_VAL[7:0]							
RESET	0	0	0	0	0	0	0	0
ADC1_VAL [7:0]	ADC1 Value Read only register for the latest ADC1 conversion (8-bit resolution)							

Table 4. ADC2_VAL Register (0x02)

ADDRESS	0x02							
MODE	Read Only							
BIT	7	6	5	4	3	2	1	0
NAME	ADC2_VAL[7:0]							
RESET	0	0	0	0	0	0	0	0
ADC2_VAL [7:0]	ADC2 Value Read only register for the latest ADC2 conversion (8-bit resolution)							

Table 5. STATUS1 Register (0x03)

ADDRESS	0x03							
MODE	Read Only							
BIT	7	6	5	4	3	2	1	0
NAME	IDET_LVL[1:0]		COM_DET	OPEN_ CABLE	JACK_ TYPE	DEVICE_ RDY	EOC1	EOC2
RESET	0	0	0	0	0	0	0	0

IDET_LVL [1:0]	I_{DETIN} Level Shows the last I_{DETIN} current level used in an ADC1 Impedance Detection 00 = No Jack Insertion Default 01 = 100µA 10 = 1.1mA 11 = 5.5mA
COM_DET	Communication Request Status Indicates a valid button press when MIC_IN drops below the threshold set by COM_THRS[1:0] 0 = No communication is requested. 1 = MIC voltage is below threshold after the debounce time.
OPEN_ CABLE	Open Cable Detected Indicates if a cable is an open connection 0 = Cable is not open 1 = High impedance is detected for both CTIA and OMTP, and SET_IDET[1:0] = 01.
JACK_ TYPE	Jack Type Shows the jack type identified by automatic jack detection. This feature is disabled if JACK_TYP_CHK_DIS = 1. 0x0B). 0 = CTIA (L-R-G-M) 1 = OMTP (L-R-M-G)
DEVICE_ RDY	Device Ready Indicates the device is ready for manual control after jack detection is complete. This bit is set after impedance detection if JACK_TYP_CHK_DIS = 1. 0 = MIC/GND switch position has NOT been finalized. 1 = MIC/GND SW position is set. Device is ready.
EOC1	End of ADC1 conversion 0 = ADC1 conversion is not started or is in progress. 1 = ADC1 conversion is complete and the result is available in ADC1_VAL (register 0x01).
EOC2	End of ADC2 conversion 0 = ADC2 conversion is not started or is in progress. 1 = ADC2 conversion is complete and the result is available in ADC2_VAL (register 0x02).

Table 6. STATUS2 Register (0x04)

ADDRESS	0x04							
MODE	Read Only							
BIT	7	6	5	4	3	2	1	0
NAME	VOL_UP	VOL_DWN	VBOOST_OV	MPSs	MIC_IN	SWD	DET	DETIN
RESET	0	0	0	0	0	0	0	0
VOL_UP	Volume Up Status Indicates a volume up press was detected in BYPASS mode. ADC2 Cleared if bypass switch is open or VMIC > COM_THRS[1:0]. Updated in bypass mode with low gain. 0 = No volume up press detected. NOT (VOL1_TH < ADC2 < VOL2_TH) 1 = Volume up press detected VOL1_TH < ADC2 < VOL2_TH							
VOL_DWN	Indicates a volume down press was detected in BYPASS mode. VOL2_TH < ADC2 < VOL3_TH Cleared if bypass switch is open or VMIC > COM_THRS[1:0]. Updated in bypass mode with low gain. Updated in bypass mode with low gain. 0 = No Volume down pressed. NOT (VOL2_TH < ADC2 < VOL3_TH) 1 = Volume down pressed. VOL2_TH < ADC2 < VOL3_TH							
VBOOST_OV	V_{BOOST} Bypass Mode Overvoltage Status 0 = V_{BOOST} operating normally 1 = Overvoltage detected on V_{BOOST} in Bypass Mode							
MPSs	RSEN Overcurrent Status 0 = Current Protection is NOT detected. 1 = Current Protection is Triggered.							
MIC_IN	MIC_IN Switch Status 0 = MIC_IN switch is open 1 = MIC_IN switch is closed							
SWD	SEND/END Status Indicates a SEND/END press was detected in BYPASS mode. VOL0_TH< ADC2 <VOL1_TH Cleared if bypass switch is open or VMIC > COM_THRS[1:0]. Updated in bypass mode with low gain. 0 = No SEND/END press detected. NOT(VOL0_TH< ADC2 <VOL1_TH) 1 = SEND/END press detected. VOL0_TH< ADC2 <VOL1_TH							
DET	Jack Insertion Debounce 0 = Jack was detected after debounce 1 = No jack detected							
DETIN	DETIN Detection 0 = DETIN is detected 1 = DETIN is not detected							

Table 7. STATUS3 Register (0x05)

ADDRESS	0x05							
MODE	Read Only							
BIT	7	6	5	4	3	2	1	0
NAME	ANC_HS	THT_CMP	SAR_CMP	V94_CMP	RFU[2:0]			VOL_RFU
RESET	0	0	0	0	0	0	0	0
ANC_HS	ANC Headset Detection 0 = No ANC headset detected. VRSEN < HSDET_VAL[7:0] 1 = ANC headset detected. VRSEN > HSDET_VAL[7:0]							
THT_CMP	Thermal Comparator Status Output of the analog thermal comparator							
SAR_CMP	SAR Comparator Status Output of the analog SAR comparator							
V94_CMP	V94 Comparator Status Output of the COM_THRS comparator.							
RFU[2:0]	Reserved for future use							
VOL_RFU	Button Press Reserved for Future Use Only. Cleared if bypass is open or VMIC > COM_THRS[1:0]. Updated in BYPASS mode, ADC2 value (VRSEN) with low gain. 0 = No RFU Button pressed. NOT (VOL3_TH < ADC2) 1 = RFU Button pressed. VOL3_TH < ADC2							

Table 8. IRQ Register (0x06)

ADDRESS	0x06							
MODE	Clear On Read							
BIT	7	6	5	4	3	2	1	0
NAME	SWDi	EOCi	COM_DETi	MPS/ VBOOST_ OVi	MIC_INi	DEVICE_ RDYi	DETi	DETINi
RESET	0	0	0	0	0	0	0	0
SWDi	SEND/END Button Press Detection Interrupt 0 = Interrupt not occurred 1 = Interrupt occurred (both edges of SWD)							
EOCi	End of ADC1/2 Conversion Interrupt 0 = Interrupt not occurred 1 = Interrupt occurred (only the rising edge of either EOC1 or EOC2)							
COM_DETi	Communication Request Interrupt (Button Press) in Bypass Mode 0 = Interrupt not occurred 1 = Interrupt occurred (both edges of COM_DET, that is button pressed or released)							
MPS/ VBOOST_ OVi	Microphone line short or Vboost overvoltage interrupt 0 = Interrupt not occurred 1 = Interrupt occurred (only rising edge of either MPS or VBOOST_OV)							
MIC_INi	MIC_IN Switch Open or Close Interrupt 0 = Interrupt not occurred 1 = Interrupt occurred (both edges of MIC_IN)							
DEVICE_ RDYi	DEVICE_RDY MIC/GND Switch position finalized Interrupt 0 = Interrupt not occurred 1 = Interrupt occurred (only rising edge of DEVICE_READY)							
DETi	Jack Insertion and Removal Detection Interrupt 0 = Interrupt not occurred 1 = Interrupt occurred (both edges of debounced DETIN)							
DETINi	DETIN Detection Interrupt 0 = Interrupt not occurred 1 = Interrupt occurred							

Table 9. MASK Register (0x07)

ADDRESS	0x07							
MODE	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	SWDm	EOCm	COM_ DETm	MPS/ VBOOST_ OVm	MIC_INm	DEVICE_ RDYm	DETm	DETINm
RESET	0	0	0	0	0	0	0	0
SWDm	SEND/END Button Press Detection Interrupt Mask 0 = Masked 1 = Not masked							
EOCm	End of ADC Conversion Interrupt Mask 0 = Masked 1 = Not masked							
COM_ DETm	Communication Request Interrupt Mask 0 = Masked 1 = Not masked							
MPS/ VBOOST_ OVm	Microphone Line Short/VBOOST_OV Interrupt Mask 0 = Masked 1 = Not masked							
MICINm	MIC_IN Switch Interrupt Mask 0 = Masked 1 = Not masked							
DEVICE_ RDYm	Device Ready Interrupt Mask 0 = Masked 1 = Not masked							
DETm	Jack Insertion Detection Interrupt Mask 0 = Masked 1 = Not masked							
DETINm	DETIN Detection Interrupt Mask 0 = Masked 1 = Not masked							

Table 10. CONTROL1 Register (0x08)

ADDRESS	0x08							
MODE	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	RFU	DET_ DEBOUNCE	DETIN_ OVERRIDE	MIC_OUT DELAY	RFU	BYPASS	COM_THRS[1:0]	
RESET	0	0**	0**	1**	0	0	0**	1**
RFU	Reserved For Future Use							
DET_ DEBOUNCE	DET Debounce Time 0 = 115ms, 1 = 300ms							
DETIN_ OVERRIDE	DETIN Override 0 = No effect 1 = Simulates a jack insertion.							
MIC_OUT_ DELAY	MIC_OUT Output Delay Control 0 = MIC SW close output follows after DET becomes low 1 = MIC SW close delayed until Impedance detection after DET becomes low							
RFU	Reserved For Future Use							
BYPASS	BYPASS MODE Enable 0 = BYPASS is OFF 1 = BYPASS is ON							
COM_ THRS[1:0]	COM (Button Press) Detection Threshold 00 = 88% 01 = 90% 10 = 92% 11 = 94%							

Table 11. CONTROL2 Register (0x09)

ADDRESS	0x09							
MODE	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	MANUAL_ G_SNS	MANUAL_ MIC_SW	MANUAL_ MG_SW	OPEN_ DETECT	FORCE_ G_SNS	FORCE_ MIC_SW	FORCE_MG_SW [1:0]	
RESET	0	0	0	1	0	0	0	0
MANUAL_ G_SNS	Manual G_SNS Switch Setting 0 = G_SNS operates normally in synch Mic/Ground switch 1 = G_SNS follows FORCE_G_SNS bit							
MANUAL_ MIC_SW	Manual MIC_IN Switch Setting 0 = MIC_SW operates normally 1 = MIC_SW follows FORCE_MIC_SW bit							
MANUAL_ MG_SW	Manual MG Switch Setting 0 = MG_SW operates normally 1 = MG_SW follows FORCE_MG_SW bit							
OPEN_ DETECT	When high, enables the first automatic impedance detection at 100uA.							
FORCE_ G_SNS	FORCE_G_SNS Switch Control (effective only when “MANUAL_G_SNS = 1”) 0 = Close Ring2 to G_SNS pin 1 = Close Sleeve to G_SNS pin							
FORCE_ MIC_SW	Force MIC_IN Switch Control (effective only when “MANUAL_MIC_SW = 1”) 0 = MIC_SW closed 1 = MIC_SW open							
FORCE_ MG_ SW [1:0]	Force MIC/GND Switch Control (effective only when “MANUAL_MG_SW = 1”) 00 = Switches closed in CTIA position 01 = Both MIC-side switches OPEN, ground connection in CTIA position 10 = Switches closed in OMTP position 11 = Both MIC-side switches OPEN, ground connection in OMTP position							

Table 12. ADC CONTROL1 Register (0x0A)

ADDRESS	0x0A							
MODE	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	IDET_ FLAT	JACK_TYP _CHK_DIS	RFU	ADC1_LI _CHK	ADC1_CTL [1:0]		ADC2_CTL [1:0]	
RESET	0**	0**	0	1	1	1	1	1
IDET_FLAT	Flat top period of the IDET for ADC conversion (OTP programmable) 0 = 10msec 1 = 100msec							
JACK_ TYP_CHK_ DIS	CTIA/OMTP Jack Type Detection Disable (OTP programmable) 0 = Automatic Jack Type Detection 1 = Disabled.							
RFU	Reserved For Future Use							
ADC1_ LI_CHK	ADC1 Low Impedance Check 0 = Disable the 1.1mA/5.5mA impedance detection if ADC1 < HIHS_VAL 1 = Enable the 1.1mA/5.5mA impedance detection if ADC1 < HIHS_VAL							
ADC1_CTL [1:0]	ADC1 Conversion Control 00 = impedance detection and A-D conversion are always off. 01 = impedance detection is manual and one conversion when forced. 10 = impedance detection is manual and multiple (ADC1_AVG#) conversions and averaged. 11 = ADC follows FSM. (After DET = 0 transition)							
ADC2_CTL [1:0]	ADC2 Conversion Control 00 = impedance detection and A-D conversion are always off. 01 = impedance detection is manual and one conversion when forced. 10 = impedance detection is manual and multiple (ADC2_AVG#) conversions and averaged. 11 = ADC2 follows FSM. If COM_DET = 0, set ADC2_HL_SET = 1, ADC2 one averaged conversion after tANC_DET from Bypass on =1. ADC2_HL_SET = 0, While COM_DET = 1, ADC2 conversion continuous.							

Table 13. ADC2 CONTROL Register (0x0B)

ADDRESS	0x0B							
MODE	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	RFU		SET_IDET[1:0]		RFU	ADC2_HL	FORCE_ ADC1_ START	FORCE_ ADC2_ START
RESET	0	0	0	0	0	0	0	0
RFU	Reserved For Future Use							
SET_IDET [1:0]	Set I_{DETIN} Set the I_{DETIN} current level in manual ADC1 mode. This should be used with Force_ADC1_START 00 = Do not use 01 = 100µA 10 = 1.1mA 11 = 5.5mA							
RFU	Reserved For Future Use							
ADC2_HL	ADC2 ANC Headset Detection Method Selection. 0 = ANC Comparator Low Gain; used for ANC Button detection 1 = ANC Comparator High Gain; used for ANC HS detection							
FORCE_ ADC1_ START	Force ADC1 Start Execute a manual ADC1 measurement when ADC1_CTL[1:0] = 01 or 10 0 = ADC1 operates normally 1 = ADC1 start (only one conversion). End of conversion set the EOC status set.							
FORCE_ ADC2_ START	Force ADC2 Start Execute a manual ADC2 measurement when ADC2_CTL[1:0] = 01 or 10 0 = ADC2 operates normally 1 = ADC2 start (only one conversion). End of conversion set the EOC status set.							

Table 14. Register (0x0C)

ADDRESS	0x0C							
MODE	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	ADC1_AVG# [1:0]		ADC2_AVG# [1:0]		tANCDET_DEB [1:0]		tANCBPD_DEB [1:0]	
RESET	0**	0**	0**	0**	0**	0**	0**	0**
ADC1_AVG #[1:0]	ADC1 Averaging Number Sets the number of samples to average when ADC1_CTL[1:0] = 10 00 = 2 01 = 4 10 = 8 11 = 16							
ADC2_AVG #[1:0]	ADC2 Averaging Number Sets the number of samples to average when ADC2_CTL[1:0] = 10 00 = 2 01 = 4 10 = 8 11 = 16							
tANCDET_ DEB [1:0]	ANC Headset Detection Debounce Time 00 = 20ms 01 = 30ms 10 = 50ms 11 = 100ms							
tANCBPD_ DEB [1:0]	ANC Button Press Detection Debounce Time 00 = 20ms 01 = 30ms 10 = 50ms 11 = 100ms							

Table 15. Short Current Control Register (0x0D)

ADDRESS	0x0D							
MODE	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	FU[5:0]						tSHO_DEB[1:0]	
RESET		0**	0**	0**	0**	0**	0**	0**
FU [5:0]	Factory Use Only. Do not overwrite							
tSHO_DEB [1:0]	Short Circuit Debounce Sets the debounce time for short-circuit current protection 00 = 360µs 01 = 600µs 10 = 1080µs 11 = 1920µs							

Table 16. HIHS_VAL Register (0x0E)

ADDRESS	0x0E							
MODE	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	HIHS_VAL[7:0]							
RESET	0	0	0	0	0	0	0	0
HIHS_VAL [7:0]	High impedance threshold for ADC1 conversions.							

Table 17. OMTP_VAL Register (0x0F)

ADDRESS	0x0F							
MODE	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	OMTP_VAL[7:0]							
RESET	0	0	0	0	0	0	0	0
OMTP_VAL [7:0]	OMTP Headset Detection Threshold for ADC1 conversion.							

Table 18. HSDET_VAL Register (0x10)

ADDRESS	0x10							
MODE	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	HSDET_VAL[7:0]							
RESET	0	0	0	0	0	0	0	0
HSDET_ VAL[7:0]	ANC Headset Detection Threshold for ADC2 conversion when ADC_HL_SET = 1. If ADC2>HSDET_VAL, then set ANC_HS (0x05h bit7) = 1.							

Table 19. VOL0_TH Register (0x11)

ADDRESS	0x11							
MODE	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	VOL0_TH[7:0]							
RESET	0	0	0	0	0	0	0	0
VOL0_TH [7:0]	Headset Button Detection Threshold in BYPASS mode for ADC2 conversion. Higher than or equal to this value and lower than VOL1_TH[7:0] means the SEND/END button is pressed.							

Table 20. VOL1_TH Register (0x12)

ADDRESS	0x12							
MODE	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	VOL1_TH[7:0]							
RESET	0	0	0	0	0	0	0	0
VOL1_TH [7:0]	Headset Button Detection Threshold in BYPASS mode for ADC2 conversion. Higher than or equal to this value and lower than VOL2_TH means the Volume up button is pressed.							

Table 21. VOL2_TH Register (0x13)

ADDRESS	0x13							
MODE	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	VOL2_TH[7:0]							
RESET	0	0	0	0	0	0	0	0
VOL2_TH [7:0]	Headset Button Detection Threshold in BYPASS mode for ADC2 conversion. Higher than or equal to this value and lower than VOL3_TH means the Volume down button is pressed.							

Table 22. VOL3_TH Register (0x14)

ADDRESS	0x14							
MODE	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	VOL3_TH[7:0]							
RESET	0	0	0	0	0	0	0	0
VOL3_TH [7:0]	Headset Button Detection Threshold in BYPASS mode for ADC2 conversion. Higher than or equal to this value means the reserved button is pressed.							

Table 23. PLC_STAT: POWER LINE COMMUNICATION STATUS Register (0x15)

ADDRESS	0x15							
MODE	Read Only							
BIT	7	6	5	4	3	2	1	0
NAME	RFU[1:0]		PLC_TX_ ERR	PLC_TX_ OK	PLC_TX_P	PLC_RX_ ERR	NEW_ DATA	PLC_RX_ DET
RESET	0	0	0	0	0	0	0	0
RFU[1:0]	Reserved for Future Use							
PLC_TX_ ERR	Power Line Communication TX Error Cleared when a new SEND_CMD is issued. 0 = No TX Error 1 = TX Error							
PLC_TX_ OK	Power Line Communication TX Successful Cleared when the new SEND_CMD issued. 0 = Communication not successful 1 = Communication successful							
PLC_TX_P	Power Line Communication TX in Progress 0 = Not Transmitting 1 = PLC Transmitting in progress							
PLC_RX_ ERR	Power Line Communication RX Error 0 = No error 1 = Error (start bit, parity, checksum or stalled line).							
NEW_ DATA	New Data Available Indicates that new data is available. Once ACC_ID/ACC_DB1/ACC_DB2 are read, it is cleared. 0 = No New Data Set 1 = New Data Set Arrived							
PLC_RX_ DET	Power Line Communication Receiving Detection (only during preamble and data excluding post-amble) 0 = No PLC (within 4-bit length of no or invalid signal) 1 = PLC is ongoing (within 4-bit of preamble signal)							

Table 24. PLC_IRQ: POWER LINE COMMUNICATION INTERRUPT Register (0x16)

ADDRESS	0x16							
MODE	Read Only							
BIT	7	6	5	4	3	2	1	0
NAME	RFU[1:0]		PLC_TX_ ERRi	PLC_TX_ OKi	PLC_TX_Pi	PLC_RX_ ERRi	NEW_ DATAi	PLC_RX_ DETi
RESET	0	0	0	0	0	0	0	0

RFU[1:0]	Reserved For Future Use
PLC_TX_ ERRi	Power Line Communication TX Error Interrupt 0 = Interrupt Not occurred 1 = Interrupt occurred (rising edge of PLC_TX_ERR)
PLC_TX_ OKi	Power Line Communication TX OK Interrupt 0 = Interrupt Not occurred 1 = Interrupt occurred (rising edge of PLC_TX_OK)
PLC_TX_ Pi	Power Line Communication TX in Progress Interrupt 0 = Interrupt Not occurred 1 = Interrupt occurred (both edges of PLC_TX_P)
PLC_RX_ ERRi	Power Line Communication RX Error Interrupt 0 = Interrupt not occurred 1 = Interrupt occurred (rising edge of PLC_RX_ERR)
NEW_ DATAi	New Data RX Interrupt. 0 = Interrupt Not occurred 1 = Interrupt occurred (rising edge of NEW_DATA)
PLC_RX_ DETi	Power Line Communication RX Detection Interrupt 0 = Interrupt Not occurred 1 = Interrupt occurred (both edges of PLC_RX_DET)

Table 25. PLC_MASK: POWER LINE COMMUNICATION MASK Register (0x17)

ADDRESS	0x17							
MODE	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	RFU[1:0]		PLC_TX_ ERRm	PLC_TX_ OKm	PLC_TX_ Pm	PLC_RX_ ERRm	NEW_ DATAm	PLC_RX_ DETm
RESET	0	0	0	0	0	0	0	0

RFU[1:0]	Reserved For Future Use
PLC_TX_ ERRM	PLC TX Error Interrupt Mask. 0 = Masked 1 = Not masked
PLC_TX_ OKm	PLC TX Successful Interrupt Mask. 0 = Masked 1 = Not masked
PLC_TX_ Pm	PLC TX in Progress Interrupt Mask. 0 = Masked 1 = Not masked
PLC_RX_ ERRm	PLC_RX_ERR mask 0 = Masked 1 = Not masked
NEW_ DATAm	New Data Interrupt Mask. 0 = Masked 1 = Not masked
PLC_RX_ DETm	Power Line Communication Receiving Detection Interrupt Mask. 0 = Masked 1 = Not masked

Table 26. PLC_CON1: POWER LINE COMMUNICATION CONTROL Register (0x18)

ADDRESS	0x18							
MODE	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	RFU	PLC_SINK	POST_ AM_DIS	FREQ	PARITY[1:0]		RFU	SEND_ CMD
RESET	0	0	0	0	0	1	0	0
RFU	Reserved for Future Use							
PLC_SINK	PLC Current Sink Selection 0 = 100mA 1 = 80mA							
POST_ AM_DIS	Transmit Post-Amble Disable 0 = Post-amble enabled. The transmitter sends 2000 low bits. The receiver expects at least 16 low bits as a proper post-amble. 1 = Post-amble disabled							
FREQ	Communication Time Unit 0 = 24µsec 1 = 30µsec							
PARITY [1:0]	Parity Bit 00/11 = No Parity. A high parity bit is transmitted, but is ignored by the receiver. 01 = Odd 10 = Even							
RFU	Reserved for Future Use							
SEND_ CMD	Send Command Send the address (ACC_ADD) and data (ACC_DATA) bytes to the slave. Clears on completion of data transmission. 0 = No action 1 = Transfer the data							

Table 27. ACCESSORY ID Register (0x19)

ADDRESS	0x19							
MODE	Read Only							
BIT	7	6	5	4	3	2	1	0
NAME	ACC_ID[3:0]				ACC_CAT[3:0]			
RESET	0	0	0	0	0	0	0	0
ACC_ID [3:0]	Accessory ID Upper four bits of the first valid transmission. Four bit ID of the connected accessory.							
ACC_CAT [3:0]	Accessory Category Lower four bits of the first valid transmission. Accessory category or revision information.							

Table 28. ACC_DATA1 Receive Register (0x1A)

ADDRESS	0x1A							
MODE	Read Only							
BIT	7	6	5	4	3	2	1	0
NAME	ACC_DATA1[7:0]							
RESET	0	0	0	0	0	0	0	0
ACC_ DATA1[7:0]	Accessory Data 1 First byte of raw data read from accessory							

Table 29. ACC_DATA2 Receive Register (0x1B)

ADDRESS	0x1B							
MODE	Read Only							
BIT	7	6	5	4	3	2	1	0
NAME	ACC_DATA2[7:0]							
RESET	0	0	0	0	0	0	0	0
ACC_ DATA2[7:0]	Accessory Data 2 Second byte of raw data read from accessory							

Table 30. ACC_ADD Transmit Register (0x1C)

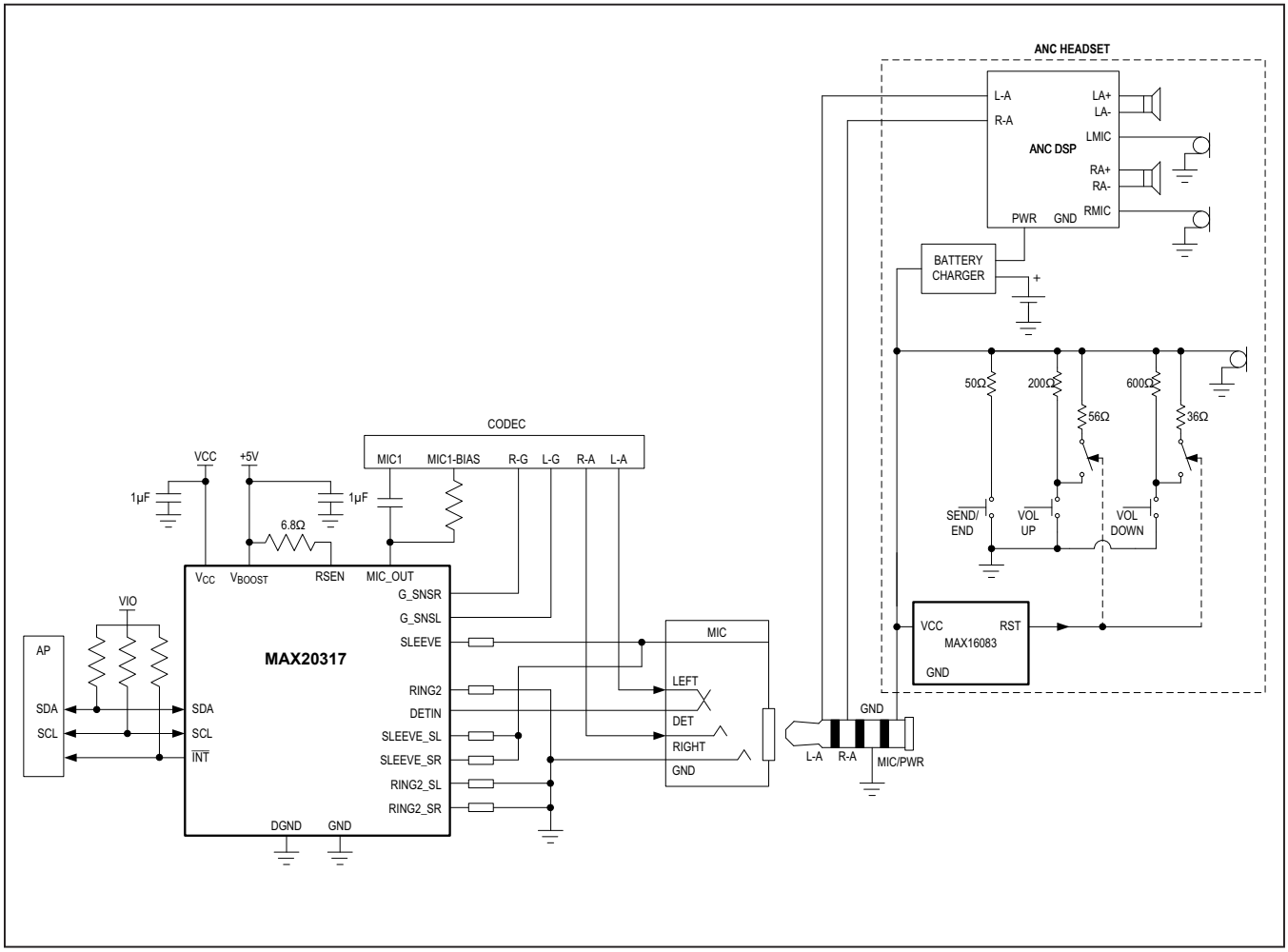
ADDRESS	0x1C							
MODE	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	ACC_ADD[7:0]							
RESET	0	0	0	0	0	0	0	0
ACC_ ADD[7:0]	Accessory Target Address							

Table 31. ACC_DATA Transmit Register (0x1D)

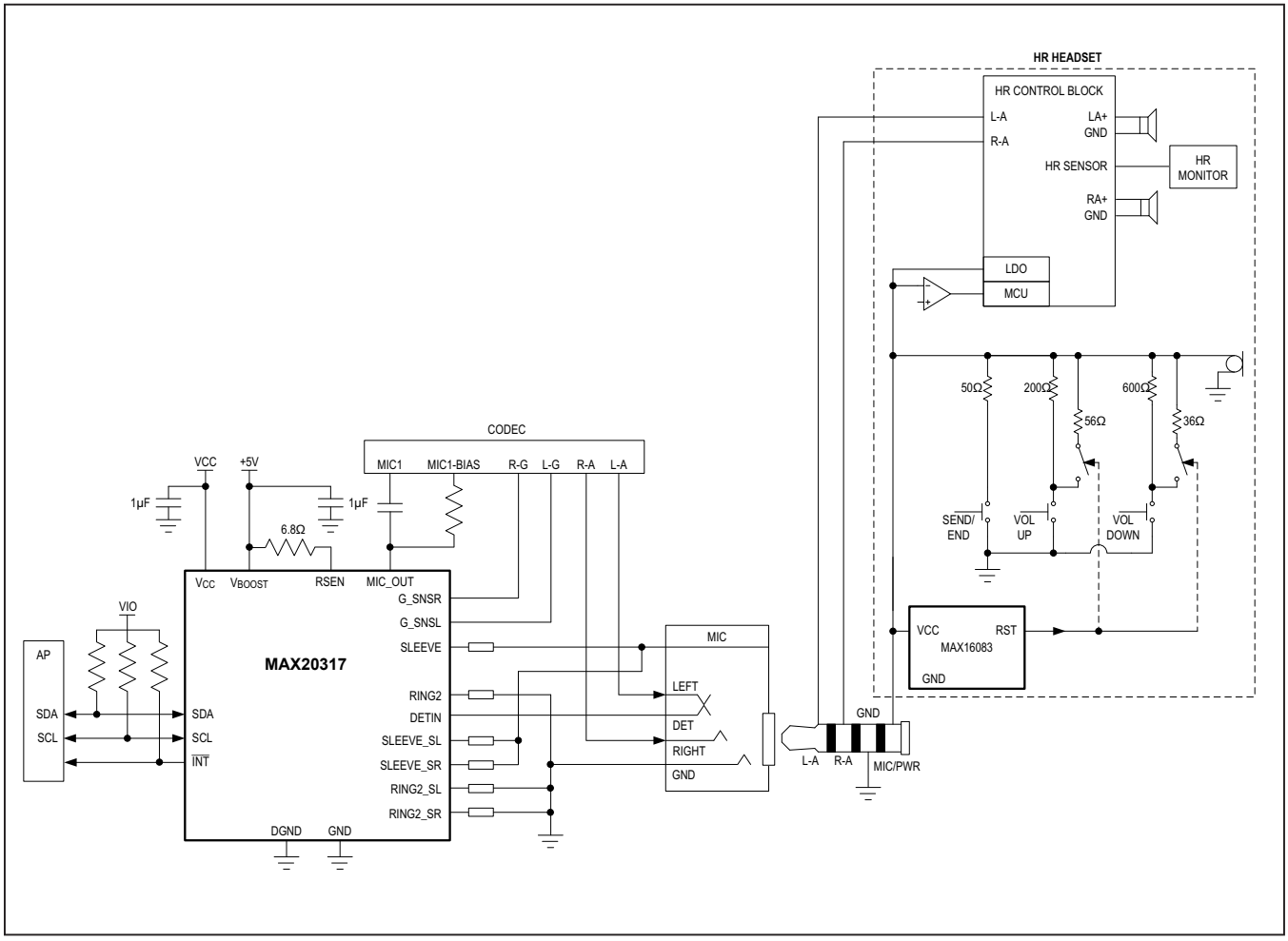
ADDRESS	0x1D							
MODE	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	ACC_DATA[7:0]							
RESET	0	0	0	0	0	0	0	0
ACC_ DATA[7:0]	Accessory Target Data							

***Denotes a factory programmable value*

Application Circuits



Application Circuits (continued)



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX20317EWP+	-40°C to +85°C	20 WLP
MAX20317EWP+T	-40°C to +85°C	20 WLP

+Denotes a lead(Pb)-free/RoHS-compliant package.

T Denotes tape-and-reel

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
20 WLP	W201H2+1	21-100120	Refer to Application Note 1891

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/17	Initial release	—

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

Maxim Integrated cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim Integrated product. No circuit patent licenses are implied. Maxim Integrated reserves the right to change the circuitry and specifications without notice at any time. The parametric values (min and max limits) shown in the Electrical Characteristics table are guaranteed. Other parametric values quoted in this data sheet are provided for guidance.

LifeElectronics
Живое партнерство

ООО «ЛайфЭлектроникс» **“LifeElectronics” LLC**

ИНН 7805602321 КПП 780501001 Р/С 40702810122510004610 ФАКБ "АБСОЛЮТ БАНК" (ЗАО) в г.Санкт-Петербурге К/С 30101810900000000703 БИК 044030703

Компания «Life Electronics» занимается поставками электронных компонентов импортного и отечественного производства от производителей и со складов крупных дистрибьюторов Европы, Америки и Азии.

С конца 2013 года компания активно расширяет линейку поставок компонентов по направлению коаксиальный кабель, кварцевые генераторы и конденсаторы (керамические, пленочные, электролитические), за счёт заключения дистрибьюторских договоров

Мы предлагаем:

- *Конкурентоспособные цены и скидки постоянным клиентам.*
- *Специальные условия для постоянных клиентов.*
- *Подбор аналогов.*
- *Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.*

- *Приемлемые сроки поставки, возможна ускоренная поставка.*
- *Доставку товара в любую точку России и стран СНГ.*
- *Комплексную поставку.*
- *Работу по проектам и поставку образцов.*
- *Формирование склада под заказчика.*

- *Сертификаты соответствия на поставляемую продукцию (по желанию клиента).*
- *Тестирование поставляемой продукции.*
- *Поставку компонентов, требующих военную и космическую приемку.*
- *Входной контроль качества.*
- *Наличие сертификата ISO.*

В составе нашей компании организован Конструкторский отдел, призванный помогать разработчикам, и инженерам.

Конструкторский отдел помогает осуществить:

- *Регистрацию проекта у производителя компонентов.*
- *Техническую поддержку проекта.*
- *Защиту от снятия компонента с производства.*
- *Оценку стоимости проекта по компонентам.*
- *Изготовление тестовой платы монтаж и пусконаладочные работы.*

Тел: +7 (812) 336 43 04 (многоканальный)
Email: org@lifeelectronics.ru

www.lifeelectronics.ru