Si5317-EVB

Si5317 Evaluation Board User's Guide

Description

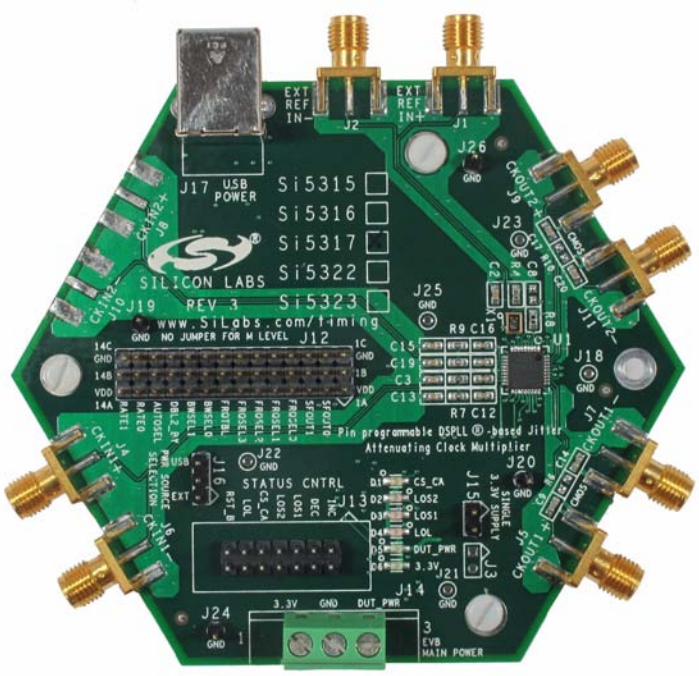
The Si5317-EVB User's Guide provides a complete and simple evaluation of the functions, features, and performance of the Si5317.

The Si5317 is a pin-controlled 1:1 jitter-attenuating clock for high-performance applications.

The Si5317 is based on Silicon Laboratories' 3rd-generation DSPLL® technology, which provides any-rate jitter attenuation in a highly integrated PLL solution that eliminates the need for external VCXO and loop filter components. The DSPLL loop bandwidth is user programmable, providing jitter performance optimization at the application level.

Features

- No software required. Simple jumpers for device configuration
- Fully powered from either a single USB port or an external power supply
- Selectable external reference clock or on-board crystal
- Status LEDs
- Header to connect to external test equipment for automated testing



1. Functional Block Diagram

A functional block diagram of the EVB is shown in Figure 1. The Si5317-EVB provides alarm and status outputs, programmable output clock signal format (LVPECL, LVDS, CML, CMOS), selectable loop bandwidths, and ultra low jitter.

The Si5317 accepts a single clock input ranging from 1 MHz to 710 MHz and generates two equal frequency clock outputs ranging from 1 to 710 MHz. The clock frequency range and loop bandwidth are selectable from a simple look-up table. The Si5317-EVB has a differential clock input that is AC terminated to 50 Ω and then AC-coupled to the Si5317. The two clock outputs are AC-coupled. The XA-XB reference is usually a 114.285 MHz crystal; but there are provisions for an external XA-XB reference (either differential or single-ended). The device status are available on a ribbon header and LEDs. Control pins are strapped using jumper headers for device configuration and various board options. The board can be powered using either external power supplies or from a PC's USB port. Refer to the Si5317 data sheet for technical details of the device.

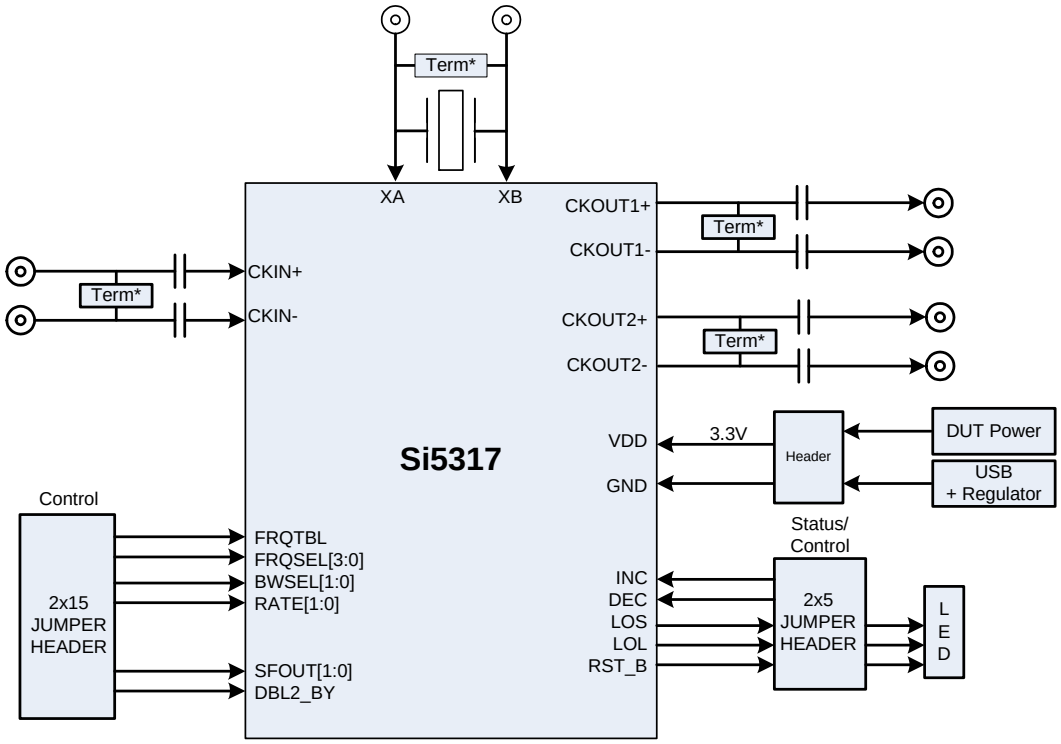


Figure 1. Si5317 EVB Block Diagram

2. Si5317-EVB Input and Output Clocks

2.1. Input Clocks

The Si5317-EVB has a differential clock input that is ac terminated and ac coupled before being presented to the Si5317. If the input clock frequencies are low (below 10 MHz), there are extra considerations that should be taken into account. The Si5317 has a maximum clock input rise time specification of 11 ns that must be met (see CKNtrf in the Si5317 data sheet). Also, if the input clock is LVCMOS, it might be advantageous to replace the input coupling capacitors (C7, C12, C16. and C18) with 0 Ω resistors. When using LVCMOS inputs, the user should consider removing the ac termination and using source series termination located at the driving source. Regardless of the input format, if the clock inputs are not approximately 50% duty cycle, it is highly recommended to avoid ac coupling. For input clocks that are far off of 50% duty cycle, the average value of the signal that passes through the coupling capacitor will be significantly off of the midpoint between the maximum and minimum value of the clock signal, resulting in a mismatch with the common mode input threshold voltage (see Vicm, in the Si5317 data sheet).

2.2. XA-XB Reference

To achieve a very low jitter generation and for stability during holdover, the Si5317 requires a stable, low jitter reference at its XA-XB pins. To that end, the EVB is configured with a 114.285 MHz third overtone crystal connected between pins 6 and 7 of the Si5317. However, the Si5317-EVB is also capable of using an external XA-XB reference oscillator, either differential or single-ended. For details concerning the allowed XA-XB reference frequencies and their RATE settings, see the Si5317 data sheet. J1 and J2 are the SMA connectors with ac termination. AC coupling is also provided that needs to be installed at C6 and C8. Table 1 explains the component changes that are needed to implement an external XA-XB reference oscillator.

Table 1. XA-XB Reference Connections

	Mode	
	Xtal	**Ext Ref**
Ext Ref In+	NC	J1
Ext Ref In-	NC	J2
C6, C8	NOPOP	install
R8	install	NOPOP
RATE0(See note 4)	M	H
RATE1(See note 4)	M	M

Notes:
1. Xtal is 114.285 MHz.
2. NC - no connect.
3. NOPOP - do not install.
4. J12 jumper, see Table 3.
5. C6 on bottom of the board.

2.3. Output Clock

The clock outputs are AC-coupled and are available on SMAs J5, J7, J9 and J11. For LVCMOS outputs, it might be desirable to replace the AC coupling capacitors (C9,C14,C17, and C20) with 0 Ω resistors. Also, if greater drive strength is desired for an LVCMOS output, R6 and R10 can be installed.

2.4. Pin Configuration

J12 is the large jumper header in the center left of the board that implements the jumper plugs that configure the pins of the Si5317. Each pin can be strapped to become either H, M, or L. The H level is achieved by installing a jumper plug between the appropriate middle row pin and its VDD row pin. L is achieved by installing a jumper plug between the appropriate middle row pin and its GND row pin. M is achieved by installing no jumper plug.

2.5. Evaluation Board Power

The EVB can be powered from two possible sources: USB or external supplies. A 3.3 V supply is required to run the LEDs because of their rather large forward drop. The Si5317 power supply can be separated from the 3.3 V supply so that the Si5317 can be evaluated at a voltage other than 3.3 V. It is important to note that when the USB supply is being used, the EVB uses the USB port only for power and that the resulting power supply is strictly 3.3 V.

Here are the instructions for the various possibilities:

2.5.1. External Power Supplies

Install a jumper between J16.1 and J16.2 (labeled EXT).

There should be no USB connection.

If the Si5317 is not being operated at 3.3 V, two supplies should be connected to J14. Connect the 3.3 V supply to J14.1 and J14.2 (labeled 3.3 V and GND). Connect the SI5317 power supply between J14.2 and J14.3 (labeled GND and DUT).

If the Si5317 is to be operated at 3.3 V, J15 (labeled ONE PWR) can be installed, requiring only one external supply. Connect 3.3 V power between J14.2 and J14.3 (labeled GND and DUT).

2.5.2. USB Power

Install a jumper between J16.2 and J16.3 (labeled USB).

Install a jumper at J15 (labeled ONE PWR).

With a USB cable, plug the EVB into a powered USB port.

2.5.3. USB 3.3V Power, External Si5317 Power

Install a jumper between J16.2 and J16.3 (labeled USB).

No jumper at J15 (labeled ONE PWR).

Connect the Si5317 power supply between J14.2 and J14.3 (labeled GND and DUT).

3. Connectors and LEDs

3.1. LEDs

Table 2. LED Descriptions

LED	Label	Significance
D1	CS_CA	Not used
D2	LOS2	Not used
D3	LOS1	ON = no valid clock input
D4	LOL	ON = Si5317 is not locked
D5	DUT_PWR	ON = Si5317 power is present
D6	3.3V	ON = 3.3 V power is present

3.2. Jumpers, Headers, and Connectors

Refer to Figure 2 to locate the items described in this section.

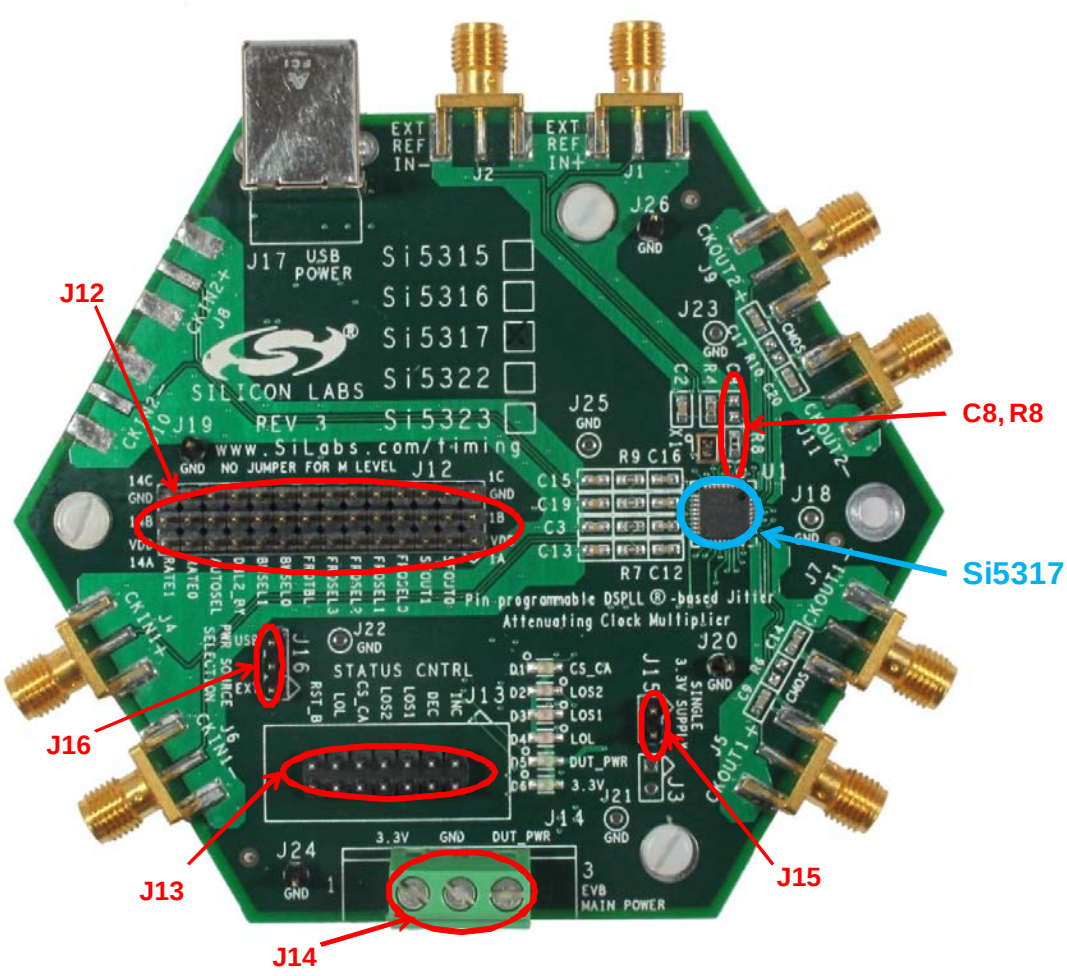


Figure 2. EVB Jumper Locations

Table 3. Configuration Header, J12

J12	Pin
J12.1	not used
J12.2	SFOUT0
J12.3	SFOUT1
J12.4	FRQSEL0
J12.5	FRQSEL1
J12.6	FRQSEL2
J12.7	FRQSEL3
J12.8	FRQTBL
J12.9	BWSEL0
J12.10	BSWEL1
J12.11	DBL2_BY
J12.12	not used
J12.13	RATE0
J12.14	RATE1

Table 4. Status Indication Header, J13

J13	Signal
J13.1	INC
J13.3	DEC
J13.5	LOS
J13.7	Not used
J13.9	Not used
J13.11	LOL
J13.13	RST_B

4. Schematic

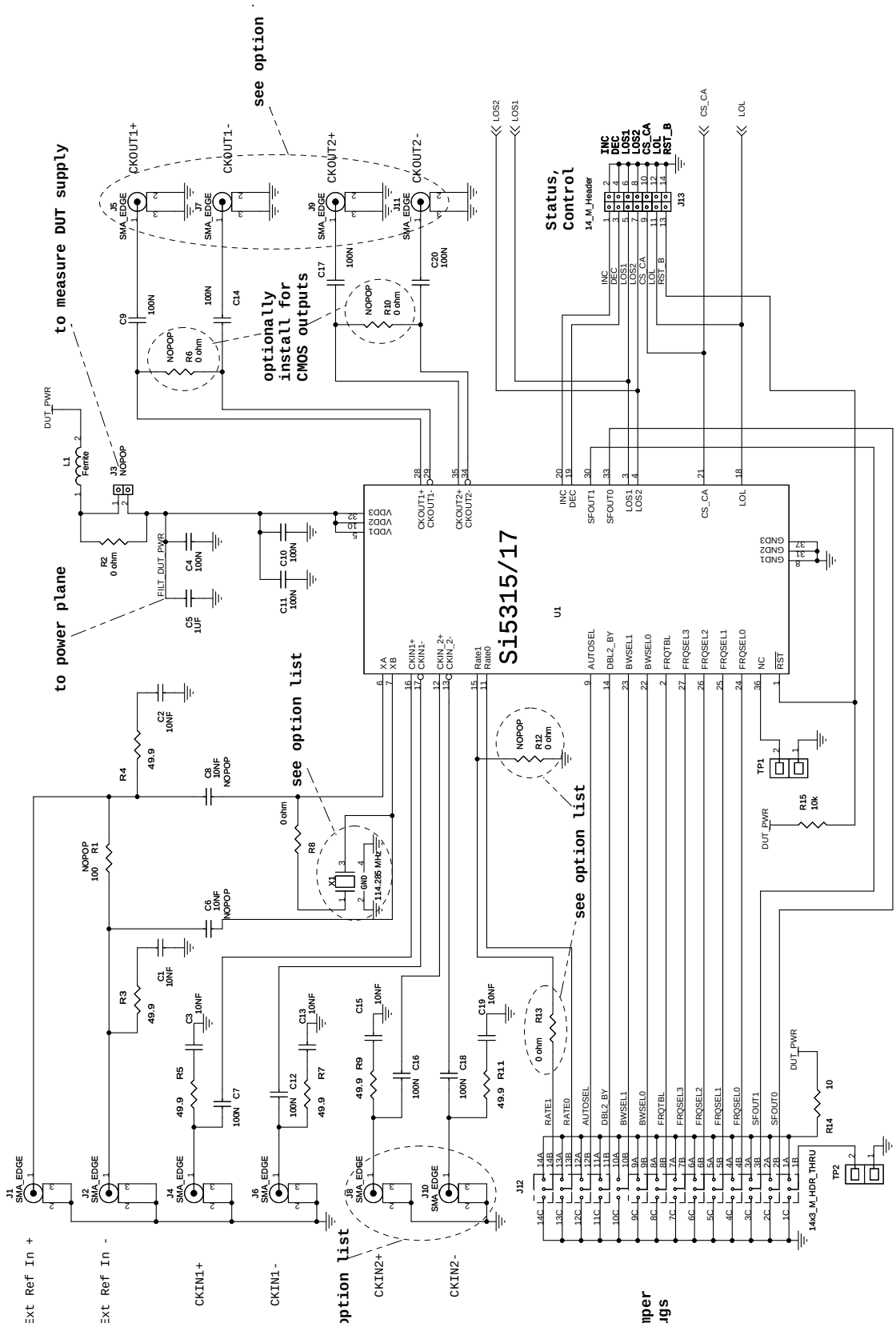


Figure 3. Si5317-EVB

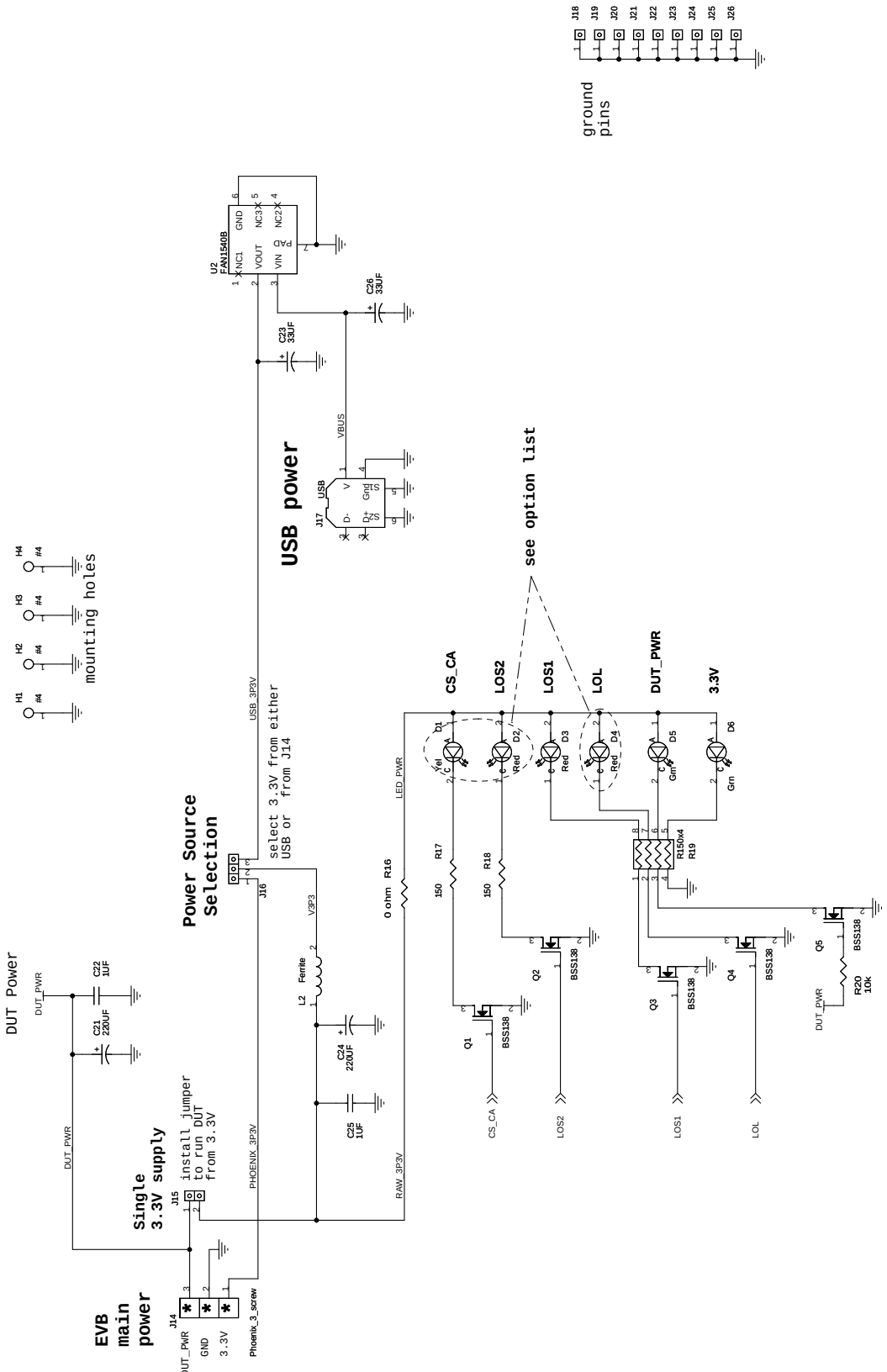


Figure 4. LED and Power/USB

5. Bill of Materials

Item	Qty	Reference	Part	Mfr	MfrPartNum	BOM	Digikey	Footprint
1	6	C1,C2,C3, C13,C15, C19	10NF	Venkel	C0603X7R160-103KNE			603
2	11	C4,C7,C9, C10,C11, C12,C14,	100N	Venkel	C0603X7R160-104KNE			603
		C16,C17, C18,C20						
3	3	C5,C22,C25	1UF	Venkel	C0603X7R6R3-105KNE			603
5	2	C21,C24	220UF	Kemet	T494B227M004AT		399-4631-1-ND	SM_C_3528_21
6	2	C23,C26	33UF	Venkel	TA006TCM336MBR			3528
7	1	D1	Yel	Panasonic	LN1471YTR		P11125CT-ND	LED_gull
8	3	D2,D3,D4	Red	Lumex	LN1271RAL		P493CT-ND	LED_gull
9	2	D5,D6	Grn	Panasonic	LN1371G		P491CT-ND	LED_gull
11	10	J1,J2,J4,J5, J6,J7,J8,J9,	SMA_ EDGE	Johnson	142-0701-801		J502-ND	SMA_EDGE_p062
		J10,J11						
13	1	J12	14x3_M_HDR_THRU	any	two and one row side by side			20x3_M_HDR_THRU
15	1	J14	Phoenix_3_screw	Phoenix	MKDSN 1.5/3-5.08		277-1248-ND	Phoenix3pinM_p2pitch
16	1	J15	Jmpr_2pin					
17	1	J16	Jmpr_3pin					3pin_p1pitch
18	1	J17	USB	FCI	61729-0010BLF		609-1039-ND	USB_typeB
19	4	J19,J20,J24, J26	Jmpr_1pin					1pin_p1pitch
20	2	L1,L2	Ferrite	Venkel	FBC1206-471H			1206
21	5	Q1,Q2,Q3, Q4,Q5	BSS138	On Semi	BSS138LT1G		BSS138LT10SCT-ND	SOT23

Item	Qty	Reference	Part	Mfr	MfrPartNum	BOM	Digikey	Footprint
23	4	R2,R8,R13, R16	0 ohm	Venkel	CR0603-16W-000T			603
24	6	R3,R4,R5, R7,R9,R11	49.9	Venkel	CR0603-16W-49R9FT			603
26	1	R14	10	Venkel	CR0603-16W-10R0FT			603
27	2	R15,R20	10k	Venkel	CR603-16W-1002FT			603
28	2	R17,R18	150	Venkel	CR0603-16W-1500FT			603
29	1	R19	R150x4	Panasonic	EXB-38V151JV		Y9151CT-ND	1206x4
31	1	U1	Si5317	Silicon Labs	Si5317A-C-GM			QFN-36
32	1	U2	FAN1540B	Fairchild	FAN1540BPMX		FAN1540 BMPXCT-ND	MLP6
33	1	X1	114.285 MHz	TXC	7MA1400014			xtal 3.2 x 2.5
34	3		standoff	SPC Tech	2397			
35	3		spacer	Richco	NSS-4-4-01			
4	2	C6,C8	10NF	Venkel	C0603X7R160-103KNE	NOPOP		603
12	1	J3	Jmpr_2pin			NOPOP		
22	1	R1	100	Venkel	CR0603-16W-1000FT	NOPOP		603
25	3	R6,R10,R12	0 Ω	Venkel	CR0603-16W-000T	NOPOP		603
30	2	TP1,TP2	test_points			NOPOP		
14	1	J13	14_M_ Header	3M	N2514-6002RB	NOPOP	MHC14K-ND	14pinMdualHeader_p1 pitch
19	9	J18,J21,J22, J23,J25	Jmpr_1pin			NOPOP		1pin_p1pitch

6. Layout

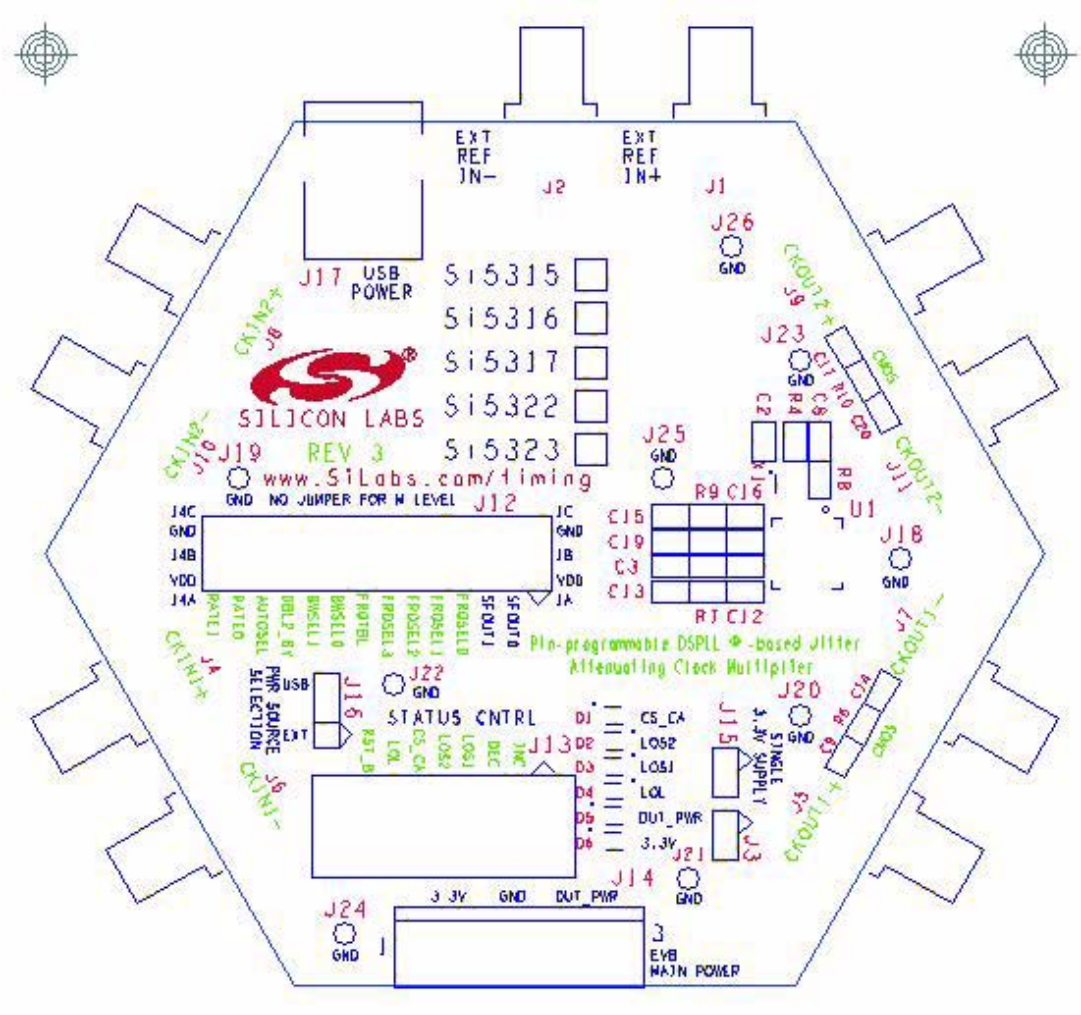


Figure 5. Silkscreen Top

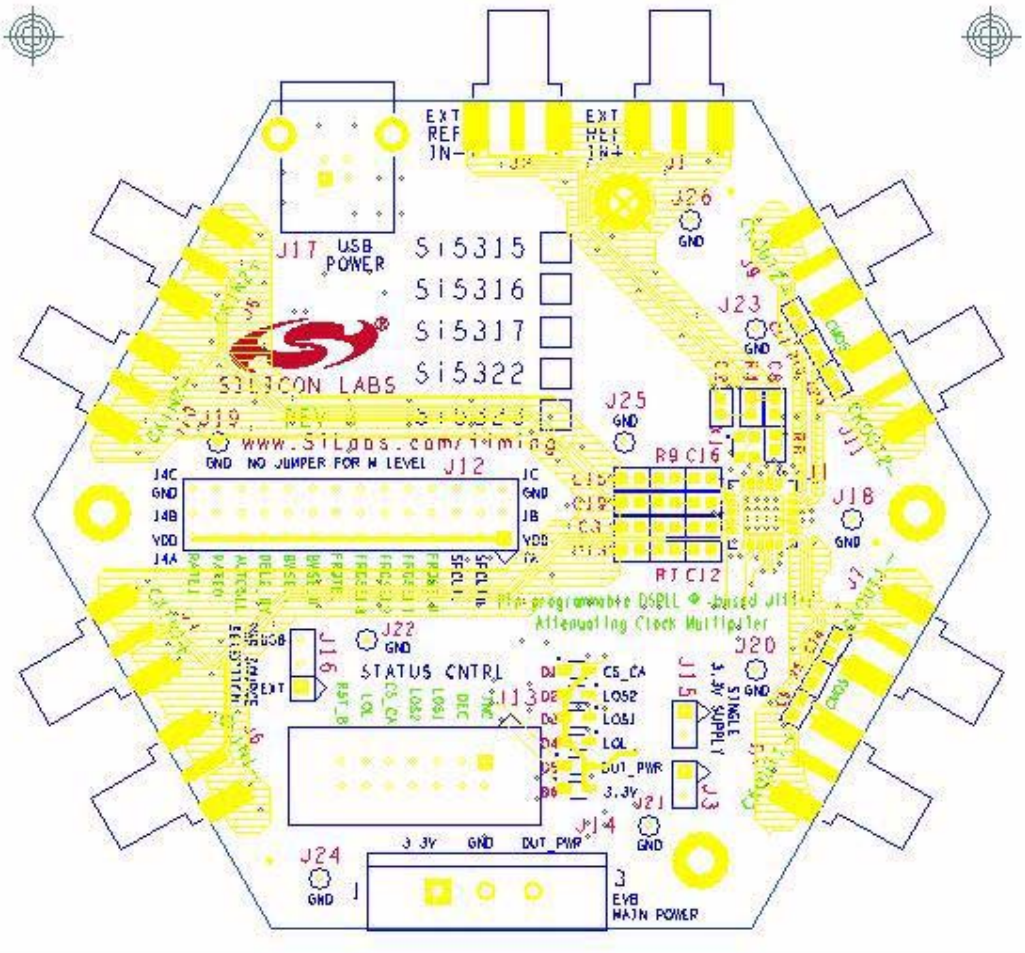


Figure 6. Layer 1

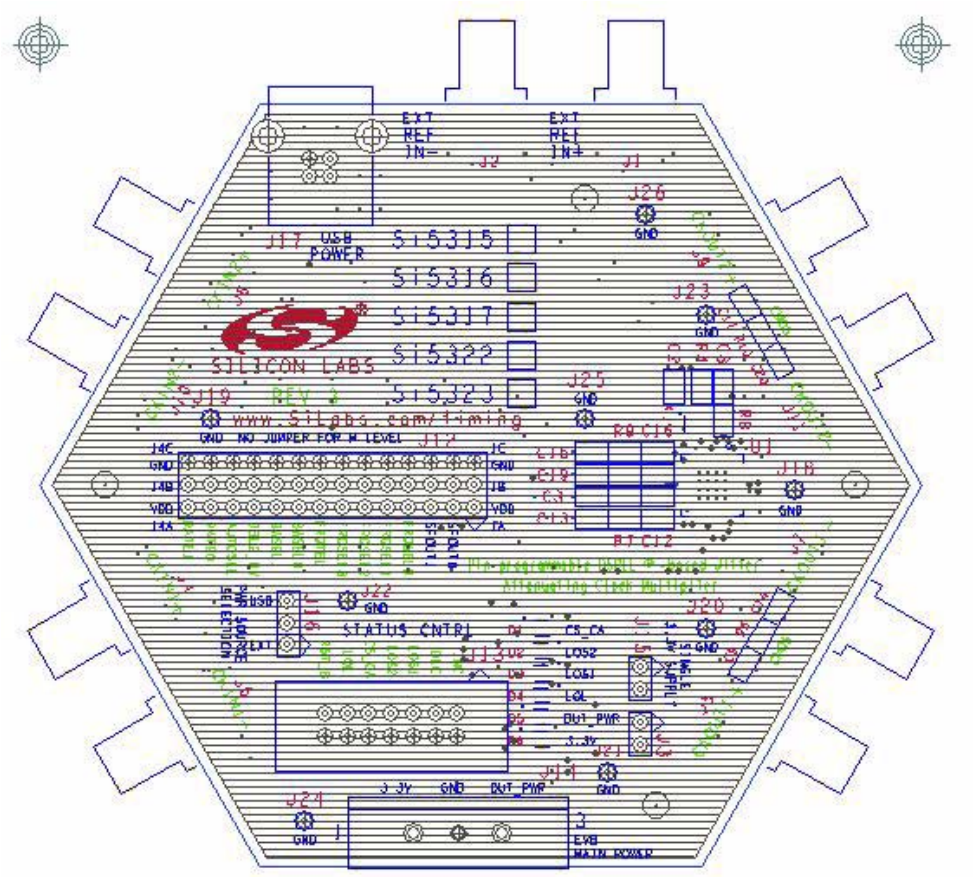


Figure 7. Layer 2—Ground Plane

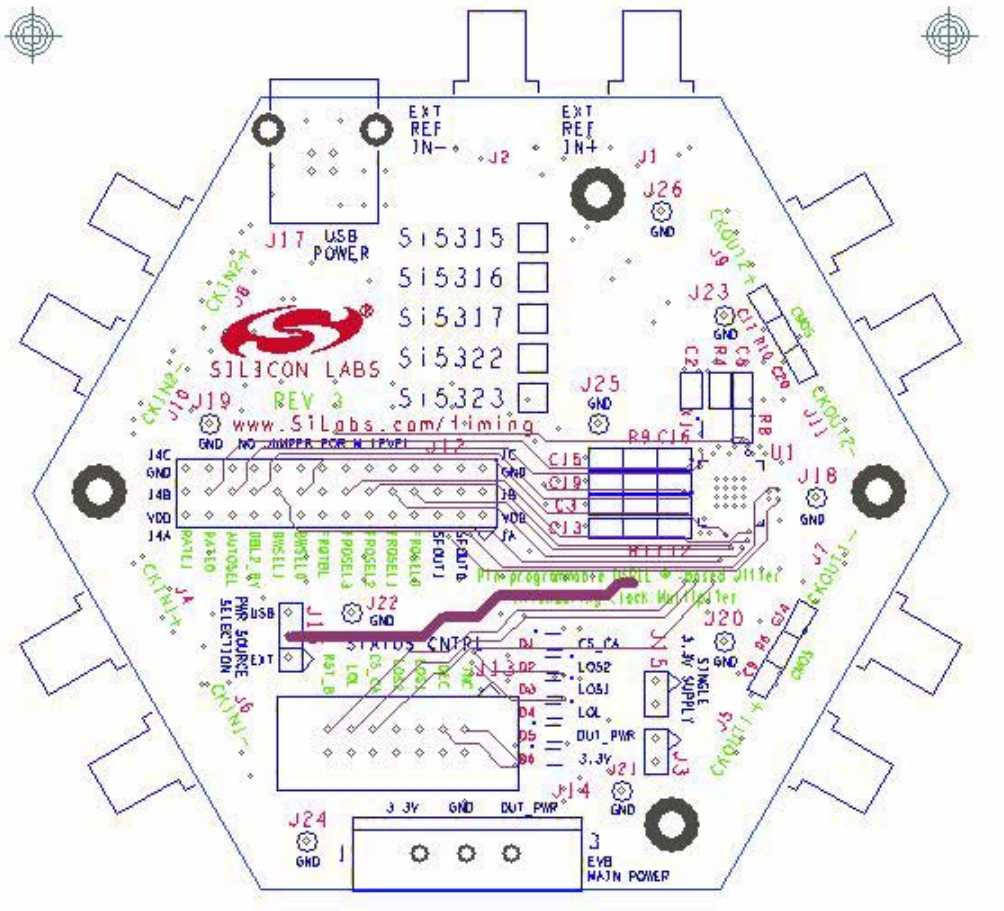


Figure 8. Layer 3

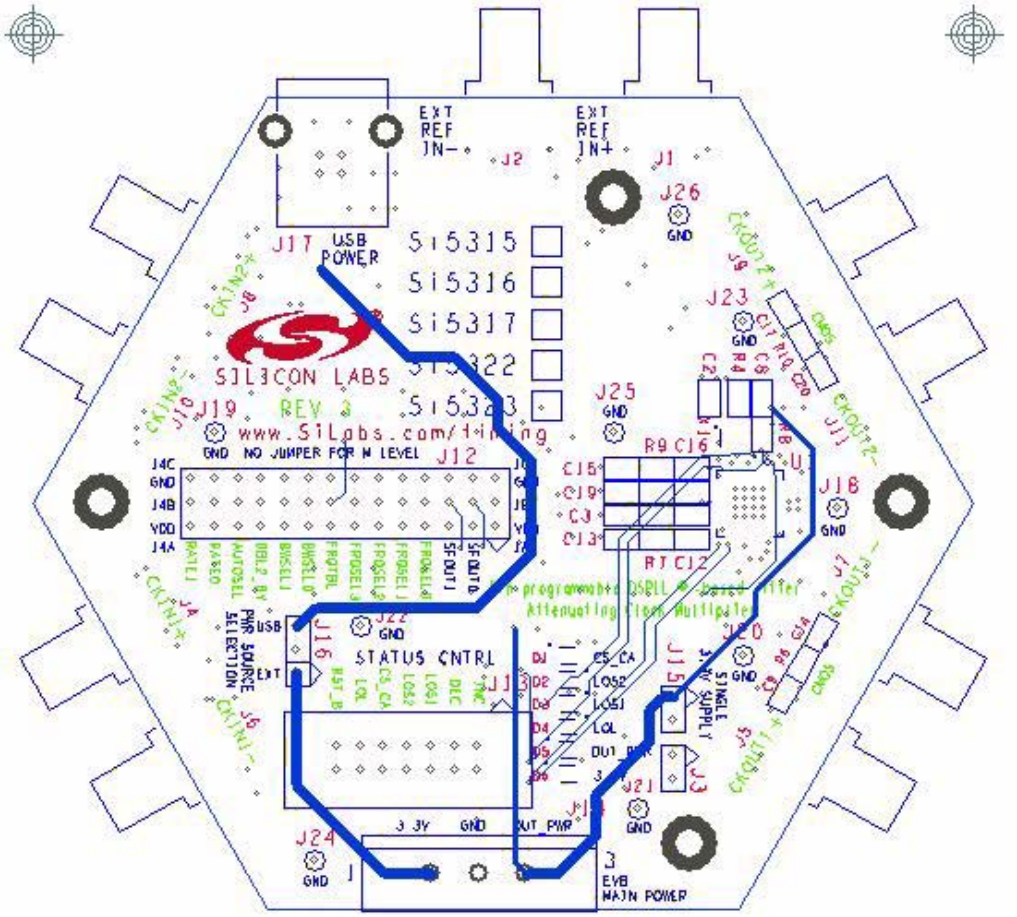


Figure 9. Layer 4

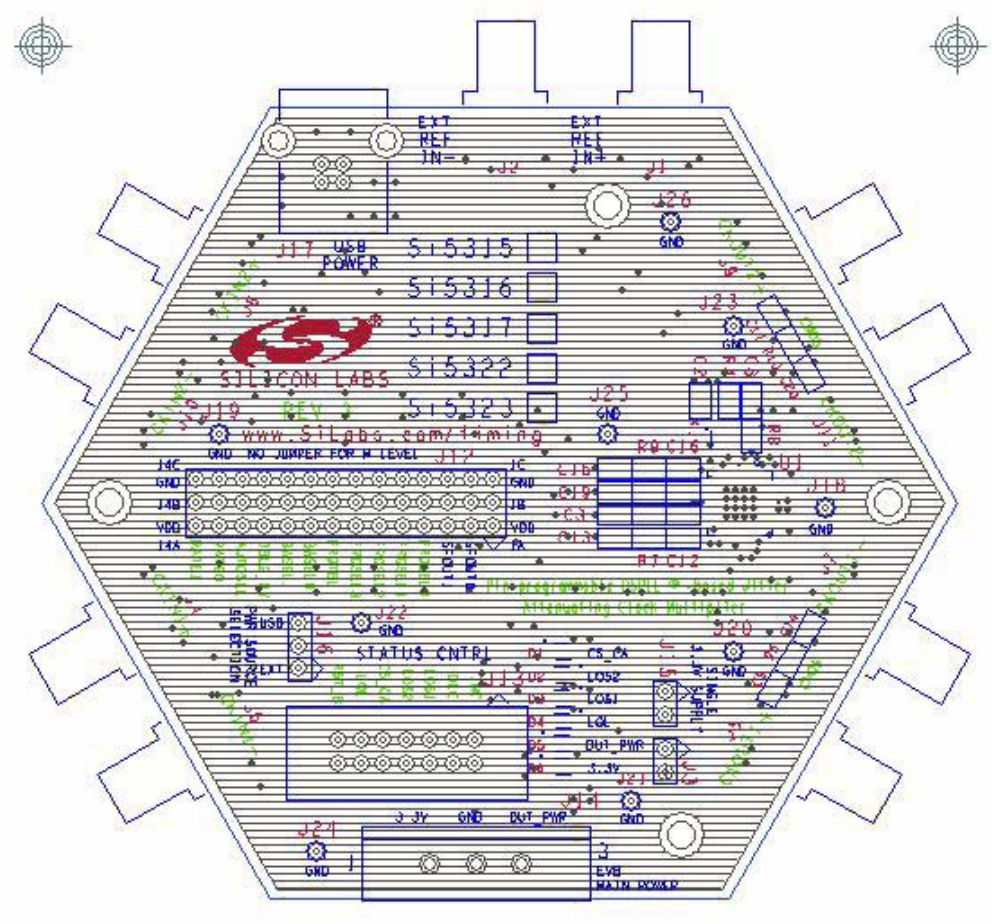


Figure 10. Layer 5, FILT_DUT_PWR

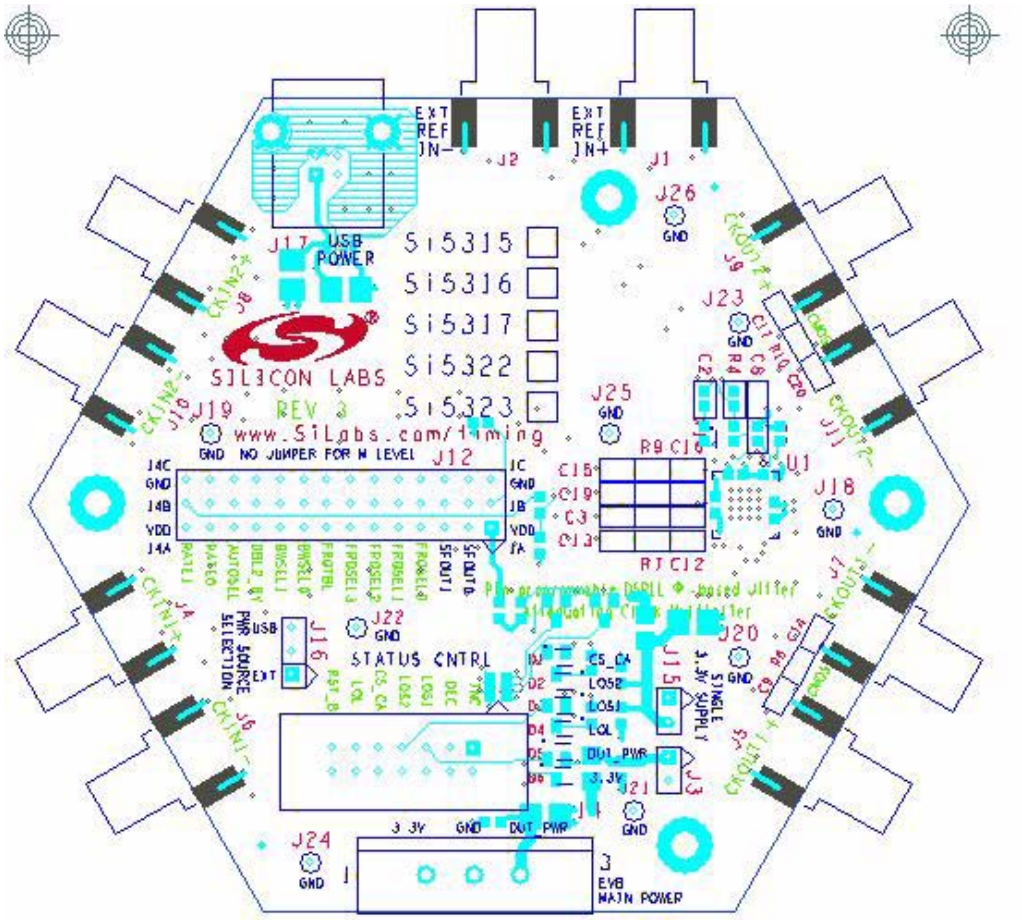


Figure 11. Layer 6, Bottom

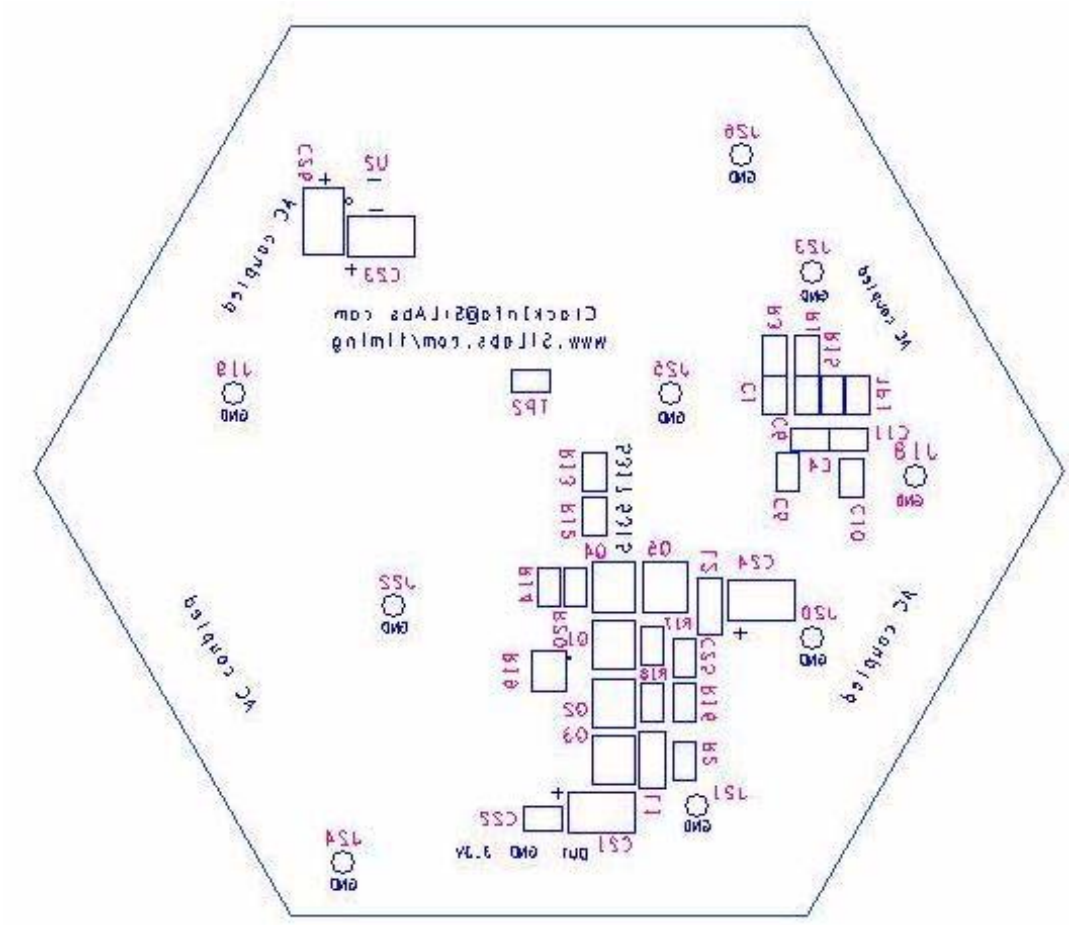


Figure 12. Bottom Silkscreen

7. Factory Default Configuration

J12	Pin	Jumper
J12.1	not used	—
J12.2	SFOUT0	H
J12.3	SFOUT1	L
J12.4	FRQSEL0	L
J12.5	FRQSEL1	M
J12.6	FRQSEL2	M
J12.7	FRQSEL3	H
J12.8	FRQTBL	L
J12.9	BWSEL0	M
J12.10	BSWEL1	H
J12.11	DBL2_BY	L
J12.12	not used	—
J12.13	RATE0	M
J12.14	RATE1	M

The above jumper settings result in the following:

- SFOUT = CMOS output
- 10.0 MHz input clock
- 10.0 MHz output clock
- BW =88 Hz
- RATE[1:0] = 114.285 MHz 3rd overtone crystal

CONTACT INFORMATION

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