Low Duty Cycle, 600 mA, 3 MHz Synchronous Step-Down DC-to-DC Converter

ADP2102

FEATURES

Input voltage range: 2.7 V to 5.5 V
600 mA maximum load current
95% efficiency
Low duty cycle operation
Only 3 tiny external ceramic components
3 MHz typical operating frequency
Fixed output voltage from 0.8 V to 1.875 V
Adjustable output voltage up to 3.3 V
0.01 µA shutdown supply current
Automatic power save mode
Internal synchronous rectifier
Internal soft start
Internal compensation
Enable/shutdown logic input
Undervoltage lockout
Current limit protection
Thermal shutdown
Small 8-lead, 3 mm × 3 mm LFCSP package

APPLICATIONS

USB powered devices
WLAN and gateways
Point of loads
Processor core power from 5 V
Digital cameras
PDAs and palmtop computers
Portable media players, GPS

GENERAL DESCRIPTION

The ADP2102 is a synchronous step-down dc-to-dc converter that converts a 2.7 V to 5.5 V unregulated input voltage to a lower regulated output voltage with up to 95% efficiency and 1% accuracy. The low duty cycle capability of the ADP2102 is ideal for USB applications or 5 V systems that power up submicron subvolt processor cores. Its 3 MHz typical operating frequency and excellent transient response allow the use of small, low cost 1 µH inductors and 2.2 µF ceramic capacitors. At medium-to-high load currents, it uses a current mode, pseudofixed frequency pulse-width modulation to extend battery life. To ensure the longest battery life in portable applications, the ADP2102 has a power save mode (PSM) that reduces the switching frequency under light load conditions to significantly reduce quiescent current.

The ADP2102 is available in both fixed and adjustable output voltage options with 600 mA maximum output current. The preset output voltage options voltage are 1.875 V, 1.8 V, 1.5 V, 1.375 V, 1.25 V, 1.2 V, 1.0 V, and 0.8 V. The adjustable voltage option is available from 0.8 V to 3.3 V. The ADP2102 requires only three external components and consumes 0.01 µA in shutdown mode.

The ADP2102 is available in an 8-lead LFCSP package and is specified for the −40 °C to +85 °C temperature range.

TYPICAL PERFORMANCE CHARACTERISTICS

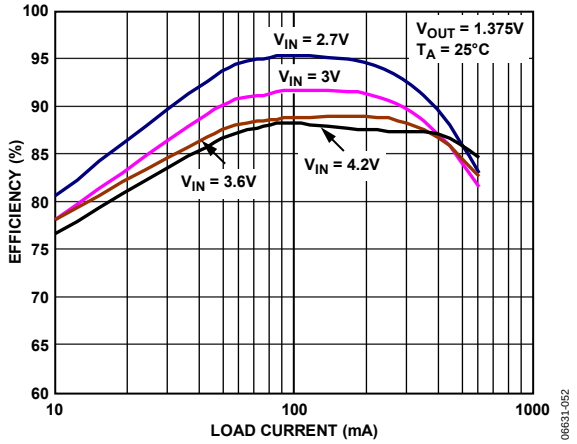

Figure 1.

TYPICAL APPLICATIONS CIRCUIT

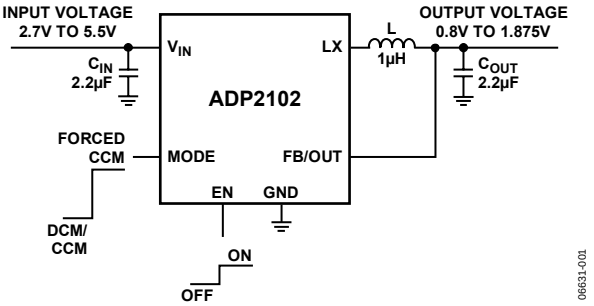

Figure 2.

Rev. B

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6/07—Rev. 0 to Rev. A

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6/07—Revision 0: Initial Version

SPECIFICATIONS

V_{IN} = 3.6 V, EN = V_{IN}, MODE = V_{IN}, T_A = 25°C, unless otherwise noted. **Bold values** indicate −40°C ≤ T_A ≤ +85°C.[1]

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS					
Input Voltage Range[2]		2.7		5.5	V
Undervoltage Lockout Threshold	V_{IN} rising	2.2	2.4	2.5	V
Undervoltage Lockout Hysteresis			220		mV
OUTPUT CHARACTERISTICS					
Output Voltage Range	ADP2102-xx	0.8		1.875	V
Output Voltage Range	ADP2102-ADJ	0.8		3.3	V
Output Voltage Initial Accuracy	ADP2102-xx, T_A= 25°C, I_{LOAD} = 0 mA	**−1**		**+1**	%
	ADP2102-xx, −40°C ≤T_A ≤ 85°C, I_{LOAD} = 0 mA	**−2**		**+2**	%
Load Regulation	V_{OUT} = 0.8 V to 1.875 V, I_{LOAD} = 0 mA to 600 mA		0.5		%
Line Regulation	V_{IN} = 2.7 V to 5.5 V, I_{LOAD} = 10 mA		0.3		%
FEEDBACK CHARACTERISTICS					
FB Regulation Voltage	ADP2102-ADJ	**784**	800	**816**	mV
FB Bias Current	ADP2102-ADJ, ADP2102-0.8			**50**	nA
FB Impedance	ADP2102-xx		375		kΩ
CURRENT CHARACTERISTICS					
Operating Current	ADP2102 PSM mode, I_{LOAD} = 0 mA		70	**99**	µA
Shutdown Current	EN = 0 V		0.01	**1**	µA
Output Current	ADP2102, V_{IN} = 2.7 V to 5.5 V			600	mA
LX (SWITCH NODE) CHARACTERISTICS					
LX On Resistance	P-channel switch, I_{LX} = 100 mA		325	**600**	mΩ
	N-channel synchronous rectifier, I_{LX} = 100 mA		200	**400**	mΩ
LX Leakage Current	V_{IN} = 5.5 V, V_{LX} = 0 V, 5.5 V			**1**	µA
LX Minimum Off-Time	ADP2102-xx, ADP2102-ADJ		100		ns
LX On-Time	ADP2102-0.8	**55**	87	**105**	ns
	ADP2102-1.0	**70**	107	**135**	ns
	ADP2102-1.2	**100**	131	**160**	ns
	ADP2102-1.25	**103**	133	**169**	ns
	ADP2102-1.375	**135**	165	**195**	ns
	ADP2102-1.5	**150**	182	**210**	ns
	ADP2102-1.8	**180**	220	**260**	ns
	ADP2102-1.875	**190**	237	**270**	ns
	ADP2102-ADJ-1.2	**80**	131	**170**	ns
	ADP2102-ADJ-1.5	**155**	177	**210**	ns
	ADP2102-ADJ-1.875	**200**	226	**275**	ns
	ADP2102-ADJ-3.3 (V_{IN} = 5 V)	**198**	238	**270**	ns
Valley Current Limit			1		A
ENABLE, MODE CHARACTERISTICS					
EN, MODE Input High Threshold		**1.3**			V
EN, MODE Input Low Threshold				**0.4**	V
EN, MODE Input Leakage Current	V_{IN} = 5.5 V, EN = MODE = 0 V, 5.5 V			**1**	µA
SOFT START PERIOD		**250**	500	**800**	µs
THERMAL CHARACTERISTICS					
Thermal Shutdown Threshold			150		°C
Thermal Shutdown Hysteresis			15		°C

[1] All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC).
[2] The input voltage (V_{IN}) range over which the rest of the specifications are valid. The part operates as expected until V_{IN} goes below the UVLO threshold.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
AVIN, EN, MODE, FB/OUT to AGND	−0.3 V to +6 V
LX to PGND	−0.3 V to (V_{IN} + 0.3 V)
PVIN to PGND	−0.3 V to +6 V
PGND to AGND	−0.3 V to +0.3 V
AVIN to PVIN	−0.3 V to +0.3 V
Operating Ambient Temperature Range	−40°C to +85°C[1]
Junction Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Soldering Conditions	JEDEC J-STD-020

[1] The ADP2102 can be damaged when junction temperature limits are exceeded. Monitoring ambient temperature does not guarantee that T_J is within the specified temperature limits. In applications where high power dissipation and poor thermal resistance are present, the maximum ambient temperature may have to be derated. In applications with moderate power dissipation and low PCB thermal resistance, the maximum ambient temperature can exceed the maximum limit as long as the junction temperature is within specification limits. The junction temperature (T_J) of the device is dependent on the ambient temperature (T_A), the power dissipation of the device (PD), and the junction-to-ambient thermal resistance of the package (θ_{JA}). Maximum junction temperature (T_J) is calculated from the ambient temperature (T_A) and power dissipation (PD) using the formula $T_J = T_A + (\theta_{JA} \times PD)$. Unless otherwise specified, all other voltages are referenced to AGND.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

Junction-to-ambient thermal resistance (θ_{JA}) of the package is based on modeling and calculation using a 4-layer board. The junction-to-ambient thermal resistance is highly dependent on the application and board layout. In applications where high maximum power dissipation exists, attention to thermal board design is required. The value of θ_{JA} may vary, depending on PCB material, layout, and environmental conditions. Specified value of θ_{JA} is based on a 4-layer, 4 in × 3 in, 2 1/2 oz copper board, as per JEDEC standards. For more information, see Application Note AN-772, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)*.

Table 3. Thermal Resistance

Package Type	θ_{JA}	Unit
8-Lead LFCSP	54	°C/W
Maximum Power Dissipation	0.74	W

BOUNDARY CONDITION

Natural convection, 4-layer board, exposed pad soldered to PCB.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

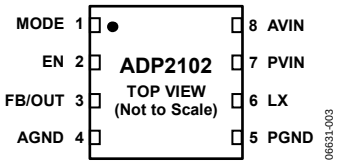

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	MODE	Mode Input. To set the ADP2102 to forced continuous conduction mode (CCM), drive MODE high. To set the ADP2102 to power save mode/auto mode (PSM), drive MODE low.
2	EN	Enable Input. Drive EN high to turn on the ADP2102. Drive EN low to turn it off and reduce the input current to 0.1 µA. This pin cannot be left floating.
3	FB/OUT	Output Sense Input or Feedback Input. For fixed output versions, OUT is the top of the internal resistive voltage divider. Connect OUT to the output voltage. For adjustable (no suffix) versions, FB is the input to the error amplifier. Drive FB through a resistive voltage divider to set the output voltage. The FB regulation threshold is 0.8 V.
4	AGND	Analog Ground. Connect AGND to PGND at a single point as close to the ADP2102 as possible. The exposed paddle is electrically common with the analog ground pin.
5	PGND	Power Ground.
6	LX	Switch Output. LX is the drain of the P-channel MOSFET switch and the N-channel synchronous rectifier. Connect the output LC filter between LX and the output voltage.
7	PVIN	Power Source Input. Drive PVIN with a 2.7 V to 5.5 V power source. A ceramic bypass capacitor of 2.2 µF or greater is required on this pin to the nearest PGND plane.
8	AVIN	Power Source Input. AVIN is the supply for the ADP2102 internal circuitry. This pin can be connected in three different ways. For noise reduction, place an external RC filter between PVIN and AVIN. The recommended values for the external RC filter are 10 Ω and 0.1 µF, respectively. This configuration can be used for all loads. For light-to-medium loads up to 300 mA, the AVIN pin and the PVIN pin can be shorted together. For light-to-heavy loads (greater than 300 mA), bypass the AVIN pin with a 1 pF to 0.01 µF capacitor to the nearest PGND plane. Do not short the AVIN and PVIN pins when using only a bypass capacitor.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.6 V, L = 2.2 µH, C_{IN} = 2.2 µF, C_{OUT} = 4.7 µF, unless otherwise noted.

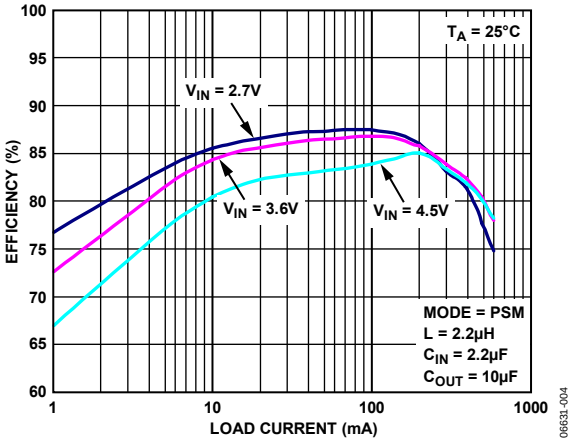

Figure 4. Efficiency vs. Load Current (V_{OUT} = 1.2 V)

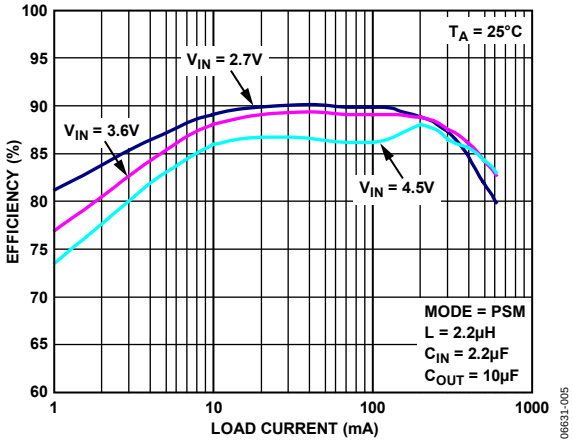

Figure 5. Efficiency vs. Load Current (V_{OUT} = 1.5 V)

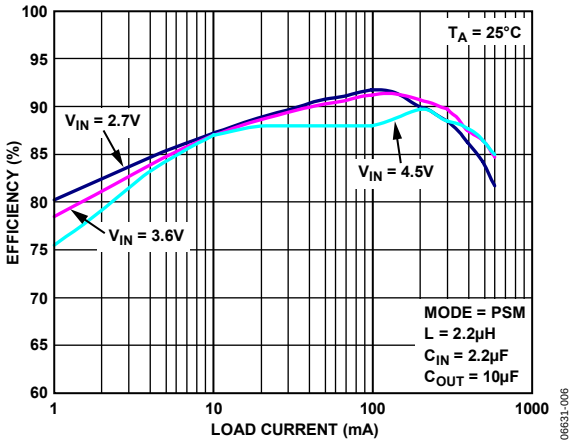

Figure 6. Efficiency vs. Load Current (V_{OUT} = 1.8 V)

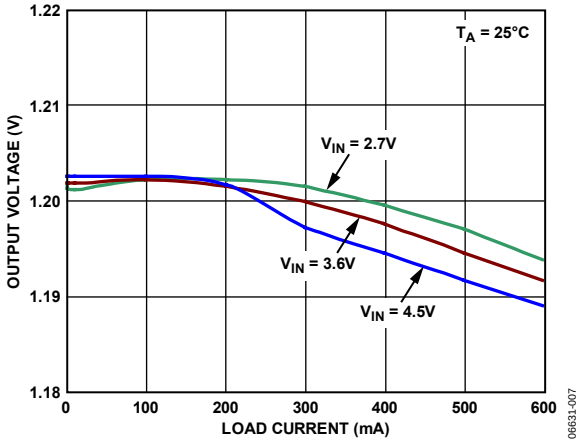

Figure 7. Output Voltage Accuracy (V_{OUT} = 1.2 V)

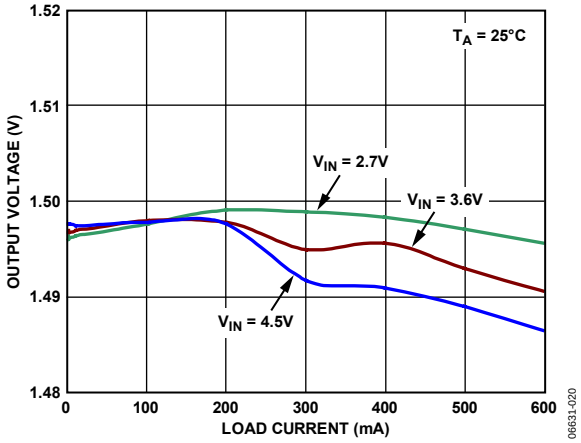

Figure 8. Output Voltage Accuracy (V_{OUT} = 1.5 V)

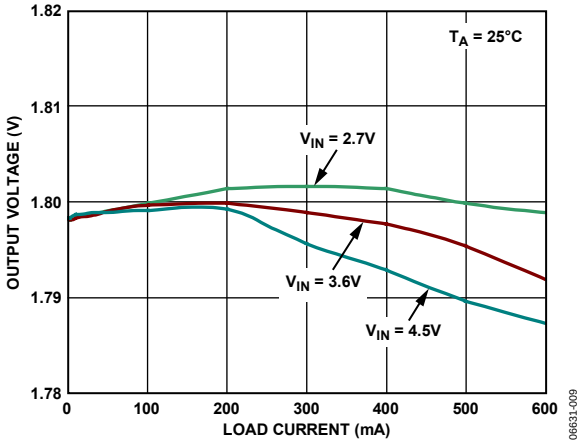

Figure 9. Output Voltage Accuracy (V_{OUT} = 1.8 V)

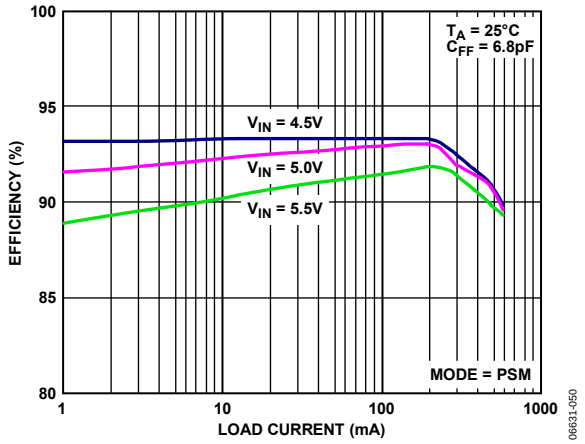

Figure 10. Efficiency vs. Load Current (V_{OUT} = 3.3 V)

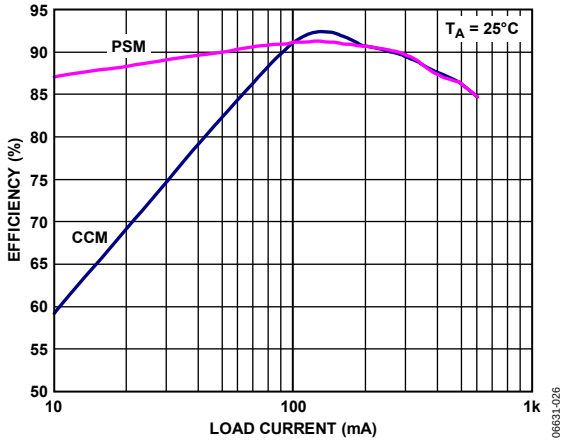

Figure 11. PSM vs. CCM Efficiency (V_{OUT} = 1.8 V)

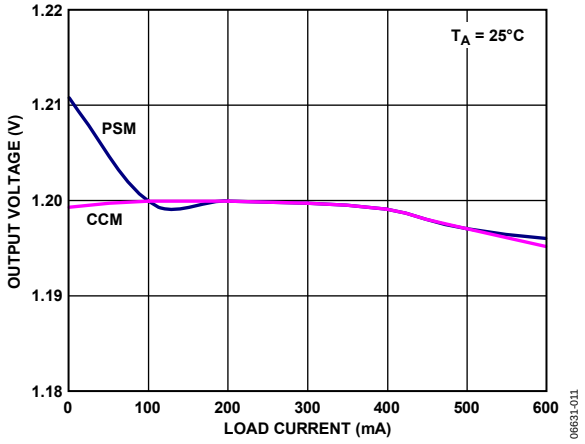

Figure 12. Output Voltage vs. Load Current (V_{OUT} = 1.2 V)

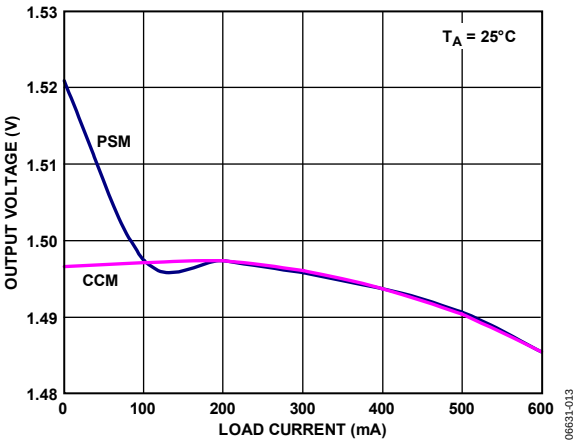

Figure 13. Output Voltage vs. Load Current (V_{OUT} = 1.5 V)

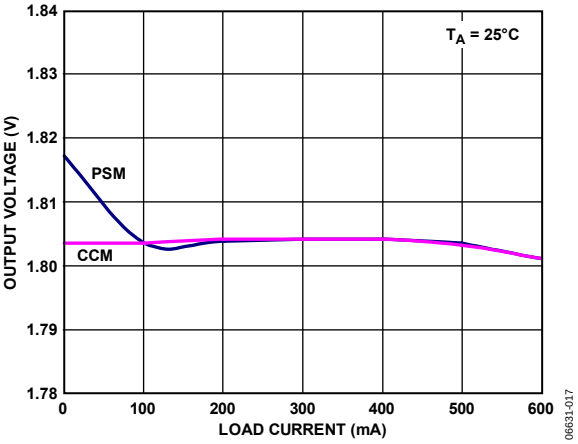

Figure 14. Output Voltage vs. Load Current (V_{OUT} = 1.8 V)

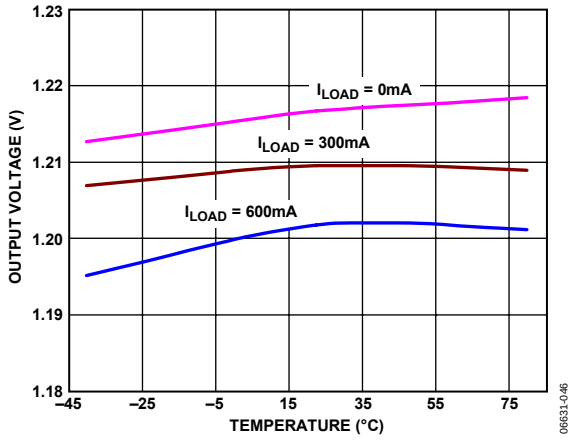

Figure 15. Output Voltage vs. Temperature (V_{OUT} = 1.2 V)

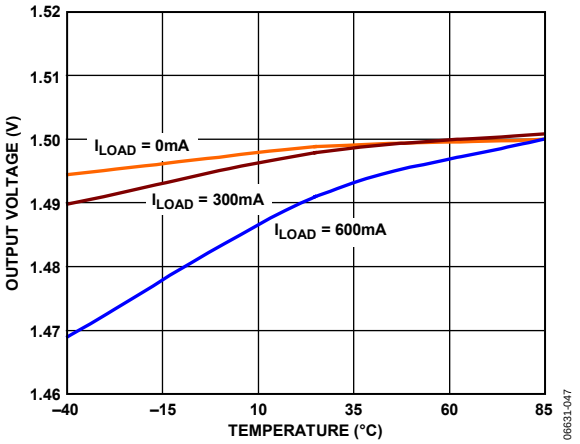

Figure 16. Output Voltage vs. Temperature (V_{OUT} = 1.5 V)

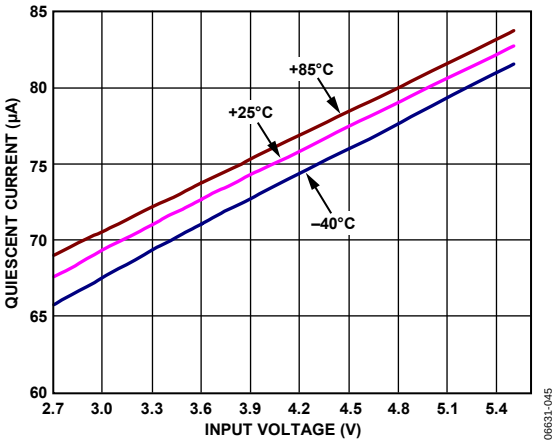

Figure 19. Quiescent Current vs. Input Voltage

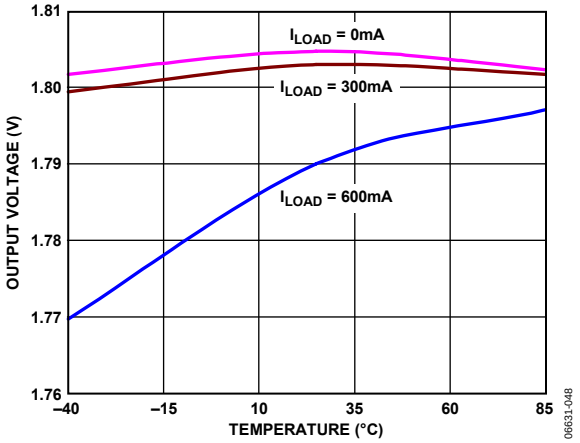

Figure 17. Output Voltage vs. Temperature (V_{OUT} = 1.8 V)

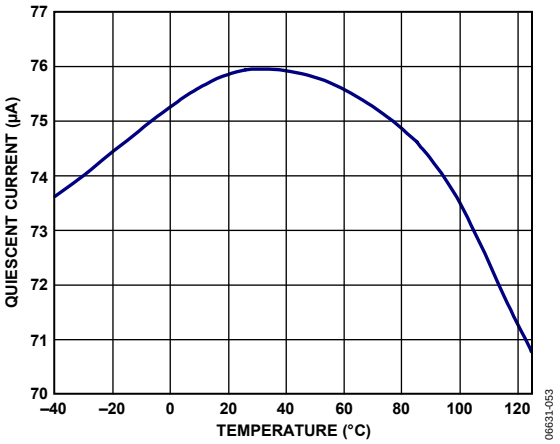

Figure 20. Quiescent Current vs. Temperature

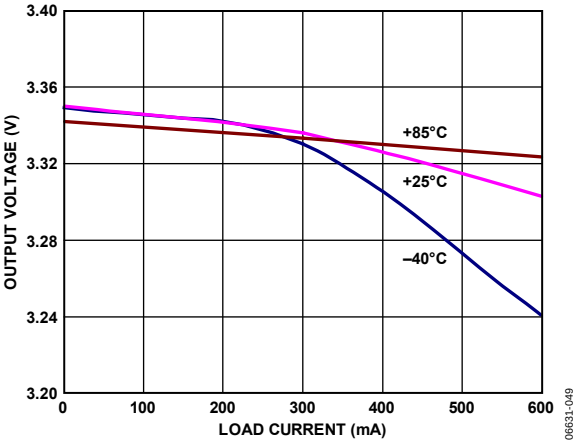

Figure 18. Output Voltage Accuracy (V_{OUT} = 3.3 V)

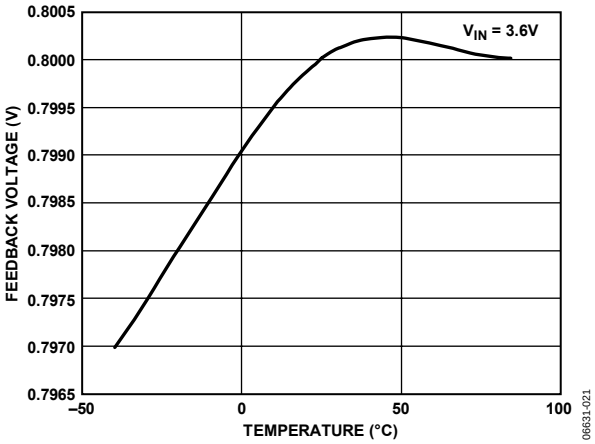

Figure 21. Feedback Voltage vs. Temperature

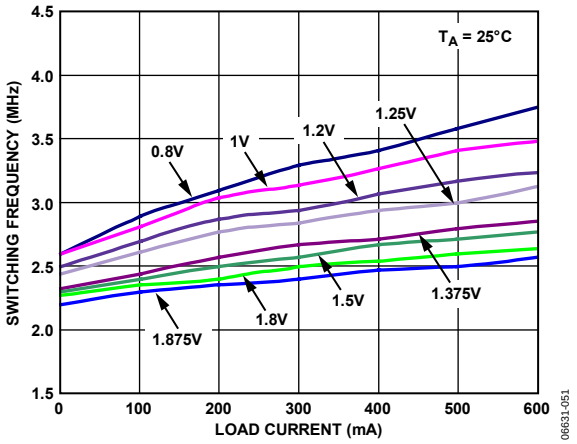

Figure 22. Switching Frequency vs. Load Current

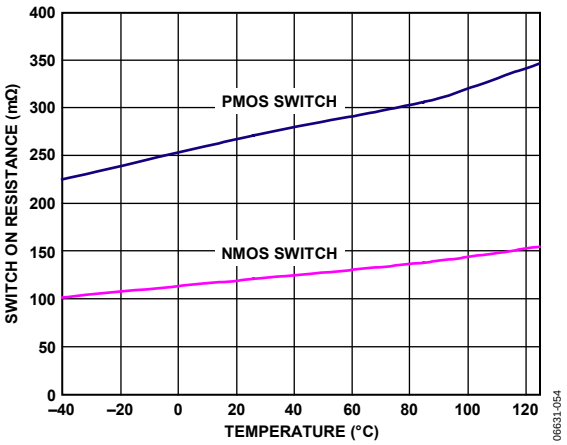

Figure 25. Switch On Resistance vs. Temperature

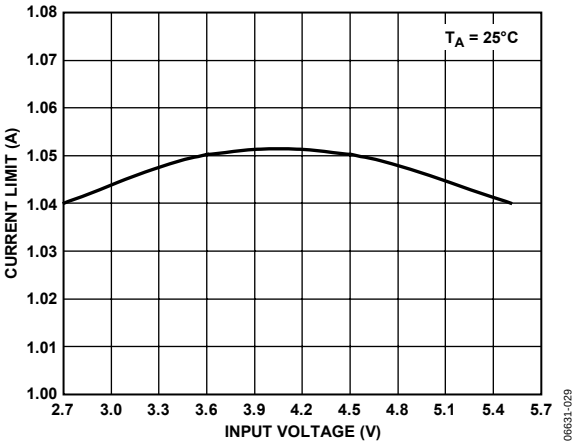

Figure 23. Valley Current Limit

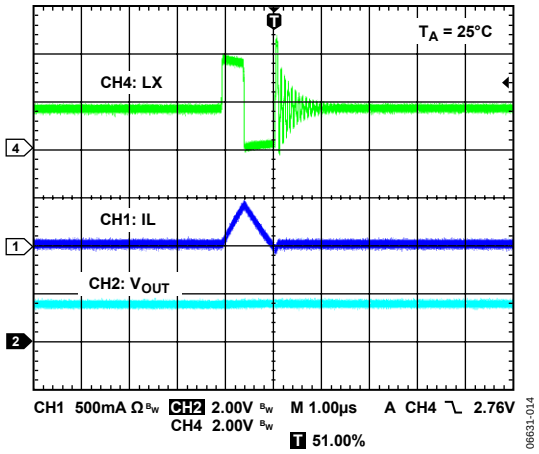

Figure 26. PSM Mode Operation at Very Light Loads (10 mA)

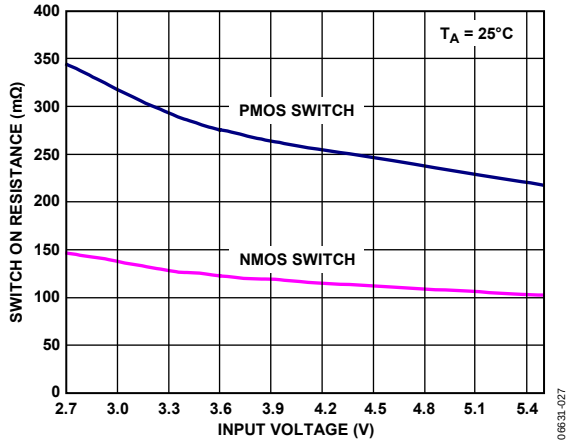

Figure 24. Switch On Resistance vs. Input Voltage

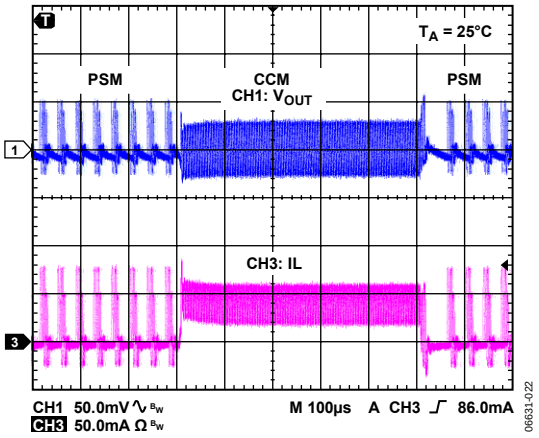

Figure 27. PSM Mode Entry—Exit Operation (10 mA to 50 mA to 10 mA)

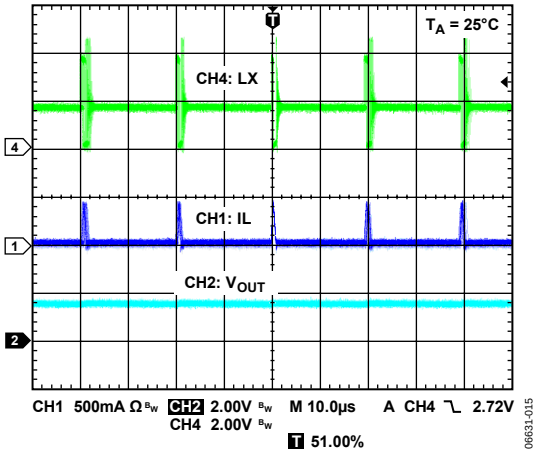

Figure 28. PSM Mode Operation at Light Loads (75 mA)

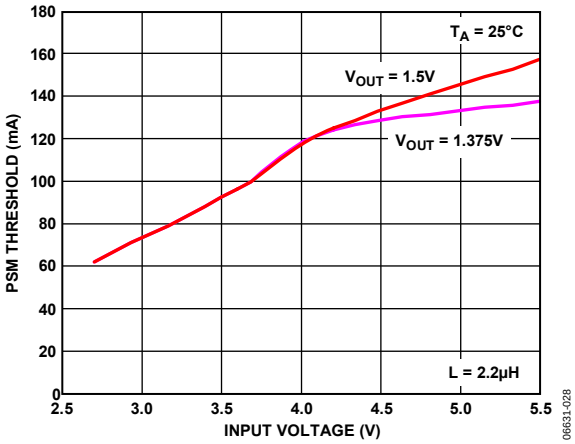

Figure 31. Typical PSM Threshold vs. Input Voltage

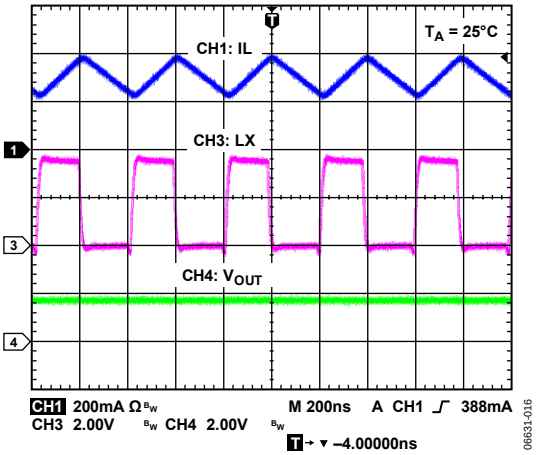

Figure 29. CCM Mode Operation at Medium/Heavy Loads (0.3 A)

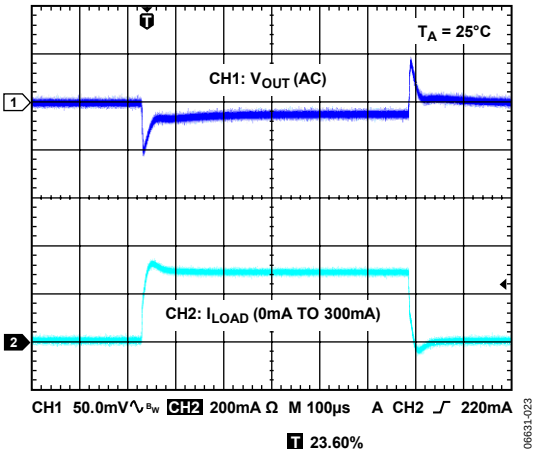

Figure 32. Load Transient Response (V_{OUT} = 1.2 V)

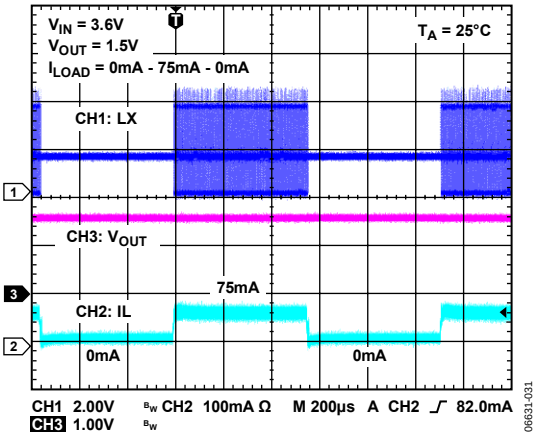

Figure 30. Light Load Behavior

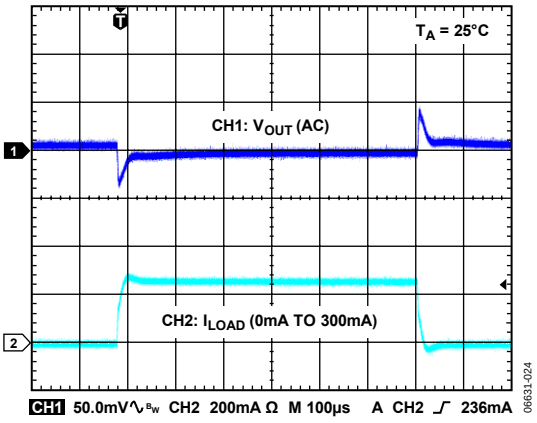

Figure 33. Load Transient Response (V_{OUT} = 1.5 V)

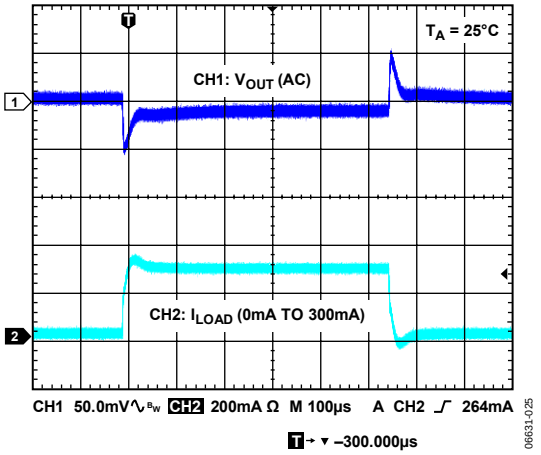

Figure 34. Load Transient Response (V_{OUT} = 1.8 V)

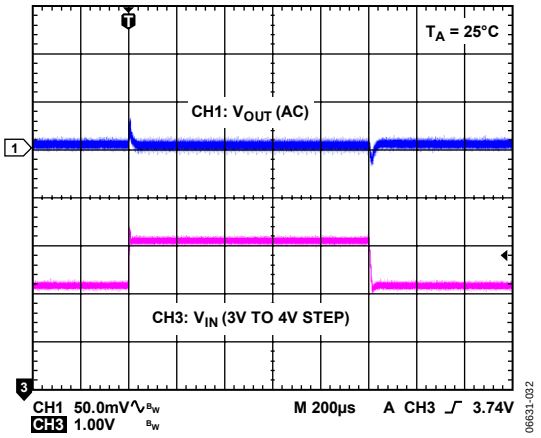

Figure 35. Line Transient Response (V_{OUT} = 1.2 V)

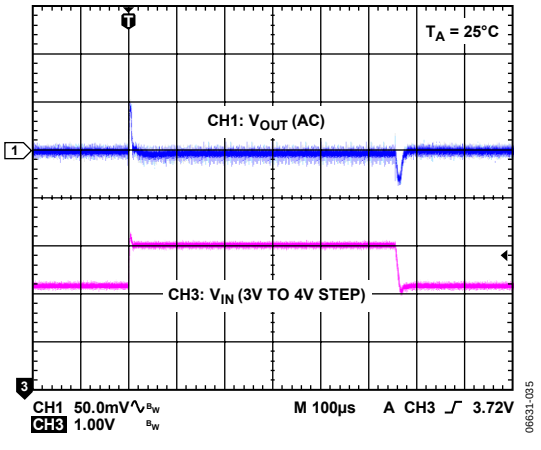

Figure 36. Line Transient Response (V_{OUT} = 1.5 V)

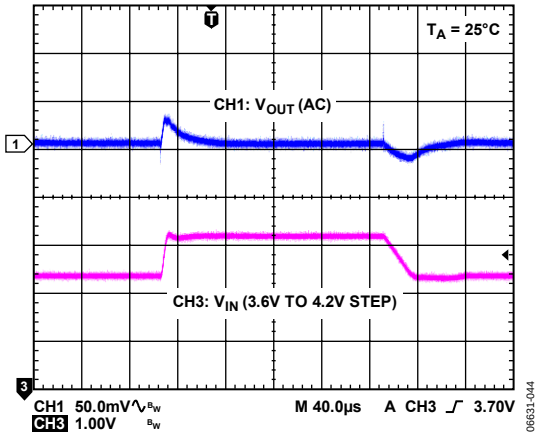

Figure 37. Line Transient Response (V_{OUT} = 1.8 V)

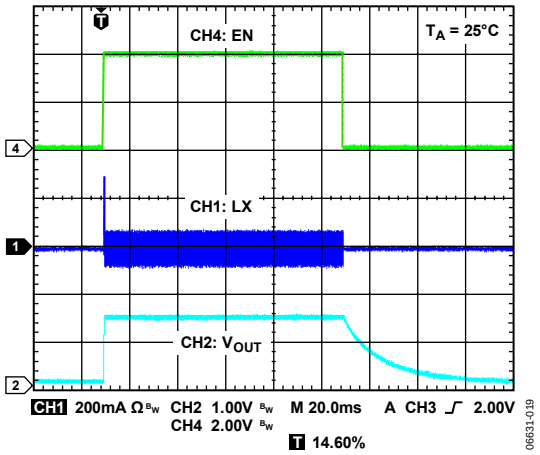

Figure 38. Start-Up and Shutdown Waveform

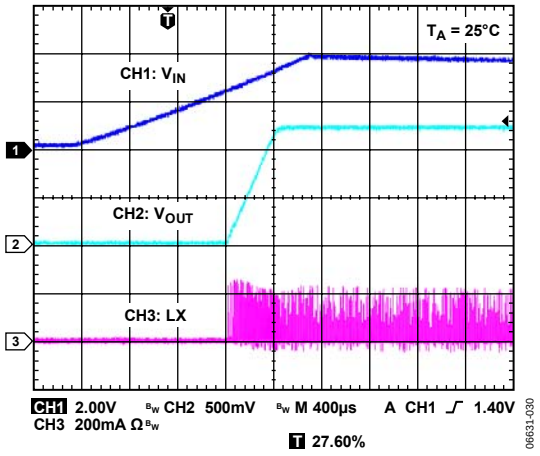

Figure 39. Light Load Start-Up Waveform

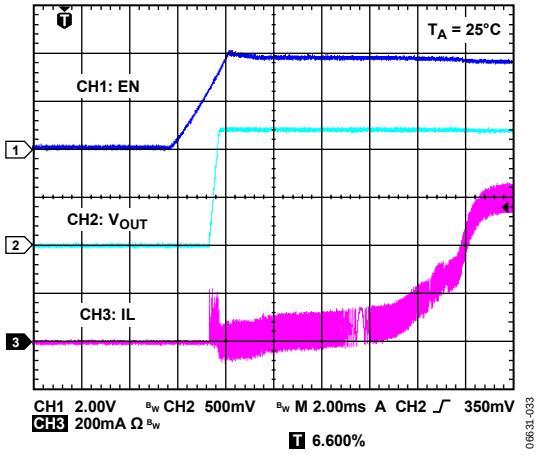

Figure 40. Heavy Load Start-Up Waveform

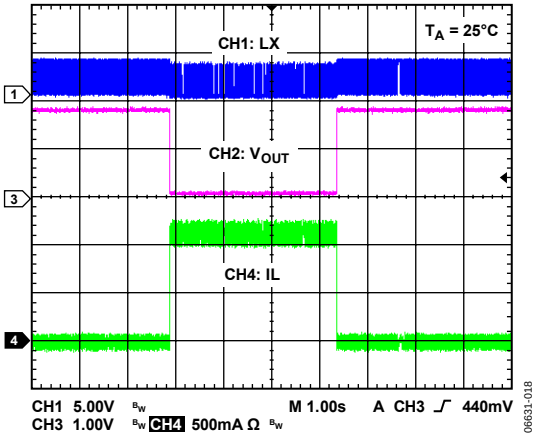

Figure 42. Short-Circuit Response at Output

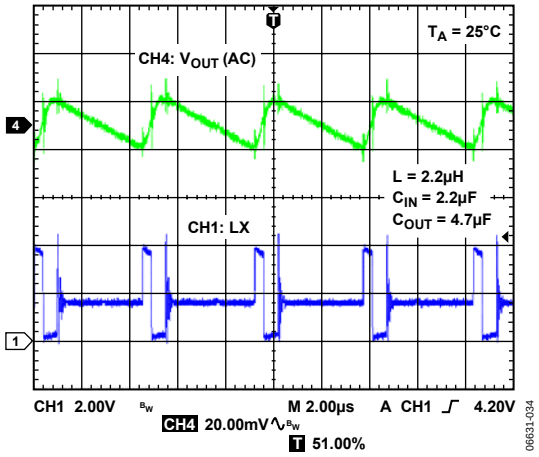

Figure 41. PSM Mode Ripple (V_{IN} = 3.6 V, Load = 50 mA)

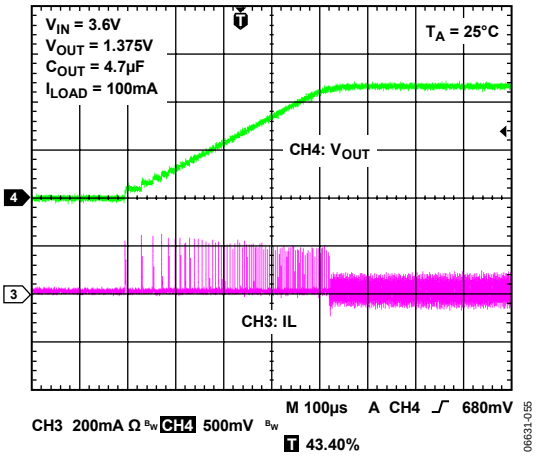

Figure 43. Soft Start Waveform

THEORY OF OPERATION

The ADP2102 is a high frequency, synchronous step-down, dc-to-dc converter optimized for battery-powered, portable applications. It is based on constant on-time current-mode control architecture with voltage feed forward to null frequency variation with line voltage, creating a pseudofixed frequency.

This type of control allows generation of very low output voltages at a higher switching frequency and offers a very fast load and line transient response with minimal external component count and size. The ADP2102 provides features such as undervoltage lockout, thermal shutdown, and short-circuit protection.

The ADP2102 uses valley current-mode control, which helps to prevent minimum on-time limitations at very low output voltages. This allows high frequency operation, resulting in low filter inductor and capacitor values.

CONTROL SCHEME

The ADP2102 high-side power switch on-time is determined by a one-shot timer whose pulse width is directly proportional to the output voltage and inversely proportional to the input or line voltage. Another one-shot timer sets a minimum off time to allow for inductor valley current sensing.

The constant on-time, one-shot timer is triggered at the rising edge of EN and, subsequently, when the low-side power switch current is below the valley current limit threshold and the minimum off-time one-shot timer has timed out.

While the constant on-time is asserted, the high-side power switch is turned on. This causes the inductor current to ramp positively. After the constant on-time has completed, the high-side power switch turns off and the low-side power switch turns on. This causes the inductor current to ramp negatively until the sensed current flowing in this switch has reached valley current limit. At this point, the low-side power switch turns off and a new cycle begins with the high-side switch turning on, provided that the minimum off-time one shot has timed out.

CONSTANT ON-TIME TIMER

The constant on-time timer sets the high-side switch on-time. This fast, low jitter, adjustable one shot varies the on-time in response to input voltage for a given output voltage. The high-side switch on-time is inversely proportional to the input voltage and directly proportional to the output voltage.

$$t_{ON} = K(V_{OUT}/V_{IN}) \quad (1)$$

The duty cycle for a buck converter operating in continuous conduction mode (CCM) is given by $D = V_{OUT}/V_{IN}$ and, by definition, $D = t_{ON}/(t_{ON} + t_{OFF})$. Therefore, equating the duty cycle terms of V_{OUT}/V_{IN} and $t_{ON}/(t_{ON} + t_{OFF})$ gives

$$t_{ON} = V_{OUT}/(V_{IN} \times f_{SW}) \quad (2)$$

Equating Equation 1 and Equation 2 gives

$$f_{SW} = 1/K \quad (3)$$

where K is an internally set on-time scale factor constant resulting in a constant switching frequency.

As shown in Equation 1, the steady state switching frequency is theoretically independent of both the input and output voltages to a first order. This means the loop switches at a nearly constant frequency until a load step occurs.

When a load step occurs, the constant on-time control loop responds by modulating the off time up or down to quickly return to regulation. This momentary frequency variation results in a faster load transient response than a fixed frequency current-mode control loop of similar bandwidth with a similar external filter inductor and capacitor. This is an advantage of a constant on-time control scheme.

Resistive voltage losses in the high-side and low-side power switches, package parasitics, inductor DCR, and board parasitic resistance cause the loop to compensate by reducing the off time and, therefore, increase the switching frequency with increasing load current.

A minimum off-time constraint is introduced to allow inductor valley current sensing on the synchronous switch.

FORCED CONTINUOUS CONDUCTION MODE

When the MODE pin is high, the ADP2102 operates in forced continuous conduction mode (CCM). In this mode, irrespective of the load current, the inductor current stays continuous, and CCM is the preferred mode of operation for low noise applications. During this mode, the switching frequency stays close to 3 MHz typical. In this mode, efficiency is lower at light loads, compared to the power save mode, but the output voltage ripple is minimized.

POWER SAVE MODE

When the MODE pin is low, the ADP2102 operates in power save mode (PSM). In this mode, at light load currents, the part automatically goes into reduced frequency operation where some pulses are skipped to increase efficiency while remaining in regulation. At light loads, a zero-crossing comparator truncates the low-side switch on-time when the inductor current becomes negative. In this condition, the part works in discontinuous conduction mode (DCM). The threshold between CCM and DCM is approximately

$$I_{LOAD}\,(\text{skip}) = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times V_{IN} \times f_{SW}} \quad (4)$$

There is a first-order dependency of this threshold on the internally set on-time scale factor indicated in Equation 3. For higher load currents, the inductor current does not cross zero threshold. The device switches to the continuous conduction mode, and the frequency is fixed to the nominal value.

As a result of this auto mode control technique, losses are minimized at light loads, improving system efficiency.

The PSM reverse current comparator controls the entry and exit into forced continuous conduction mode. Some minor jitter is normal during transition from DCM to CCM with loads at approximately 100 mA typical, and it has no adverse impact on regulation.

SYNCHRONOUS RECTIFICATION

In addition to the P-channel MOSFET switch, the ADP2102 includes an integrated N-channel MOSFET synchronous rectifier. The synchronous rectifier improves efficiency, especially at low output voltages, and reduces cost and board space by eliminating the need for an external rectifier.

CURRENT LIMIT

The current limit circuit employs a valley current sensing scheme. Current limit detection occurs during the off time through sensing of the voltage drop across the on resistance of the synchronous rectifier switch. The detection threshold is 1 A typical.

Figure 45 illustrates the inductor current waveform during normal operation and during current limit. The output current, I_{OUT}, is the average of the inductor ripple current waveform. The low-to-medium load current waveform illustrates the continuous conduction mode operation with peak and valley inductor currents below the current limit threshold. When the load current is increased, the ripple waveform maintains the same amplitude and frequency because the current falls below the current limit threshold at the valley of the ripple waveform. As the current falls below the threshold during the normal off-time of each cycle, the start of each on-time is not delayed, and the circuit output voltage is regulated at the correct value.

When the load current is further increased such that the lower peak is above the current limit threshold, the off time is lengthened to allow the current to decrease to this threshold before the next on-time begins.

Both V_{OUT} and the switching frequency are reduced as the circuit operates in constant current mode. The load current (I_{OCL}) under these conditions is equal to the current limit threshold plus half the ripple current, as shown in Equation 5 and in Figure 44.

$$I_{OCL} = I_{VALLEY} + \Delta I_L/2 \quad (5)$$

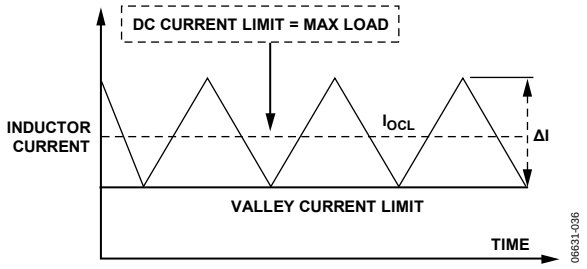

Figure 44. Valley Current Limit

The ripple current is calculated using Equation 6.

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L} \quad (6)$$

The ADP2102 also provides a negative current limit to prevent an excessive reverse inductor current when the switching section sinks current from the load in forced continuous conduction mode. Under negative current limit conditions, both the high-side and low-side switches are disabled.

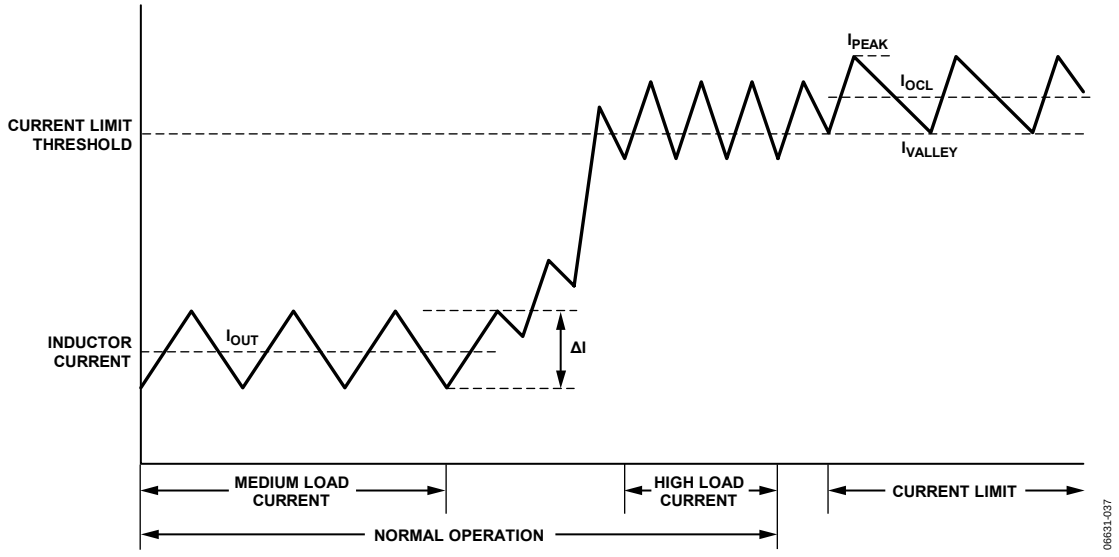

Figure 45. Inductor Current—Current Limit Operation

SOFT START

The ADP2102 has an internal soft start function that ramps the output voltage in a controlled manner upon startup, therefore limiting the inrush current. This prevents possible input voltage drops when a battery or a high impedance power source is connected to the input of the converter.

ENABLE

The device starts operation with soft start when the EN pin is toggled from logic low to logic high. Pulling the EN pin low forces the device into shutdown mode, with a typical shutdown current of 0.01 μA. In shutdown mode, both the high-side and low-side power switches are turned off, the internal resistor feedback divider is disconnected, and the entire control circuitry is switched off. For proper operation, the device is in shutdown mode when voltage applied to this pin is less than 0.4 V and enabled when voltage applied is greater than 1.3 V. This pin must not be left floating.

UNDERVOLTAGE LOCKOUT

The undervoltage lockout circuit prevents the device from operating incorrectly at low input voltages. It prevents the converter from turning on the main switch and the synchronous switch under undefined conditions and, therefore, prevents deep discharge of the battery supply.

THERMAL SHUTDOWN

When the junction temperature, T_J, exceeds 150°C typical, the device goes into thermal shutdown. In this mode, the high-side and low-side power switches are off. The device resumes operation when the junction temperature again falls below 135°C typical.

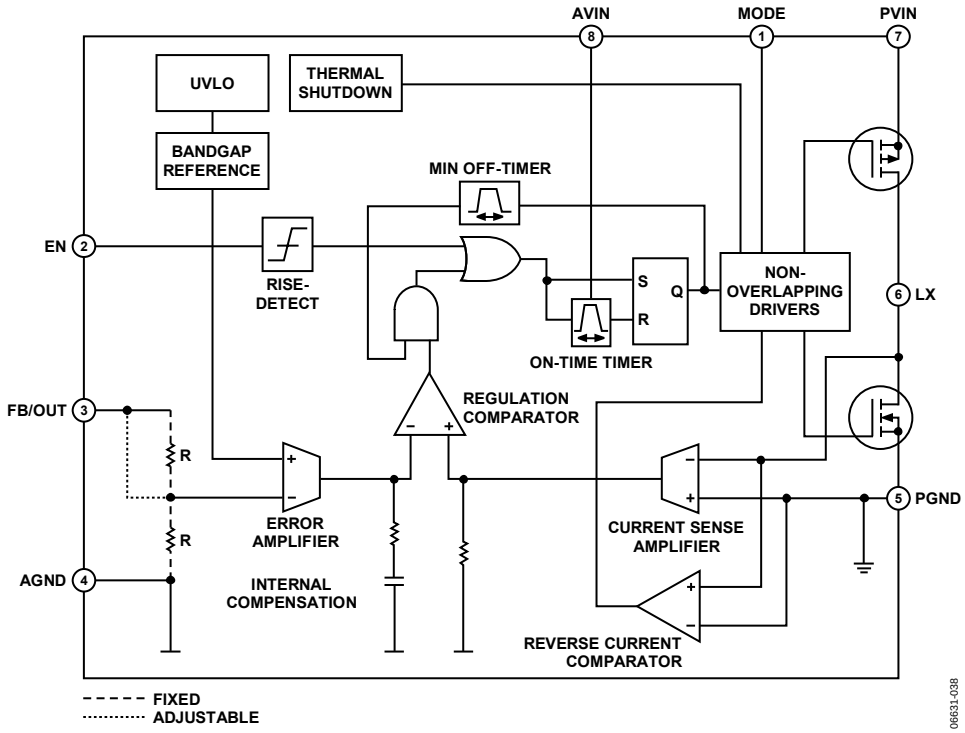

Figure 46. Internal Block Diagram

APPLICATIONS INFORMATION

The external component selection for the ADP2102 applications circuit, as shown in Figure 2, is driven by the load requirement and begins with the selection of Inductor L. Once the inductor is chosen, C_{IN} and C_{OUT} can be selected.

INDUCTOR SELECTION

The high switching frequency of the ADP2102 allows for minimal output voltage ripple, even with small inductors. Inductor sizing is a trade-off between efficiency and transient response. A small inductor leads to a larger inductor current ripple that provides excellent transient response but degrades efficiency. Due to the high switching frequency of the ADP2102, multilayer ceramic inductors can be used for an overall smaller solution size. Shielded ferrite core inductors are recommended for their low core losses and low electromagnetic interference (EMI).

As a guideline, the inductor peak-to-peak current ripple, ΔI_L, is typically set to 1/3 of the maximum load current for optimal transient response and efficiency.

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L} \approx \frac{I_{LOAD(MAX)}}{3} \quad (7)$$

$$L_{IDEAL} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times 0.3 \times I_{LOAD(MAX)}}$$

where f_{SW} is the switching frequency.

Finally, it is important that the inductor be capable of handling the maximum peak inductor current, I_{PK}, determined by the following equation:

$$I_{PK} = I_{LOAD(MAX)} + \Delta I_L/2 \quad (8)$$

The dc current rating of the inductor should be at least equal to the maximum load current plus half the ripple current to prevent core saturation. Table 5 shows some typical surface mount inductors that work well in ADP2102 applications.

INPUT CAPACITOR SELECTION

The input capacitor must be able to support the maximum input operating voltage and the maximum rms input current. The rms input current flowing through the input capacitor is, at maximum, $I_{OUT}/2$. Select an input capacitor capable of withstanding the rms input current for the maximum load current in the application to be used.

$$I_{rms} = I_{OUTMAX} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}} \quad (9)$$

The input capacitor reduces input voltage ripple caused by the switch currents on the PVIN pin. Place the input capacitor as close as possible to the PVIN pin.

In principle, different types of capacitors can be considered, but for battery-powered applications, the best choice is a multilayer ceramic capacitor, due to its small size and equivalent series resistance (ESR).

It is recommended that the PVIN pin be bypassed with a 2.2 µF or larger ceramic input capacitor. The size of the input capacitor can be increased without any limit for better input voltage filtering. X5R or X7R dielectrics are recommended, with a voltage rating of 6.3 V or 10 V. Y5U and Z5U dielectrics are not recommended, due to their poor temperature and dc bias characteristics.

In applications with greater than 300 mA load current, a ceramic bypass capacitor of 0.01 µF is recommended on the AVIN pin for better regulation performance.

OUTPUT CAPACITOR SELECTION

The output capacitor selection affects both the output voltage ripple and the loop dynamics of the converter. For a given loop crossover frequency (the frequency at which the loop gain drops to 0 dB), the maximum voltage transient excursion (overshoot) is inversely proportional to the value of the output capacitor. The ADP2102 is designed to operate with small ceramic capacitors that have low ESR and equivalent series inductance (ESL) and are thus comfortably able to meet tight output voltage ripple specifications. X5R or X7R dielectrics are recommended with a voltage rating of 6.3 V or 10 V. Y5V and Z5U dielectrics are not recommended, due to their poor temperature and dc bias characteristics. When choosing output capacitors, it is also important to account for the loss of capacitance due to output voltage dc bias. If ceramic output capacitors are used, the capacitor rms ripple current rating should always meet the application requirements. The rms ripple current is calculated as

$$I_{rms(COUT)} = \frac{1}{2\sqrt{3}} \times \frac{V_{OUT} \times (V_{IN\_MAX} - V_{OUT})}{L \times f_{SW} \times V_{IN\_MAX}} \quad (10)$$

At nominal load currents, the converter operates in forced continuous conduction mode, and the overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor.

$$\Delta V_{OUT} = \Delta I_L \times (\text{ESR} + 1/(8 \times C_{OUT} \times f_{SW})) \quad (11)$$

The largest voltage ripple occurs at the highest input voltage, V_{IN}. At light load currents, the converter operates in power save mode, and the output voltage ripple is dependent on the output capacitor value. The ADP2102 control loop is stable with a ceramic output capacitor of 2.2 µF. For better transient performance, a 10 µF ceramic capacitor is recommended at the output. Table 6 lists input and output MLCC capacitors recommended for ADP2102 applications.

Table 5. Recommended Inductor Selection

Manufacturer	Series	Value (µH)	DCR (Ω)	Current Rating (mA)	Size (L × W × H) (mm)
FDK Corporation	MIPF2520D	2.2	0.08	1300	2.5 × 2.0 × 1.0
TDK	MLP2520S2R2L	2.2	0.08	1300	2.5 × 2.0 × 1.0
Murata	LQM2HPN2R2MJ0	2.2	0.13	1000	2.5 × 2.0 × 1.1
Coilcraft, Inc.	LPS3015-222ML	2.2	0.11	1500	2.9 × 2.9 × 1.5
Taiyo Yuden	NR3010T2R2M	2.2	0.10	1100	3.0 × 3.0 × 1.0

Table 6. Recommended Input and Output Capacitor Selection

Capacitor	Murata	Taiyo Yuden	TDK	Vishay
2.2 µF 6.3 V X5R 0603	GRM188R60J225K	JMK107BJ225KA	C1608X5R0J225M	
4.7 µF 6.3 V X5R 0603	GRM188R60J475K	JMK107BJ475KA	C1608X5R0J475M	
10 µF 6.3 V X5R 0603	GRM188R60J106M	JMK107BJ106MA	C2012X5R0J106M	
0.01 µF 25 V X7R 0402	GRM155R71E103KA01D	TMK105BJ103KV-F	C1005X7R1E103K	
1 pF 50 V X7R 0402	GJM1554C1H1R0JB01C			VJ0402A1R2CXACW1BC
6.8 pF 25 V X7R 0402				VJ0402A6R8KXAA

TYPICAL APPLICATIONS CIRCUITS

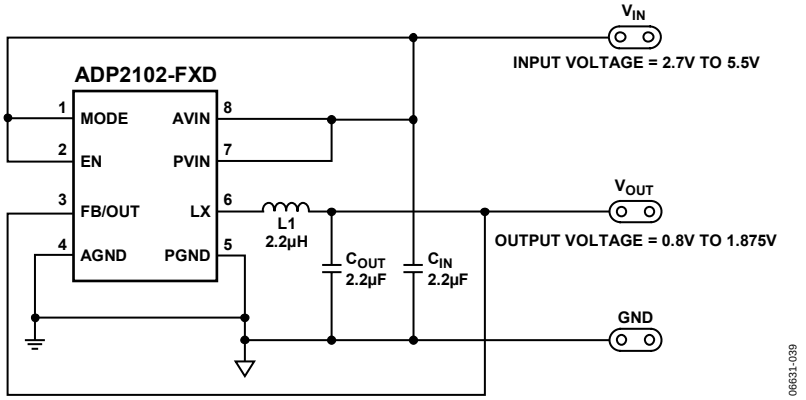

Figure 47. ADP2102-FXD (0 mA ≤ I_{LOAD} ≤ 300 mA)

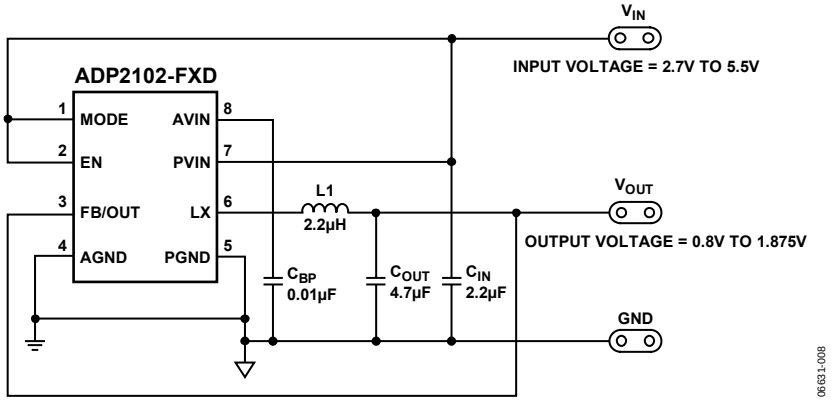

Figure 48. ADP2102-FXD (0 mA ≤ I_{LOAD} ≤ 600 mA)

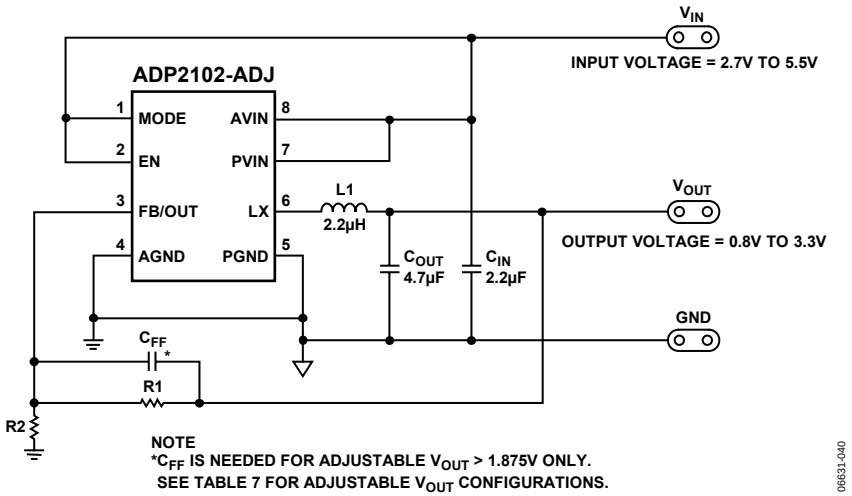

Figure 49. ADP2102-ADJ (0 mA ≤ I_{LOAD} ≤ 300 mA)

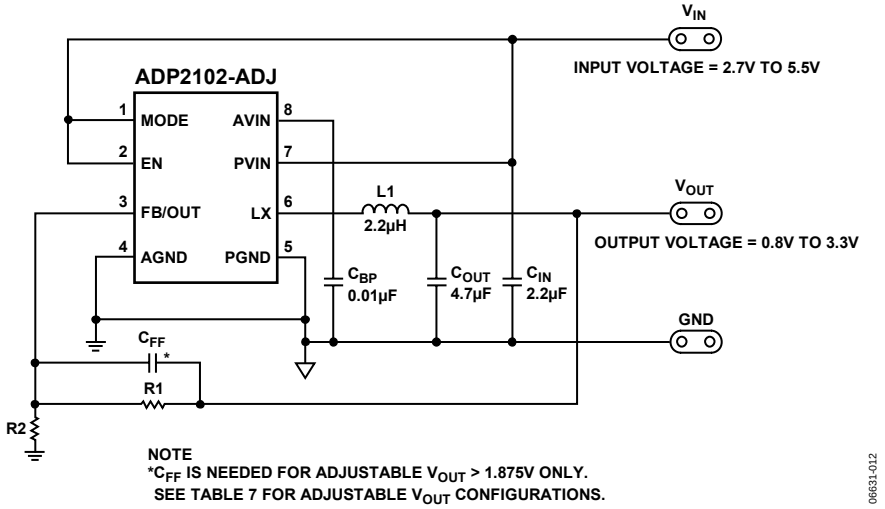

Figure 50. ADP2102-ADJ (0 mA ≤ I_{LOAD} ≤ 600 mA)

SETTING THE OUTPUT VOLTAGE

The output voltage of the ADP2102-ADJ is externally set by a resistive voltage divider from the output voltage to FB. The ratio of the resistive voltage divider sets the output voltage, and the absolute value of those resistors sets the divider string current. For lower divider string currents, the small 10 nA (50 nA maximum) FB bias current should be taken into account when calculating resistor values. The FB bias current can be ignored for a higher divider string current, but doing so degrades the efficiency at very light loads.

For the ADP2102-ADJ, the equation for output voltage selection is

$$V_{OUT} = V_{FB} (1 + R_1/R_2) \quad (12)$$

where:
V_{OUT} is the output voltage.
V_{FB} is the feedback voltage, 0.8 V.
R_1 is the feedback resistor from V_{OUT} to FB.
R_2 is the feedback resistor from FB to GND.

For any adjustable output voltage greater than 1.875 V, a feed-forward capacitor must be added across R1 for better transient performance and stability. The formula for calculation of C1 is

$$C_{FF} = 1/(2\pi \times R1 \times f_{CO}/2) \quad (13)$$

For example, in a 5 V to 3.3 V application, if a 4.7 µF capacitor is used at the output, a 6.8 pF feed-forward capacitor is recommended. The output capacitor value dictates the loop crossover frequency, f_{CO}. For an output capacitor of 4.7 µF, the loop crossover frequency is 150 kHz.

The high frequency zero created by C_{FF} and R1 can be very important for transient load applications. Capacitor C_{FF} provides phase lead and functions as a speed-up capacitor to output voltage changes, so it tends to short out R1 and improve the high frequency response. This zero tends to produce a positive-going bump in the phase plot. Ideally, the peak of this bump is centered over the crossover frequency of the loop. The R1 and C_{FF} zero is located at

$$f_Z = 1/(2\pi \times R1 \times C_{FF}) \quad (14)$$

The ADP2102-xx (where xx represents the fixed output voltage) includes the resistive voltage divider internally, reducing the external circuitry required. For improved load regulation, connect the FB/OUT to the output voltage as close as possible to the load.

For more information about the ADP2102-ADJ configurations for V_{OUT}, see Table 7.

Table 7. ADP2102-ADJ Configurations for V_{OUT}

V_{OUT} (V)	R_1 (kΩ)	R_2 (kΩ)	C_{FF} (pF)	L (µH)	C_{IN} (µF)	C_{OUT} (µF)
0.8	1	80.6	None	2.2	2.2	4.7
1.0	20	100	None	2.2	2.2	4.7
1.2	49.9	100	None	2.2	2.2	4.7
1.25	56.2	100	None	2.2	2.2	4.7
1.375	71.5	100	None	2.2	2.2	4.7
1.5	88.7	100	None	2.2	2.2	4.7
1.8	124	100	None	2.2	2.2	4.7
1.875	133	100	None	2.2	2.2	4.7
2.0	150	100	15	2.2	2.2	4.7
2.5	215	100	10	2.2	2.2	4.7
3.0	274	100	8.2	2.2	2.2	4.7
3.3	316	100	6.8	2.2	2.2	4.7

EFFICIENCY CONSIDERATIONS

Efficiency is defined as the ratio of output power to input power. The high efficiency of the ADP2102 has two distinct advantages. First, only a small amount of power is lost in the dc-to-dc converter package that reduces thermal constraints. In addition, high efficiency delivers the maximum output power for the given input power, extending battery life in portable applications.

Following are the four major sources of power loss in dc-to-dc converters like the ADP2102:

- Power switch conduction losses
- Inductor losses
- Switching losses
- Transition losses

Power Switch Conduction Losses

Power switch conduction losses are caused by the flow of output current through the P-channel power switch and the N-channel synchronous rectifier, which have internal resistances ($R_{DS(ON)}$) associated with them. The amount of power loss can be approximated by

$$P_{SW\_COND} = (R_{DS\,(ON)\_P} \times D + R_{DS\,(ON)\_N} \times (1 - D)) \times I_{OUT}^2 \quad (15)$$

where $D = V_{OUT}/V_{IN}$.

The internal resistance of the power switches increases with temperature but decreases with higher input voltage. Figure 24 in the Typical Performance Characteristics section shows the change in $R_{DS\,(ON)}$ vs. input voltage, and Figure 25 shows the change in $R_{DS\,(ON)}$ vs. temperature for both power devices.

Inductor Losses

Inductor conduction losses are caused by the flow of current through the inductor, which has an internal resistance (DCR) associated with it. Larger sized inductors have smaller DCR, which may decrease inductor conduction losses.

Inductor core losses are related to the magnetic permeability of the core material. Because the ADP2102 is a high switching frequency dc-to-dc converter, shielded ferrite core material is recommended for its low core losses and low EMI.

The total amount of inductor power loss can be calculated by

$$P_L = DCR \times I_{OUT}^2 + Core\ Losses \quad (16)$$

Switching Losses

Switching losses are associated with the current drawn by the driver to turn on and turn off the power devices at the switching frequency. Each time a power device gate is turned on and turned off, the driver transfers a charge ΔQ from the input supply to the gate and then from the gate to ground.

The amount of power loss can be calculated by

$$P_{SW} = (C_{GATE\_P} + C_{GATE\_N}) \times V_{IN}^2 \times f_{SW} \quad (17)$$

where:
C_{GATE_P} is the gate capacitance of the internal high-side switch.
C_{GATE_N} is the gate capacitance of the internal low-side switch.
f_{SW} is the switching frequency.

Transition Losses

Transition losses occur because the P-channel switch cannot turn on or turn off instantaneously. In the middle of an LX node transition, the power switch provides all the inductor current. The source to drain voltage of the power switch is half the input voltage, resulting in power loss. Transition losses increase with load current and input voltage and occur twice for each switching cycle.

The amount of power loss can be calculated by

$$P_{TRAN} = V_{IN}/2 \times I_{OUT} \times (t_R + t_F) \times f_{SW} \quad (18)$$

where:
t_R is the rise time of the LX node.
t_F is the fall time of the LX node.

THERMAL CONSIDERATIONS

In most applications, the ADP2102 does not dissipate a lot of heat, due to its high efficiency. However, in applications with maximum loads at high ambient temperature, low supply voltage, and high duty cycle, the heat dissipated in the package is great enough that it may cause the junction temperature of the die to exceed the maximum junction temperature of 125°C. Once the junction temperature exceeds 150°C, the converter goes into thermal shutdown. It recovers only after the junction temperature has decreased to below 135°C to prevent any permanent damage. Therefore, thermal analysis for the chosen application solution is very important to guarantee reliable performance over all conditions.

The junction temperature of the die is the sum of the ambient temperature of the environment and the temperature rise of the package due to power dissipation, shown in the following equation:

$$T_J = T_A + T_R \quad (19)$$

where:
T_J is the junction temperature.
T_A is the ambient temperature.
T_R is the rise in temperature of the package due to power dissipation in it.

The rise in temperature of the package is directly proportional to the power dissipation in the package. The proportionality constant for this relationship is defined as the thermal resistance from the junction of the die to the ambient temperature, as shown in the following equation:

$$T_R = \theta_{JA} \times P_D \quad (20)$$

where:
T_R is the rise in temperature of the package.
θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature of the package.
P_D is the power dissipation in the package.

DESIGN EXAMPLE

The calculations in this section provide only a rough estimate and are no substitute for bench evaluation.

Consider an application where the ADP2102 is used to step down from 3.6 V to 1.8 V with an input voltage range of 2.7 V to 4.2 V.

V_{OUT} = 1.8 V @ 600 mA

Pulsed Load = 300 mA

V_{IN} = 2.7 V to 4.2 V (3.6 V typical)

f_{SW} = 3 MHz (typical)

T_A = 85°C

Inductor

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L} \approx \frac{I_{LOAD\,(MAX)}}{3} = 0.6/3 = 200\ \text{mA}$$

$$L = \frac{V_{OUT} \times (1 - V_{OUT}/V_{INMAX})}{f_{SW} \times 0.3 \times I_{LOAD\,(MAX)}} = \frac{1.8 \times (1 - 1.8/4.2)}{(3 \times 10^6 \times 0.3 \times 0.6)} = 1.90\ \mu\text{H}$$

Choose a 2.2 µH inductor for this application.

$I_{PK} = I_{LOAD(MAX)} + \Delta I_L/2 = 0.6 + 0.2/2 = 0.7$ A

$P_L = I_{OUTMAX}^2 \times DCR =$
$(0.6\ \text{A})^2 \times 0.08\ \Omega$ (FDK MIPF2520D) = 29 mW

Output Capacitor

For transient applications, assume a droop of 0.1 V. Typically, it takes two to three cycles for the output to settle from a load transient because the capacitor alone supplies the load current until the loop responds.

Under these conditions, a minimum required output capacitance is calculated as follows:

$$C_{OUT\_MIN} = 3 \times \frac{\Delta I_{LOAD}}{V_{DROOP} \times f_{SW}} = \frac{3 \times 0.3}{0.1 \times 3 \times 10^6} = 3\ \mu F$$

Choose a 4.7 µF capacitor for this application.

For an instantaneous step decrease in load current, the output capacitor required to limit the output voltage overshoot (V_{OS}) during a full load to no load transient must be determined. This transient requires the excess energy stored in the output inductor to be absorbed by the output capacitor with a limited overshoot in the output voltage.

Assuming an overshoot of 50 mV for a full load transient,

$$C_{OUT} = \frac{L \times {I_{OUT}}^2}{(V_{OUT} + V_{OS})^2 - {V_{OUT}}^2} = \frac{2.2\ \mu H \times (0.6)^2}{(1.85)^2 - (1.8)^2} = 4.33\ \mu F$$

Choose a 4.7 µF capacitor for this application.

$$I_{rms} = \frac{1}{2\sqrt{3}} \times \frac{V_{OUT} \times (V_{IN\_MAX} - V_{OUT})}{L \times f_{SW} \times V_{IN\_MAX}} = \frac{1}{2\sqrt{3}} \times \frac{1.8 \times (4.2 - 1.8)}{2.2 \times 10^{-6} \times 3 \times 10^6 \times 4.2} = 45\ mA\ rms$$

$P_{COUT} = I_{rms}^2 \times ESR = (0.045)^2 \times 0.005 = 10.12\ \mu W$

Input Capacitor

Assume an input ripple of 27 mV based on 1% of V_{IN_MIN}.

For ceramic capacitors, the typical ESR is from 5 mΩ to 15 mΩ.

$$C_{IN} = \frac{1}{(\Delta V_{IN} / I_{OUT} - ESR) \times 4 \times f_{SW}} = \frac{1}{(0.027/0.6 - 0.005) \times 4 \times 3 \times 10^6} = 2.2\ \mu F$$

$I_{rms} = I_{OUT}/2 = 0.3$ A rms

$P_{CIN} = I_{rms}^2 \times ESR = (0.3)^2 \times 0.005 = 450\ \mu W$

Losses

$P_{SW\_COND} = (R_{DS\ (ON)\_P} \times D + R_{DS\ (ON)\_N} \times (1 - D)) \times I_{OUT}^2 =$
$(0.310 \times 0.5 + 0.145 \times 0.5) \times (0.6)^2 = 82$ mW

$P_{TRAN} = (V_{IN}/2) \times I_{OUT} \times (t_R + t_F) \times f_{SW} =$
$(3.6/2) \times 0.6 \times (5\ ns + 5\ ns) \times 3 \times 10^6 = 32.4$ mW

$P_{SW} = (C_{GATE\_P} + C_{GATE\_N}) \times V_{IN}^2 \times f_{SW} = (200\ pF) \times$
$(3.6)^2 \times 3 \times 10^6 = 7.8$ mW

$P_L = DCR \times I_{OUT}^2 = 0.08 \times (0.6)^2 = 28.8$ mW

$P_{LOSS} = P_{SW\_COND} + P_{TRAN} + P_{SW} + P_L =$
82 mW + 32.4 mW + 7.8 mW + 28.8 mW = 151 mW

$T_{JMAX} = T_A + \theta_{JA}$

$P_{LOSS} = 85°C + 54°C/W \times 151\ mW = 93.15°C$

P_{LOSS} is well below the junction temperature maximum of 125°C.

CIRCUIT BOARD LAYOUT RECOMMENDATIONS

Good circuit board layout is essential in obtaining the best performance from the ADP2102. Poor circuit layout degrades the output ripple and regulation, as well as the EMI and electromagnetic compatibility performance.

Figure 52 and Figure 53 show the ideal circuit board layout for the typical applications circuit shown in Figure 48. Use this layout to achieve the highest performance. Refer to the following guidelines for optimum layout:

- Use separate analog and power ground planes. Connect the ground reference of sensitive analog circuitry, such as output voltage divider components, to analog ground. In addition, connect the ground references of power components, such as input and output capacitors, to power ground. Connect both ground planes to the exposed pad of the ADP2102.
- Place the input capacitor as close to the PVIN pin as possible and connect the other end to the closest power ground plane.
- For low noise and better transient performance, a filter is recommended between PVIN and AVIN. Place the 0.1 µF, 10 Ω low-pass input filter between the AVIN pin and the PVIN pin, as close to AVIN as possible; or the AVIN pin can be bypassed with a ≥1 pF capacitor to the nearest GND plane.
- Ensure that the high current loops are as short and as wide as possible. Make the high current path from C_{IN} through L, C_{OUT}, and the PGND plane back to C_{IN} as short as possible. To accomplish this, ensure that the input and output capacitors share a common PGND plane. In addition, make the high current path from the PGND pin through L and C_{OUT} back to the PGND plane as short as possible. To do this, ensure that the PGND pin of the ADP2102 is tied to the PGND plane as close as possible to the input and output capacitors.
- Place the feedback resistor divider network as close as possible to the FB pin to prevent noise pickup. Try to minimize the length of trace connecting the top of the feedback resistor divider to the output while keeping away from the high current traces and the switch node (LX) that can lead to noise pickup. To reduce noise pickup, place an analog ground plane on either side of the FB trace and make it as small as possible to reduce the parasitic capacitance pickup.

RECOMMENDED LAYOUT

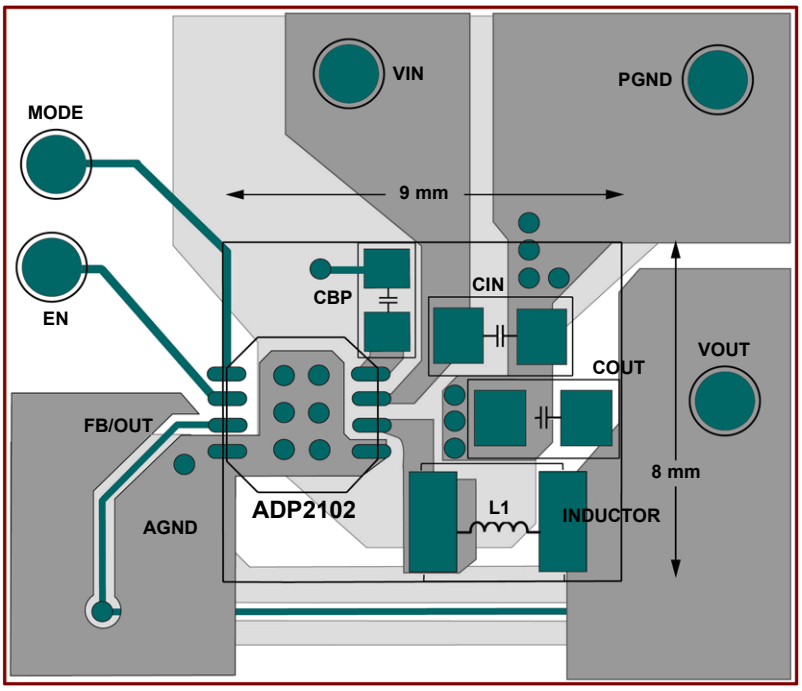

Figure 51. Recommended PCB Layout of the ADP2102-FXD

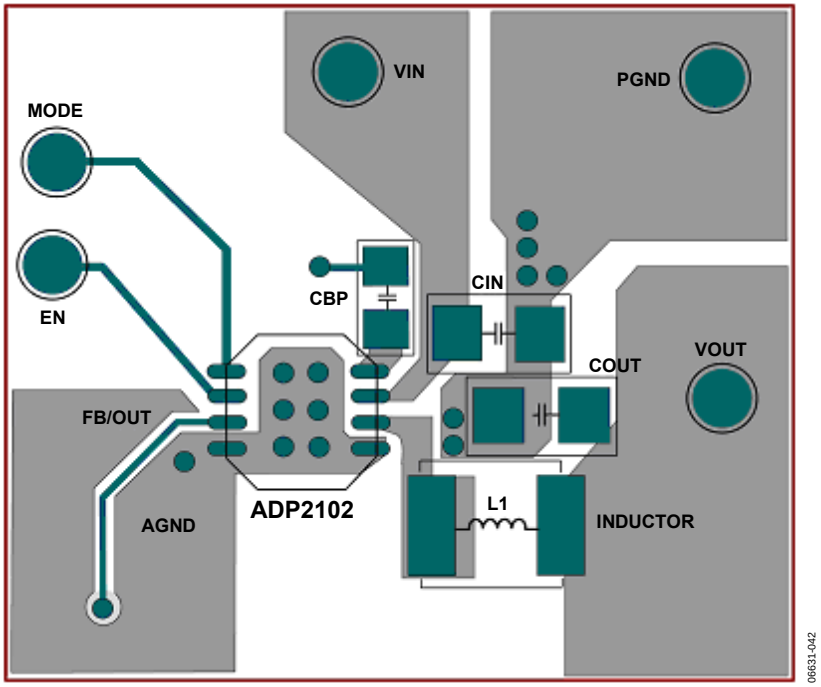

Figure 52. Recommended Layout of the Top Layer of the ADP2102-FXD Application Board

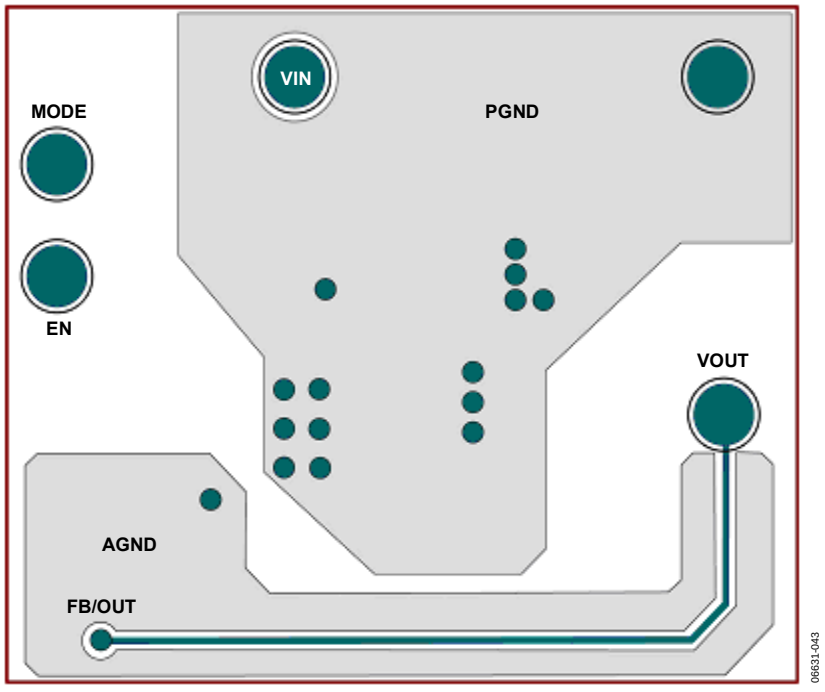

Figure 53. Recommended Layout of the Bottom Layer of the ADP2102-FXD Application Board

OUTLINE DIMENSIONS

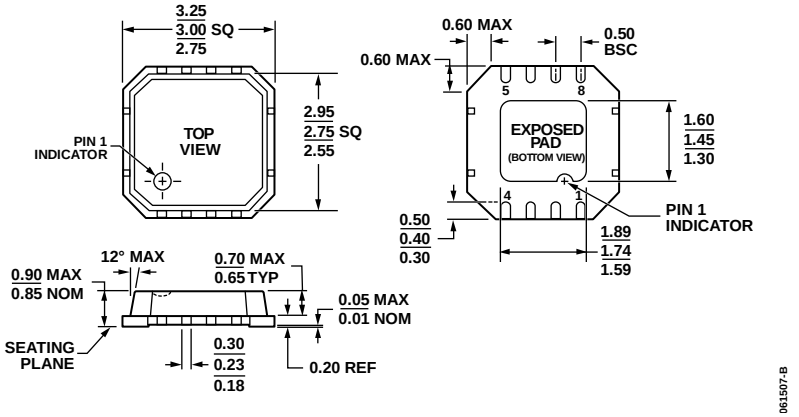

Figure 54. 8-Lead Lead Frame Chip Scale Package [LFCSP_VD]
3 mm × 3 mm Body, Very Thin, Dual Lead
(CP-8-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Output Current (mA)	Temperature Range[3]	Output Voltage	Package Description	Package Option	Branding
ADP2102YCPZ-0.8-R7[1]	600	−40°C to +85°C	0.8 V	8-Lead LFCSP_VD	CP-8-2	L5T
ADP2102YCPZ-1.0-R7[1]	600	−40°C to +85°C	1.0 V	8-Lead LFCSP_VD	CP-8-2	L5U
ADP2102YCPZ-1.2-R7[1]	600	−40°C to +85°C	1.2 V	8-Lead LFCSP_VD	CP-8-2	L5V
ADP2102YCPZ-1.25R7[1]	600	−40°C to +85°C	1.25 V	8-Lead LFCSP_VD	CP-8-2	L5W
ADP2102YCPZ-1.37R7[1]	600	−40°C to +85°C	1.375 V	8-Lead LFCSP_VD	CP-8-2	L5X
ADP2102YCPZ-1.5-R7[1]	600	−40°C to +85°C	1.5 V	8-Lead LFCSP_VD	CP-8-2	L5Y
ADP2102YCPZ-1.8-R7[1]	600	−40°C to +85°C	1.8 V	8-Lead LFCSP_VD	CP-8-2	L5Z
ADP2102YCPZ-1.87R7[1]	600	−40°C to +85°C	1.875 V	8-Lead LFCSP_VD	CP-8-2	L60
ADP2102YCPZ-1-R7[1]	600	−40°C to +85°C	0.8 V to 1.2 V	8-Lead LFCSP_VD	CP-8-2	L6K
ADP2102YCPZ-2-R7[1]	600	−40°C to +85°C	1.2 V to 1.5 V	8-Lead LFCSP_VD	CP-8-2	L6L
ADP2102YCPZ-3-R7[1]	600	−40°C to +85°C	1.5 V to 1.875 V	8-Lead LFCSP_VD	CP-8-2	L6M
ADP2102YCPZ-4-R7[1]	600	−40°C to +85°C	2.5 V to 3.3 V[2]	8-Lead LFCSP_VD	CP-8-2	L6N
ADP2102-0.8-EVALZ[1]			Fixed Output 0.8 V	Evaluation Board		
ADP2102-1.0-EVALZ[1]			Fixed Output 1.0 V	Evaluation Board		
ADP2102-1.2-EVALZ[1]			Fixed Output 1.2 V	Evaluation Board		
ADP2102-1.25-EVALZ[1]			Fixed Output 1.25 V	Evaluation Board		
ADP2102-1.375-EVALZ[1]			Fixed Output 1.375 V	Evaluation Board		
ADP2102-1.5-EVALZ[1]			Fixed Output 1.5 V	Evaluation Board		
ADP2102-1.8-EVALZ[1]			Fixed Output 1.8 V	Evaluation Board		
ADP2102-1.875EVALZ[1]			Fixed Output 1.875 V	Evaluation Board		
ADP2102-1-EVALZ[1]			Adjustable Output 0.8 V to 1.2 V	Evaluation Board		
ADP2102-2-EVALZ[1]			Adjustable Output 1.2 V to 1.5 V	Evaluation Board		
ADP2102-3-EVALZ[1]			Adjustable Output 1.5 V to1.875 V	Evaluation Board		
ADP2102-4-EVALZ[1]			Adjustable Output 2.5 V to 3.3 V	Evaluation Board		

[1] Z = RoHS Compliant Part.
[2] 2.5 V to 3.3 V adjustable output voltage option is from 4.5 V < V_{IN} < 5.5 V only.
[3] Operating junction temperature range: −40°C to +125°C.

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