

ISL90462

Single Volatile 32-tap XDCP Digitally Controlled Potentiometer (XDCP™)

FN8230
Rev 4.00
October 20, 2015

The Intersil ISL90462 is a digitally controlled potentiometer (XDCP). Configured as a variable resistor, the device consists of a resistor array, wiper switches, a control section, and volatile memory. The wiper position is controlled by a 2-pin Up /Down interface.

The potentiometer is implemented by a resistor array composed of 31 resistive elements and a wiper switching network. Between each element and at either end are tap points accessible to the wiper terminal. The position of the wiper element is controlled by the \overline{CS} and U/\overline{D} inputs.

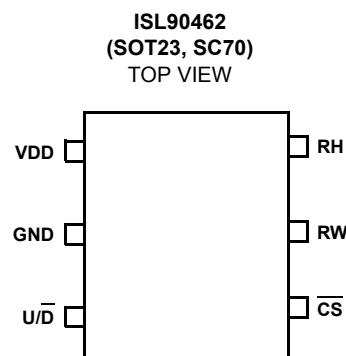
The device can be used in a wide variety of applications including:

- LCD contrast control
- Parameter and bias adjustments
- Industrial and Automotive Control
- Transducer adjustment of pressure, temperature, position, chemical, and optical sensors
- Laser Diode driver biasing
- Gain control and offset adjustment

Features

- Volatile Solid-State Potentiometer
- 2-pin UP/DN Interface
- DCP Terminal Voltage, 2.7V to 5.5V
- Tempco 35ppm/°C Typical
- 32 Wiper Tap Points
- Low Power CMOS
 - Active current, 25µA max.
 - Supply current 0.3µA
- Available R_{TOTAL} Values = 10kΩ, 50kΩ, 100kΩ
- Temperature Range -40°C to +85°C
- Packages
 - 6 Ld SC-70, SOT-23
- Pb-Free Plus Anneal Available (RoHS Compliant)

Pinout

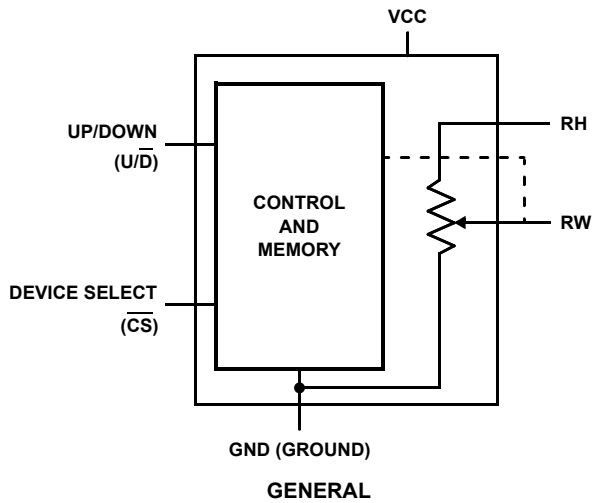


Ordering Information

| PART NUMBER | PART MARKING | R_{TOTAL} (K) | TEMP RANGE (°C) | PACKAGE (Tape and Reel) | PKG. DWG. # |
|---|--------------|-----------------|-----------------|-------------------------|-------------|
| ISL90462WIE627Z-TK (See Note) | DEK | 10 | -40 to +85 | 6 Ld SC-70 (Pb-free) | P6.049 |
| ISL90462WIH627Z-TK (See Note) | DEL | | -40 to +85 | 6 Ld SOT-23 (Pb-free) | P6.064 |
| ISL90462UIE627Z-TK (See Note) | DEI | 50 | -40 to +85 | 6 Ld SC-70 (Pb-free) | P6.049 |
| ISL90462UIH627Z-TK (See Note) | DEJ | | -40 to +85 | 6 Ld SOT-23 (Pb-free) | P6.064 |
| ISL90462TIE627Z-TK (See Note) | DEG | 100 | -40 to +85 | 6 Ld SC-70 (Pb-free) | P6.049 |
| ISL90462TIH627Z-TK (See Note) (No longer available, recommended replacement: SL90462UIE627Z-TK) | DEH | | -40 to +85 | 6 Ld SOT-23 (Pb-free) | P6.064 |

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020

Block Diagram



Pin Descriptions

| 6-PIN | SYMBOL | DESCRIPTION |
|-------|-------------|---------------------|
| 1 | VDD | Supply voltage |
| 2 | GND | Ground/Low terminal |
| 3 | U/\bar{D} | Up - Down |
| 4 | CS | Chip select |
| 5 | RW | Wiper terminal |
| 6 | RH | High terminal |

Absolute Maximum Ratings

Storage Temperature -65°C to +150°C
 Voltage on CS, U/D and VCC With Respect to GND . . . -1V to +7V
 Lead Temperature (soldering 10s) 300°C
 I_W (10s) ±6mA
 Power Rating 1mW

Recommended Operating Conditions

Temperature Range (Industrial) -40°C to 85°C
 V_{CC} 2.7V to 5.5V

CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device (at these or any other conditions above those listed in the operational sections of this specification) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

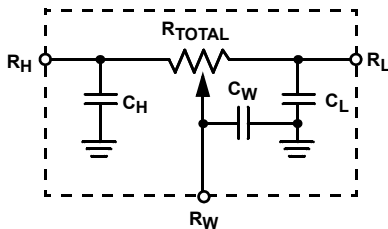
Potentiometer Specifications

Over recommended operating conditions unless otherwise stated.

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN | TYP (Note 4) | MAX | UNIT |
|---------------|-------------------------------------|---|-----|-----------------|----------|----------------|
| R_{TOT} | End to end resistance | W version | 8 | 10 | 12 | k Ω |
| | | U version | 40 | 50 | 60 | k Ω |
| | | T version | 80 | 100 | 120 | k Ω |
| V_R | RH, R_L terminal voltages | | 0 | | V_{CC} | V |
| | Noise | Ref: 1kHz | | -120 | | dBV |
| R_W | Wiper Resistance | | | 600 | | Ω |
| I_W | Wiper Current | | | | 0.6 | mA |
| | Resolution | | 1 | | 32 | Taps |
| | Absolute linearity (Note 1) | $R_{H(n)}(\text{actual}) - R_{H(n)}(\text{expected})$ | | | ±1 | MI (Note 3) |
| | Relative linearity (Note 2) | $R_{H(n+1)} - [R_{H(n)} + MI]$ | | | ±0.5 | MI (Note 3) |
| | R_{TOTAL} temperature coefficient | | | ±35 | | ppm/°C |
| $C_H/C_L/C_W$ | Potentiometer capacitances | See Equivalent Circuit | | 10/10/25 | | pF |

NOTES:

- Absolute linearity is utilized to determine actual wiper voltage versus expected voltage = $(R_{H(n)}(\text{actual}) - R_{H(n)}(\text{expected})) = \pm 1$ MI Maximum. $n = 1 \dots 29$ only
- Relative linearity is a measure of the error in step size between taps = $R_{H(n+1)} - [R_{H(n)} + MI] = \pm 0.5$ MI, $n = 1 \dots 29$ only.
- 1 MI = Minimum Increment = $R_{TOTAL}/31$.
- Typical values are for $T_A = 25^\circ\text{C}$ and nominal supply voltage.

Equivalent Circuit

DC Electrical Specifications Over recommended operating conditions unless otherwise specified.

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN | TYP (NOTE 4) | MAX | UNIT |
|----------|--|---|---------------------|--------------|---------------------|---------|
| I_{CC} | V_{CC} active current (Increment) | $\overline{CS} = 0V, U/\overline{D} = f_{clock} = 1MHz$ and $V_{CC} = 3V$ | | | 25 | μA |
| I_{SB} | Standby supply current | $\overline{CS} = V_{CC}, U/\overline{D} = GND$ or $V_{CC} = 3V$ | | 0.3 | 1 | μA |
| I_{LI} | CS input leakage current | $V_{IN} = GND$ to V_{CC} | | | ± 1 | μA |
| V_{IH} | $\overline{CS}, U/\overline{D}$ input HIGH voltage | | $V_{CC} \times 0.7$ | | | V |
| V_{IL} | $\overline{CS}, U/\overline{D}$ input LOW voltage | | | | $V_{CC} \times 0.3$ | V |
| C_{IN} | $\overline{CS}, U/\overline{D}$ input capacitance | $V_{CC} = 3V, V_{IN} = GND, T_A = 25^\circ C, f = 1MHz$ | | 10 | | pF |

Timing Specifications Over recommended operating conditions unless otherwise specified

| SYMBOL | PARAMETER | MIN | TYP (Note 4) | MAX | UNIT |
|--------------|---|-----|--------------|-----|---------|
| t_{CU} | U/\overline{D} to \overline{CS} setup | 25 | | | ns |
| t_{CI} | \overline{CS} to U/\overline{D} setup | 50 | | | ns |
| t_{IC} | \overline{CS} to U/\overline{D} hold | 25 | | | ns |
| t_{iL} | U/\overline{D} LOW period | 300 | | | ns |
| t_{iH} | U/\overline{D} HIGH period | 300 | | | ns |
| f_{TOGGLE} | Up/Down toggle Rate | | 1 | | MHz |
| t_{SETTLE} | Output settling time | | 1 | | μs |

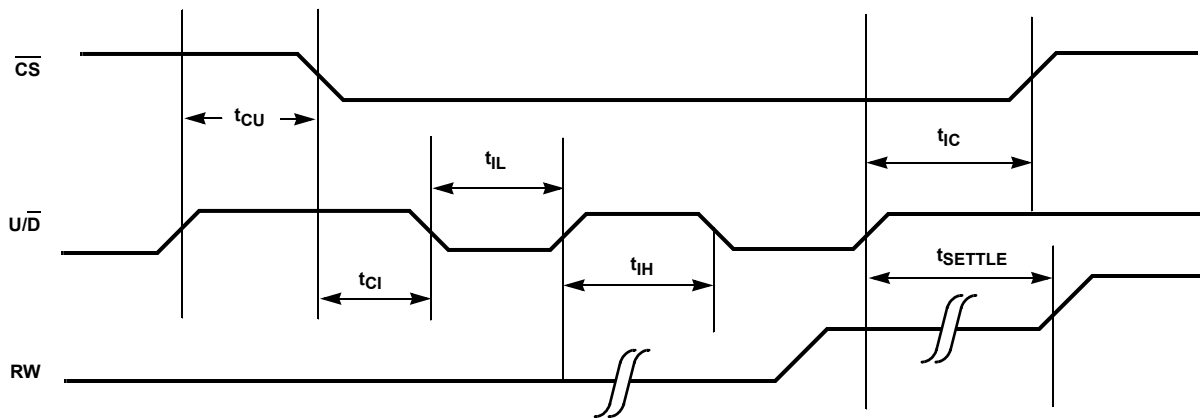


FIGURE 1. SERIAL INTERFACE TIMING DIAGRAM, INCREMENT

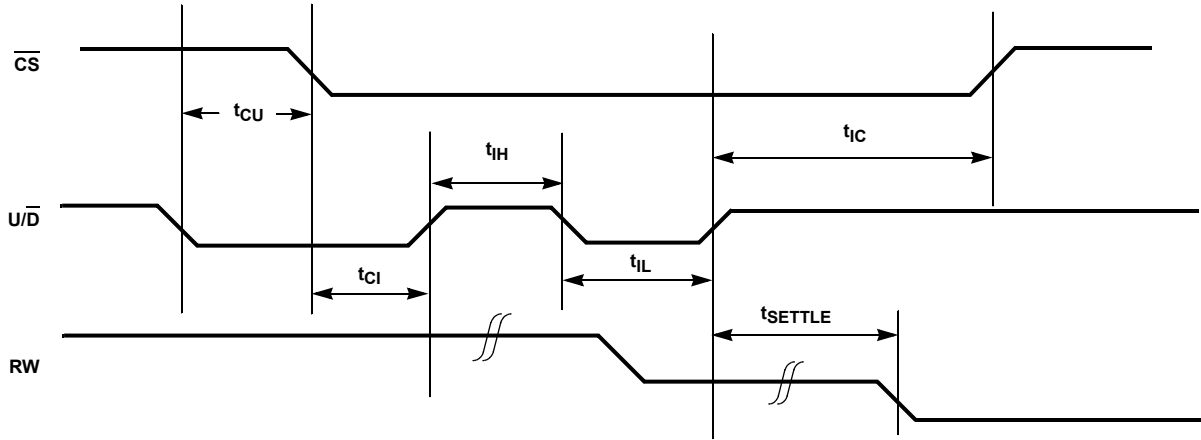


FIGURE 2. SERIAL INTERFACE TIMING DIAGRAM DECREMENT

Pin Descriptions

RH and RW

The ISL90462 contains a digital potentiometer with one terminal tied to the ground pin (GND) of the device. The RH pin is the other potentiometer terminal, and the RW pin is the wiper terminal. The position of the wiper is controlled by the \overline{CS} - and U/\overline{D} - inputs, with a movement "up" connecting the wiper closer to the RH pin, and movement "down" connection the wiper closer to the GND pin.

Up/Down (U/\overline{D})

The U/\overline{D} input controls the direction of the wiper movement and whether the counter is incremented or decremented.

Chip Select (\overline{CS})

The device is selected when the \overline{CS} input is LOW. The current counter value is stored in volatile memory when \overline{CS} is returned HIGH. When \overline{CS} is high, the device is placed in low power standby mode.

Principles of Operation

There are two sections of the ISL90462: the input control, counter and decode section; and the resistor array. The input control section operates just like an up/down counter. The output of this counter is decoded to turn on a single electronic switch connecting a point on the resistor array to the wiper output. The resistor array is comprised of 31 individual resistors connected in series. At either end of the array and between each resistor is an electronic switch that transfers the connection at that point to the wiper. The RH and RW terminals are uncommitted, and can for a variable voltage divider if RH is connected to a voltage source.

The direction of the wiper movement is defined when the device is selected. If during \overline{CS} transition from High to Low the U/\overline{D} input is LOW, the wiper will move down on each rising edge of U/\overline{D} toggling. Similarly, the wiper will move up on each rising edge of U/\overline{D} toggling if, during \overline{CS} transition from High to Low, the U/\overline{D} input is High.

The wiper, when at either fixed terminal, acts like its mechanical equivalent and does not move beyond the last position. That is, the counter does not wrap around when clocked to either extreme.

If the wiper is moved several positions, multiple taps are connected to the wiper for t_{SETTLE} (U/\overline{D} to RW change). The 2-terminal resistance value for the device can temporarily change by a significant amount if the wiper is moved several positions.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

| DATE | REVISION | CHANGE |
|------------------|----------|--|
| October 20, 2015 | FN8230.4 | <ul style="list-style-type: none"> - Updated Ordering Information Table on page 1. - Added Revision History. - Added About Intersil Verbiage. - Updated POD P6.064 to latest revision changes are as follow: Update to new format (same dimensions, added land pattern and moved dimensions from table onto drawing) - Updated POD P6.049 to latest revision changes are as follow: Added pin 1 cross-hatched index area to top view. Added Note 8, it reference to Pin 1 Index Area. A2 minimum measurement changed from 0.00 to 0.79. |

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You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

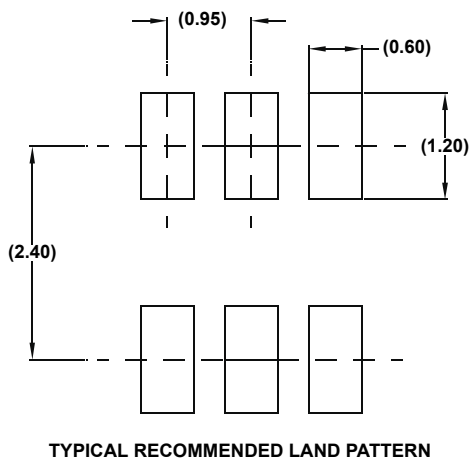
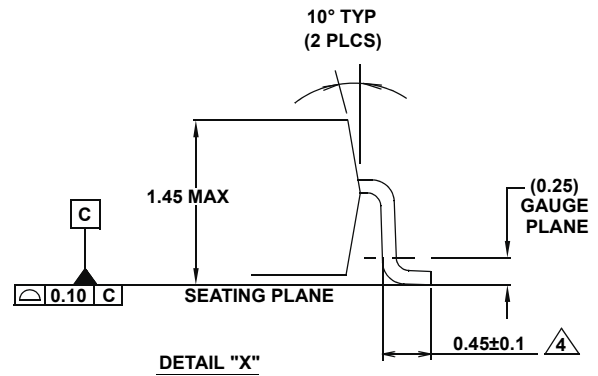
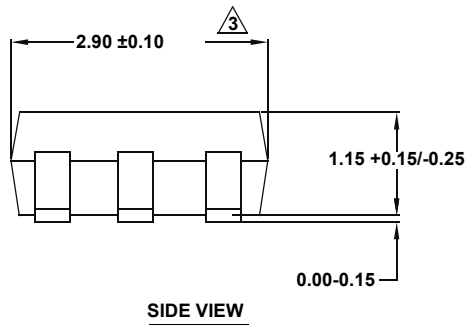
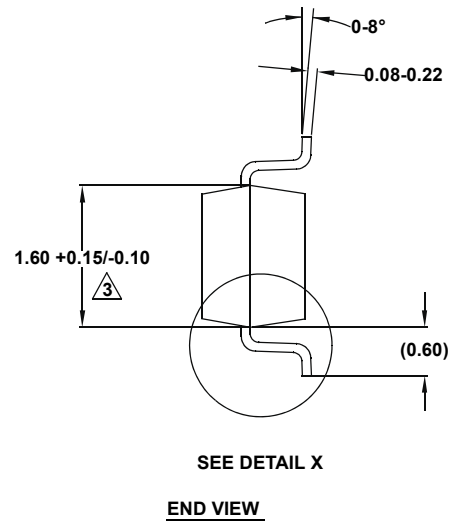
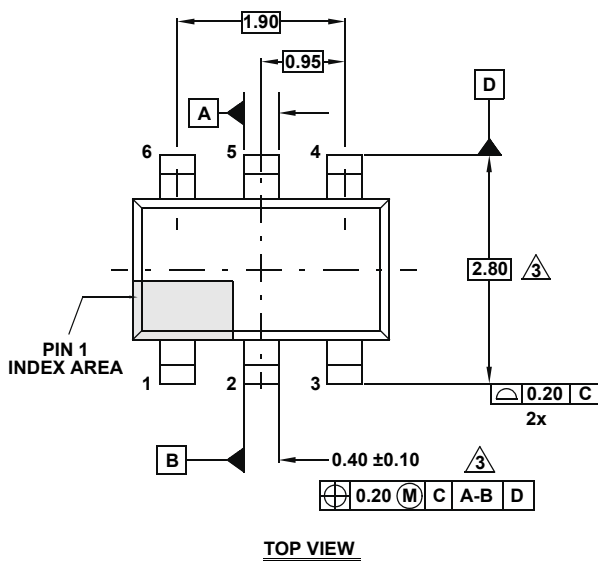
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Package Outline Drawing

P6.064

6 LEAD SMALL OUTLINE TRANSISTOR PLASTIC PACKAGE

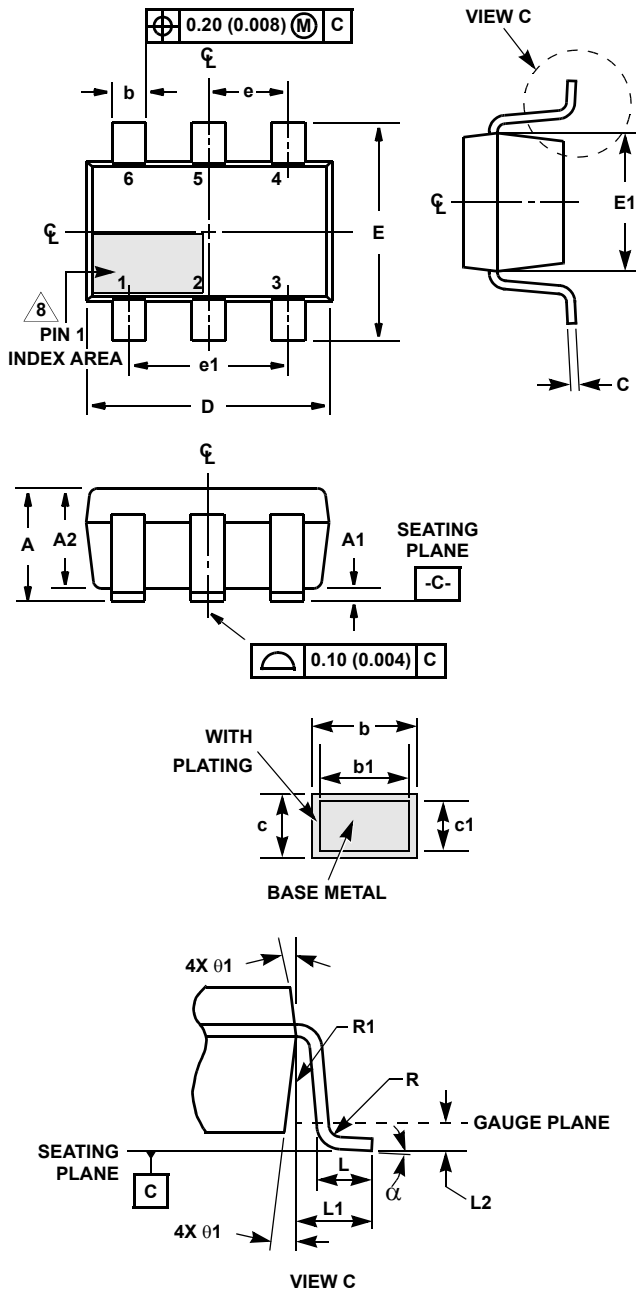
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NOTES:

1. Dimensions are in millimeters.
Dimensions in () for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
3. Dimension is exclusive of mold flash, protrusions or gate burrs.
4. Foot length is measured at reference to gauge plane.
5. Package conforms to JEDEC MO-178AB.

Small Outline Transistor Plastic Packages (SC70-6)



P6.049

6 LEAD SMALL OUTLINE TRANSISTOR PLASTIC PACKAGE

| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|--------|------------|-------|-------------|------|-------|
| | MIN | MAX | MIN | MAX | |
| A | 0.031 | 0.043 | 0.80 | 1.10 | - |
| A1 | 0.000 | 0.004 | 0.00 | 0.10 | - |
| A2 | 0.031 | 0.039 | 0.79 | 1.00 | - |
| b | 0.006 | 0.012 | 0.15 | 0.30 | - |
| b1 | 0.006 | 0.010 | 0.15 | 0.25 | |
| c | 0.003 | 0.009 | 0.08 | 0.22 | 6 |
| c1 | 0.003 | 0.009 | 0.08 | 0.20 | 6 |
| D | 0.073 | 0.085 | 1.85 | 2.15 | 3 |
| E | 0.071 | 0.094 | 1.80 | 2.40 | - |
| E1 | 0.045 | 0.053 | 1.15 | 1.35 | 3 |
| e | 0.0256 Ref | | 0.65 Ref | | - |
| e1 | 0.0512 Ref | | 1.30 Ref | | - |
| L | 0.010 | 0.018 | 0.26 | 0.46 | 4 |
| L1 | 0.017 Ref. | | 0.420 Ref. | | |
| L2 | 0.006 BSC | | 0.15 BSC | | |
| N | 6 | | 6 | | 5 |
| R | 0.004 | - | 0.10 | - | |
| R1 | 0.004 | 0.010 | 0.15 | 0.25 | |
| α | 0° | 8° | 0° | 8° | - |

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NOTES:

1. Dimensioning and tolerance per ASME Y14.5M-1994.
2. Package conforms to EIAJ SC70 and JEDEC MO203AB.
3. Dimensions D and E1 are exclusive of mold flash, protrusions, or gate burrs.
4. Footlength L measured at reference to gauge plane.
5. "N" is the number of terminal positions.
6. These Dimensions apply to the flat section of the lead between 0.08mm and 0.15mm from the lead tip.
7. Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only.
8. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

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