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FAIRCHILD SEMICONDUCTOR®

December 2010

NC7SP126
TinyLogic® ULP Buffer with Three-State Output

Features

- 0.9V to 3.6V V_{CC} Supply Operation
- 3.6V Over-Voltage Tolerant I/O's at V_{CC} from 0.9V to 3.6V
- Extremely High Speed t_{PD}
  - 3.0ns: Typical for 3.0V to 3.6V V_{CC}
  - 4.0ns: Typical for 2.3V to 2.7V V_{CC}
  - 5.0ns: Typical for 1.65V to 1.95V V_{CC}
  - 6.0ns: Typical for 1.4V to 1.6V V_{CC}
  - 10.0ns: Typical for 1.1V to 1.3V V_{CC}
  - 26.0ns: Typical for 0.9V V_{CC}
- Power-Off High-Impedance Inputs and Outputs
- Static Drive (I_{OH}/I_{OL})
  - ±2.6mA at 3.00V V_{CC}
  - ±2.1mA at 2.30V V_{CC}
  - ±1.5mA at 1.65V V_{CC}
  - ±1.0mA at 1.4V V_{CC}
  - ±0.5mA at 1.1V V_{CC}
  - ±020µA at 0.9V V_{CC}
- Uses Proprietary Quiet Series™ Noise/EMI Reduction Circuitry
- Ultra-Small MicroPak™ Leadfree Package
- Ultra-Low Dynamic Power

Description

The NC7SP126 is a single Buffer with 3-STATE output from Fairchild's Ultra-Low Power (ULP) series of Tiny-Logic®. Ideal for applications where battery life is critical, this product is designed for ultra-low power consumption within the V_{CC} operating range of 0.9V to 3.6V V_{CC}.

The internal circuit is composed of a minimum of inverter stages, including the output buffer, to enable ultra-low static and dynamic power.

The NC7SP126, for lower drive requirements, is uniquely designed for optimized power and speed, and is fabricated with an advanced CMOS technology to achieve best in class speed operation while maintaining extremely low CMOS power dissipation.

Ordering Information

Part Number	Top Mark	Package	Packing Method
NC7SP126P5X	P26	5-Lead SC70, EIAJ SC-88a, 1.25mm Wide	3000 Units on Tape & Reel
NC7SP126L6X	L6	6-Lead MicroPak™, 1.00mm Wide	5000 Units on Tape & Reel
NC7SP126FHX	L6	6-Lead, MicroPak2™, 1x1mm Body, .35mm Pitch	5000 Units on Tape & Reel

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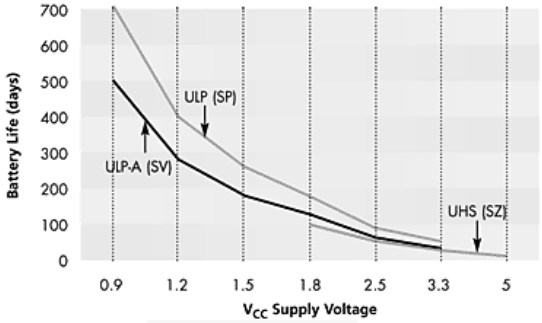
Battery Life



Notes:

1. TinyLogic® ULP and ULP-A with up to 50% less power consumption can extend your battery life significantly.
   Battery Life = $(V_{battery} \bullet I_{battery} \bullet .9)/(P_{device})/24hrs/day$
   Where, $P_{device} = (I_{CC} \bullet V_{CC}) + (C_{PD} + C_L) \bullet V_{CC2} \bullet f$.
2. Assumes ideal 3.6V Lithium Ion battery with current rating of 900mAH and derated 90% and device frequency at 10MHz, with C_L = 15pF load.

Figure 1. Battery Life vs. V_{CC} Supply Voltage

Connection Diagram

Figure 2. Logic Symbol

Pin Configurations

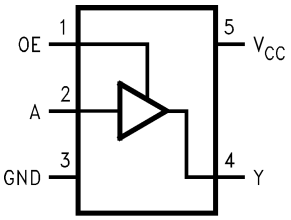


Figure 3. SC70 (Top View)

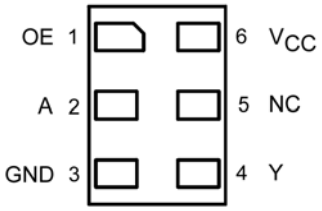


Figure 4. MicroPak™ (Top Through View)

Pin Definitions

Pin # SC70	Pin # MicroPak™	Name	Description
1	1	OE	Input
2	2	A	Input
3	3	GND	Ground
4	4	Y	Output
5	6	V_{CC}	Supply Voltage
	5	NC	No Connect

Function Table

Inputs		Output
OE	**A**	**Out Y**
H	L	L
H	H	H
L	X	Z

H = HIGH Logic Level
L = LOW Logic Level
X = HIGH or LOW Logic Level
Z = HIGH Impedance State

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Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	Supply Voltage		-0.5	4.6	V
V_{IN}	DC Input Voltage		-0.5	4.6	V
V_{OUT}	DC Output Voltage	HIGH or LOW State[3]	-0.5	V_{CC} + 0.5	V
		V_{CC}=0V	-0.5	4.6	
I_{IK}	DC Input Diode Current	V_{IN} < 0V		-50	mA
I_{OK}	DC Output Diode Current	V_{OUT} < 0V		-50	mA
		V_{OUT} > V_{CC}		+50	
I_{OH}/I_{OL}	DC Output Source/Sink Current			±50	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current per Supply Pin			±50	mA
T_{STG}	Storage Temperature Range		-65	+150	°C
T_J	Junction Temperature under Bias			+150	°C
T_L	Junction Lead Temperature, Soldering 10 Seconds			+260	°C
P_D	Power Dissipation at +85°C	SC70-5		150	mW
		MicroPak™-6		130	
		MicroPak2™-6		120	
ESD	Human Body Model, JEDEC:JESD22-A114			4000	V
	Charge Device Model, JEDEC:JESD22-C101			2000	

Note:

3. IO absolute maximum rating must be observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{CC}	Supply Voltage Operating		0.9	3.6	V
V_{IN}	Input Voltage		0	3.6	V
V_{OUT}	Output Voltage	V_{CC}=0V	0	3.6	V
		HIGH or LOW State	0	V_{CC}	
I_{OH}/I_{OL}	Output Current	V_{CC}=3.0V to 3.6V		±2.6	mA
		V_{CC}=2.3V to 2.7V		±2.1	
		V_{CC}=1.65V to 1.95V		±1.5	
		V_{CC}=1.4V to 1.6V		±1.0	
		V_{CC}=1.1V to 1.3V		±0.5	
		V_{CC}=0.9V		±20	µA
T_A	Operating Temperature, Free Air		-40	+85	°C
$\Delta t/\Delta V$	Minimum Input Edge Rate	V_{IN}=0.8V to 2.0, V_{CC}=3.0V		10	ns/V
θ_{JA}	Thermal Resistance	SC70-5		425	°C/W
		MicroPak™-6		500	
		MicroPak2™-6		560	

Note:

4. Unused inputs must be held HIGH or LOW. They may not float.

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DC Electrical Characteristics

Symbol	Parameter	V_{CC}	Conditions	T_A=+25°C		T_A=-40 to +85°C		Units
				Min.	Max.	Min.	Max.	
V_{IH}	HIGH Level Input Voltage	0.90		.65 x V_{CC}		.65 x V_{CC}		V
		1.10 ≤ V_{CC} ≤ 1.30		.65 x V_{CC}		.65 x V_{CC}		
		1.40 ≤ V_{CC} ≤ 1.60		.65 x V_{CC}		.65 x V_{CC}		
		1.65 ≤ V_{CC} ≤ 1.95		.65 x V_{CC}		.65 x V_{CC}		
		2.30 ≤ V_{CC} ≤ 2.70		1.6		1.6		
		3.00 ≤ V_{CC} ≤ 3.60		2.1		2.1		
V_{IL}	LOW Level Input Voltage	0.90			.35 x V_{CC}		.35 x V_{CC}	V
		1.10 ≤ V_{CC} ≤ 1.30			.35 x V_{CC}		.35 x V_{CC}	
		1.40 ≤ V_{CC} ≤ 1.60			.35 x V_{CC}		.35 x V_{CC}	
		1.65 ≤ V_{CC} ≤ 1.95			.35 x V_{CC}		.35 x V_{CC}	
		2.30 ≤ V_{CC} ≤ 2.70			0.7		0.7	
		3.00 ≤ V_{CC} ≤ 3.60			0.9		0.9	
V_{OH}	HIGH Level Output Voltage	0.90	I_{OH}=-20µA	V_{CC}-0.1		V_{CC}-0.1		V
		1.10 ≤ V_{CC} ≤ 1.30		V_{CC}-0.1		V_{CC}-0.1		
		1.40 ≤ V_{CC} ≤ 1.60		V_{CC}-0.1		V_{CC}-0.1		
		1.65 ≤ V_{CC} ≤ 1.95		V_{CC}-0.1		V_{CC}-0.1		
		2.30 ≤ V_{CC} ≤ 2.70		V_{CC}-0.1		V_{CC}-0.1		
		3.00 ≤ V_{CC} ≤ 3.60		V_{CC}-0.1		V_{CC}-0.1		
		1.10 ≤ V_{CC} ≤ 1.30	I_{OH}=-0.5mA	.75 x V_{CC}		.70 x V_{CC}		
		1.40 ≤ V_{CC} ≤ 1.60	I_{OH}=-1mA	1.07		0.99		
		1.65 ≤ V_{CC} ≤ 1.95	I_{OH}=-1.5mA	1.24		1.22		
		2.30 ≤ V_{CC} ≤ 2.70	I_{OH}=-2.1mA	1.95		1.87		
		3.00 ≤ V_{CC} ≤ 3.60	I_{OH}=-2.6mA	2.61		2.55		
V_{OL}	LOW Level Output Voltage	0.90	I_{OL}=20µA		0.1		0.1	V
		1.10 ≤ V_{CC} ≤ 1.30			0.1		0.1	
		1.40 ≤ V_{CC} ≤ 1.60			0.1		0.1	
		1.65 ≤ V_{CC} ≤ 1.95			0.1		0.1	
		2.30 ≤ V_{CC} ≤ 2.70			0.1		0.1	
		3.00 ≤ V_{CC} ≤ 3.60			0.1		0.1	
		1.10 ≤ V_{CC} ≤ 1.30	I_{OL}=0.5mA		.30 x V_{CC}		.30 x V_{CC}	
		1.40 ≤ V_{CC} ≤ 1.60	I_{OL}=1mA		0.31		0.37	
		1.65 ≤ V_{CC} ≤ 1.95	I_{OL}=1.5mA		0.31		0.35	
		2.30 ≤ V_{CC} ≤ 2.70	I_{OL}=2.1mA		0.31		0.33	
		3.00 ≤ V_{CC} ≤ 3.60	I_{OL}=2.6mA		0.31		0.33	
I_{IN}	Input Leakage Current	0.90 to 3.60	0 ≤ V_{IN} ≤ 3.60		±0.1		±0.5	µA
I_{OZ}	3-STATE Output Leakage	0.90 to 3.6	V_{IN}=V_{IH} or V_{IL} 0 ≤ V_{IN} ≤ 3.60		±0.5		±0.5	µA
I_{OFF}	Power Off Leakage Current	0	0 ≤ ($V_{IN,}$ V_O) ≤ 3.60		0.5		0.5	µA
I_{CC}	Quiescent Supply Current	0.90 to 3.60	V_{IN}=V_{CC}, or GND		0.9		0.9	µA

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AC Electrical Characteristics

Symbol	Parameter	V_{CC}	Conditions	T_A=+25°C			T_A=-40 to +85°C		Units	Figure
				Min.	Typ.	Max.	Min.	Max.		
t_{PHL}, t_{PLH}	Propagation Delay	0.90	C_L=10pF, R_L=1MΩ		26				ns	Figure 5 Figure 6
		1.10 ≤ V_{CC} ≤ 1.30		4.0	10.0	19.1	3.5	39.6		
		1.40 ≤ V_{CC} ≤ 1.60		2.0	6.0	11.2	1.5	14.5		
		1.65 ≤ V_{CC} ≤ 1.95		1.5	5.0	8.6	1.0	11.6		
		2.30 ≤ V_{CC} ≤ 2.70		1.0	4.0	6.3	0.8	8.2		
		3.00 ≤ V_{CC} ≤ 3.60		1.0	3.0	5.3	0.5	7.2		
t_{PZL},t_{PZH}	Output Enable Time	0.90	C_L=10pF, R_U=5000Ω R_D=5000Ω		29				ns	Figure 5 Figure 6
		1.10 ≤ V_{CC} ≤ 1.30		4.0	8.0	17.5	3.5	40.4		
		1.40 ≤ V_{CC} ≤ 1.60		2.0	6.0	11.9	1.5	14.8		
		1.65 ≤ V_{CC} ≤ 1.95		1.5	5.0	9.7	1.0	12.3		
		2.30 ≤ V_{CC} ≤ 2.70		1.0	4.0	7.7	0.8	10.5		
		3.00 ≤ V_{CC} ≤ 3.60		1.0	3.0	6.9	0.5	8.6		
t_{PHZ},t_{PLZ}	Output Disable Time	0.90	C_L=10pF, R_U=5000Ω R_D=5000Ω		28				ns	Figure 5 Figure 6
		1.10 ≤ V_{CC} ≤ 1.30		4.0	8.0	20.5	3.5	42.0		
		1.40 ≤ V_{CC} ≤ 1.60		2.0	6.0	15.3	1.5	18.0		
		1.65 ≤ V_{CC} ≤ 1.95		1.5	5.0	14.7	1.0	17.8		
		2.30 ≤ V_{CC} ≤ 2.70		1.0	4.0	13.7	0.8	15.0		
		3.00 ≤ V_{CC} ≤ 3.60		1.0	3.0	13.5	0.5	14.8		
t_{PHL}, t_{PLH}	Propagation Delay	0.90	C_L=15pF, R_L=1MΩ		28				ns	Figure 5 Figure 6
		1.10 ≤ V_{CC} ≤ 1.30		5.0	10.0	20.5	4.5	42.5		
		1.40 ≤ V_{CC} ≤ 1.60		3.0	7.0	11.8	2.5	15.4		
		1.65 ≤ V_{CC} ≤ 1.95		2.0	5.0	9.1	2.0	12.2		
		2.30 ≤ V_{CC} ≤ 2.70		1.5	4.0	6.6	1.0	8.6		
		3.00 ≤ V_{CC} ≤ 3.60		1.0	3.0	5.6	0.5	7.5		
t_{PZL},t_{PZH}	Output Enable Time	0.90	C_L=15pF, R_U=5000Ω R_D=5000Ω		31				ns	Figure 5 Figure 6
		1.10 ≤ V_{CC} ≤ 1.30		5.0	11.0	18.2	4.5	43.3		
		1.40 ≤ V_{CC} ≤ 1.60		3.0	7.0	12.5	2.5	15.5		
		1.65 ≤ V_{CC} ≤ 1.95		2.0	5.0	10.2	2.0	12.9		
		2.30 ≤ V_{CC} ≤ 2.70		1.5	4.0	8.0	1.0	9.9		
		3.00 ≤ V_{CC} ≤ 3.60		1.0	3.0	7.2	0.5	8.9		
t_{PHZ},t_{PLZ}	Output Disable Time	0.90	C_L=15pF, R_U=5000Ω R_D=5000Ω		30				ns	Figure 5 Figure 6
		1.10 ≤ V_{CC} ≤ 1.30		5.0	11.0	21.6	4.5	44.9		
		1.40 ≤ V_{CC} ≤ 1.60		3.0	7.0	15.9	2.5	18.8		
		1.65 ≤ V_{CC} ≤ 1.95		2.0	5.0	15.2	2.0	18.2		
		2.30 ≤ V_{CC} ≤ 2.70		1.5	4.0	14.1	1.0	15.4		
		3.00 ≤ V_{CC} ≤ 3.60		1.0	3.0	13.9	0.5	15.1		

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AC Electrical Characteristics (Continued)

Symbol	Parameter	V_{CC}	Conditions	T_A=+25°C			T_A=-40 to +85°C		Units	Figure
				Min.	Typ.	Min.	Typ.	Min.		
t_{PHL}, t_{PLH}	Propagation Delay	0.90	C_L=30pF, R_L=1MΩ		34				ns	Figure 5 Figure 6
		1.10 ≤ V_{CC} ≤ 1.30		5.5	12.0	23.4	5.0	51.1		
		1.40 ≤ V_{CC} ≤ 1.60		4.0	8.0	13.8	3.0	17.7		
		1.65 ≤ V_{CC} ≤ 1.95		2.0	6.0	10.6	2.0	14.0		
		2.30 ≤ V_{CC} ≤ 2.70		1.0	5.0	7.6	1.0	9.9		
		3.00 ≤ V_{CC} ≤ 3.60		0.8	4.0	6.4	0.5	8.9		
t_{PZL},t_{PZH}	Output Enable Time	0.90	C_L=30pF, R_U=5000Ω R_D=5000Ω		37				ns	Figure 5 Figure 6
		1.10 ≤ V_{CC} ≤ 1.30		6.0	13.0	24.4	5.0	51.9		
		1.40 ≤ V_{CC} ≤ 1.60		4.0	8.0	14.5	3.0	17.9		
		1.65 ≤ V_{CC} ≤ 1.95		2.0	6.0	11.7	2.0	14.7		
		2.30 ≤ V_{CC} ≤ 2.70		1.0	5.0	9.1	1.0	11.1		
		3.00 ≤ V_{CC} ≤ 3.60		0.8	4.0	8.1	0.5	10.1		
t_{PHZ},t_{PLZ}	Output Disable Time	0.90	C_L=30pF, R_U=5000Ω R_D=5000Ω		36				ns	Figure 5 Figure 6
		1.10 ≤ V_{CC} ≤ 1.30		6.0	13.0	24.8	5.0	53.5		
		1.40 ≤ V_{CC} ≤ 1.60		4.0	8.0	17.1	3.0	21.1		
		1.65 ≤ V_{CC} ≤ 1.95		2.0	6.0	16.5	2.0	20.5		
		2.30 ≤ V_{CC} ≤ 2.70		1.0	5.0	15.2	1.0	16.7		
		3.00 ≤ V_{CC} ≤ 3.60		0.8	4.0	14.8	0.5	16.3		
C_{IN}	Input Capacitance	0.00			2				pF	
C_{OUT}	Output Capacitance	0.00			4				pF	
C_{PD}	Power Dissipation Capacitance	0.90 to 3.60	V_{IN}=0V or V_{CC}, f=10MHz		8				pF	

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AC Loadings and Waveforms

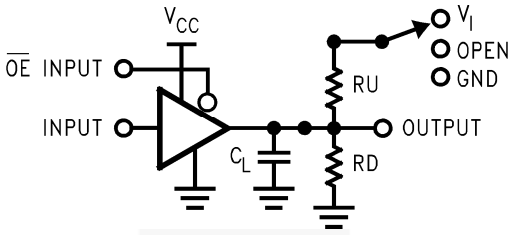

Figure 5. AC Test Circuit

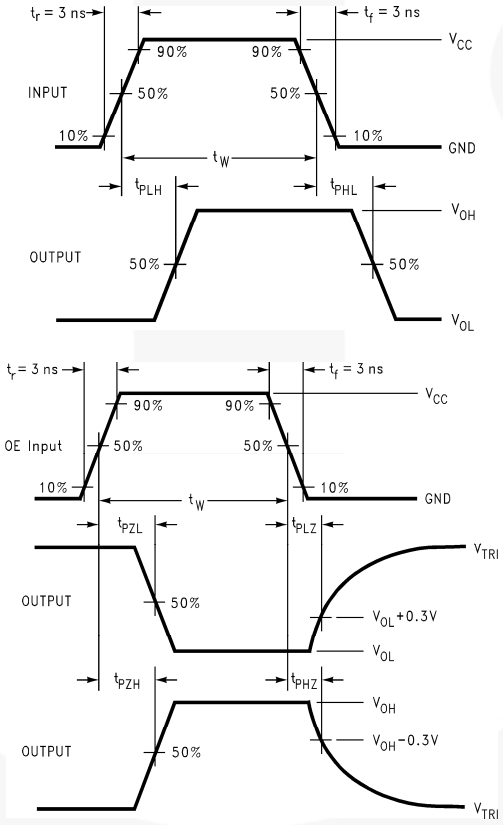

Figure 6. AC Waveforms

Symbol	V_{CC}					
	3.3V ± 0.3V	**2.5V ± 0.2V**	**1.8V ± 0.15V**	**1.5V ± 0.10V**	**1.2V ± 0.10V**	**0.9V**
V_{mi}	1.5V	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_{mo}	0.3V	0.15V	0.15V	0.10V	0.10V	0.10V

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Physical Dimensions

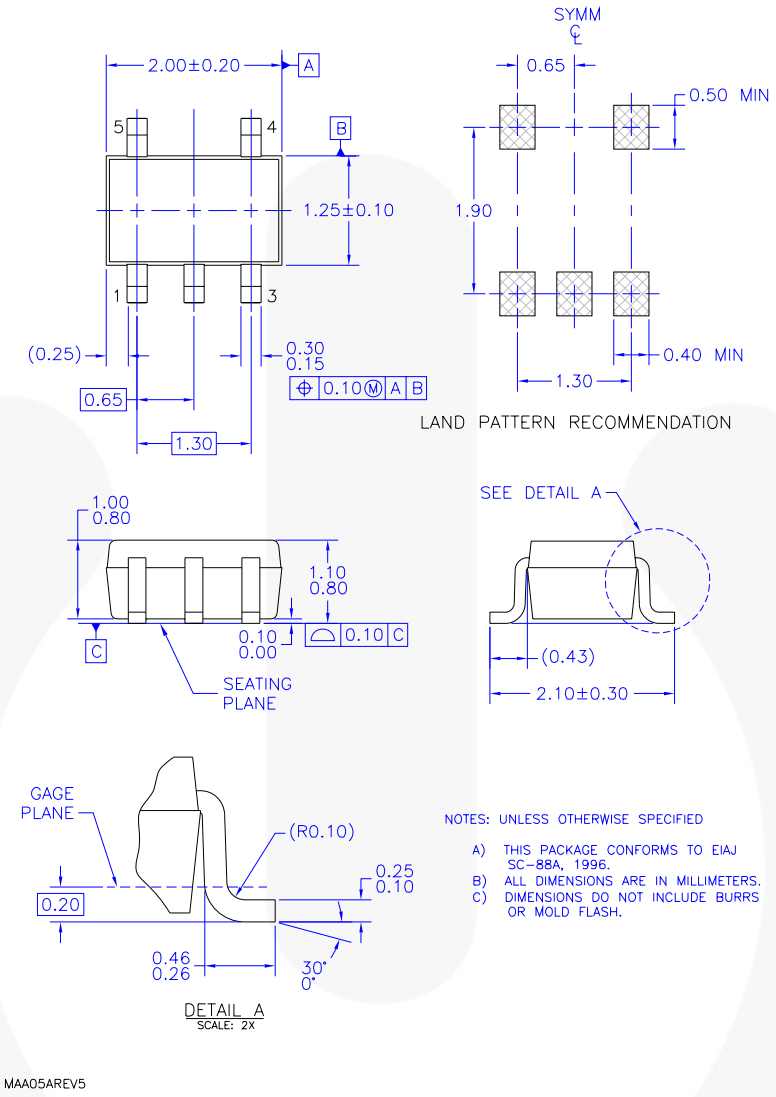

Figure 7. 5-Lead, SC70, EIAJ SC-88a, 1.25mm Wide

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http://www.fairchildsemi.com/packaging/.

Tape and Reel Specification

Please visit Fairchild Semiconductor's online packaging area for the most recent tape and reel specifications:
http://www.fairchildsemi.com/products/analog/pdf/sc70-5_tr.pdf.

Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
P5X	Leader (Start End)	125 (Typical)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed

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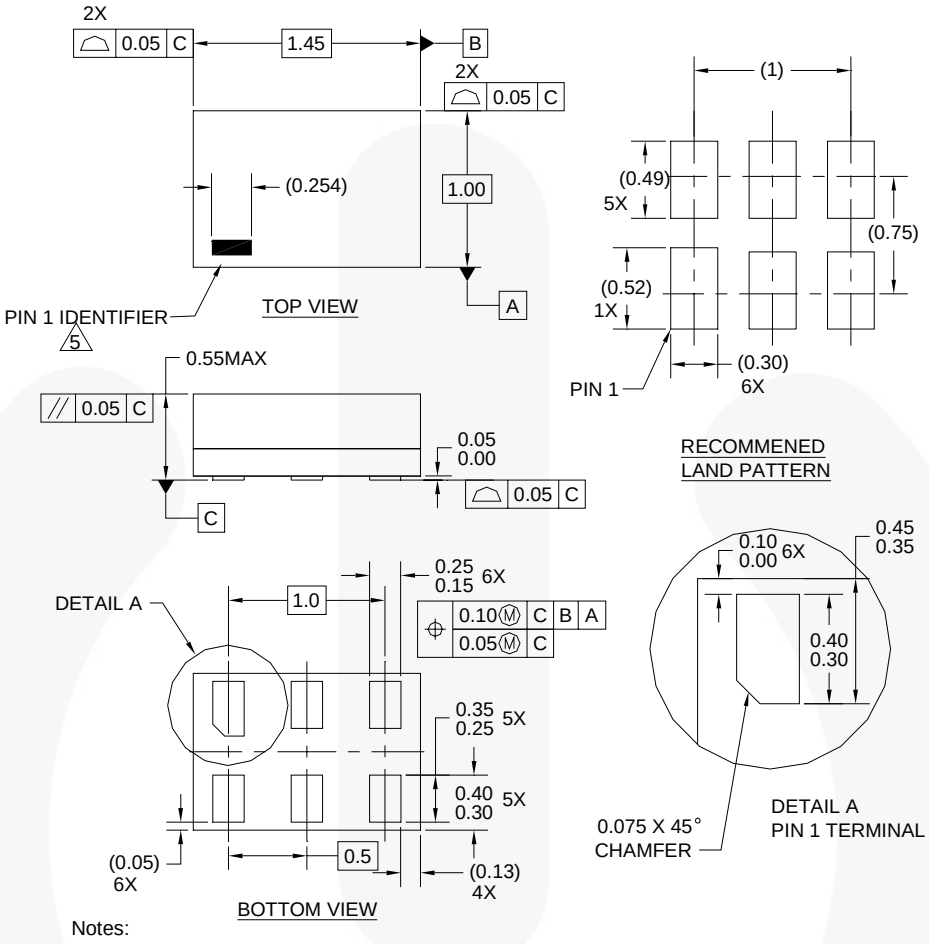
Physical Dimensions



Notes:

1. CONFORMS TO JEDEC STANDARD M0-252 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y14.5M-1994
4. FILENAME AND REVISION: MAC06AREV4
5. PIN ONE IDENTIFIER IS 2X LENGTH OF ANY OTHER LINE IN THE MARK CODE LAYOUT.

Figure 8. 6-Lead, MicroPak™, 1.0mm Wide

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:
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Tape and Reel Specification

Please visit Fairchild Semiconductor's online packaging area for the most recent tape and reel specifications:
http://www.fairchildsemi.com/products/logic/pdf/micropak_tr.pdf.

Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
L6X	Leader (Start End)	125 (Typical)	Empty	Sealed
	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed

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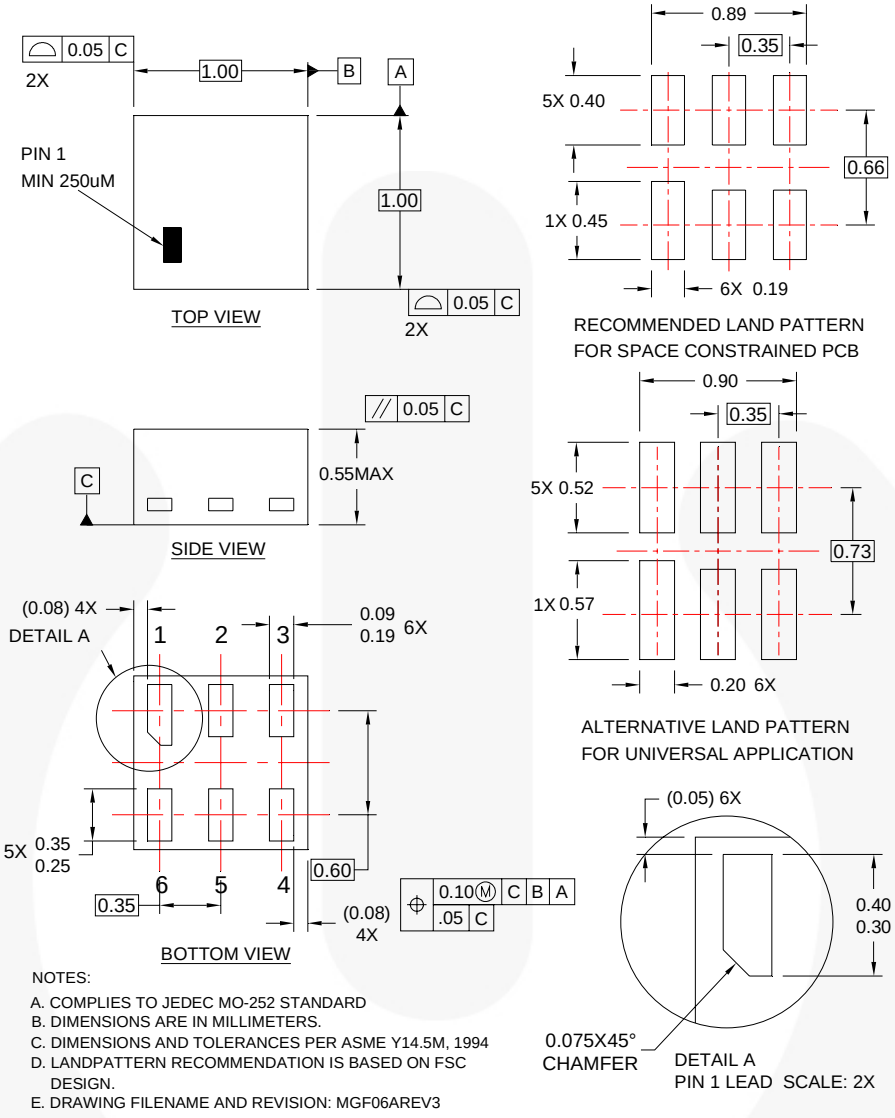
Physical Dimensions



NOTES:

A. COMPLIES TO JEDEC MO-252 STANDARD
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994
D. LANDPATTERN RECOMMENDATION IS BASED ON FSC DESIGN.
E. DRAWING FILENAME AND REVISION: MGF06AREV3

Figure 9. 6-Lead, MicroPak2™, 1x1mm Body, .35mm Pitch

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Tape and Reel Specifications

Please visit Fairchild Semiconductor's online packaging area for the most recent tape and reel specifications:
http://www.fairchildsemi.com/packaging/MicroPAK2_6L_tr.pdf.

Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
FHX	Leader (Start End)	125 (Typical)	Empty	Sealed
	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed

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