MP8007

Fully-Integrated 802.3af-Compatible PoE PD Interface with 13W Primary-side Regulated Flyback or Buck Converter

The Future of Analog IC Technology

DESCRIPTION

The MP8007 is an integrated IEEE 802.3af compatible PoE Powered Device with PD interface and power converter. It is targeted for isolated or non-isolated 13W PoE application.

The PD interface has all the functions of IEEE 802.3af, including detection, classification, 120mA inrush current, 840mA operation current limit as well as 100V Hot-swap MOSFET.

The DCDC converter uses fixed peak current and variable frequency discontinuous conduction mode (DCM) to regulate constant output voltage. The primary-side regulation without opto-coupler feedback in flyback mode simplifies the design while buck mode continues minimizes the solution size for non-isolated applications. A 180V integrated power MOSFET optimizes the device for various wide voltage applications.

The MP8007 features protection including over current protection, over voltage protection, open circuit protection and thermal shutdown.

The MP8007 can support a front-end solution for PoE-PD application with minimum external component, it is available in QFN-28 (4mmX5mm) package.

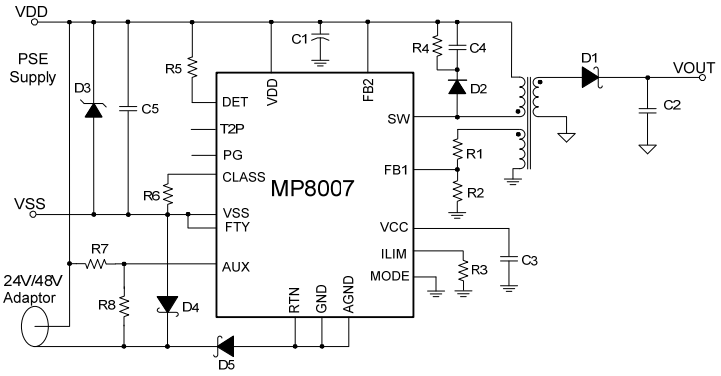
FEATURES

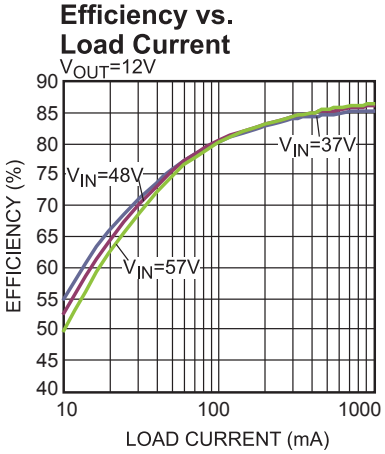
- Compatible with 802.3af Specifications
- Support 13W PoE Power Application
- 100V 0.48Ω PD Integrated Pass Switch
- 120mA PD Inrush Current
- 840mA PD Operation Current Limit
- Auxiliary Adaptor ORing Power Supply
- Integrated 180V Switching Power MOSFET
- Supports Primary-Side Regulated Flyback without Opto-Coupler Feedback
- Supports Low-side Switch Buck Converter
- Up to 3A Programmable Switching Current Limit
- OLP, OVP, Open-Circuit, and Thermal Protection
- Minimal External Components
- Available in QFN-28 (4mmx5mm) Package

APPLICATIONS

- IEEE 802.3af-Compliant Devices
- Security Camera
- VoIP Phones
- WLAN Access Points
- IoT Devices

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking
MP8007GV	QFN-28 (4mm X 5mm)	*See blew*

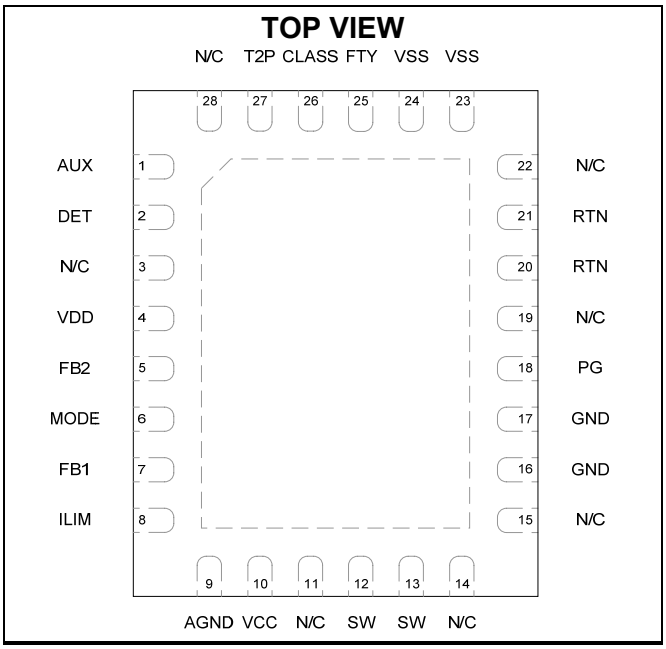
* For Tape & Reel, add suffix –Z (e.g. MP8007GV–Z)

TOP MARKING

MPSYWW
MP8007
LLLLLL

MPS: MPS prefix:
Y: year code;
WW: week code:
MP8007: part number;
LLLLLL: lot number;

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

Pins Voltage Respects to VSS: (2)

VDD, RTN, DET, T2P, AUX, GND, AGND .....-0.3V to +100V

CLASS, FTY .....-0.3V to +6.5V

Pins Voltage Respects to GND(2):

VDD .....-0.3V to +100V

SW .....-0.7V to +180V

FB1 .....-0.7V to +6.5V(3)

VCC(4), MODE, ILIM, PG.....-0.3V to +6.5V

Pins Voltage Respects to VDD:

AUX, FB2 .....-6.5V to +0.3V

Pins Current:

T2P 10mA

VCC Sinking Current..... 1.5 mA(4)

AUX Sinking Current..... -5 mA(5)

FB1 Sinking Current..... ±1 mA(3)

Continuous Power Dissipation (T_A=+25°)(6)

QFN28 4X5……..……3.12W

Junction Temperature .....150°C

Lead Temperature .....260°C

Storage Temperature..... -65°C to +150°C

Recommended Operating Conditions (7)

Supply Voltage V_{DD} .....0V to 57V

Switching Voltage V_{SW} .....-0.5V to +150V

Maximum T2P Current..... 5mA

Maximum VCC Sinking Current..... 1.2mA(4)

Maximum AUX Sinking Current ..... -3 mA(5)

Maximum FB1 Sinking Current..... ±0.5 mA(3)

Maximum Switching Frequency..... 200 kHz

Maximum Switching Current Limit 3A

Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (8)	θ_{JA}	θ_{JC}
QFN-28 (4mmx5mm) ……. ……..	40	9 °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) GND and AGND must be connected to RTN
3) Refer to the “Converter Output Voltage Setting” section.
4) VCC voltage can be pulled higher than this rating, but the external pull-up current should be limited. Refer to “VCC sinking current” rating and “VCC Power Supply Setting” section.
5) When VDD to Adapter-ground voltage is high, AUX-VDD voltage may exceed -6.5V if the divider resistor is not appropriate, in this condition VDD will clamp the -6.5V voltage on AUX pin, but the current should be limited by external resistor.
6) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
7) The device is not guaranteed to function outside of its operating conditions.
8) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

VDD, CLASS, DET, T2P and RTN voltages are referred to VSS, and all other pin voltages are referred to GND, GND and RTN are shorted together. VDD – VSS = 48V, VSS = 0V; R_{DET} = 24.9kΩ, R_{CLASS} =41.2Ω. T_J = -40°C to +125°C, typical values are tested at T_J = 25°C, unless otherwise noted.

PD Interface Section

Parameter	Symbol	Condition	Min	Typ	Max	Units
Detection						
Detection on	V_{DET-ON}	V_{DD} Rising		1.9		V
Detection off	$V_{DET-OFF}$	V_{DD} Rising		11		V
DET Leakage Current	V_{DET-LK}	V_{DET}=V_{DD}=57V, Measure I_{DET}		0.1	5	μA
Bias Current		V_{DD}=10.1V, float DET pin, not in Mark event, Measure I_{SUPPLY}			12	μA
Detection Current	I_{DET}	V_{DD}=2.5V, Measure I_{SUPPLY}	96	99	102	μA
		V_{DD}=10.1V, Measure I_{SUPPLY}	395	410	425	μA
Classification						
Classification Stability Time				90		μs
V_{CLASS} Output Voltage	V_{CLASS}	13V<V_{DD}< 21V 1mA<I_{CLASS}< 42mA	1.1	1.16	1.21	V
Classification Current	I_{CLASS}	13≤V_{VDD}≤21V, Guaranteed by V_{CLASS}				
		R_{CLASS}=578Ω, 13V≤V_{DD}≤21V	1.8	2	2.4	mA
		R_{CLASS}=110Ω, 13V≤V_{DD}≤21V	9.9	10.55	11.3	
		R_{CLASS}=62Ω, 13V≤V_{DD}≤21V	17.7	18.7	19.8	
		R_{CLASS}=41.2Ω, 13V≤V_{DD}≤21V	26.6	28.15	29.7	
		R_{CLASS}=28.7Ω, 13V≤V_{DD}≤21V	38.2	40.4	42.6	
Classification Lower Threshold	V_{CL-ON}	Class Regulator Turns on, V_{DD} Rising	11.8	12.5	13	V
Classification Upper Threshold	V_{CL-OFF}	Class Regulator Turns off, V_{DD} Rising	21	22	23	V
Classification Hysteresis	V_{CL-HYS}	Low side Hysteresis		0.8		V
		High side Hysteresis		0.5		
Mark Event Reset Threshold	V_{MARK-L}		4.5	5	5.5	V
Max Mark Event Voltage	V_{MARK-H}		11	11.5	12	V
Mark Event Current	I_{MARK}		0.5	1.5	2	mA
Mark Event Resistance	R_{MARK}	2-point Measure at 7V and 10V			12	kΩ
IC Supply Current during Classification	$I_{IN-CLASS}$	V_{DD} = 17.5V, CLASS Floating		220	300	μA
Class Leakage Current	$I_{LEAKAGE}$	V_{CLASS} = 0 V, V_{DD} = 57V			1	μA
PD UVLO						
VDD Turn on Threshold	$V_{DD-VSS-R}$	V_{DD} Rising	35	37.5	40	V
VDD Turn off Threshold	$V_{DD-VSS-F}$	V_{DD} Falling	29	31	33	V
VDD UVLO Hysteresis	$V_{DD-VSS-HYS}$		4.9			V
IC Supply Current during Operation	I_{IN}			450		μA

ELECTRICAL CHARACTERISTICS *(continued)*

VDD, CLASS, DET, T2P and RTN voltages are referred to VSS, and all other pin voltages are referred to GND, GND and RTN are shorted together. VDD – VSS = 48V, VSS = 0V; R_{DET} = 24.9kΩ, R_{CLASS} =41.2Ω. T_J = -40°C to +125°C, typical values are tested at T_J = 25°C, unless otherwise noted.

PD Interface Section

Parameter	Symbol	Condition	Min	Typ	Max	Units
Pass Device and Current Limit						
On Resistance	R_{ON-RTN}	I_{RTN}=600mA		0.48		Ω
Leakage Current	I_{RTN-LK}	V_{DD}=V_{RTN}=57V		1	15	μA
Current Limit	I_{LIMIT}	V_{RTN}=1V	720	840	920	mA
Inrush Current Limit	I_{INRUSH}	V_{RTN}=2V		120		mA
Inrush Current Termination		V_{RTN} Falling		1.2		V
Inrush to Operation Mode Delay	T_{DELAY}		80	100		ms
Current Fold-back Threshold		V_{RTN} Rising		10		V
Fold-back Deglitch Time		V_{RTN} Rising to Inrush Current Fold-back		1		ms
T2P						
T2P Output Low Voltage		I_{T2P}=2mA, respect to VSS		0.1	0.3	V
T2P Output High Leakage Current		V_{T2P}=48V			1	μA
AUX						
AUX High Threshold Voltage[9]		Respect to VDD			-2.3	V
AUX Low Threshold Voltage[9]		Respect to VDD	-0.6			V
AUX Leakage Current		V_{DD} -V_{AUX}=6V			2	μA
PG						
PG Output High Voltage		PG pin floating		5.5		V
Source Current Capability		PG is logic high, pull down PG pin to 0V		30		μA
PG Pull Down Resistance		PG is logic low, pull up PG pin to 1V		460		kΩ
PG High-Level Voltage to Enable DCDC Converter	$V_{PG-EN-H}$		3.9			V
PG Low-Level Voltage to Disable DCDC Converter	$V_{PG-EN-L}$				1.3	V
PD Thermal Shutdown						
Thermal Shut down Temperature[10]	T_{PD-SD}			150		ºC
Thermal Shut down Hysteresis[10]	T_{PD-HYS}			20		ºC

ELECTRICAL CHARACTERISTICS *(continued)*

VDD, CLASS, DET, T2P and RTN voltages are referred to VSS, and all other pin voltages are referred to GND, GND and RTN are shorted together. VDD – VSS = 48V, VSS = 0V; R_{DET} = 24.9kΩ, R_{CLASS} =41.2Ω. T_J = -40°C to +125°C, typical values are tested at T_J = 25°C, unless otherwise noted.

DCDC Converter Section

Parameter	Symbol	Condition	Min	Typ	Max	Units
Converter Power Supply and UVLO						
Converter VDD UVLO Rising Threshold	$V_{DD-RTN-R}$	PG-RTN=5V, Test VDD-RTN	10.5	11.6	12.8	V
Converter VDD UVLO Falling Threshold	$V_{DD-RTN-F}$	PG-RTN=5V, Test VDD-RTN	7.4	8.2	9	V
VCC Regulation(11)	V_{CC}	Load = 0mA to 10mA	4.8	5.4	5.9	V
VCC UVLO Rising Threshold(11)	V_{CC-R}	VDD is higher than UVLO, VCC rising	4.3	4.7	5.1	V
VCC UVLO Falling Threshold(11)	V_{CC-F}	VDD is higher than UVLO, VCC falling	4	4.5	4.8	V
Quiescent Current	I_Q	V_{FB1} = 2.2 V, V_{FB2} = VDD, Test supply from VDD to VSS		0.87		mA
Voltage Feedback						
FB1 Reference Voltage	V_{REF1}	Respect to GND, T_J = 25°C	1.94	1.99	2.04	V
		Respect to GND, T_J = -40°C to +125°C	1.93	1.99	2.05	V
FB1 Leakage Current	I_{FB1}	Respect to GND, V_{FB1} = 2V		10	50	nA
Flyback Mode DCM Detect Threshold on FB1	V_{DCM1}	Respect to GND	25	50	75	mV
FB1 Open-circuit Threshold	$V_{FB1OPEN}$		-90	-60	-20	mV
FB1 OVP Threshold	V_{FB1OVP}		120%	125%	130%	V_{REF1}
Minimum Diode Conduction Time for FB1 Sample	T_{SAMPLE}		1.4	2.2	3	µs
FB2 Reference Voltage	V_{REF2}	Respect to VDD, T_J = 25°C	-1.955	-1.88	-1.805	V
		Respect to VDD, T_J = -40°C to +125°C	-1.96	-1.88	-1.8	V
FB2 Leakage Current	I_{FB2}	Respect to VDD, V_{FB2} = -2V		10	50	nA
Buck Mode DCM Detect Threshold on SW	V_{DCM2}	Respect to VDD	0		0.14	V
Switching Power Device						
On Resistance	R_{ON-SW}	V_{CC} = 5.4V		0.8		Ω
Current Sense						
Switching Current Limit	I_{LIMIT}	R_{ILIM} = 53.6kΩ, L = 47µH	1.85	2.05	2.25	A
Switching Current Leading-edge Blanking Time	T_{LEB}			450		ns

ELECTRICAL CHARACTERISTICS *(continued)*

VDD, CLASS, DET, T2P and RTN voltages are referred to VSS, and all other pin voltages are referred to GND, GND and RTN are shorted together. VDD – VSS = 48V, VSS = 0V; R_{DET} = 24.9kΩ, R_{CLASS} =41.2Ω. T_J = -40°C to +125°C, typical values are tested at T_J = 25°C, unless otherwise noted.

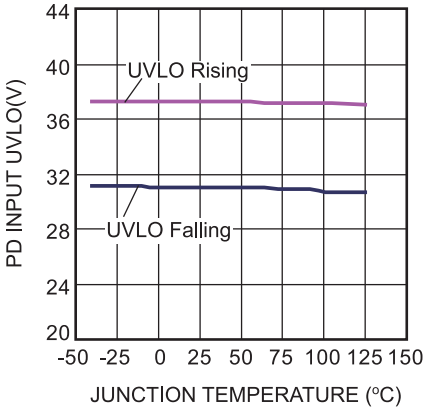
DCDC Converter Thermal Shutdown						
Thermal Shutdown Temperature(10)	T_{SD}			150		ºC
Thermal Shutdown Hysteresis(10)	T_{HYS}			20		ºC

9) If VDD-AUX>2.3V, IC enable adapter input, if VDD-AUX<0.6V, IC enable PSE input. Refer to "Wall adaptor detection and operation" section for AUX setting.
10) Guaranteed by characterization, not tested in production.
11) The maximum VCC UVLO rising threshold is higher than the minimum VCC regulation in the EC table due to production distribution. However, for one unit, VCC regulation is higher than the VCC UVLO rising threshold. The VCC UVLO rising threshold is about 87 percent of the VCC regulation voltage, and the VCC UVLO falling threshold is about 83 percent of the VCC regulation voltage in one unit.

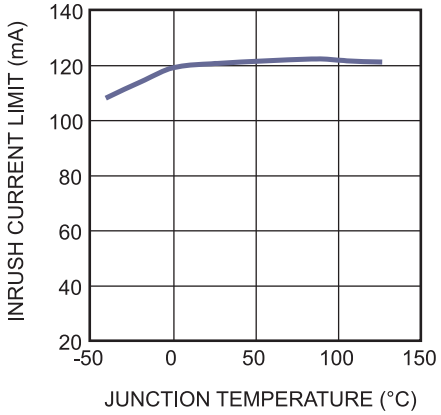
TYPICAL CHARACTERISTICS

V_{IN} = 48V, V_{OUT} = 12V, I_{OUT} = 1A, T_A = 25°C, unless otherwise noted.

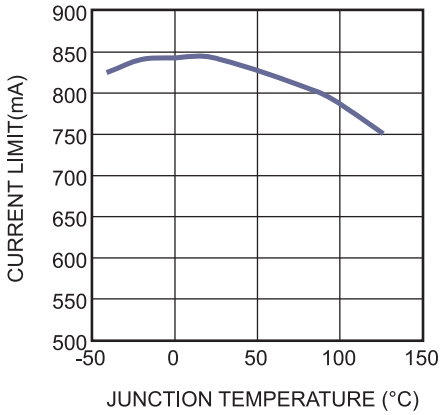
PD Input UVLO vs. Junction Temperature



PD Inrush Current Limit vs. Junction temperature

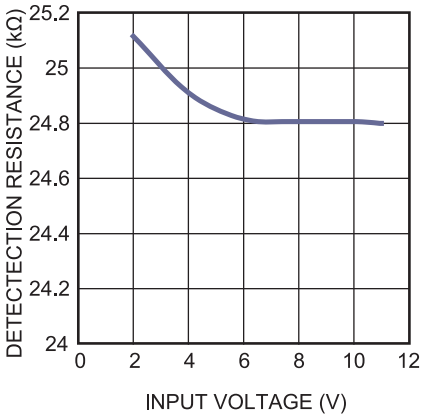


PD Current Limit vs. Junction temperature

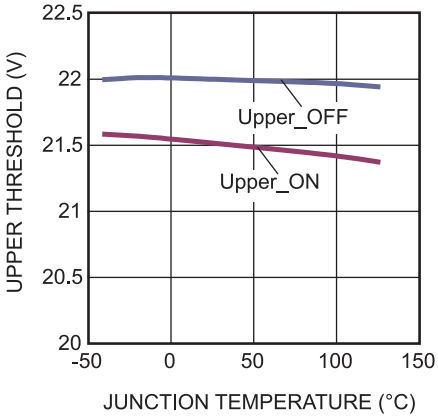


Detection Resistance vs. Input Voltage

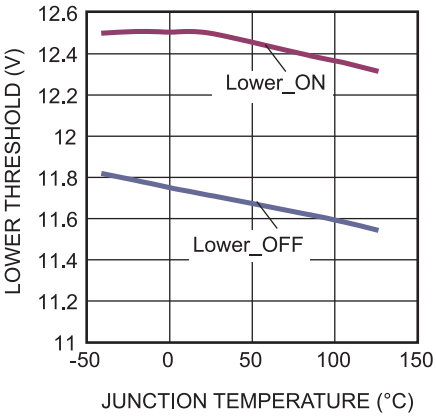
R_{DET}=24.9kΩ



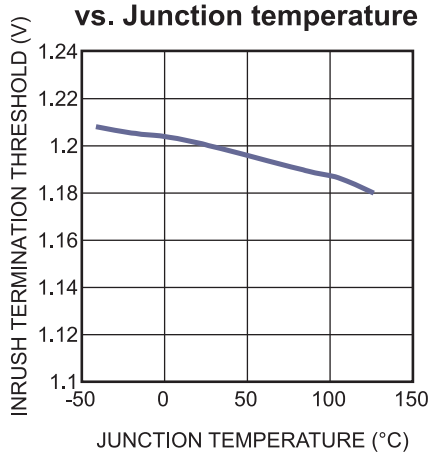
Class Upper Threshold vs. Junction temperature



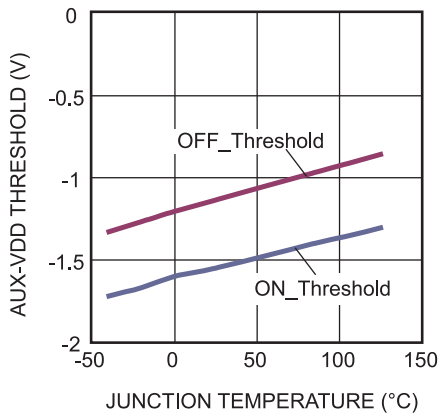
Class Lower Threshold vs. Junction temperature



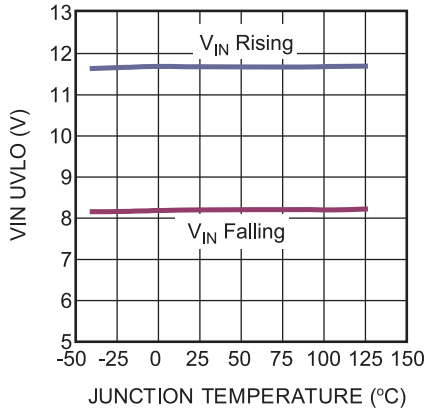
Inrush Current Termination Threshold vs. Junction temperature



Aux-VDD Threshold vs. Junction temperature



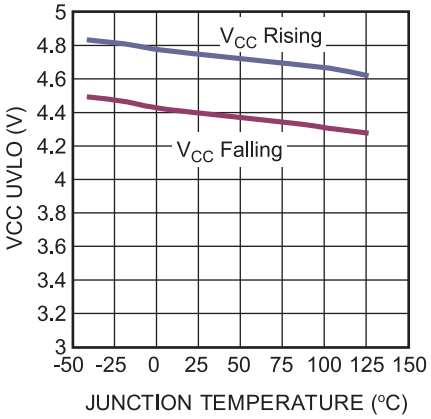
Converter Input UVLO vs. Junction Temperature



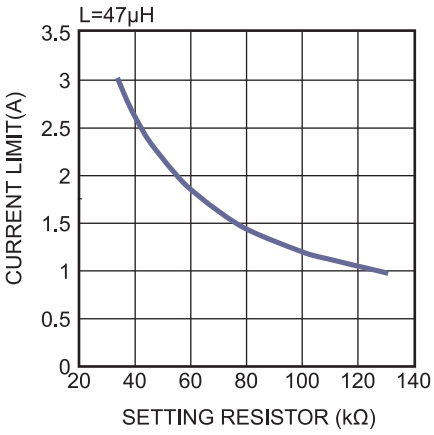
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 48V, V_{OUT} = 12V, I_{OUT} = 1A, T_A = 25°C, unless otherwise noted.

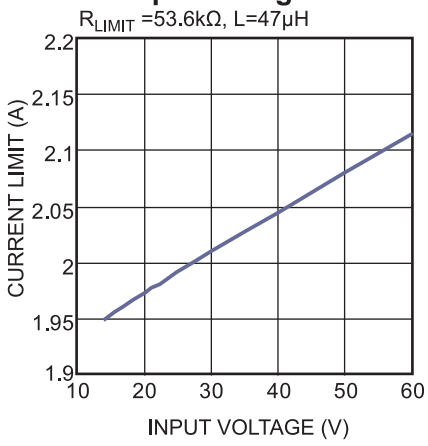
V_{CC} UVLO vs. Junction Temperature



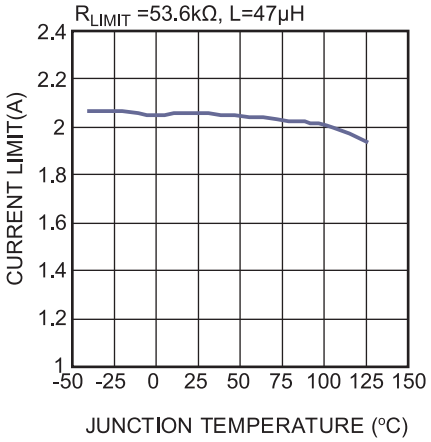
Switching Current Limit vs. Setting Resistor



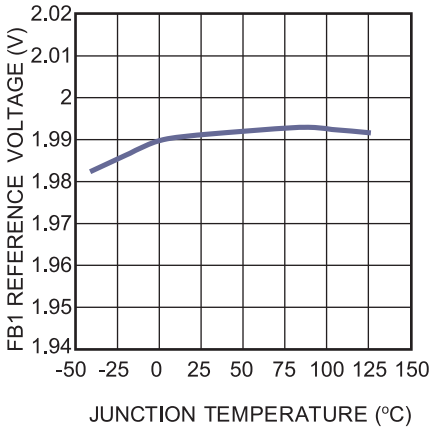
Switching Current Limit vs. Input Voltage



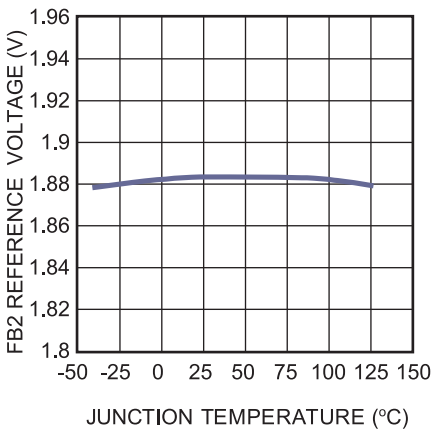
Switching Current Limit vs. Junction Temperature



FB1 Reference Voltage vs. Junction Temperature



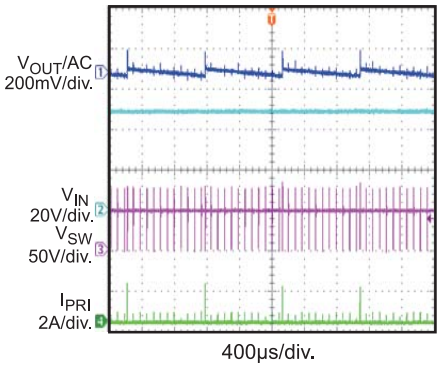
FB2 Reference Voltage vs. Junction Temperature



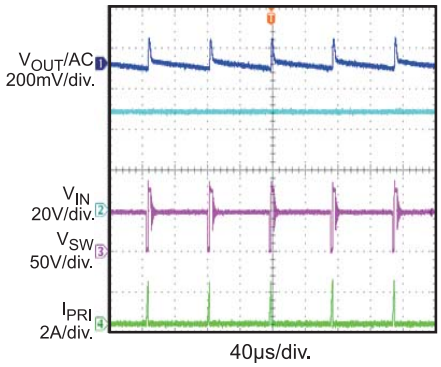
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 48V, V_{OUT} = 12V, I_{OUT} = 1A, T_A = 25°C, unless otherwise noted.

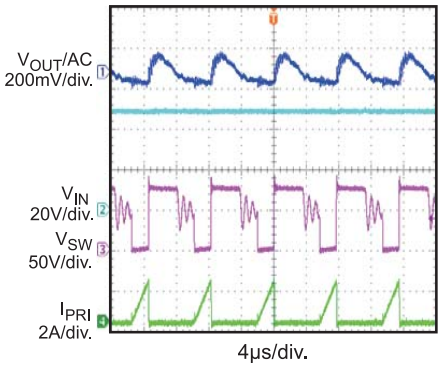
Steady State
I_{OUT} = 10mA



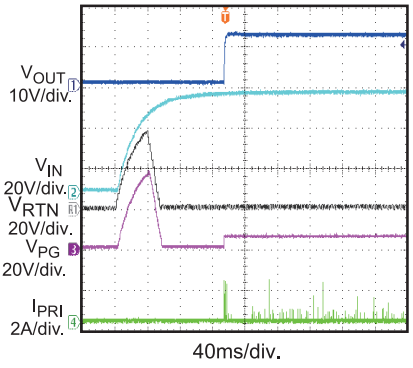
Steady State
I_{OUT} = 100mA



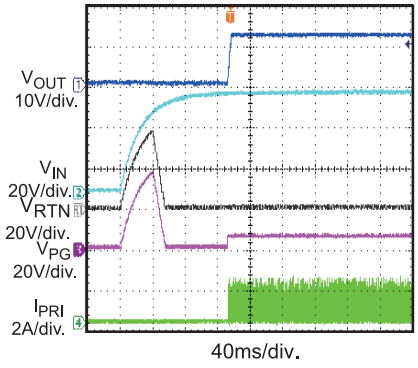
Steady State
I_{OUT} = 1A



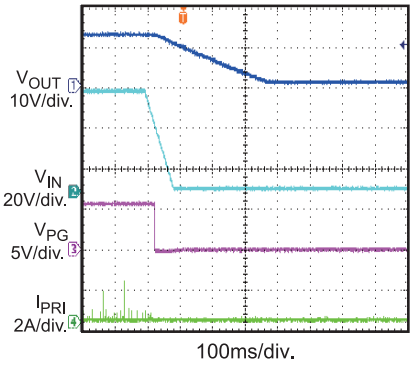
V_{IN} Start-Up
I_{OUT} = 10mA



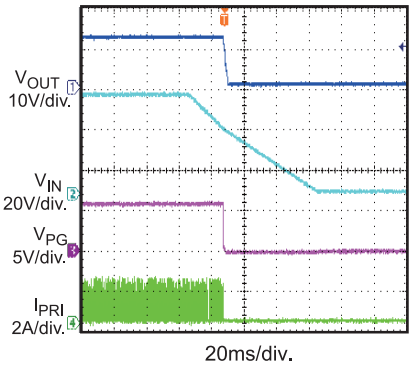
V_{IN} Start-Up
I_{OUT} = 1A



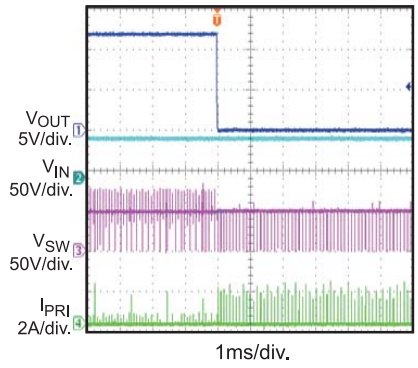
V_{IN} Shutdown
I_{OUT} = 10mA



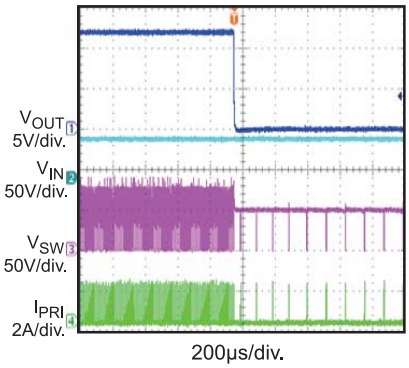
V_{IN} Shutdown
I_{OUT} = 1A



SCP Entry
I_{OUT} = 10mA



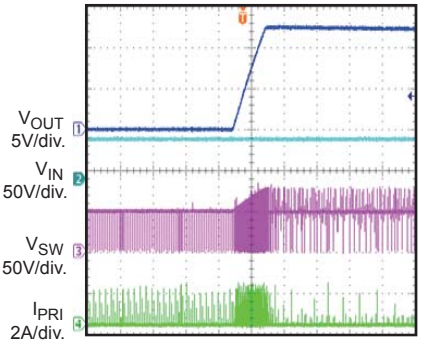
SCP Entry
I_{OUT} = 1A



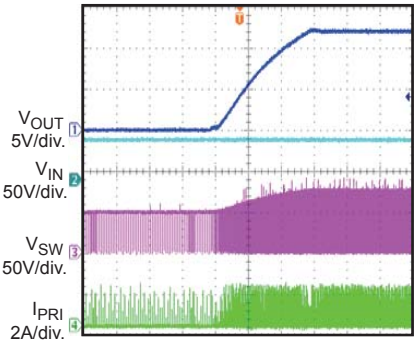
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 48V, V_{OUT} = 12V, I_{OUT} = 1A, T_A = 25°C, unless otherwise noted.

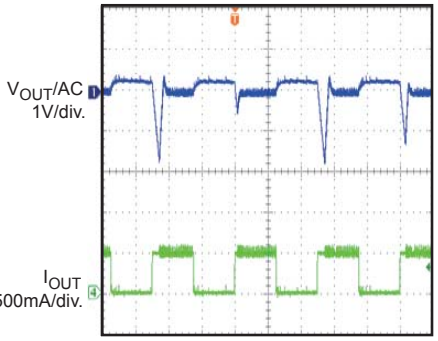
SCP Recovery
I_{OUT} = 10mA



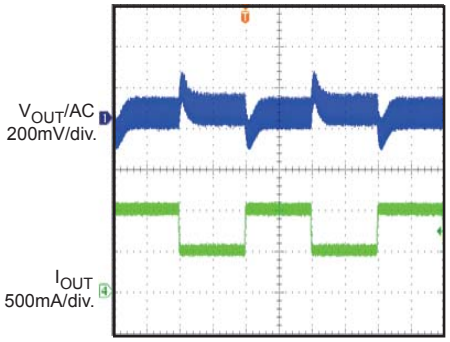
SCP Recovery
I_{OUT} = 1A



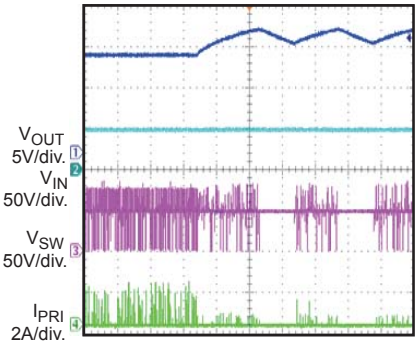
Load Transient
I_{OUT} =10mA to 0.5A,
I_{RAMP}=25mA/µs



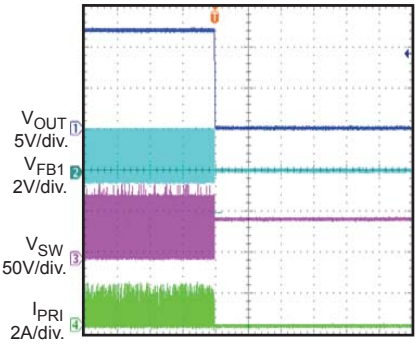
Load Transient
I_{OUT} =0.5A to 1A,
I_{RAMP}=25mA/µs



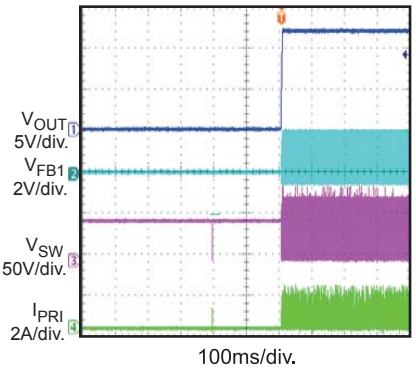
OVP
I_{OUT} = 100mA to 2mA



FB1 Open-Circuit Entry
I_{OUT} = 1A



FB1 Open-Circuit Recovery
I_{OUT} = 1A



PIN FUNCTIONS

PIN#	Name	Description
1	AUX	Auxiliary power input detector. Use this pin for adaptor power supply application. Drive VDD-AUX higher than 2.3V to disable hot-swap MOSFET and CLASS pin function, and force T2P and PG active.
2	DET	Connect 24.9kΩ resistor between VDD and DET for PoE detection.
3, 11, 14, 15, 19, 22, 28	N/C	Not connected internally, can be connected to GND pin and exposed thermal pad in layout.
4	VDD	Positive power supply terminal from PoE input power rail.
5	FB2	Feedback pin for non-isolated buck solution. Connect FB2 to VDD in flyback application
6	MODE	Buck mode or flyback mode select pin. MODE is pulled up internally to VCC through a 1.5μA current source. Float MODE for buck application mode; connect MODE to GND for flyback application mode.
7	FB1	Feedback for fly-back solution. Connect FB1 to GND in buck application
8	ILIM	DCDC converter switching current limit program pin. Connect ILIM to GND through a resistor to program the peak current limit.
9	AGND	Analog power return for DCDC converter control circuit. Connect to GND through single point.
10	VCC	Supply bias voltage pin, powered through internal LDO from VIN. It is recommended to connect a capacitor (no less than 1μF) between VCC and GND.
12,13	SW	Drain of converter switching MOSFET.
16,17	GND	Switching converter power return. Connect to RTN for PoE power supply. Exposed thermal pad can be connected to GND plane for heat sink.
18	PG	PD supply power good indicator. This signal will enable the DCDC converter internally. It is pulled up by internal current source in output high condition, suggest float it in application.
20,21	RTN	Drain of PD Hot-swap MOSFET, connect GND and AGND to this pin.
23,24	VSS	Negative power supply terminal from PoE input power rail.
25	FTY	Factory use only, must be connected to VSS in application.
26	CLASS	Connect resistor from CLASS to VSS to program classification current.
27	T2P	Type 2 PSE indicator, open-drain output. Pulled low to VSS indicates the presence of a Type-2 PSE or AUX is enabled.

FUNCTION DIAGRAM

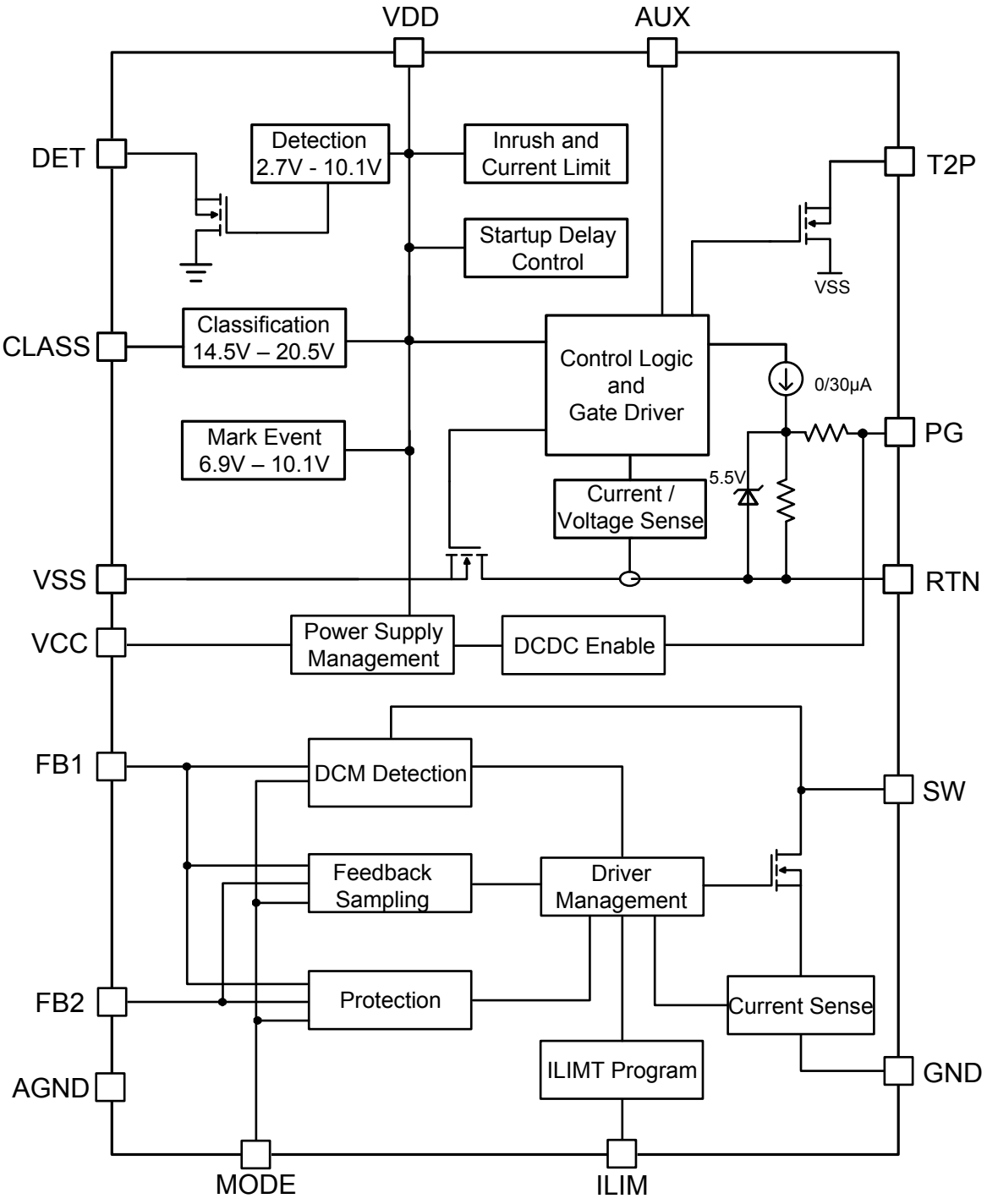


Figure 1: Functional Block Diagram

OPERATION

Compared with IEEE802.3af, the IEE802.3at standard establishes a higher power allocation for Power-over-Ethernet while maintaining backwards compatibility with the existing IEEE802.3af systems. Power Sourcing Equipments (PSE) and Powered Devices (PD) are distinguished as Type-1 complying with the IEEE 802.3af power levels, or Type-2 complying with the IEEE 802.3at power levels. IEEE802.3af/at standard establishes a method of communication between PD and PSE with detection, classification and mark event.

The MP8007 is one integrated PoE solution with IEEE 802.3af PD interface and 13W DCDC converter. The PD interface also has 802.3at function, but DCDC converter only support 13 W output, so MP8007 is only used for 802.3af power design. Along with the PSE it operates as a safety device to supply voltage only when the power sourcing equipment recognizes a unique, tightly specified resistance at the end of an unknown length of Ethernet cable. After powered from PSE, the MP8007 will regulate the output voltage based on application with isolated or non-isolated topology. Figure 1 shows the function diagram of this device, and Figure 2 shows typical PD interface power operation sequence.

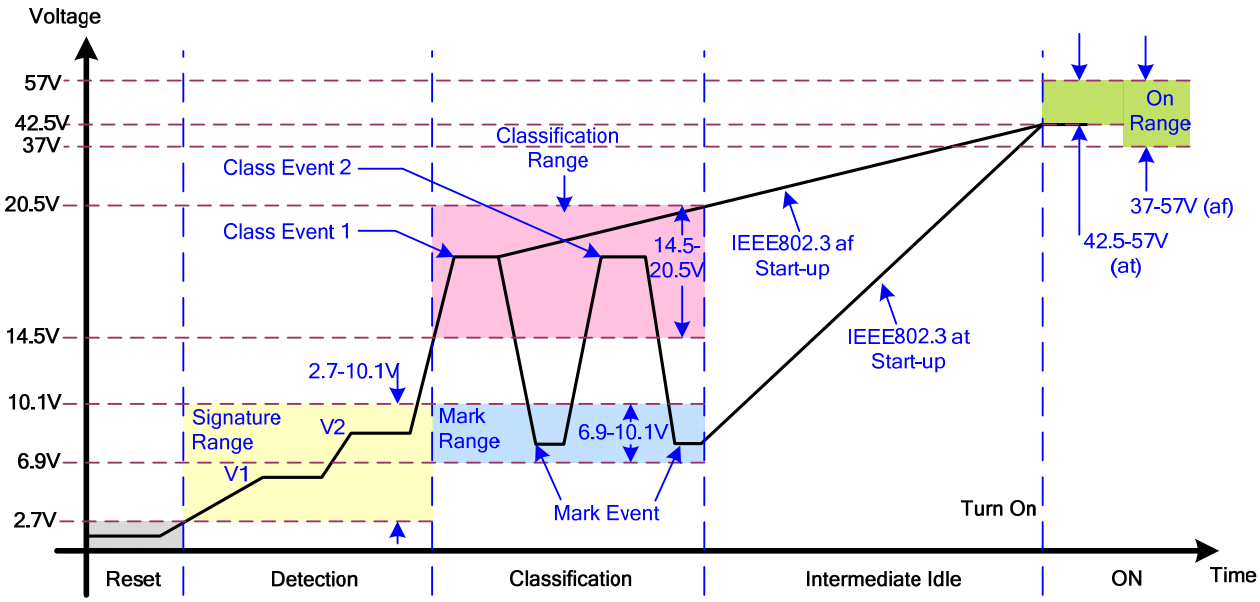


Figure 2: PD Interface Operation Description

Detection

The R_{DET} connected between DET and VDD pin is presented as a load to the PSE in the Detection Mode, when the PSE applies two “safe” voltages between 2.7V to 10.1V while measuring the change in current drawn in order to determine the load resistance. 24.9kΩ(1%) resistor between VDD and DET pins is recommended to present one correct signature, and the valid signature resistance seen from power interface (PI) is between 23.7kΩ and 26.3kΩ.

The detection resistance seen from PI is the result of the input bridge resistance in series with the VDD loading. The input bridge resistance is partially cancelled by MP8007 effective leakage resistance during detection.

Classification

The classification mode can specify to the PSE the expected load range of the device under power, so that the PSE can intelligently distribute power to as many loads as it can within its maximum current capability. The classification mode is active between 14.5V and

20.5V. MP8007 presents a current in classification mode as showing in Table 1.

Table 1– CLASS Resistor Selection

Class	Max. Input Power to PD (W)	Classification Current (mA)	R_{CLASS} (Ω)
0	12.95	2	578
1	3.84	10.55	110
2	6.49	18.7	62
3	12.95	28.15	41.2
4	25.5	40.4	28.7

2-Event Classification

MP8007 can be used as a Type-1 PD as class 0–3 in Table 1, it also distinguishes class 4 with 2-event classification. Generally it is recommended to set MP8007 in class 0-3 because the DCDC converter can only deal with 13W power.

In 2-event classification, the Type-2 PSE reads the power classification twice. Figure 2 presents an example of a 2-event classification. The first classification event occurs when the PSE presents a voltage between 14.5V-to-20.5V to MP8007 and the MP8007 presents a class 4 loads current. The PSE then drops the input voltage into the mark voltage range of 6.9V to 10.1V, signaling the first mark event. MP8007 presents a load current between 0.5mA to 2mA in the mark event voltage range

The PSE repeats this sequence, signaling the second classification and second mark event. The PSE then applies power to MP8007 and MP8007 charges up the DCDC input capacitor C_{BULK} (C1 of schematic on page 1) with a controlled inrush current. When C_{BULK} is fully charged, the T2P pin presents an active low signal with respect to VSS after T_{DELAY}. The T2P output becomes inactive when the MP8007 input voltage VDD falls below UVLO as figure 3 work flow shows. With class 0-3 setting in MP8007, 2-event classification and T2P can be ignored.

PD Interface UVLO and Current Limit

When PD is powered by PSE and VDD is higher than turn on threshold, the Hot-swap switch will start pass a limited current I_{INRUSH} to charge the down stream DC-to-DC converter's input capacitor C_{BULK}. The startup charging current is around 120mA.

If RTN drops to lower than 1.2V, the hot-swap current limit will change to 840mA. After the T_{DELAY} from UVLO starting, MP8007 will assert PG signal and go from the startup mode to the running mode if inrush period elapse, the PG signal can enable down-stream DCDC converter internally.

If V_{DD}-V_{SS} drops below falling UVLO, the Hot-swap MOSFET and DCDC converter both are disabled.

If output current overloads on the internal pass MOSFET, current limit works and V_{RTN}-V_{SS} rises. If V_{RTN} rises above 10V for longer than 1ms, or rises above 20V, the current limit reverts to the inrush value, and PG is pulled down internally to disable DCDC regulator at the same time.

Figure 3 shows the current limit, PG and T2P work logic during startup from PSE power supply.

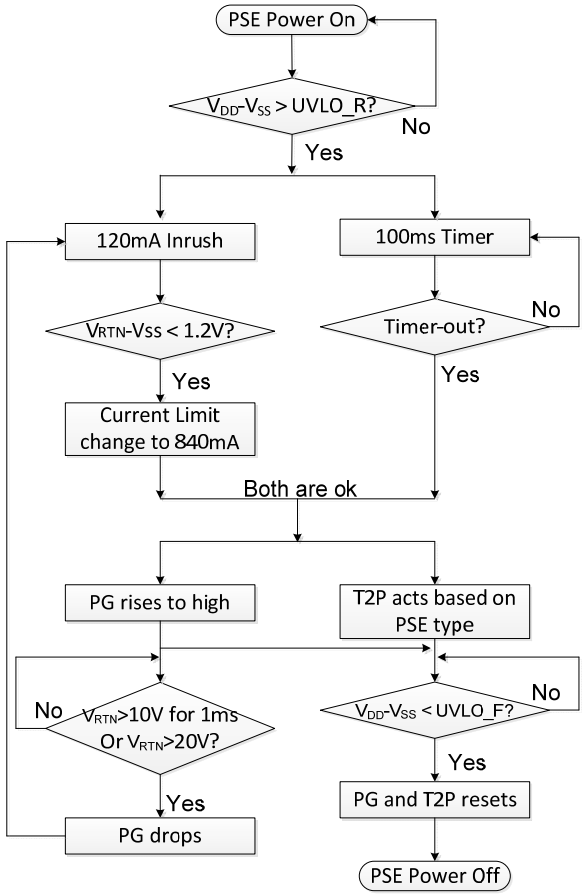


Figure 3: Startup Sequence

Wall Power Adaptor Detection and Operation

For applications where an auxiliary power source such as a wall adapter is used to power the device, the MP8007 features wall power adapter detection as showing in figure 4. Once the input voltage (V_{DD} - V_{SS}) exceeds about 11.5V, the MP8007 enable wall adapter detection. The wall power adapter detection resistor divider is connected from VDD to negative terminal of adaptor, and D_{ADP3} is added for more accurate hysteresis. There is a -2.3V reference voltage from AUX to VDD for adaptor detection. The adaptor is detected when AUX voltage triggers:

$$V_{DD} - V_{AUX} = (V_{ADP} - V_{DADP3}) \times \frac{R_{ADPUP}}{R_{ADPUP} + R_{ADPDOWN}} > 2.3V \quad (1)$$

Where, V_{ADP} is adaptor voltage, V_{DADP3} is the zener voltage, R_{ADPUP} and $R_{ADPDOWN}$ are the AUX divider resistors from adaptor power.

If applied adapter voltage is much higher than the design adapter voltage, VDD-VAUX voltage will be high, if it is higher than 6.5V, the MP8007 inner circuit will clamp the VDD-VAUX voltage at 6.5V, then a current will flow out through the AUX pin, the current should be limited lower than 3mA by external resistor (R_{ADPUP}/$R_{ADPDOWN}$ or R_T resistor from the resistor divider to AUX PIN.)

To make MP8007 work stable with adaptor power, one Schottky diode D_{APD1} (D4 in schematic on page 1) is required between negative terminal of adaptor and VSS. D_{APD2} (D5 in schematic on page 1) is used to block reverse current between adaptor and PSE power source. When a wall adapter is detected, the internal MOSFET between RTN and VSS turns off, classification current is disabled and T2P becomes active. The PG signal is active when adaptor power is detected, so that it can enable the downstream DCDC converter even input hot-swap MOSFET is disabled.

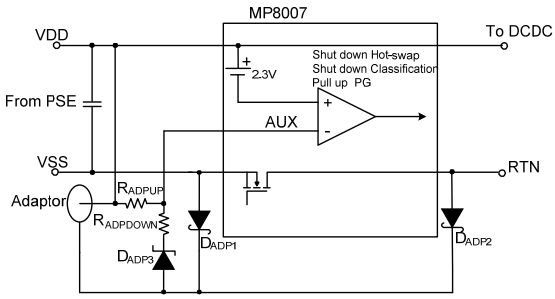


Figure 4: Adaptor Power Detection

Power Good Indicator (PG)

The PG signal is driven by internal current source. After T_{DELAY} from UVLO starting and RTN drops to 1.2V, or a wall power adapter is detected, the PG signal will be pulled high to indicate power condition and enable the downstream DCDC converter. Figure 3 shows the PG logic when powering from PSE, PG will be high if adaptor is detected.

DCDC Converter Startup and Power Supply

Once PD input overrides its UVLO, it will charge DCDC converter's input capacitor (between VDD and RTN) with PD inrush current limit.

DCDC converter has an internal start-up circuit. When voltage between VDD and GND is higher than 4.3 V, the capacitor at VCC is charged through the internal LDO. Normally V_{CC} is regulated at 5.4 V (if VDD is high enough). With the exception of PD interface UVLO, the DCDC converter has an additional V_{IN} UVLO (11.6V) and V_{CC} UVLO (4.7V). When VDD-GND is higher than the 11.6V UVLO, V_{CC} is charged higher than the 4.7V UVLO, and PG pin is pulled high by PD interface, DCDC converter starts switching.

V_{CC} can be powered from the transformer auxiliary winding to save IC power loss. Refer to the "Vcc Power Supply Setting" section for more details.

Flyback and Buck Mode Converter

The DCDC converter supports both flyback and buck topology applications. Connect MODE to GND to set the DCDC converter in flyback mode, and float MODE to set the DCDC converter in buck mode. MODE is pulled up internally to V_{CC} through a 1.5μA current source. Do not connect MODE to VDD externally in

buck mode, and do not place a resistor between MODE and GND in flyback mode.

Converter Switching Work Principle

After startup, DCDC converter works in discontinuous conduction mode (DCM). The second switching cycle will not start until the inductor current drops to 0A. In each cycle, the internal MOSFET is turned on, and the current-sense circuit senses the current $I_{P(t)}$ internally.

Use Equation (2) to calculate the rate at which the current rises linearly in flyback mode:

$$\frac{dI_{p(t)}}{dt} = \frac{V_{IN}}{L_M} \quad (2)$$

When $I_{P(t)}$ rises up to I_{PK}, the internal MOSFET turns off (see Figure 5). The energy stored in the primary-side inductance transfers to the secondary-side through the transformer.

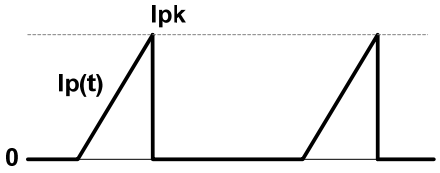


Figure 5—Primary-side current waveform

The primary-side inductance (L_M) stores energy in each cycle as a function of Equation (3):

$$E = \frac{1}{2} L_M I_{PK}^2 \quad (3)$$

Calculate the power transferred from the input to the output with Equation (4):

$$P = \frac{1}{2} L_M I_{PK}^2 F_S \quad (4)$$

Where F_S is the switching frequency. When I_{PK} is constant, the output power depends on F_S and L_M.

Use Equation (5) to calculate the rate at which the current rises linearly in buck mode:

$$\frac{dI_{p(t)}}{dt} = \frac{V_{IN} - V_{OUT}}{L_M} \quad (5)$$

The internal MOSFET turns off when $I_{P(t)}$ rises to I_{PK} (see Figure 6). The output current is calculated with Equation (6):

$$I_{OUT} = \frac{1}{2} D I_{PK} \quad (6)$$

Where, D is the inductor current conducting duty cycle.

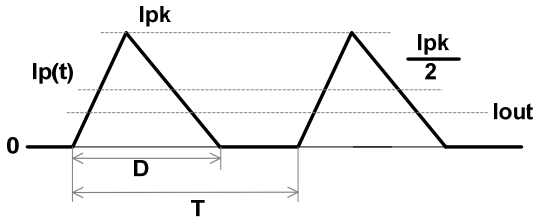


Figure 6—Inductor current waveform

Converter Light-Load Control

In flyback mode (if the load decreases), DCDC converter stretches down the frequency automatically to reduce the power transferring while keeping the same I_{PK} in each cycle. An approximate 10 kHz minimum frequency is applied to detect the output voltage even at a very light load. During this condition, the switching I_{PK} jumps between 20 percent of the normal I_{PK} and 100 percent of the normal I_{PK} to reduce the power transferring. The DCDC converter still transfers some energy to the output even if there is no load on the output due to the 10 kHz minimum frequency. This means that some load is required to keep the output voltage in regulation, or else V_{OUT} will rise and trigger OVP.

In buck mode, the DCDC converter has no minimum frequency limit, so it stretches down to a very low frequency and regulates the output automatically even there is no load on the output.

Frequency Control

By monitoring the auxiliary winding voltage in flyback mode or monitoring the SW voltage in buck mode, the DCDC converter detects and regulates the inductor current in DCM. The frequency is controlled by the peak current, the current ramp slew rate, and the load current. The maximum frequency occurs when the DCDC converter runs in critical conduction mode, providing the maximum load power. The DCDC converter switching frequency should be lower than 200 kHz in the design.

Output Voltage Control

In flyback application, the DCDC converter detects the auxiliary winding voltage from FB1 during the secondary-side diode conduction period.

Assume the secondary winding is the master, and the auxiliary winding is the slave. When the secondary-side diode conducts, the FB1 voltage is calculated with Equation (7):

$$V_{FB1} = \frac{N_A}{N_S} \times (V_{OUT} + V_{D1F}) \times \frac{R_2}{R_1 + R_2} \quad (7)$$

Where:

V_{D1F} is the output diode forward-drop voltage.

V_{OUT} is the output voltage.

N_A and N_S are the turns of the auxiliary winding and the secondary-side winding, respectively.

R1 and R2 are the resistor dividers for sampling.

The output voltage differs from the secondary-winding voltage due to the current-dependant diode forward voltage drop. If the secondary-winding voltage is always detected at a fixed secondary current, the difference between the output voltage and the secondary-winding voltage is a fixed V_{D1F}. DCDC converter starts sampling the auxiliary-winding voltage after the internal power MOSFET turns off for 0.7 μs and finishes the sampling after the secondary-side diode conducts for 3μs. This provides good regulation when the load changes. However, the secondary diode conducting period must be longer than 3μs in each cycle, and the FB1 signal must be smooth in 0.7μs after the switch turns off.

With a buck solution, there is one FB2 pin referred to VDD. It can be used as the reference voltage for the buck application. The output voltage is referred to VDD and does not have the same GND as the input power.

Programming the Switching Current Limit

The switching converter current limit is set by an external resistor (R3 in schematic on page 1) from ILIM to ground. The value of R3 can be estimated with Equation (8):

$$I_{LIM} = \frac{100}{R3} + \frac{V_L \times 0.18}{L} \quad (8)$$

Where I_{LIM} is the current limit in A, V_L is the voltage applied on the inductor when the MOSFET turns on, R3 is the setting resistor in kΩ, and L is the inductor in μH.

The current limit cannot be programmed higher than 3A.

If Input voltage is very low, the inductor current may increase slowly, it will take a long time to meet the setting current limit. MP8007 integrates a ~7us max on time. After the max on time, MOSFET will turn off, even the inductor current doesn`t meet the setting current limit.

Converter Leading-Edge Blanking

Transformer parasitic capacitance induces a current spike on the switching power FET when the power switch turns on. The DCDC converter includes a 450 ns leading-edge blanking period to avoid falsely terminating the switching pulse. During this blanking period, the current sense comparator is disabled, and the gate driver cannot switch off.

DCDC Converter DCM Detection

The DCDC switching regulator operates in discontinuous conduction mode in both flyback and buck modes.

In flyback mode, the DCDC converter detects the falling edge of the FB1 voltage in each cycle. The second cycle switching will not start unless the chip detects a 50 mV falling edge on FB1.

In buck mode, the DCDC converter detects the falling edge of the SW voltage in each cycle. The second cycle switching will not start unless the chip detects 0.14 V falling edge between V_{SW}-V_{DD}.

Over-Voltage & Open-Circuit Protection

In flyback mode, the DCDC converter includes over-voltage protection (OVP) and open-circuit protection. If the voltage at FB1 exceeds 125 percent of V_{REF1}, or FB1's -60 mV falling edge cannot be detected because the feedback resistor is removed, immediately the DCDC converter shuts off the driving signal and enters hiccup mode by re-charging the internal capacitor. The DCDC converter resumes normal operation when the fault is removed.

In buck mode, if the voltage at FB2 is higher than the reference voltage, the DCDC converter stops switching immediately.

Thermal Shutdown

Thermal shutdown is implemented to prevent the chip from thermally running away. MP8007 has separated temperature monitor circuit for PD and switching devices, DC converter thermal protection won't affect PD interface but PD temperature protection will turn off both PD and DC converter. When the temperature is lower than its recovery threshold, thermal shutdown is gone and the chip is enabled.

APPLICATION INFORMATION

Detection Resistor

In the Detection Mode, a resistor connected between DET and VDD pin is needed as a load to the PSE. The resistance is calculated as a ΔV/ΔI, with an acceptable range of 23.7kΩ to 26.3kΩ. Use a typical value of 24.9kΩ as detection resistor.

Classification Resistor

In order to distribute power to as many loads as possible from PSE, a resistor between CLASS and VSS pins is used to classify the PD power level, which draws a fixed current set by classification resistor. The power supplied to PD set by classification resistor is shown in Table 1. Typical voltage on CLASS pin is 1.16V in classification range, and it produces about 33mW power loss on class resistor in Class 3 condition.

Protection TVS

To limit input transient voltage within the absolute maximum rating, a TVS across the rectified voltage (V_{DD}-V_{SS}) must be used. A SMAJ58A, or equivalent, is recommended for general indoor applications. Outdoor transient levels or special applications require additional protection.

PD Input Capacitor

An input bypass capacitor (from VDD to VSS) of 0.05μF to 0.12μF is needed for IEEE 802.3af/at standard specification. Typically a 0.1μF, 100V ceramic capacitor is used.

Wall Power Adaptor Detection Circuit

When an auxiliary power source such as a wall power adapter is used to power the device, the divider resistors R_{ADPUP}, $R_{ADPDOWN}$ and D_{ADP3} must be chosen as shown in figure 7 to satisfy the Equation (1) for correct wall power adaptor detection.

R_{ADPUP} with typical 3kΩ value is suggested to balance the power loss and D_{ADP1}&D_{ADP2} leakage current discharge.

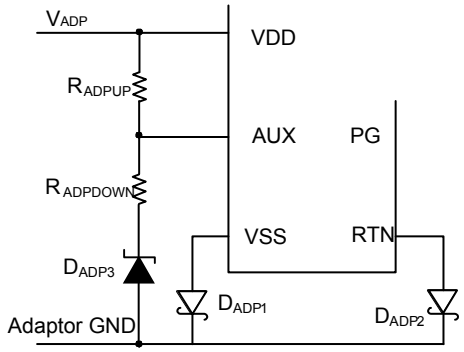


Figure 7: Wall Adaptor Detection Circuit

To prevent the converter from operating at an excessively low adapter voltage, choose a startup voltage, V_{START} approximately 80% of nominal. Assuming that the adapter voltage is 48V, Let R_{ADPUP}=3kΩ, $R_{ADPDOWN}$=8.06kΩ and D_{ADP3}=30V as Equation (1). Re-check the adapter turn-on and turn-off voltage:

$$V_{ADP-ON} = 30 + 2.3 \times \frac{R_{ADPUP} + R_{ADPDOWN}}{R_{ADPUP}} = 38.5V \quad (9)$$

$$V_{ADP-OFF} = 30 + 0.6 \times \frac{R_{ADPUP} + R_{ADPDOWN}}{R_{ADPUP}} = 32.2V \quad (10)$$

The VDD-AUX voltage differential voltage is 4.88V when adapter input is 48V. If much higher adapter voltage is applied and divided voltage on AUX pin is higher than 6.5V, $R_{ADPDOWN}$ and D_{ADP3} must be able to limit the current from AUX to adapter-GND less than 3mA, or else additional resistor from tap of resistor divider to AUX pin is needed to limit the current.

One small package Schottky diode with 100V voltage rating (such as BAT46W) is usually suggested for D_{ADP1}. The voltage rating of D_{ADP2} must also be 100V or higher while current rating must be higher than load current. Low voltage drop Schottky diode (such as SS1H10) is recommended to reduce conduction power-loss.

Power Good (PG) Indicator Signal

MP8007 integrates one PG indicator. PG pin is used to indicate the PD inrush period finishes and enable the DCDC converter internally. The PG pin is an active-high output with internal driven, consequently it can be floated to enable DCDC converter. Pull PG pin low externally can disable the DCDC regulator of MP8007.

In PG high condition, PG pin is pulled up by internal 30μA current source while clamped by one 5.5V zener between PG and RTN. In PG low condition, internal 30μA current source is disabled and PG pin is pulled low by about 460k Ω pull-down resistor between PG and RTN(GND). Generally, float PG for automatic startup after power is connected. PG pin can be pulled low externally but the signal sink current capability must be higher than the internal current source. The zener on PG pin is used to clamp internal 30μA current, do not connect external signal with higher than 5.5V voltage to PG pin.

T2P Indicator Connection

The T2P pin is an active-low, open-drain output which indicates the presence of a Type-2 PSE or AUX is enabled. An opto-coupler is usually used as the interface from the T2P pin to circuitry on output of the converter as figure 8 shown. A high-gain opto-coupler and a high-impedance (for example, CMOS) receiver are recommended.

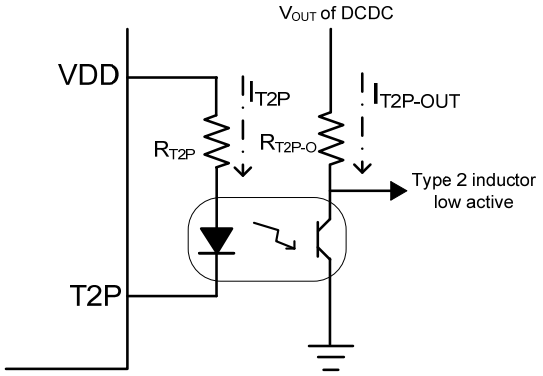


Figure 8: T2P Indicator Circuit

Considering T2P sinking current (2mA typical), T2P output low voltage 0.1V and diode forward voltage drop, choose R_{T2P}=23.7kΩ to match the typical 48V VDD input. Suppose V_{OUT} of DCDC converter is 12V, usually choose R_{T2P-O}=20kΩ based on the CRT even it may vary with temperature, LED bias current and aging.

If lighten a LED from VDD to T2P to indicate the T2P`s activity, the $R_{T2P}$'s resistance can be higher to match the LED`s max current and reduce the power-loss.

V_{CC} Power Supply Setting

The V_{CC} voltage is charged through the internal LDO by VDD. Normally, V_{CC} is regulated at 5.4V, typically. A capacitor no less than 1μF is recommended for decoupling between V_{CC} and GND.

In flyback mode, V_{CC} can be powered from the transformer auxiliary winding to save the high-voltage LDO power loss.

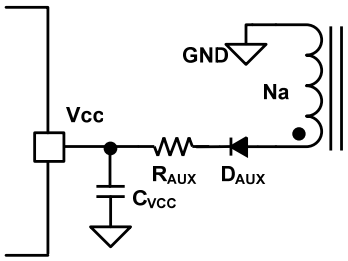


Figure 9: Supply V_{CC} from auxiliary winding

The auxiliary winding supply voltage can be calculated with Equation (11):

$$V_{CC} = \frac{N_A}{N_S} \times (V_{OUT} + V_{D1F}) - V_{DAUXF} \quad (11)$$

Where N_A and N_S are the turns of the auxiliary winding and the output winding, V_{D1F} is the output rectifier diode voltage drop, and V_{DAUXF} is the D_{AUX} voltage drop in Figure 9.

V_{CC} voltage is clamped at about 6.2V by one internal Zener diode. The clamp current capability is about 1.2mA. If the auxiliary winding power voltage is higher than 6.2V (especially in a heavy-load condition), a series resistor (R_{AUX}) is necessary to limit the current to V_{CC}. For simple application, supply the V_{CC} power through the internal LDO directly.

Converter Output Voltage Setting

In DCDC converter, there are two feedback pins for different application modes.

In flyback mode, the converter detects the auxiliary winding voltage from FB1. R1 and R2 are the resistor dividers for the feedback sampling (see Figure 10).

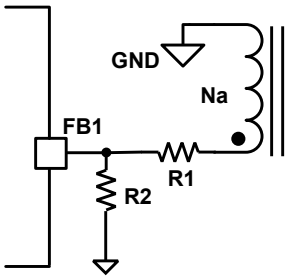


Figure 10: Feedback in isolation application

When the primary-side power MOSFET turns off, the auxiliary-winding voltage is sampled.

The output voltage is estimated:

$$V_{OUT} = \frac{V_{REF1} \times (R_1 + R_2)}{R_2} \times \frac{N_S}{N_A} - V_{D1F} \quad (12)$$

Where,
N_S is the transformer secondary-side winding turns.
N_A is the transformer auxiliary winding turns.
V_{D1F} is the rectifier diode forward drop.
V_{REF1} is the reference voltage of FB1 (1.99V, typically).

When the primary-side power MOSFET turns on, the auxiliary winding forces a negative voltage to FB1. The FB1 voltage is clamped to less than -0.7V internally, but the clamp current should be limited to less than -0.5mA by R1. For example, if the auxiliary winding forces -11V to R1, to make the current flowing from FB1 to R1 lower than -0.5mA, R1 resistance must be higher than 22kΩ (if ignoring R2 current).

Generally, select R2 with a 10kΩ to 50kΩ resistor to limit noise and provide an appropriate R1 for the -0.5mA negative current limit.

In buck application, the feedback pin is FB2. The output voltage can be estimated:

$$V_{OUT} = -\frac{R_1 + R_2}{R_2} \times V_{REF2} \quad (13)$$

Where, V_{REF2} is the reference voltage of FB2 -1.88V, typically.

Maximum Switching Frequency

When DCDC converter works in DCM, the frequency reaches its maximum value during a full-load condition. The maximum frequency is affected by the peak current limit, the inductance, and the input/output voltage. Generally, design the maximum frequency must be lower than 200kHz.

In buck mode, the maximum frequency occurs when the buck runs in critical continuous conduction mode. The frequency can be calculated:

$$F_{SW\_MAX} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{I_{LIM} \times L \times V_{IN}} \quad (14)$$

Where, I_{LIM} is the I_{PK} set by the current limit resistor.

With a lighter load, the frequency is lower than the maximum frequency above.

In flyback mode, design the maximum frequency with the minimum input voltage and the maximum load condition. Calculate the frequency with Equation:

$$F_{SW} \le \frac{1}{T_{ON} + T_{CON} + T_{DELAY}} \quad (15)$$

Where:

T_{ON} is the MOSFET one pulse turn-on time determined with Equation:

$$T_{ON} = \frac{I_{LIM} \times L_M}{V_{IN}} \quad (16)$$

L_M is the transformer primary-winding inductance.

T_{CON} is the rectifier diode current conducting time and can be calculated:

$$T_{CON} = \frac{N_S \times I_{LIM} \times L_M}{N_P \times (V_{OUT} + V_{D1F})} \quad (17)$$

Where, N_S is the transformer secondary-side winding turns. N_P is the transformer primary-side winding turns.

T_{DELAY} is the resonant delay time from the rectifier diode current drop to 0A to the auxiliary-winding voltage drop to 0V. The resonant time can be tested on the board (estimate around 0.5μs).

In flyback mode, the DCDC converter samples the feedback signal within 3μs after the primary-

side MOSFET turns off. The secondary-side diode conduction time in Equation (17) should be higher than 3μs. This time period, combined with the duty cycle, determines the maximum frequency.

Converter Input Capacitor Selection

An input capacitor is required to supply the AC ripple current to the inductor while limiting noise at the input source. A low ESR capacitor is required to keep the noise to the IC at a minimum. Ceramic capacitors are preferred, but tantalum or low ESR electrolytic capacitors will suffice. For ceramic capacitors, the capacitance dominates the impedance at the switching frequency. The ripple will be the worst at light load. The required input capacitance can be estimated:

$$C_1 = \frac{0.5 \times I_{LIM} \times T_{ON}}{V_{INP\_P}} \quad (18)$$

Where C_1 is the DCDC converter input bulk capacitor value, V_{INP-P} is the expected input ripple, and T_{ON} is the MOSFET turn-on time.

In an isolated application, T_{ON} is calculated:

$$T_{ON} = \frac{I_{LIM} \times L_M}{V_{IN}} \quad (19)$$

In a non-isolation application, T_{ON} is calculated:

$$T_{ON} = \frac{I_{LIM} \times L}{V_{IN} - V_{OUT}} \quad (20)$$

Where L is the buck`s inductor value.

Converter Output Capacitor Selection

The output capacitor maintains the DC output voltage. For best results, use ceramic capacitors or low ESR capacitors to minimize the output voltage ripple. For ceramic capacitors, the capacitance dominates the impedance at the switching frequency.

In flyback application, the worst output ripple occurs under a light-load condition; the worst output ripple can be estimated:

$$V_{OUTP\_P} = \frac{0.5 \times N_P \times I_{LIM} \times T_{CON}}{N_S \times C2} \quad (21)$$

Where,

C2 is the output capacitor value.

V_{OUTP-P} is the output ripple.

Normally, a 44μF or higher ceramic capacitor is recommended as the output capacitor. This allows a small Vo ripple and stable operation.

In buck application, the worst Vout ripple can be estimated with Equation (22):

$$V_{OUTP\_P} = \frac{0.5 \times {I_{LIM}}^2 \times L \times (V_{IN} + V_{D1F})}{C2 \times (V_{IN} - V_{OUT}) \times (V_{OUT} + V_{D1F})} \quad (22)$$

Leakage Inductance

The transformer's leakage inductance decreases system efficiency and affects the output current and voltage precision. Optimize the transformer structure to minimize the leakage inductance. Aim for a leakage inductance less than 3 percent of the primary-winding inductance.

RCD Snubber for Flyback

The transformer leakage inductance causes spikes and excessive ringing on the MOSFET drain voltage waveform, affecting the output voltage sampling 0.7μs after the MOSFET turns off. The RCD snubber circuit limits the SW voltage spike (see Figure 11).

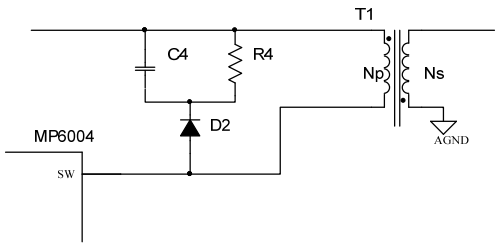


Figure 11: RCD snubber

The power dissipation in the snubber circuit is estimated with Equation (23):

$$P_{SN} = \frac{1}{2} \times L_K \times {I_{LIM}}^2 \times F_S \quad (23)$$

Where, L_K is the leakage inductance.

Since R4 consumes the majority of the power, R4 is estimated with Equation (24):

$$R4 = \frac{{V_{SN}}^2}{P_{SN}} \quad (24)$$

Where, V_{SN} is the expected snubber voltage on C4.

The snubber capacitor C4 can be designed to get appropriate voltage ripple on the snubber using Equation (25):

$$\Delta V_{SN} = \frac{V_{SN}}{R4 \times C4 \times F_S} \quad (25)$$

Generally, a 15 percent ripple is acceptable.

Buck Inductor Selection

The inductor is required to transfer the energy between the input source and the output capacitors. Unlike normal application where inductors determine the inductor ripple, the DCDC converter always works in DCM while V_{IN}, $V_{OUT,}$ and I_{LIM} are constant. The inductor only determines the speed of the current rising and falling, which determines the switching period. The expected maximum frequency can determine the inductor value using Equation (26):

$$L \approx \frac{(V_{IN} - V_{OUT}) \times (V_{OUT} + V_{D1F})}{(V_{IN} + V_{D1F}) \times I_{PEAK}} \times \frac{1}{F_{SW}} \quad (26)$$

F_{SW} is the expected maximum switching frequency, which should be lower than 200kHz in general setting.

Converter Output Diode Selection

The output rectifier diode supplies current to the output capacitor when the internal MOSFET is off. Use a Schottky diode to reduce loss due to the diode forward voltage and recovery time.

In isolation application, the diode should be rated for a reverse voltage greater than Equation (27):

$$V_{D1} = V_{OUT} + \frac{V_{IN} \times N_S}{N_P} + V_{PD1} \quad (27)$$

V_{PD1} can be selected at 40 percent to 100 percent of V_{OUT} + V_{IN} x N_S/N_P. An RC or RCD snubber circuit for the output diode D1 is recommended.

In buck mode, the diode reverse voltage equates to the input voltage. A 20 percent ~ 40 percent margin is recommended.

In both applications, the current rating should be higher than the maximum output current.

Converter Dummy Load

When the system operates without a load in flyback mode, the output voltage rises above the normal operation voltage because of the minimum switching frequency limitation. Use a dummy load for good load regulation. A large dummy load decreases efficiency, so the dummy load is a tradeoff between efficiency and load regulation. For applications using Figure 14, a minimum load of around 10mA is recommended.

PCB Layout Guide

A good layout of the PoE front-end and high-frequency switching power supply is critical. Poor layout may result in reduced performance, excessive EMI, resistive loss, and system instability. For best results, refer to Figure 12 and Figure 13 and follow the guidelines in below:

For PD interface circuit:

1. All components place must follow power flow, from RJ-45, Ethernet transformer, diode bridges, TVS, to 0.1-μF capacitor and DCDC converter input bulk capacitor.
2. Make all leads as short as possible with wide power traces.
3. The spacing between V_{DD} (48V) and V_{SS} must comply with safety standards like IEC60950.
4. Place the PD interface circuit ground planes referenced to VSS, while place the switching converter ground planes referenced to RTN/GND.
5. The exposed PAD must be connected to GND, it can not be connected to VSS.
6. If adaptor power detection is enabled, the AUX divider resistor should be close to AUX pin. And diode D5 (between VSS and RTN) should be placed close to VSS and RTN.

For flyback circuit:

1. Keep the input loop as short as possible between the input capacitor, transformer, SW, and GND plane for minimal noise and ringing.
2. Keep the output loop between the rectifier diode, the output capacitor, and the transformer as short as possible.
3. Keep the clamp loop circuit between D2, C4, and the transformer as small as possible.
4. Place the VCC capacitor close to VCC for the best decoupling. The current setting resistor R3 should be placed as close to ILIM and AGND as possible.

5. Keep the feedback trace far away from noise sources (such as SW). The trace connecting FB1 should be short.
6. Use a single point connection between power GND and signal GND. Vias around GND and the thermal pad are recommended to lower the die temperature.

Refer to Figure 12 for flyback circuit layout, which is referred to schematic on page 1.

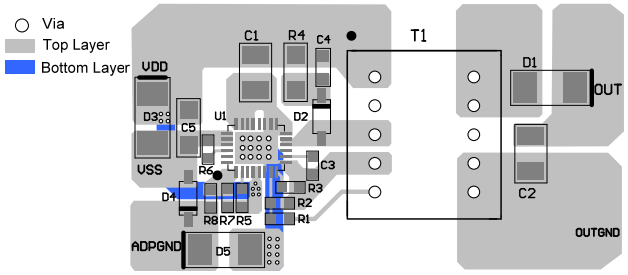


Figure 12: Recommended flyback layout

For buck circuit:

1. Keep the input loop as short as possible between the input capacitor, rectifier diode, SW, and GND plane for minimal noise and ringing.
2. Keep the output loop between the rectifier diode, the output capacitor, and the inductor as short as possible.
3. Place the VCC capacitor close to VCC for the best decoupling. The current setting resistor R3 should be placed as close to ILIM and AGND as possible.
4. Connect the output voltage sense and VDD power supply from the output capacitor with parallel traces. The feedback trace should be far away from noise sources (such as SW). The trace connected to FB2 should be short. The trace for VDD power should be wider.
5. Use a single point connection between power GND and signal GND. Vias around GND and the thermal pad are recommended to lower the die temperature

Refer to Figure 13 for buck circuit layout.

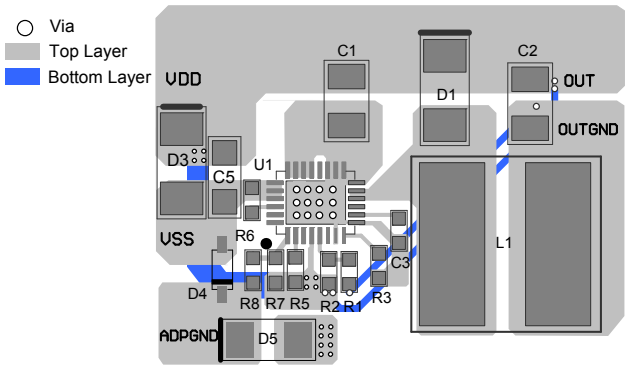


Figure 13: Recommended buck layout

Design Example

Below is a design example following the application guidelines for the following specifications:

Table 2 – Flyback Design Example

V_{DD}-V_{SS}	37V–57V (PoE Supply)
R_{DET}	24.9kΩ
R_{CLASS}	41.2Ω
$V_{ADAPTER}$	48V
V_{OUT}	12V
I_{OUT}	1A

The typical application circuit in Figure 14 shows the detailed application schematic, and is the basis for the typical performance waveforms. Typically, the device is powered by PSE (V_{DD}-V_{SS}=48V). When an adapter voltage above than 38.5V presents, the internal MOSFET between RTN and VSS turns off, instead the device is powered by the adapter whatever the PSE voltage is. For more detailed device applications, please refer to the related Evaluation Board Datasheets.

TYPICAL APPLICATION CIRCUIT

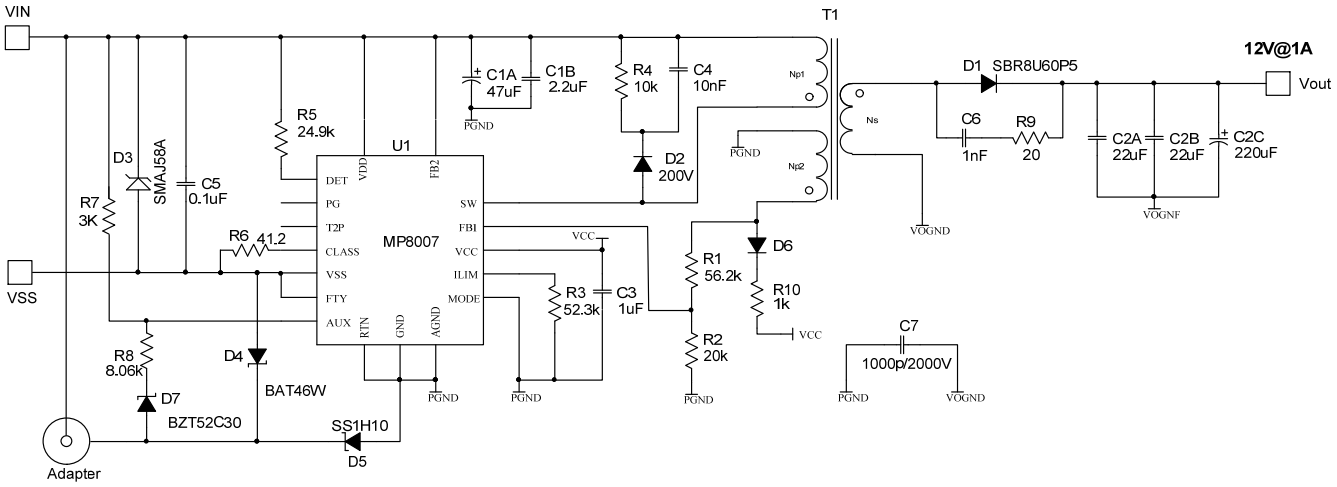


Figure 14: Flyback Application Circuit, VIN=37-57V PoE oring 48V Adaptor Input, VOUT=12V@1A.

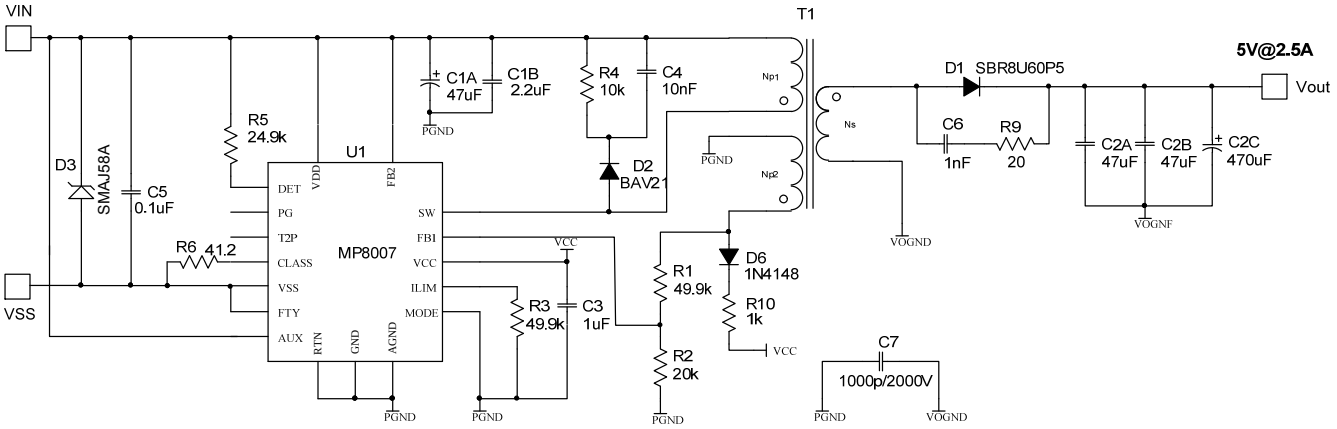


Figure 15: Flyback Application Circuit, VIN=37-57V, No adaptor input, VOUT=5V@2.5A.

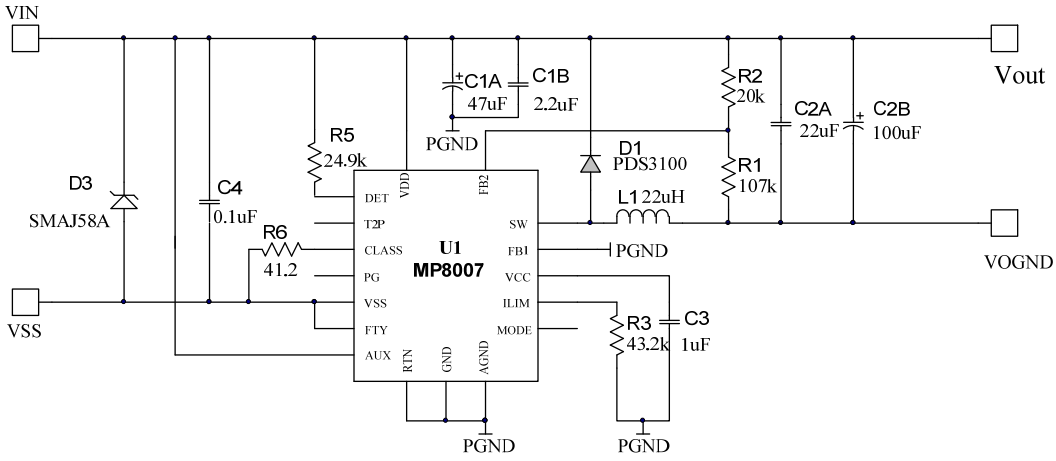
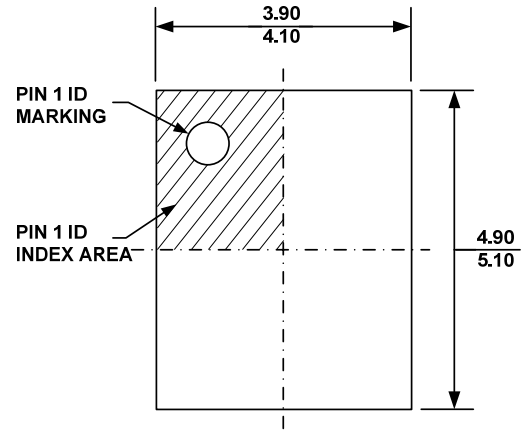


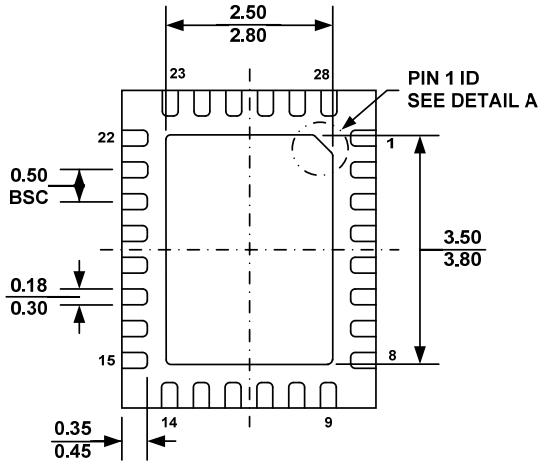
Figure 16: Buck Application Circuit, VIN=37-57V PoE Input, No adapter input, VOUT=12V@1A

PACKAGE INFORMATION

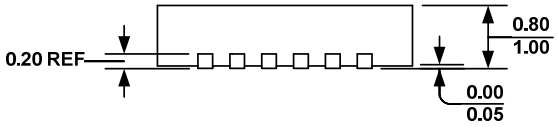
QFN28 (4mmX5mm)



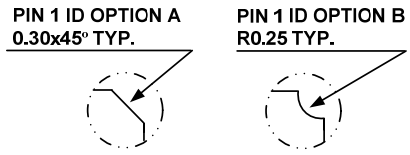
TOP VIEW



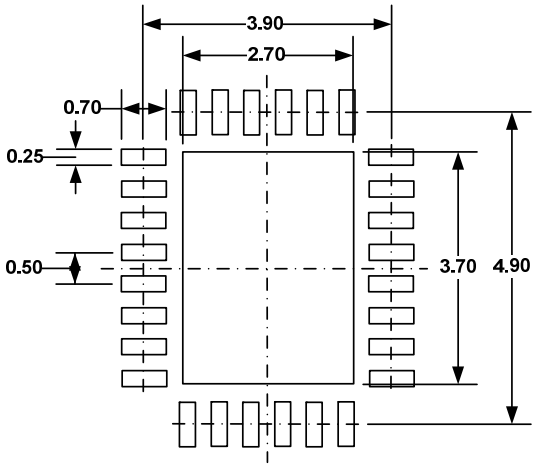
BOTTOM VIEW



SIDE VIEW



DETAIL A



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) DRAWING CONFORMS TO JEDEC MO-220, VARIATION VGHD-3.
5) DRAWING IS NOT TO SCALE.

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