

### **DS28EL22**

## **DeepCover Secure Authenticator with 1-Wire SHA-256 and 2Kb User EEPROM**

#### **General Description**

DeepCover® embedded security solutions cloak sensitive data under multiple layers of advanced physical security to provide the most secure key storage possible. The DeepCover Secure Authenticator (DS28EL22) combines crypto-strong, bidirectional, secure challenge-and-response authentication functionality with an implementation based on the FIPS 180-3-specified Secure Hash Algorithm (SHA-256). A 2Kb user-programmable EEPROM array provides nonvolatile storage of application data and additional protected memory holds a read-protected secret for SHA-256 operations and settings for user memory control. Each device has its own guaranteed unique 64-bit ROM identification number (ROM ID) that is factory programmed into the chip. This unique ROM ID is used as a fundamental input parameter for cryptographic operations and also serves as an electronic serial number within the application. A bidirectional security model enables two-way authentication between a host system and slave-embedded DS28EL22. Slave-to-host authentication is used by a host system to securely validate that an attached or embedded DS28EL22 is authentic. Host-to-slave authentication is used to protect DS28EL22 user memory from being modified by a nonauthentic host. The SHA-256 message authentication code (MAC), which the DS28EL22 generates, is computed from data in the user memory, an onchip secret, a host random challenge, and the 64-bit ROM ID. The DS28EL22 communicates over the single-contact 1-Wire<sup>®</sup> bus at overdrive speed. The communication follows the 1-Wire protocol with the ROM ID acting as node address in the case of a multiple-device 1-Wire network.

### **Applications**

Authentication of Network-Attached Appliances

Printer Cartridge ID/Authentication

Reference Design License Management

System Intellectual Property Protection

Sensor/Accessory Authentication and Calibration

Secure Feature Setting for Configurable Systems

Key Generation and Exchange for Cryptographic Systems

Ordering Information appears at end of data sheet.

#### Features

- Symmetric Key-Based Bidirectional Secure Authentication Model Based on SHA-256
- Dedicated Hardware-Accelerated SHA Engine for Generating SHA-256 MACs
- Strong Authentication with a High Bit Count, User-Programmable Secret, and Input Challenge
- 2048 Bits of User EEPROM Partitioned Into 8 Pages of 256 Bits
- User-Programmable and Irreversible EEPROM Protection Modes Including Authentication, Write and Read Protect, and OTP/EPROM Emulation
- Unique, Factory-Programmed 64-Bit Identification Number
- Single-Contact 1-Wire Interface Communicates with Host at Up to 76.9kbps
- ♦ Operating Range: 1.8V ±5%, -40°C to +85°C
- ♦ Low-Power 5µA (typ) Standby
- ±8kV Human Body Model ESD Protection (typ)
- ♦ 6-Pin TDFN Package

### **Typical Application Circuit**



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For related parts and recommended products to use with this part, refer to: www.maximintegrated.com/DS28EL22.related

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

## **DS28EL22**

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#### **ABSOLUTE MAXIMUM RATINGS**

IO Voltage Range to GND	0.5V to 4.0V
IO Sink Current	20mA
Operating Temperature Range	40°C to +85°C
Junction Temperature	+150°C

Storage Temperature Range	55°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
Soldering Temperature (reflow)	+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### **ELECTRICAL CHARACTERISTICS**

 $(T_A = -40^{\circ}C \text{ to } +85^{\circ}C, \text{ unless otherwise noted.})$  (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	МАХ	UNITS
IO PIN: GENERAL DATA						
1-Wire Pullup Voltage	V <sub>PUP</sub>	(Note 2)	1.71		1.89	V
1-Wire Pullup Resistance	R <sub>PUP</sub>	V <sub>PUP</sub> = 1.8V ± 5% (Note 3)	300		750	Ω
Input Capacitance	C <sub>IO</sub>	(Notes 4, 5)		1500		pF
Input Load Current	١L	IO pin at V <sub>PUP</sub>		5	19.5	μA
High-to-Low Switching Threshold	V <sub>TL</sub>	(Notes 6, 7) 0.65 x V <sub>PUP</sub>		Р	V	
Input Low Voltage	VIL	(Notes 2, 8)			0.3	V
Low-to-High Switching Threshold	V <sub>TH</sub>	(Notes 6, 9)	9) 0.75 x V <sub>PUP</sub>		Р	V
Switching Hysteresis	V <sub>HY</sub>	(Notes 6, 10)		0.3		V
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 4mA (Note 11)			0.4	V
Recovery Time	t <sub>REC</sub>	$R_{PUP} = 750\Omega$ (Notes 2, 12)	5			μs
Time-Slot Duration	t <sub>SLOT</sub>	(Notes 2, 13) 13				μs
IO PIN: 1-Wire RESET, PRESENC	E-DETECT	CYCLE	·			
Reset Low Time	t <sub>RSTL</sub>	(Note 2)	48		80	μs
Reset High Time	t <sub>RSTH</sub>	(Note 14)	48			μs
Presence-Detect Sample Time	t <sub>MSP</sub>	(Notes 2, 15)	8		10	μs
IO PIN: 1-Wire WRITE		·				
Write-Zero Low Time	t <sub>WOL</sub>	(Notes 2, 16)	8		16	μs
Write-One Low Time	t <sub>W1L</sub>	(Notes 2, 16) 1		2	μs	
IO PIN: 1-Wire READ						
Read Low Time	t <sub>RL</sub>	(Notes 2, 17) 1			2 - δ	μs
Read Sample Time	t <sub>MSR</sub>	(Notes 2, 17)	t <sub>RL</sub> + δ		2	μs
EEPROM						
Programming Current	IPROG	V <sub>PUP</sub> = 1.89V (Notes 5, 18)			1	mA
Programming Time for a 32-Bit Segment or Page Protection	tprd	Refer to the full data sheet.				ms
Programming Time for the Secret	t <sub>PRS</sub>				ms	
Write/Erase Cycling Endurance	N <sub>CY</sub>	T <sub>A</sub> = +85°C (Notes 21, 22) 100k			_	
Data Retention	t <sub>DR</sub>	T <sub>A</sub> = +85°C (Notes 23, 24, 25) 10			Years	

### **DS28EL22**

## **DeepCover Secure Authenticator with 1-Wire SHA-256 and 2Kb User EEPROM**

#### **ELECTRICAL CHARACTERISTICS (continued)**

 $(T_A = -40^{\circ}C \text{ to } +85^{\circ}C, \text{ unless otherwise noted.})$  (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	МАХ	UNITS
SHA-256 ENGINE						
Computation Current	ICSHA	Refer to the full data sheet.		mA		
Computation Time	t <sub>CSHA</sub>				ms	
Note 1: Limits are 100% producti	on tested at T	$A_{\rm A}$ = +25°C and/or $T_{\rm A}$ = +85°C. Limits over the	e operatir	a temper	ature ran	and

relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed. **Note 2:** System requirement.

Note 3: Maximum allowable pullup resistance is a function of the number of 1-Wire devices in the system and 1-Wire recovery times. The specified value here applies to systems with only one device and with the minimum 1-Wire recovery times.

**Note 4:** Typical value represents the internal parasite capacitance when V<sub>PUP</sub> is first applied. Once the parasite capacitance is charged, it does not affect normal communication.

Note 5: Guaranteed by design and/or characterization only; not production tested.

**Note 6:** V<sub>TL</sub>, V<sub>TH</sub>, and V<sub>HY</sub> are a function of the internal supply voltage, which is a function of V<sub>PUP</sub>, R<sub>PUP</sub>, 1-Wire timing, and capacitive loading on IO. Lower V<sub>PUP</sub>, higher R<sub>PUP</sub>, shorter t<sub>REC</sub>, and heavier capacitive loading all lead to lower values of V<sub>TL</sub>, V<sub>TH</sub>, and V<sub>HY</sub>.

- **Note 7:** Voltage below which, during a falling edge on IO, a logic-zero is detected.
- Note 8: The voltage on IO must be less than or equal to VILMAX at all times when the master is driving IO to a logic-zero level.
- Note 9: Voltage above which, during a rising edge on IO, a logic-one is detected.

Note 10: After V<sub>TH</sub> is crossed during a rising edge on IO, the voltage on IO must drop by at least V<sub>HY</sub> to be detected as logic-zero.

Note 11: The I-V characteristic is linear for voltages less than 1V.

- Note 12: Applies to a single device attached to a 1-Wire line.
- Note 13: Defines maximum possible bit rate. Equal to  $1/(t_{WOLMIN} + t_{RECMIN})$ .

Note 14: An additional reset or communication sequence cannot begin until the reset high time has expired.

- **Note 15:** Interval after t<sub>RSTL</sub> during which a bus master can read a logic 0 on IO if there is a DS28EL22 present. The power-up presence detect pulse could be outside this interval. See the *Typical Operating Characteristics* for details.
- Note 16:  $\epsilon$  in Figure 11 represents the time required for the pullup circuitry to pull the voltage on IO up from V<sub>IL</sub> to V<sub>TH</sub>. The actual maximum duration for the master to pull the line low is t<sub>W1LMAX</sub> + t<sub>F</sub>  $\epsilon$  and t<sub>W0LMAX</sub> + t<sub>F</sub>  $\epsilon$ , respectively.
- Note 17: δ in Figure 11 represents the time required for the pullup circuitry to pull the voltage on IO up from V<sub>IL</sub> to the input-high threshold of the bus master. The actual maximum duration for the master to pull the line low is t<sub>RLMAX</sub> + t<sub>F</sub>.
- Note 18: Current drawn from IO during the EEPROM programming interval or SHA-256 computation. The pullup circuit on IO during the programming and computation interval should be such that the voltage at IO is greater than or equal to V<sub>PUPMIN</sub>. A low-impedence bypass of R<sub>PUP</sub> activated during programming and computation is the recommended way to meet this requirement.

Note 19: Refer to the full data sheet.

#### Note 20: Refer to the full data sheet.

- Note 21: Write-cycle endurance is tested in compliance with JESD47G.
- Note 22: Not 100% production tested; guaranteed by reliability monitor sampling.
- Note 23: Data retention is tested in compliance with JESD47G.
- Note 24: Guaranteed by 100% production test at elevated temperature for a shorter time; equivalence of this production test to the data sheet limit at operating temperature range is established by reliability testing.
- Note 25: EEPROM writes can become nonfunctional after the data retention time is exceeded. Long-term storage at elevated temperatures is not recommended.

# DS28EL22 DeepCover Secure Authenticator with 1-Wire SHA-256 and 2Kb User EEPROM

**ELECTRICAL CHARACTERISTICS (continued)** 

(T<sub>A</sub> = -40°C to +85°C, unless otherwise noted.) (Note 1)

Note 26: Refer to the full data sheet.

### **Typical Operating Characteristics**

 $(V_{PUP} = 1.71V, V_{IL} = 0.3V, unless otherwise noted.)$ 



#### TOP VIEW DS28EL22 6 N.C. N.C. 1 28L22 ymrrF 5 N.C. 10 2 4 N.C. GND 3 EP TDFN (3mm × 3mm)

### **Pin Description**

PIN	NAME	FUNCTION
1, 4, 5, 6	N.C.	Not Connected
2	IO	1-Wire Bus Interface. Open-drain signal that requires an external pullup resistor.
3	GND	Ground Reference
_	EP	Exposed Pad. Solder evenly to the board's ground plane for proper operation. Refer to Application Note 3273: <i>Exposed Pads: A Brief Introduction</i> for additional information.

**Pin Configuration** 

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Note to readers: This document is an abridged version of the full data sheet. Additional device information is available only in the full version of the data sheet. To request the full data sheet, go to <u>www.maximintegrated.com/DS28EL22</u> and click on **Request Full Data Sheet**.

#### **Ordering Information**

PART	TEMP RANGE	PIN-PACKAGE
DS28EL22Q+T	-40°C to +85°C	6 TDFN-EP* (2.5k pcs)

+Denotes a lead(Pb)-free/RoHS-compliant package. T = Tape and reel. \*EP = Exposed pad.

### **Package Information**

For the latest package outline information and land patterns (footprints), go to <u>www.maximintegrated.com/packages</u>. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE	PACKAGE	OUTLINE	LAND
TYPE	CODE	NO.	PATTERN NO.
6 TDFN-EP	T633+2	<u>21-0137</u>	<u>90-0058</u>



#### ООО "ЛайфЭлектроникс"

ИНН 7805602321 КПП 780501001 Р/С 40702810122510004610 ФАКБ "АБСОЛЮТ БАНК" (ЗАО) в г.Санкт-Петербурге К/С 3010181090000000703 БИК 044030703

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