

FEATURES

- 50 Mbps to 2.7 Gbps Operation
- Typical Rise/Fall Time 80 ps
- Bias Current Range 2 to 100 mA
- Modulation Current Range 5 to 80 mA
- Monitor Photodiode Current 50 μ A to 1200 μ A
- Closed-Loop Control of Power and Extinction Ratio
- Laser Fail and Laser Degrade Alarms
- Automatic Laser Shutdown, ALS
- Dual MPD Functionality for DWDM
- Optional Clocked Data
- Full Current Parameter Monitoring
- 5 V Operation
- 48-Lead LFCSP Package
- 32-Lead LFCSP Package (Reduced Functionality)

APPLICATIONS

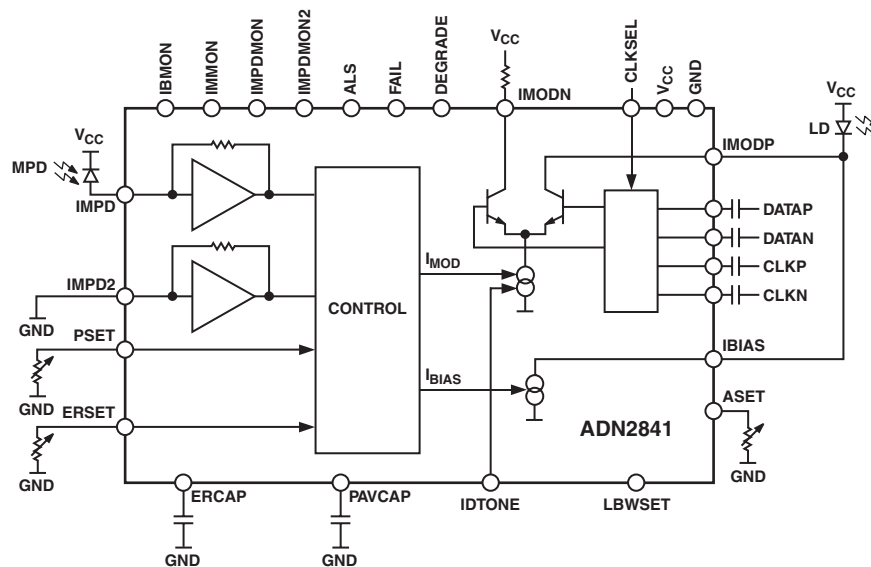
- DWDM Dual MPD Wavelength Fixing
- SONET OC-1/3/12/48
- SDH STM-1/4/16
- Fiber Channel
- Gigabit Ethernet

GENERAL DESCRIPTION

The ADN2841 uses a unique control algorithm to control both average power and extinction ratio of the laser diode (LD) after initial factory set up. External component count and PCB area are low as both power and extinction ratio control are fully integrated. Programmable alarms are provided for laser fail (end of life) and laser degrade (impending fail).

The ADN2841 has circuitry for a second monitor photodiode which enables DWDM wavelength control.

FUNCTIONAL BLOCK DIAGRAM



REV. 0

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ADN2841—SPECIFICATIONS ($V_{CC} = 5\text{ V} \pm 10\%$. All specifications T_{MIN} to T_{MAX} unless otherwise noted¹. Typical values as specified at 25°C.)

| Parameter | Min | Typ | Max | Unit | Conditions/Comments |
|--|------|------|----------------|---------------|---|
| LASER BIAS (BIAS) | | | | | |
| Output Current I_{BIAS} | 2 | | 100 | mA | |
| Compliance Voltage | 1.2 | | V_{CC} | V | |
| I_{BIAS} during ALS | | | 0.1 | mA | |
| ALS Response Time | | 10 | | μs | |
| CCBIAS Compliance Voltage | | 1.2 | | V | |
| MODULATION CURRENT (IMODP, IMODN) | | | | | |
| Output Current I_{MOD} | 5 | | 80 | mA | |
| Compliance Voltage | 1.8 | | V_{CC} | V | |
| I_{MOD} during ALS | | | 0.1 | mA | |
| Rise Time | | 80 | 120 | ps | |
| Fall Time | | 80 | 120 | ps | |
| Jitter | | | 20 | ps p-p | |
| Pulsewidth Distortion | | 18 | | ps | |
| MONITOR PD (MPD, MPD2) | | | | | |
| Current | 50 | | 1200 | μA | Average Current |
| Input Voltage | | | 1.6 | V | |
| POWER SET INPUT (PSET) | | | | | |
| Capacitance | | | 80 | pF | |
| Input Current | 50 | | 1200 | μA | Average Current |
| Voltage | 1.15 | 1.23 | 1.35 | V | |
| EXTINCTION RATIO SET INPUT (ERSET) | | | | | |
| Allowable Resistance Range | 1.2 | | 25 | k Ω | |
| Voltage | 1.15 | 1.23 | 1.35 | V | |
| ALARM SET (ASET) | | | | | |
| Allowable Resistance Range | 1.2 | | 25 | k Ω | |
| Voltage | 1.15 | 1.23 | 1.35 | V | |
| Hysteresis | | 5 | | % | |
| CONTROL LOOP | | | | | |
| Time Constant | | 0.22 | | sec | (LBWSET = GND) |
| | | 2.25 | | sec | (LBWSET = V_{CC}) |
| DATA INPUTS (DATAP, DATAN, CLKP, CLKN) | | | | | |
| AC-Coupled ² | | | | | |
| V p-p (Single-Ended peak-to-peak) | 100 | | 500 | mV | |
| Input Impedance | | 50 | | Ω | |
| t_{SETUP} ³ | 150 | 95 | | ps | |
| t_{HOLD} ³ | 0 | -70 | | ps | |
| LOGIC INPUTS (ALS, LBWSET, CLKSEL) | | | | | |
| V_{IH} | 2.4 | | | V | |
| V_{IL} | | | 0.8 | V | |
| ALARM OUTPUTS (Internal 30 k Ω Pull-up) | | | | | |
| V_{OH} | 2.4 | | | V | |
| V_{OL} | | | 0.8 | V | |
| IDTONE | | | | | |
| Compliance Voltage | | | $V_{CC} - 1.5$ | V | User to Supply Current Sink in the range 50 μA to 4 mA |
| $\left(\frac{I_{OUT}}{I_{IN}}\right)_{RATIO}$ | | 2 | | | |
| f_{IN} ⁴ | 0.01 | | 1 | MHz | |

| Parameter | Min | Typ | Max | Unit | Conditions/Comments |
|---|-----|----------|-----|----------------------|--|
| IBMON, IMMON, IMPDMON, IMPDMON2 IBMON, IMMON Division Ratio IMPDMON, IMPDMON2 IMPDMON to IMPDMON2 Matching Compliance Voltage | | 100 1 | | A/A A/A % V | IMP _D = 1200 μA |
| SUPPLY I _{CC} ⁵ V _{CC} ⁶ | 4.5 | 5.0 | 5.5 | A V | I _{BIAS} = I _{MOD} = 0 |

NOTES

¹Temperature Range: -40°C to +85°C

²When the voltage on DATAP is greater than the voltage on DATAN, the modulation current flows in the IMODP pin.

³Guaranteed by design and characterization. Not production tested.

⁴IDTONE may cause eye distortion.

⁵I_{CC} for power calculation is the typical I_{CC} given.

⁶All V_{CC}s should be shorted together.

Specifications subject to change without notice.

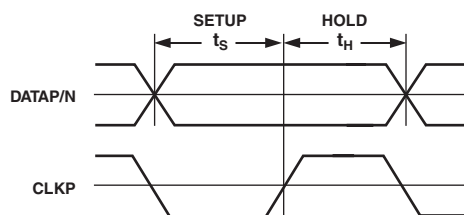


Figure 1. Setup and Hold Time

ABSOLUTE MAXIMUM RATINGS¹

(T_A = 25°C unless otherwise noted.)

V_{CC} to GND 7 V

Operating Temperature Range

Industrial -40°C to +85°C

Storage Temperature Range -65°C to +150°C

Junction Temperature (T_J MAX) 150°C

48-Lead LFCSP Package

Power Dissipation (T_J MAX - T_A)/θ_{JA} mW

θ_{JA} Thermal Impedance² 25°C/W

Lead Temperature (Soldering for 10 sec) 300°C

32-Lead LFCSP Package

Power Dissipation (T_J MAX - T_A)/θ_{JA} mW

θ_{JA} Thermal Impedance² 32°C/W

Lead Temperature (Soldering for 10 sec) 300°C

NOTES

¹Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Transient currents of up to 100 mA will not cause SCR latch-up.

²θ_{JA} is defined when the part is soldered onto a four-layer board.

ORDERING GUIDE

| Model | Temperature Range | Package Description |
|-------------------|-------------------|---------------------|
| ADN2841ACP-32 | -40°C to +85°C | 32-Lead LFCSP |
| ADN2841ACP-48 | -40°C to +85°C | 48-Lead LFCSP |
| ADN2841ACP-32-RL | -40°C to +85°C | 32-Lead LFCSP |
| ADN2841ACP-32-RL7 | -40°C to +85°C | 32-Lead LFCSP |
| ADN2841ACP-48-RL | -40°C to +85°C | 48-Lead LFCSP |

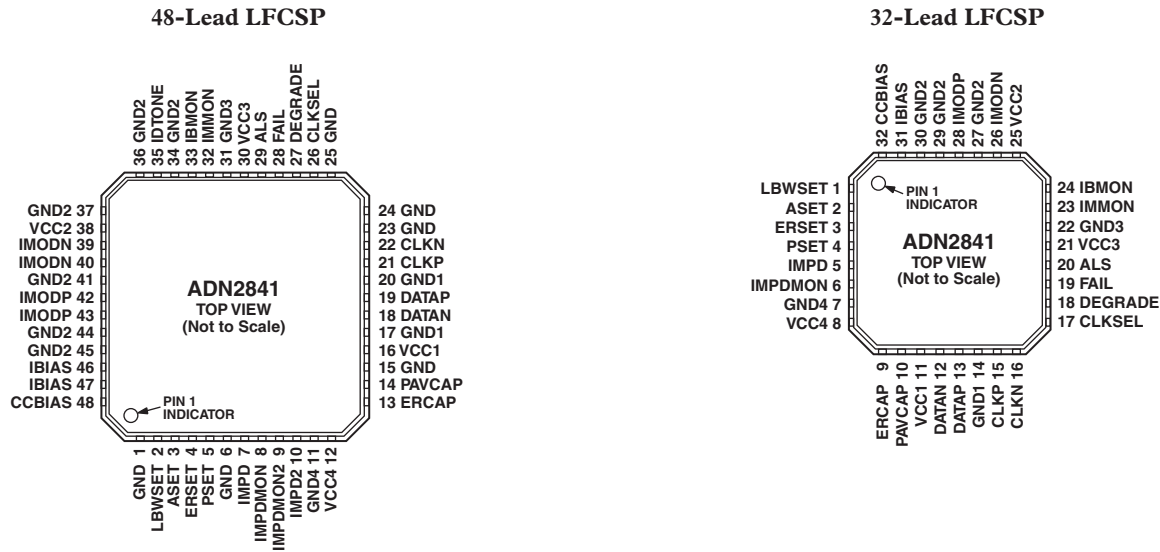
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADN2841 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



ADN2841

PIN CONFIGURATIONS



PIN FUNCTION DESCRIPTIONS

| Pin No. | | Mnemonic | Function |
|---------|---------|----------|--|
| 48-Lead | 32-Lead | | |
| 1 | | GND | Supply Ground |
| 2 | 1 | LBWSET | Select Low Loop Bandwidth (Active = V_{CC}) |
| 3 | 2 | ASET | Alarm Current Threshold Setting Pin |
| 4 | 3 | ERSET | Extinction Ratio Set Pin |
| 5 | 4 | PSET | Average Optical Power Set Pin |
| 6 | | GND | Ground |
| 7 | 5 | IMPD | Monitor Photodiode Input |
| 8 | 6 | IMPDMON | Mirrored Current from Monitor Photodiode |
| 9 | | IMPDMON2 | Mirrored Current from Monitor Photodiode 2 (for use with two MPDs) |
| 10 | | IMPD2 | Monitor Photodiode Input 2- (for use with two MPDs) |
| 11 | 7 | GND4 | Supply Ground |
| 12 | 8 | VCC4 | Supply Voltage |
| 13 | 9 | ERCAP | Extinction Ratio Loop Capacitor |
| 14 | 10 | PAVCAP | Average Power Loop Capacitor |
| 15 | | GND | Ground |
| 16 | 11 | VCC1 | Supply Voltage |
| 17 | | GND1 | Supply Ground |
| 18 | 12 | DATAN | Data, Negative Differential Terminal |
| 19 | 13 | DATAP | Data, Positive Differential Terminal |
| 20 | 14 | GND1 | Supply Ground |
| 21 | 15 | CLKP | Data Clock Positive Differential Terminal, used if $CLKSEL = V_{CC}$ |
| 22 | 16 | CLKN | Data Clock Negative Differential Terminal, used if $CLKSEL = V_{CC}$ |
| 23 | | GND | Ground |
| 24 | | GND | Ground |
| 25 | | GND | Ground |
| 26 | 17 | CLKSEL | Clock Select (Active = V_{CC}), used if data is clocked into chip |
| 27 | 18 | DEGRADE | DEGRADE Alarm Output |
| 28 | 19 | FAIL | FAIL Alarm Output |
| 29 | 20 | ALS | Automatic Laser Shutdown |
| 30 | 21 | VCC3 | Supply Voltage |
| 31 | 22 | GND3 | Supply Ground |
| 32 | 23 | IMMON | Modulation Current Mirror Output |
| 33 | 24 | IBMON | Bias Current Mirror Output |
| 34 | | GND2 | Supply Ground |
| 35 | | IDTONE | IDTONE (Requires external current sink to ground) |
| 36 | | GND2 | Supply Ground |

PIN FUNCTION DESCRIPTIONS (continued)

| Pin No. | | Mnemonic | Function |
|---------|---------|----------|--|
| 48-Lead | 32-Lead | | |
| 37 | | GND2 | Supply Ground |
| 38 | 25 | VCC2 | Supply Voltage |
| 39 | 26 | IMODN | Modulation Current Negative Output, connect to 25 Ω |
| 40 | | IMODN | Modulation Current Negative Output, connect to 25 Ω |
| 41 | 27 | GND2 | Supply Ground |
| 42 | 28 | IMODP | Modulation Current Positive Output, connect to laser diode |
| 43 | | IMODP | Modulation Current Positive Output, connect to laser diode |
| 44 | 29 | GND2 | Supply Ground |
| 45 | 30 | GND2 | Supply Ground |
| 46 | 31 | IBIAS | Laser Diode Bias Current |
| 47 | | IBIAS | Laser Diode Bias Current |
| 48 | 32 | CCBIAS | Extra Laser Diode Bias when AC-Coupled |

ADN2841

GENERAL

Laser diodes have current-in to light-out transfer functions as shown in Figure 2. Two key characteristics of this transfer function are the threshold current, I_{TH} , and slope in the linear region beyond the threshold current, referred to as slope efficiency, LI.

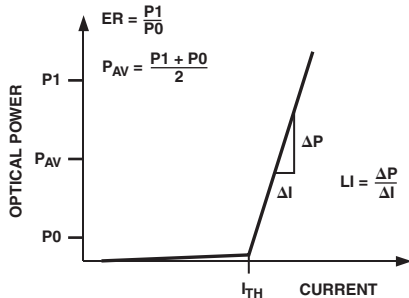


Figure 2. Laser Transfer Function

CONTROL

A monitor photodiode (MPD) is required to control the LD. The MPD current is fed into the ADN2841 to control the optical power and extinction ratio, continuously adjusting the bias current and modulation current in response to the laser's changing threshold current and light-to-current (LI) slope (slope efficiency).

The ADN2841 uses automatic power control (APC) to maintain a constant power over time and temperature.

The ADN2841 uses closed-loop extinction ratio control to allow optimum setting of extinction ratio for every device. Hence SONET/SDH interface standards can be met over device variation, temperature, and time. Closed-loop modulation control eliminates the need to either overmodulate the LD or include external components for temperature compensation. This reduces research and development time and second-sourcing issues caused by characterizing LDs.

Average Power and Extinction Ratio are set using the PSET and ERSET pins, respectively. Potentiometers are connected between these pins and ground. The potentiometer, R_{PSET} , is used to change the average power. The potentiometer, R_{ERSET} , is used to adjust the extinction ratio. Both PSET and ERSET are kept 1.23 V above GND.

R_{PSET} and R_{ERSET} can be calculated using the following formulas:

$$R_{PSET} = \frac{1.23 V}{I_{AV}}$$

where I_{AV} is average MPD current.

$$R_{ERSET} = \frac{1.23 V}{\frac{I_{MPD_CW}}{P_{CW}} \times \frac{ER - 1}{ER + 1} \times 0.2 \times P_{AV}}$$

where P_{CW} is the dc optical power specified on the laser data sheet, I_{MPD_CW} is MPD current at that specified P_{CW} , and P_{AV} is the required average power.

Note that I_{ERSET} and I_{PSET} will change from device to device. However, the control loops will determine actual values. It is not required to know exact values for LI or MPD optical coupling.

LOOP BANDWIDTH SELECTION

For anyrate operation the user should hardwire the LBWSET pin high and use 1 μ F capacitors to set the actual loop bandwidth. These capacitors are placed between the PAVCAP and ERCAP pins and ground. It is important that these capacitors be low-leakage multilayer ceramics with an insulation resistance greater than 100 G Ω or a time constant of 1000 sec, whichever is less. The ADN2841 may be optimized for 2.7 Gbps operation by keeping the LBWSET pin low. This results in a much shorter loop time constant (a 10 \times reduction). The value of PAVCAP and ERCAP capacitors required for 2.5 Gbps operation is 22 nF.

ALARMS

The ADN2841 alarms are designed to allow interface compliance to ITU-T-G958 (11/94) section 10.3.1.1.2 (transmitter fail) and section 10.3.1.1.3 (transmitter degrade). The ADN2841 has two active high alarms, DEGRADE and FAIL. A resistor between ground and the ASET pin is used to set the current at which these alarms are raised. The current through the ASET resistor is a ratio of 100:1 to the FAIL alarm threshold. The DEGRADE alarm will be raised at 90% of this level.

Example:

$$I_{FAIL} = 50 mA \therefore I_{DEGRADE} = 45 mA$$

$$I_{ASET} = \frac{I_{BIASSTRIP}}{100} = \frac{50 mA}{100} = 500 \mu A$$

$$R_{ASET} = \frac{1.23 V}{I_{ASET}} = \frac{1.23 V}{500 \mu A} = 2.46 k\Omega$$

NOTE: The smallest value for R_{ASET} is 1.2 k Ω , as this corresponds to the I_{BIAS} maximum of 100 mA.

The laser degrade alarm, DEGRADE, gives a warning of imminent laser failure if the laser diode degrades further or environmental conditions continue to stress the LD, e.g., increasing temperature.

The laser fail alarm, FAIL, is activated when the transmitter can no longer be guaranteed to be SONET/SDH-compliant. This occurs when one of the following conditions arises:

- The ASET threshold is reached.
- The ALS pin is set high. This shuts off the modulation and bias currents to the LD, resulting in the MPD current dropping to zero. This gives closed-loop feedback to the system in which ALS has been enabled.

DEGRADE will only be raised when the bias current exceeds 90% of ASET current.

MONITOR CURRENTS

IBMON, IMMON, and IMPDMON and IMPDMON2 are current controlled current sources from V_{CC} . They mirror the bias, modulation, and MPD current for increased monitoring functionality. An external resistor to GND gives a voltage proportional to the current monitored.

DUAL MPD DWDM FUNCTION (48-PIN LFCSP ONLY)

The ADN2841 has circuitry for an optional second monitor photodiode, MPD2.

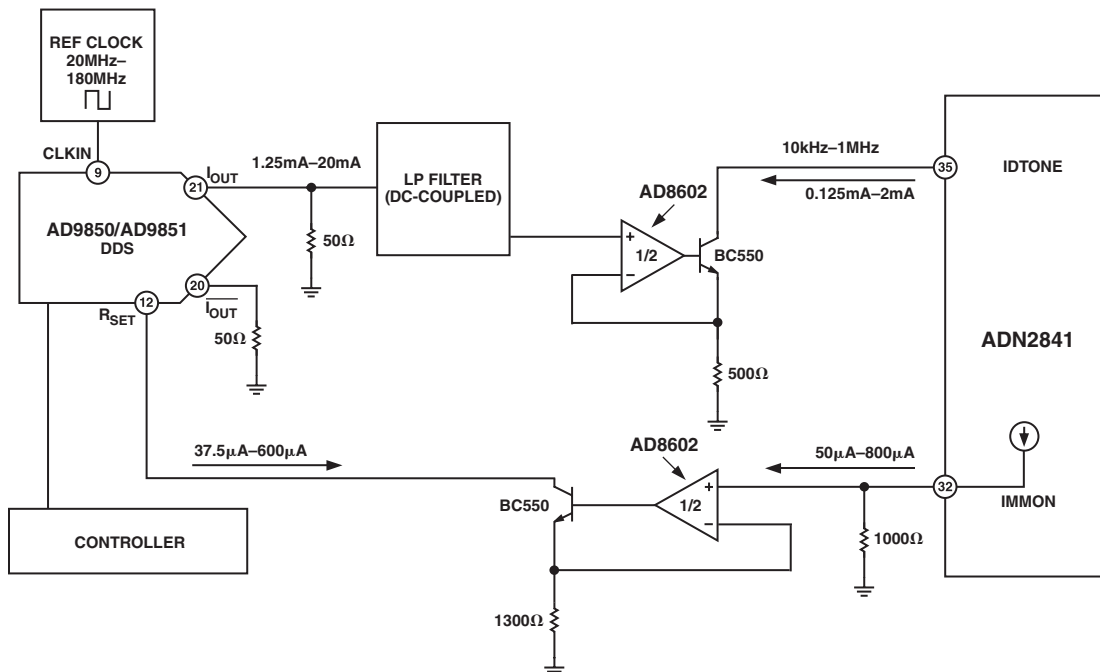


Figure 3. Circuitry to Allow Fiber Identification

The second photodiode current is mirrored to IMPDMON2 for wavelength control purposes and is summed internally for the power control loop. For single MPD circuits the MPD2 pin is tied to GND.

This enables the system designer to use the two currents to control the wavelength of the laser diode using various optical filtering techniques inside the laser module.

If the monitor current functions IMPDMON and IMPDMON2 are not required, the IMPD and IMPD2 pins can be grounded and the monitor photodiode output can be connected directly to PSET.

IDTONE (48-PIN LFCSP ONLY)

The IDTONE pin is supplied for fiber identification/supervisory channels or control purposes in WDM. This pin modulates the optical one level over a possible range of 2% of minimum IMOD to 10% of maximum IMOD. The level of modulation is set by connecting an external current sink between the IDTONE pin and ground. There is a gain of two from this pin to the IMOD current.

Figure 3 shows how an AD9850/AD9851 DDS may be used with the ADN2841 to allow fiber identification.

Note that using IDTONE during transmission may cause optical eye degradation.

DATA, CLOCK INPUTS

Data and Clock inputs are ac-coupled (10 nF recommended) and terminated via a 100 Ω internal resistor between DATAP and DATAN, and also between CLKP and CLKN pins. There is a high-impedance circuit to set the common-mode voltage that is designed to change over temperature. It is recommended that ac coupling be used to eliminate the need for matching between common-mode voltages.

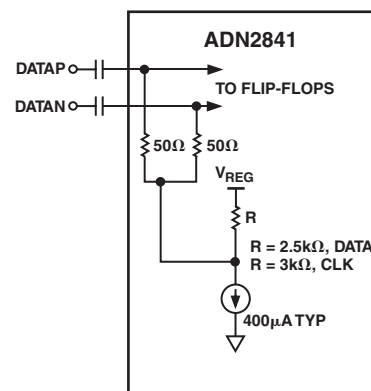


Figure 4. AC Coupling of Data Inputs

CCBIAS

CCBIAS should be connected to the BIAS pin if the laser diode is connected to the ADN2841 using a capacitor. CCBIAS is a current sink to GND.

AUTOMATIC LASER SHUTDOWN

The ADN2841 ALS allows compliance to ITU-T-G958 (11/94), section 9.7.

When ALS is logic high, both bias and modulation currents are turned off.

Correct operation of ALS can be confirmed by the fail alarm being raised when ALS is asserted. Note this is the only time that DEGRADE will be low while FAIL is high.

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ALARM INTERFACES

A 30 kΩ internal pull-up resistor is employed to pull the digital high value of the alarm outputs to V_{CC}. However, the ADN2841 has a feature that allows the user to externally wire resistors in parallel with the 30 kΩ pull-up resistors thus enabling the user to interface to non-V_{CC} levels. *Non-V_{CC} alarm output levels must be below the V_{CC} used for the ADN2841.*

POWER CONSUMPTION

The ADN2841 die temperature must be kept below 125°C. The θ_{JA} for the 48-lead LFCSP is 25°C/W and the 32-lead LFCSP is 32°C/W when soldered in a four-layered board. Both LFCSP packages have an exposed paddle and as such need to be soldered to the PCB to achieve this thermal performance.

$$T_{DIE} = T_{AMBIENT} + \theta_{JA} \times P$$

$$I_{CC} = I_{CCMIN} + 0.3 I_{MOD}$$

$$P = V_{CC} \times I_{CC} + (I_{BIAS} \times V_{BIAS_PIN}) + (I_{MOD} \times V_{MOD_PIN})$$

Hence the maximum combination of I_{BIAS} + I_{MOD} must be calculated.

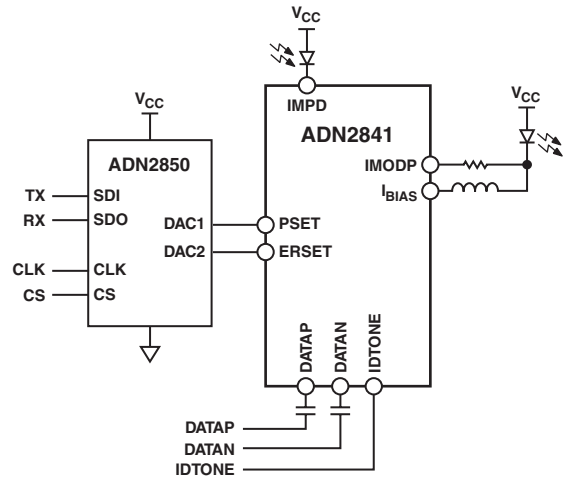


Figure 5. Application Using Optical Supervisor ADN2850 as a Dual 10-Bit Digital Potentiometer Using Thin-Film Resistor Technology to Give Very Low Temperature Coefficients

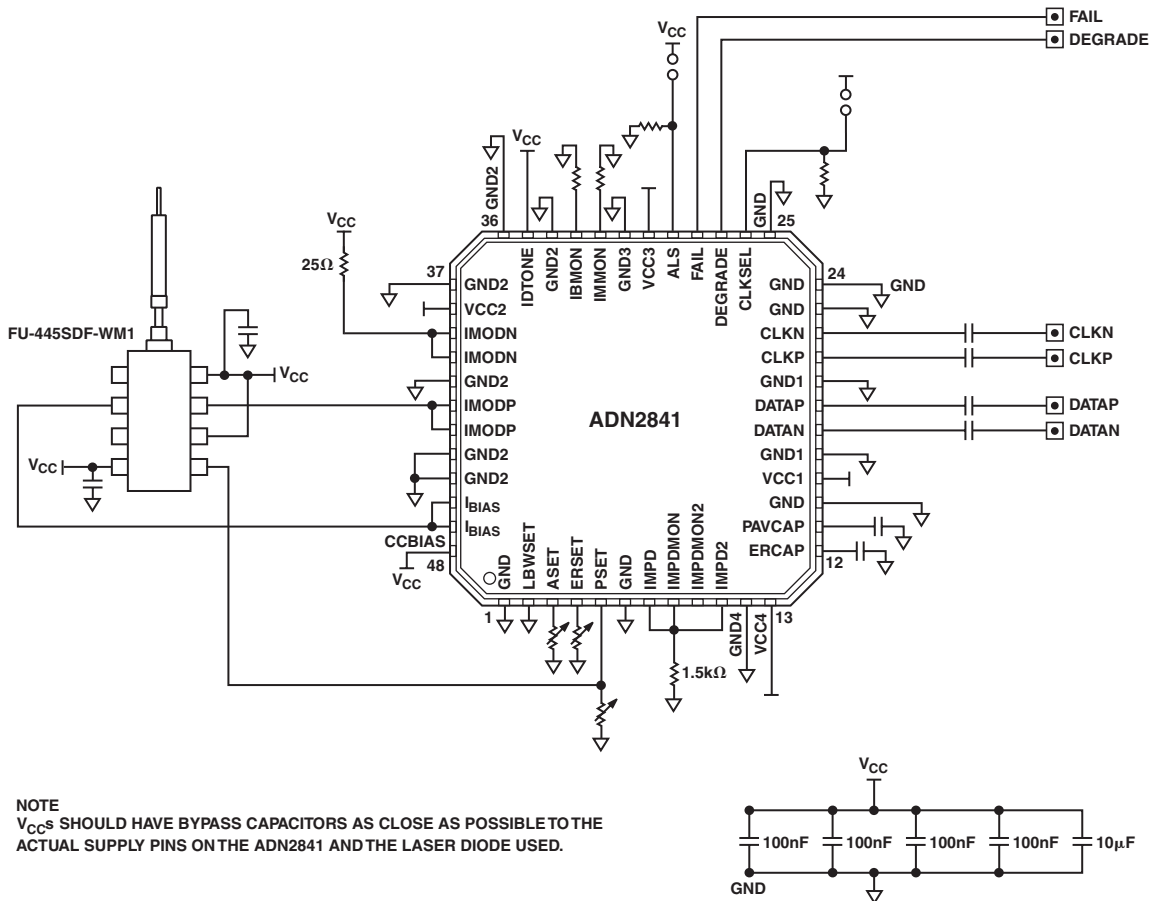


Figure 6. 2.7 Gbps Test Circuit, DC-Coupled, Data Not Clocked, Fast Loop Time Constant Selected

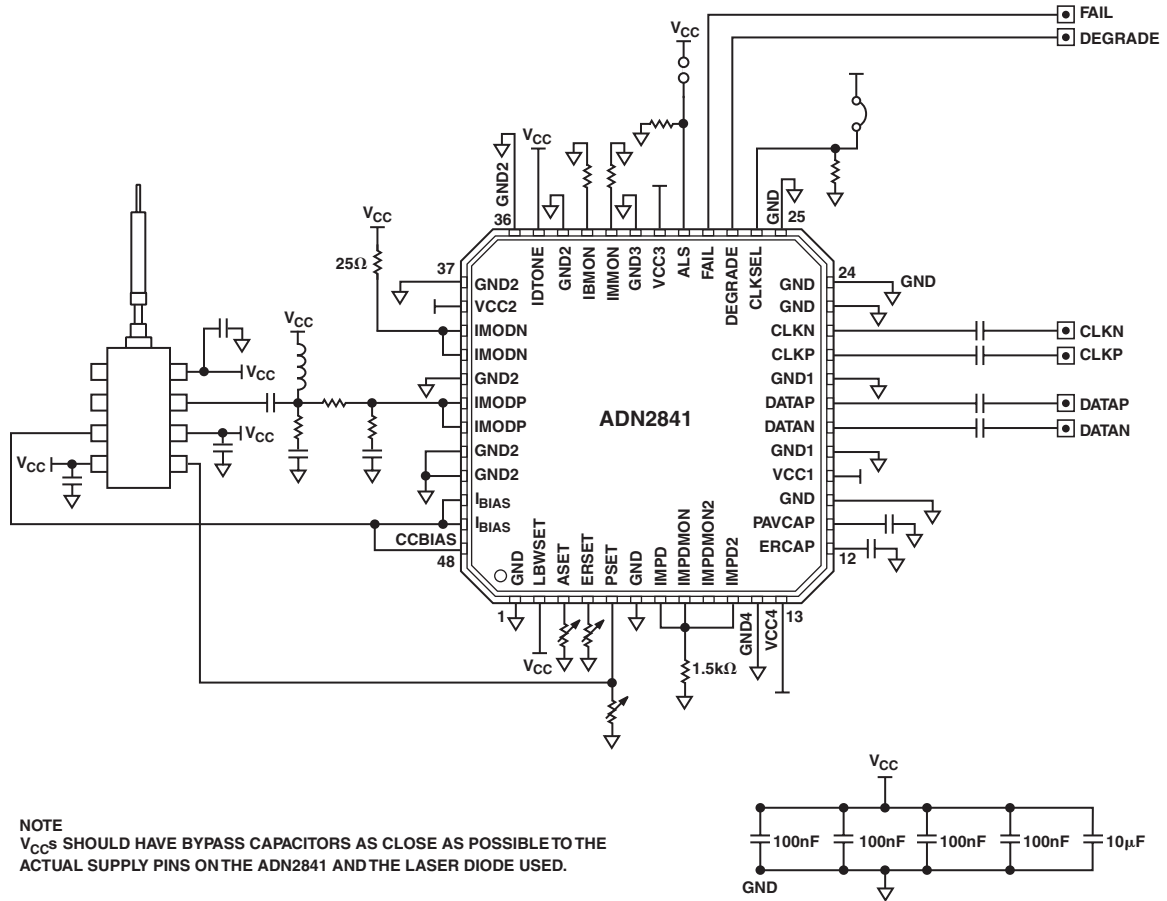


Figure 7. Any Rate Test Circuit, Capacitively Coupled, Data Clocked, Slow Loop Time Constant Selected

ADN2841

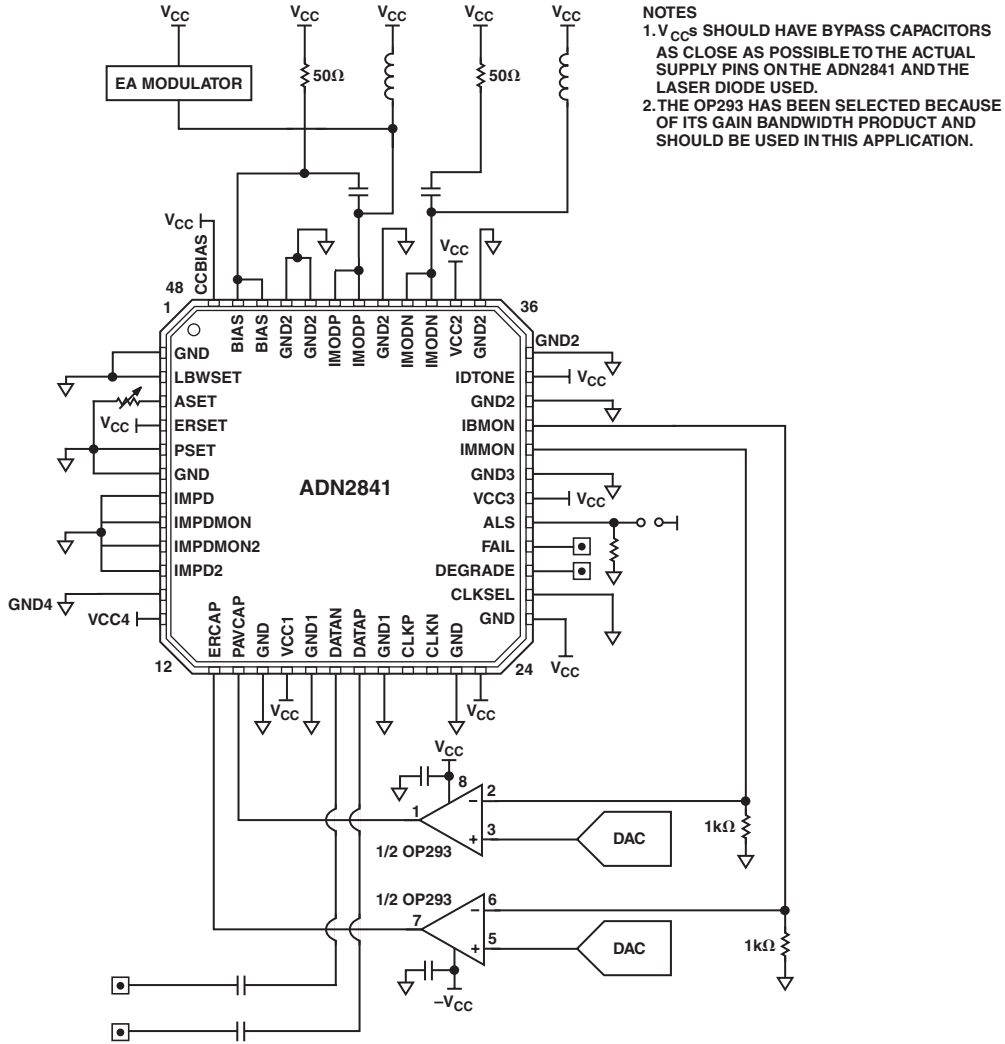


Figure 8. EA Modulator Application

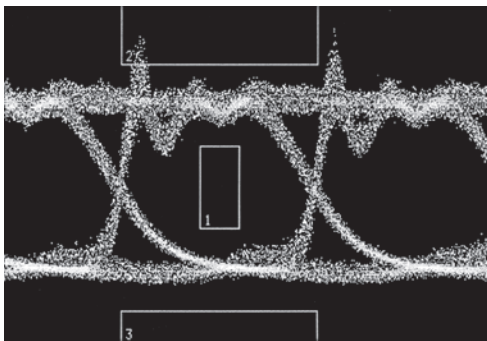


Figure 9. Unfiltered 2.5 Gbps Optical Eye. Average Power = -3 dBm, Extinction Ratio = 9.5 dB. Eye obtained using a Mitsubishi FU-445-SDF.

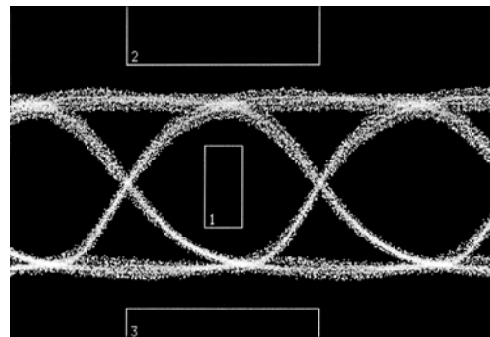
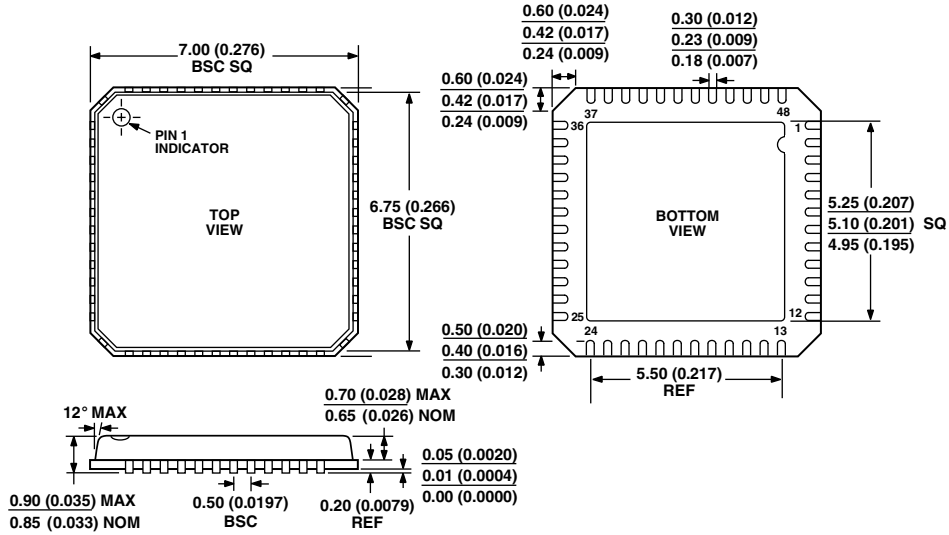


Figure 10. Filtered 2.5 Gbps Optical Eye. Average Power = -3 dBm, Extinction Ratio = 9 dB. Eye obtained using a Mitsubishi FU-445-SDF.

OUTLINE DIMENSIONS

Dimensions shown in millimeters and (inches).

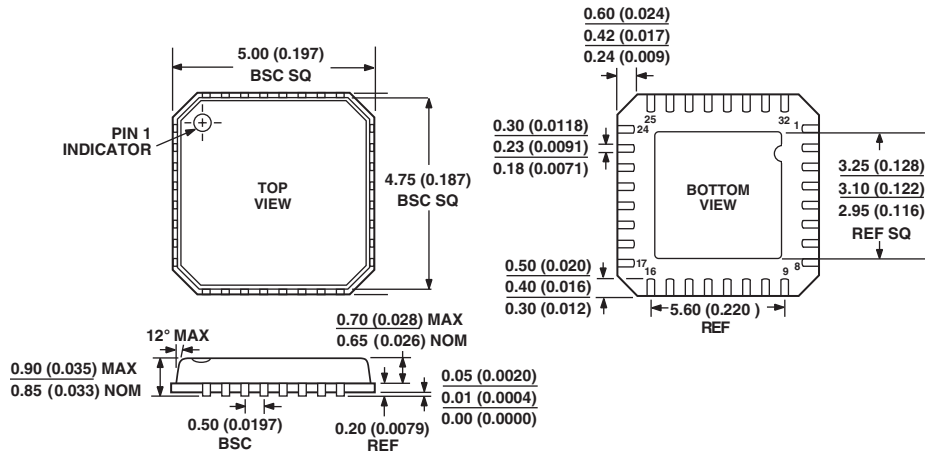
48-Lead (7x7) LFCSP (Exposed Paddle)
(CP-48)



NOTE

EXPOSED PADDLE SHOULD BE SOLDERED TO THE MOST NEGATIVE SUPPLY OF THE ADN2841

32-Lead (5x5) LFCSP (Exposed Paddle)
(CP-32)



NOTES

1. DIMENSIONS MEET JEDEC MO-220-VHHD-2
2. EXPOSED PADDLE SHOULD BE SOLDERED TO THE MOST NEGATIVE SUPPLY OF THE ADN2841

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