STI150N10F7, STP150N10F7

N-channel 100 V, 0.0036 Ω typ., 110 A, STripFET™ F7 Power MOSFETs in I^{2}PAK and TO-220 packages

Datasheet — production data

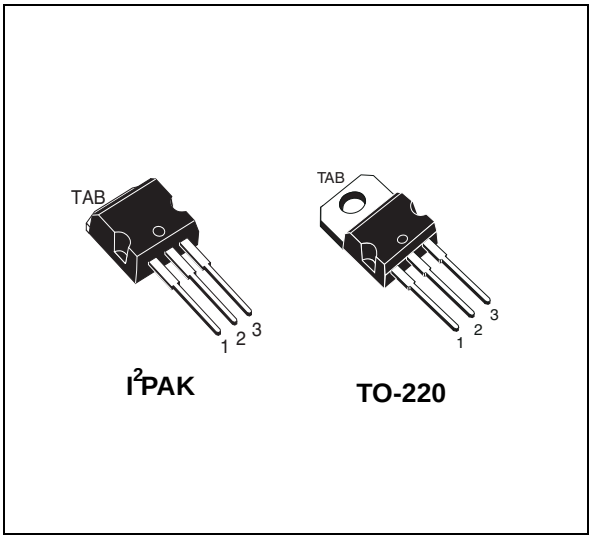
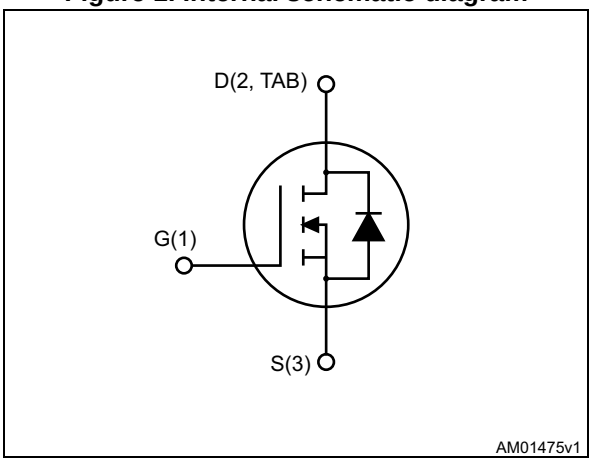


Figure 1. Internal schematic diagram



Features

Order codes	V_{DS}	$R_{DS(on)max}$	I_D	P_{TOT}
STI150N10F7	100 V	0.0042 Ω	110 A	250 W
STP150N10F7				

- Among the lowest $R_{DS(on)}$ on the market
- Excellent figure of merit (FoM)
- Low Crss/Ciss ratio for EMI immunity
- High avalanche ruggedness

Applications

- Switching applications

Description

These N-channel Power MOSFETs utilize STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STI150N10F7	150N10F7	I^{2}PAK	Tube
STP150N10F7		TO-220	

This is information on a product in full production. www.st.com

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	100	V
V_{GS}	Gate- source voltage	±20	V
I_D	Drain current (continuous) at T_C = 25 °C	110	A
I_D	Drain current (continuous) at T_C = 100 °C	110	A
I_{DM} (1)	Drain current (pulsed)	440	A
P_{TOT}	Total dissipation at T_C = 25 °C	250	W
E_{AS}(2)	Single pulse avalanche energy	495	mJ
T_J	Operating junction temperature	-55 to 175	°C
T_{stg}	Storage temperature		°C

1. Pulse width is limited by safe operating area
2. Starting T_j=25 °C, I_D=30 A, V_{DD}=50 V

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	0.6	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max	62.5	°C/W

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0, I_D = 250 µA	100			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0, V_{DS} = 100 V			1	µA
		V_{GS} = 0, V_{DS} = 100 V, T_C=125 °C			100	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0, V_{GS} = +20 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2.5		4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 55 A		0.0036	0.0042	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 50 V, f = 1 MHz, V_{GS} = 0	-	8115	-	pF
C_{oss}	Output capacitance		-	1510	-	pF
C_{rss}	Reverse transfer capacitance		-	67	-	pF
Q_g	Total gate charge	V_{DD} = 50 V, I_D = 110 A, V_{GS} = 10 V (see *Figure 14*)	-	117	-	nC
Q_{gs}	Gate-source charge		-	47	-	nC
Q_{gd}	Gate-drain charge		-	26	-	nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 50 V, I_D = 55 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 13*)	-	33	-	ns
t_r	Rise time		-	57	-	ns
$t_{d(off)}$	Turn-off delay time		-	72	-	ns
t_f	Fall time		-	33	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		110	A
I_{SDM} (1)	Source-drain current (pulsed)		-		440	A
V_{SD} (2)	Forward on voltage	I_{SD} = 110 A, V_{GS} = 0	-		1.2	V
t_{rr}	Reverse recovery time	I_{SD} = 110 A, di/dt = 100 A/µs V_{DD} = 80 V, T_J=150 °C (see *Figure 15*)	-	70		ns
Q_{rr}	Reverse recovery charge		-	165		nC
I_{RRM}	Reverse recovery current		-	4.7		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

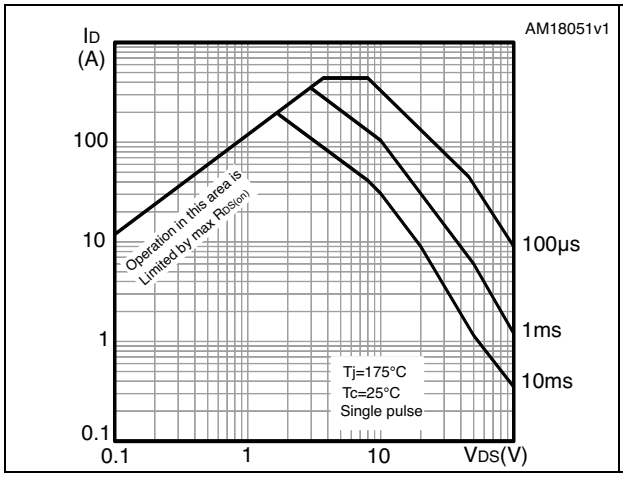


Figure 3. Thermal impedance

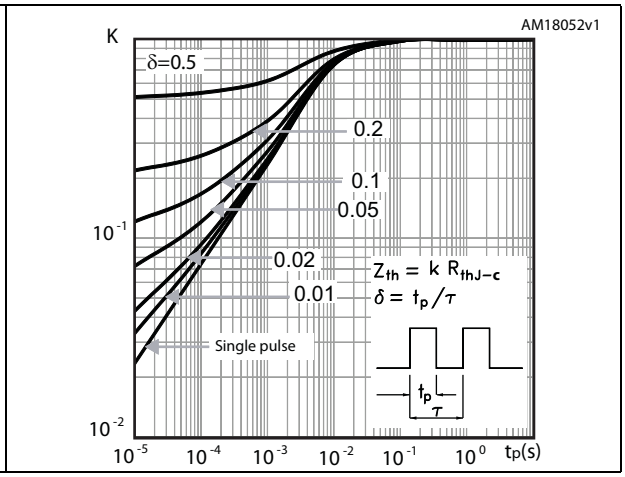


Figure 4. Output characteristics

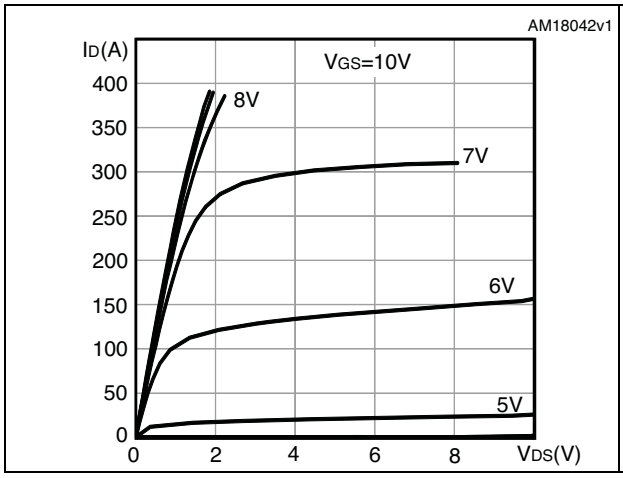


Figure 5. Transfer characteristics

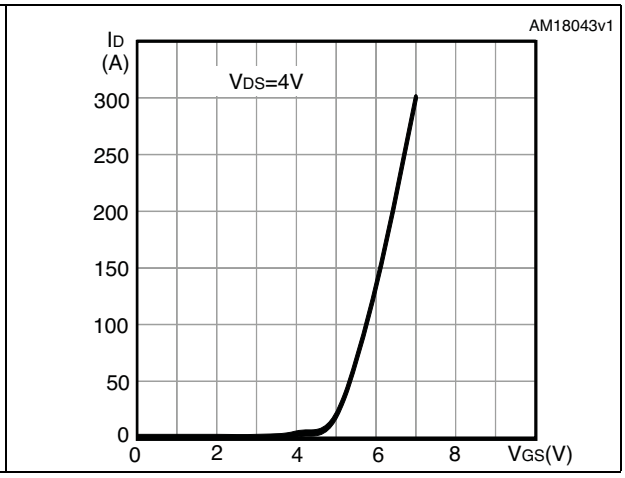


Figure 6. Gate charge vs gate-source voltage

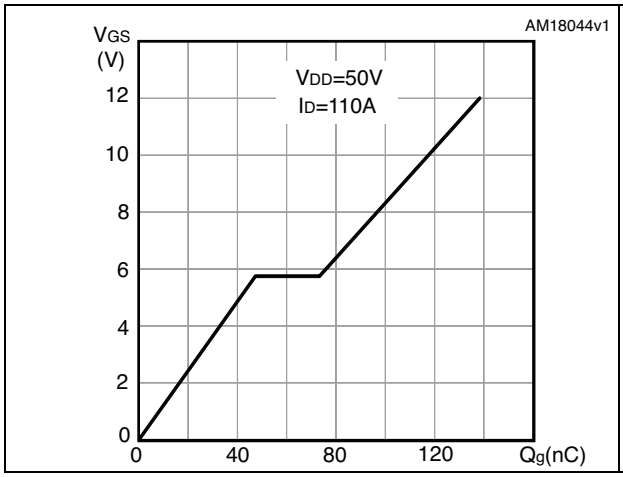


Figure 7. Static drain-source on-resistance

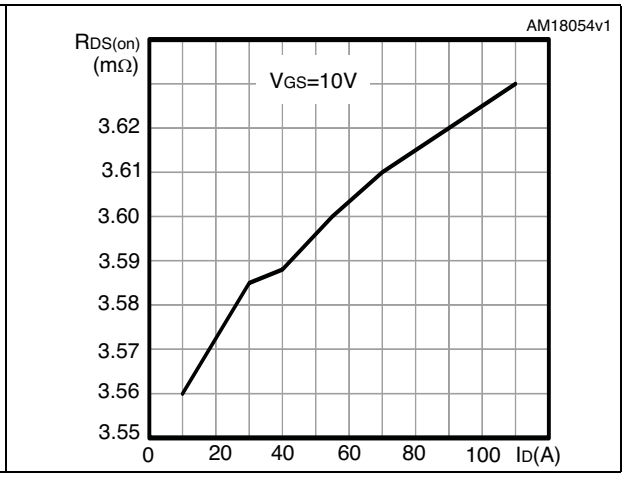


Figure 8. Capacitance variations

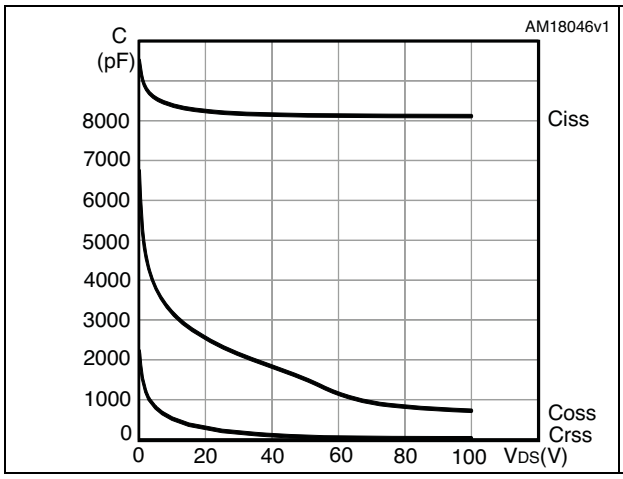


Figure 9. Normalized gate threshold voltage vs temperature

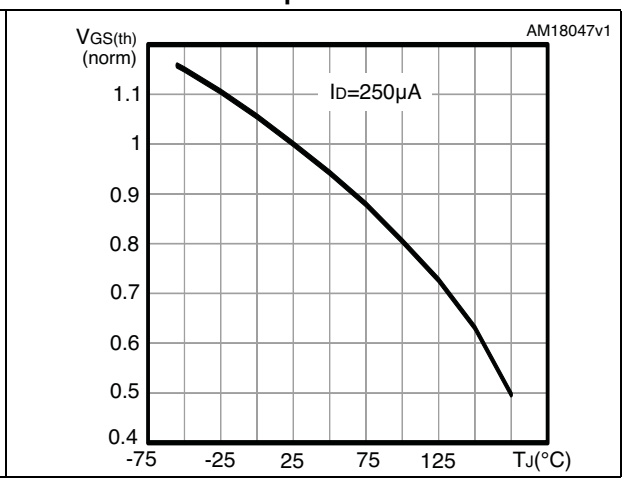


Figure 10. Normalized on-resistance vs temperature

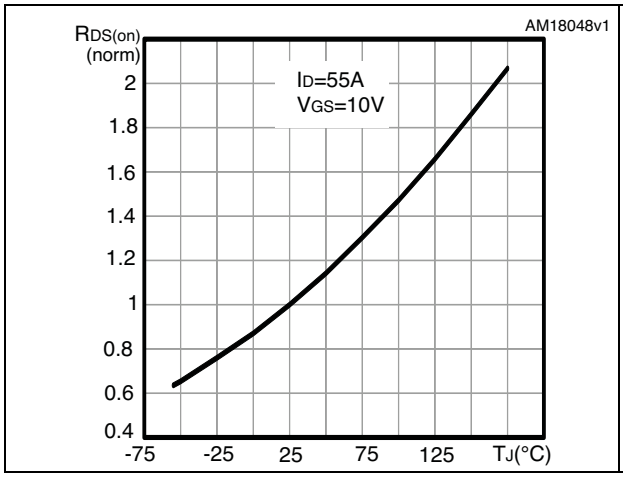


Figure 11. Normalized $V_{(BR)DSS}$ vs temperature

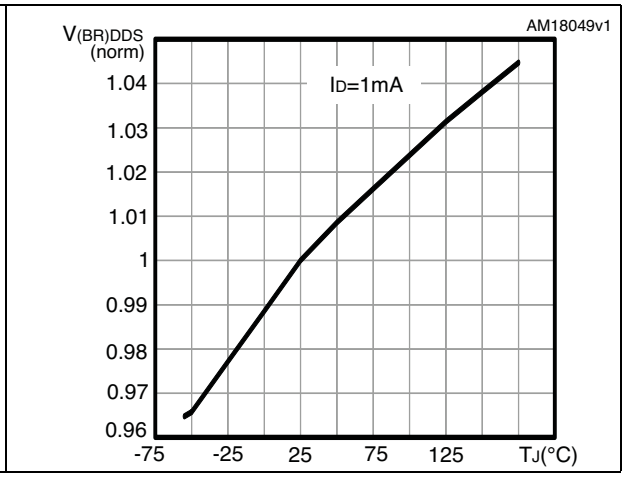
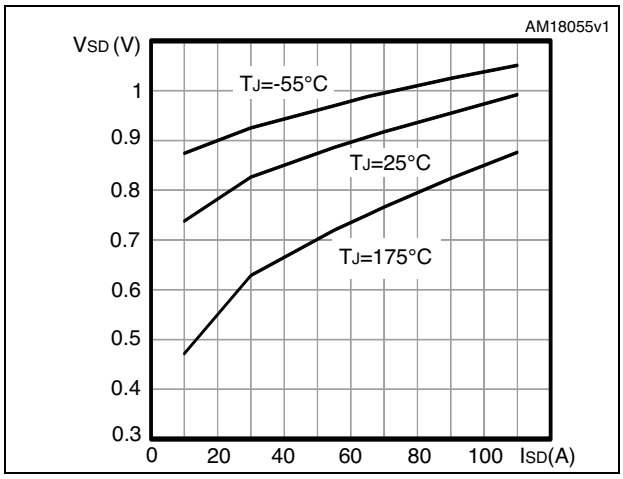


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

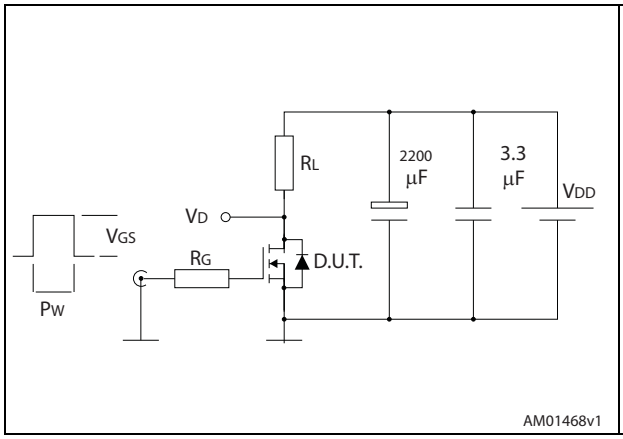


Figure 14. Gate charge test circuit

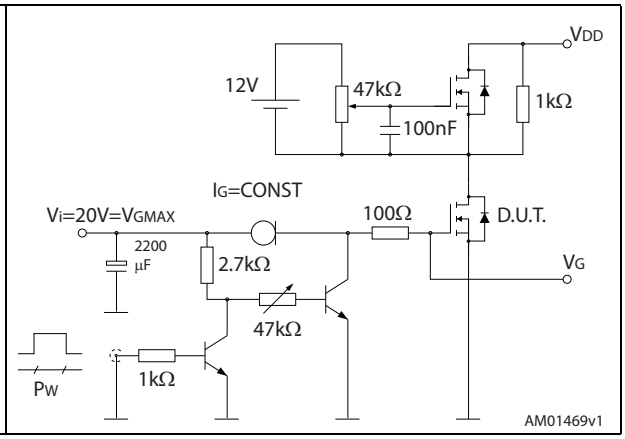


Figure 15. Test circuit for inductive load switching and diode recovery times

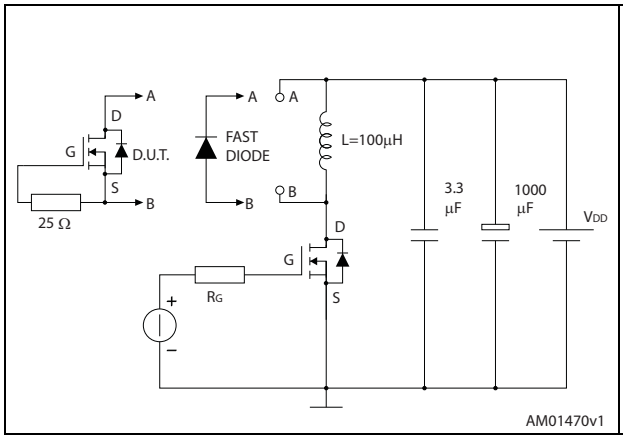


Figure 16. Unclamped inductive load test circuit

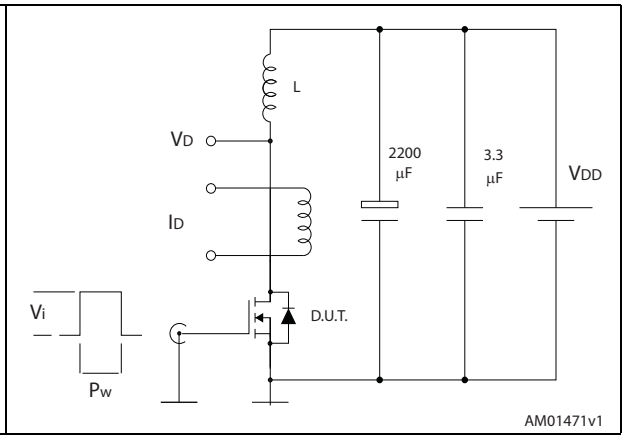


Figure 17. Unclamped inductive waveform

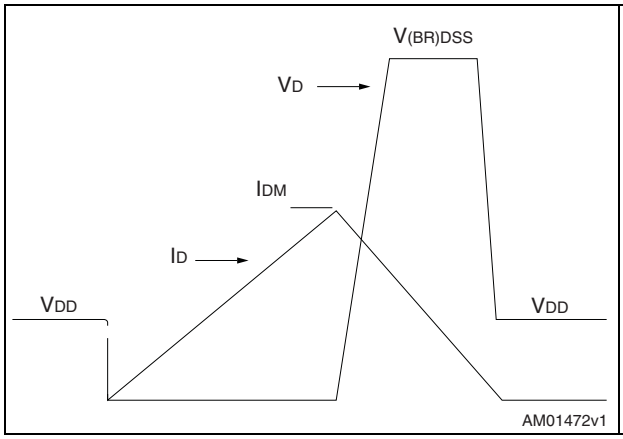
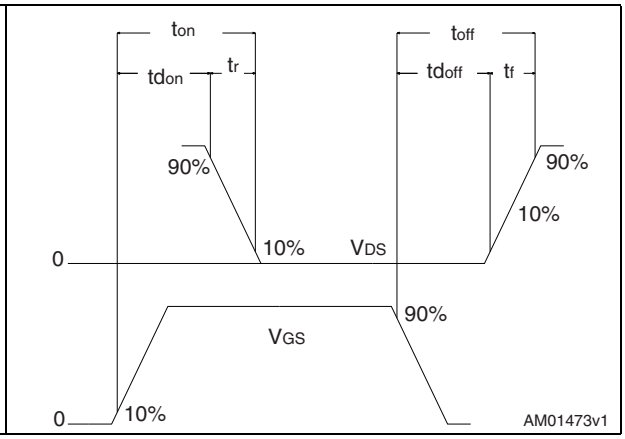


Figure 18. Switching time waveform



4 Package mechanical data

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Figure 19. I²PAK (TO-262) drawing

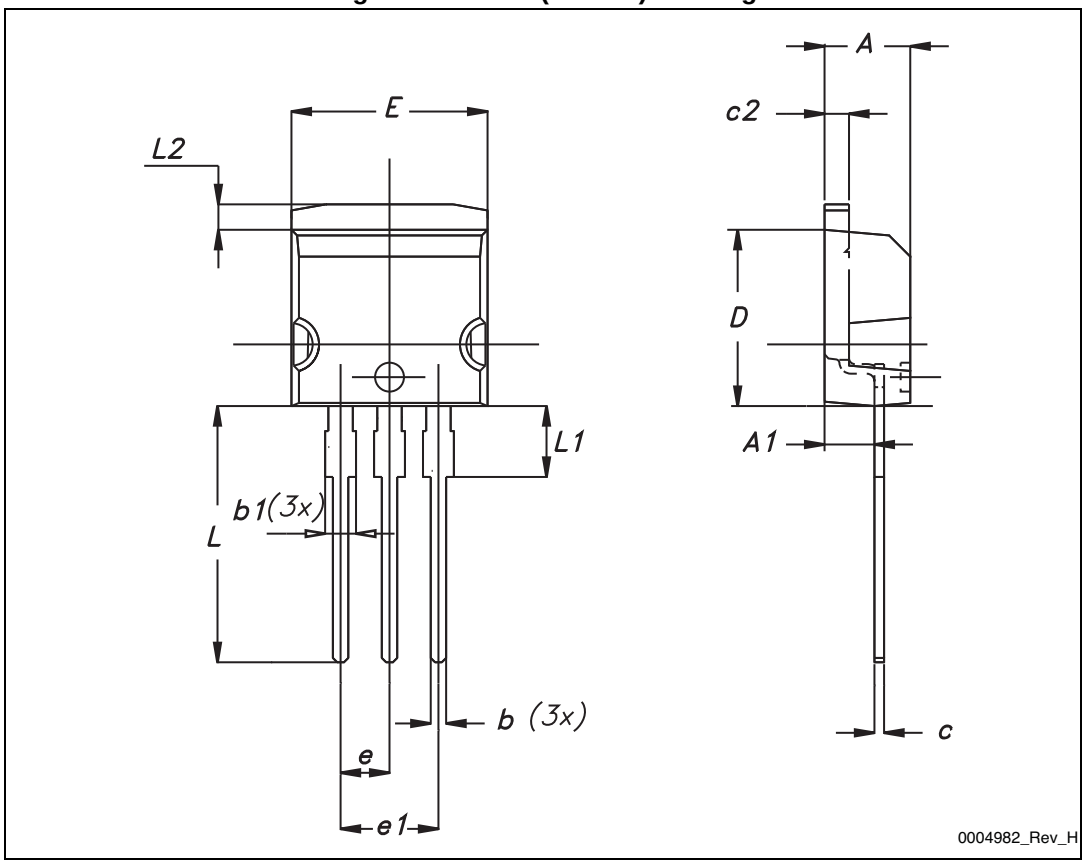

Table 8. I²PAK (TO-262) mechanical data

DIM.	mm.		
	min.	typ	max.
A	4.40		4.60
A1	2.40		2.72
b	0.61		0.88
b1	1.14		1.70
c	0.49		0.70
c2	1.23		1.32
D	8.95		9.35
e	2.40		2.70
e1	4.95		5.15
E	10		10.40
L	13		14
L1	3.50		3.93
L2	1.27		1.40

Figure 20. TO-220 type A drawing

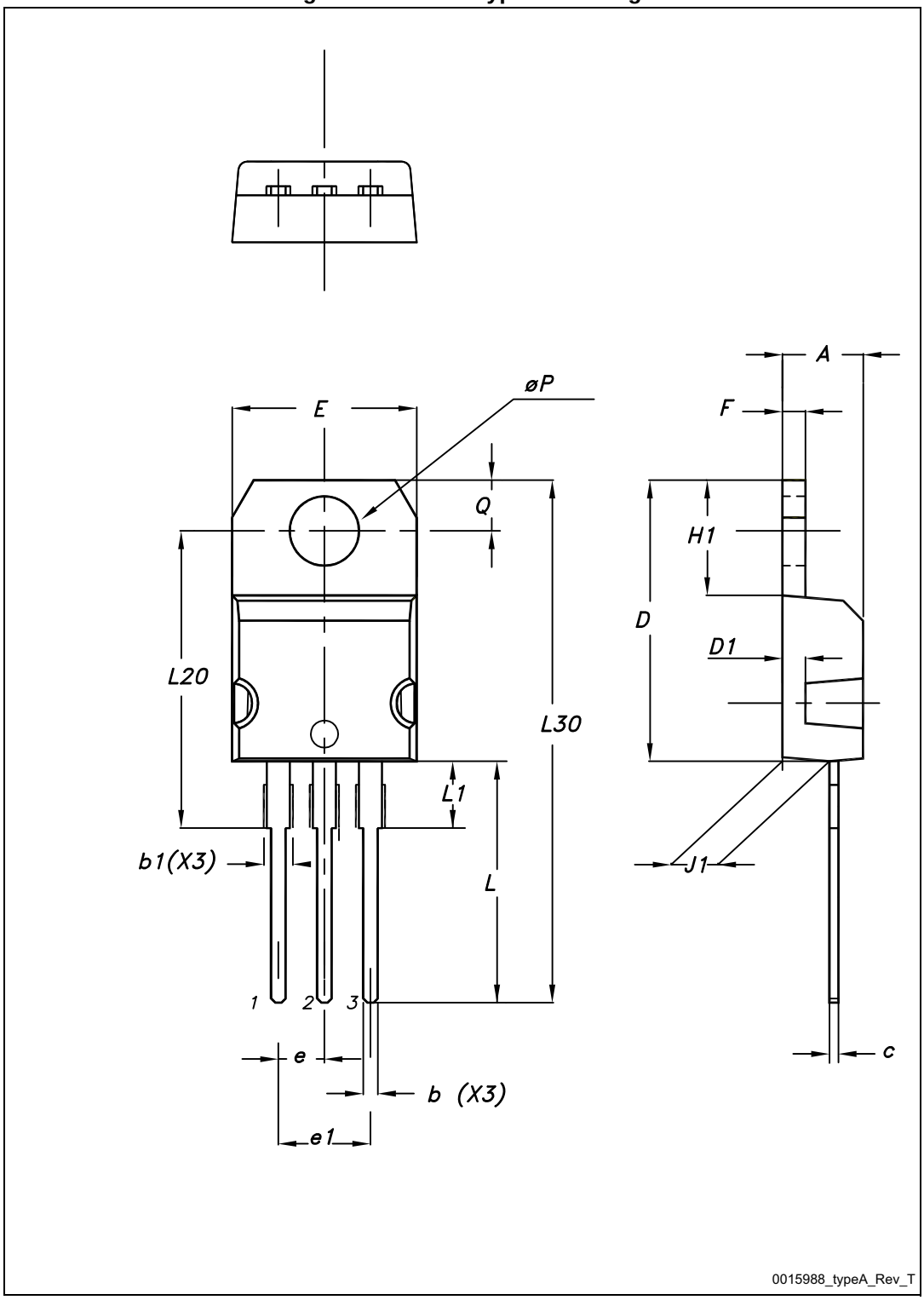

Table 9. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
∅P	3.75		3.85
Q	2.65		2.95

5 Revision history

Table 10. Document revision history

Date	Revision	Changes
16-Apr-2013	1	First release.
22-Jan-2014	2	– The part number STH150N10F7-2 has been moved to a separate datasheet – Added: I^2PAK package – Modified: *Figure 1* – Modified: I_D and I_{DM} values in *Table 2* – Modified: $R_{thj-case}$ value in *Table 3* – Modified: $R_{DS(on)}$ values in *Table 4* – Modified: V_{SD}, I_D and the entire typical values in *Table 5*, *6* and *7* – Updated: *Figure 13*, *14*, *15* and *16* – Updated: *Section 4: Package mechanical data* – Added: *Section 2.1: Electrical characteristics (curves)* – Minor text changes
24-Feb-2014	3	– Datasheet status promoted from preliminary data to production data – Modified: *Figure 10* – Minor text changes
20-Aug-2014		– Updated title, features and description in cover page. – Added E_{AS} parameter in *Table 2: Absolute maximum ratings*. – Minor text changes

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