NB3N502

14 MHz to 190 MHz PLL Clock Multiplier

Description

The NB3N502 is a clock multiplier device that generates a low jitter, TTL/CMOS level output clock which is a precise multiple of the external input reference clock signal source. The device is a cost efficient replacement for the crystal oscillators commonly used in electronic systems. It accepts a standard fundamental mode crystal or an external reference clock signal. Phase−Locked−Loop (PLL) design techniques are used to produce an output clock up to 190 MHz with a 50% duty cycle. The NB3N502 can be programmed via two select inputs (S0, S1) to provide an output clock (CLKOUT) at one of six different multiples of the input frequency source, and at the same time output the input aligned reference clock signal (REF).

Features

- Clock Output Frequency up to 190 MHz
- Operating Range: V_{DD} = 3 V to 5.5 V
- Low Jitter Output of 15 ps One Sigma (rms)
- Zero ppm Clock Multiplication Error
- 45% − 55% Duty Cycle
- 25 mA TTL−level Drive Outputs
- Crystal Reference Input Range of 5 − 27 MHz
- Input Clock Frequency Range of 2 − 50 MHz
- Available in 8−pin SOIC Package or in Die Form
- Full Industrial Temperature Range −40°C to 85°C
- This is a Pb−Free Device

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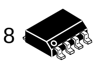
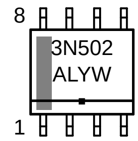


SOIC−8
D SUFFIX
CASE 751

MARKING DIAGRAM



3N502	=	Specific Device Code
A	=	Assembly Location
L	=	Wafer Lot
Y	=	Year
W	=	Work Week
▪	=	Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NB3N502DG	SOIC−8 (Pb−Free)	98 Units/Rail
NB3N502DR2G	SOIC−8 (Pb−Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

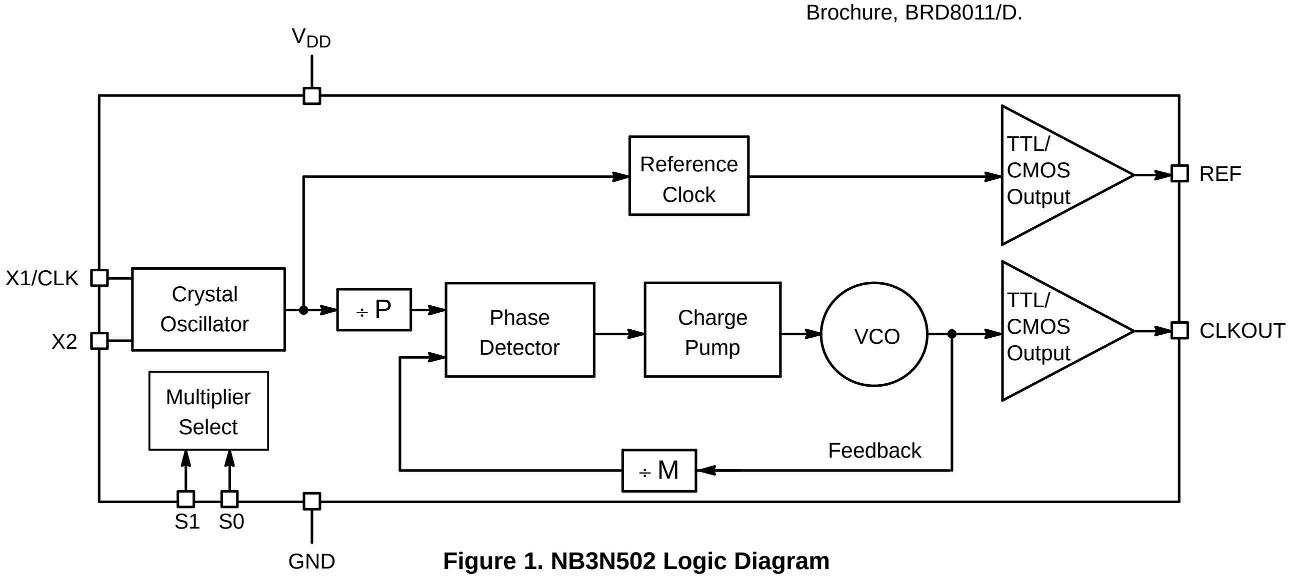


Figure 1. NB3N502 Logic Diagram

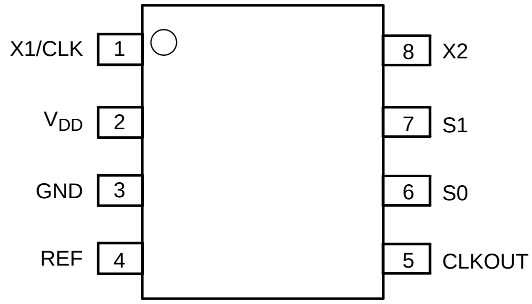


Figure 2. Pin Configuration (Top View)

Table 1. CLOCK MULTIPLIER SELECT TABLE

S1*	S0**	Multiplier
L	L	2X
L	H	5X
M	L	3X
M	H	3.33X
H	L	4X
H	H	2.5X

L = GND
H = V_{DD}
M = OPEN (unconnected)
* Pin S1 defaults to M when left open
** Pin S0 defaults to H when left open

Table 2. OUTPUT FREQUENCY EXAMPLES

Output Frequency (MHz)	20	25	33.3	48	50	54	64	66.66	75	100	108	120	135
Input Frequency (MHz)	10	10	10	16	20	13.5	16	20	15	20	27	24	27
S1, S0	0 ,0	1, 1	M, 1	M, 0	1, 1	1, 0	1, 0	M, 1	0, 1	0, 1	1, 0	0, 1	0, 1

Table 3. PIN DESCRIPTION

Pin #	Name	I/O	Description
1	X1/CLK	Input	Crystal or External Reference Clock Input
2	V_{DD}	Power Supply	Positive Supply Voltage (3 V to 5.5 V)
3	GND	Power Supply	0 V Ground.
4	REF	CMOS/TTL Output	Buffered Crystal Oscillator Clock Output
5	CLKOUT	CMOS/TTL Output	Clock Output
6	S0	CMOS/TTL Input	Multiplier Select Pin − Connect to V_{DD} or GND**.** Internal Pull−up Resistor.
7	S1	Three−level Input	Multiplier Select Pin − Connect to V_{DD}, GND or Float to M.
8	X2	Crystal Input	Crystal Input − Do Not Connect when Providing an External Clock Reference

Table 4. ATTRIBUTES

Characteristic		Value
ESD Protection	Human Body Model Machine Model	> 8 kV > 600 V
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)		Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Transistor Count		6700 Devices
Meets or Exceeds JEDEC Standard EIA/JESD78 IC Latchup Test		

1. For additional Moisture Sensitivity information, refer to Application Note AND8003/D.

Table 5. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{DD}	Positive Power Supply	GND = 0 V		7	V
V_I	Input Voltage			GND – 0.5 = V_I = V_{DD} + 0.5	V
T_A	Operating Temperature Range			−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient)	0 LFPM 500 LFPM	SOIC−8 SOIC−8	190 130	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	(Note 1)	SOIC−8	41 to 44	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. JEDEC standard multilayer board − 2S2P (2 signal, 2 power).

Table 6. DC CHARACTERISTICS (V_{DD} = 3 V to 5.5 V unless otherwise noted, GND = 0 V, T_A = −40°C to +85°C) (Note 2)

Symbol	Characteristic	Min	Typ	Max	Unit
I_{DD}	Power Supply Current (unloaded CLKOUT operating at 100 MHz with 20 MHz crystal)		20		mA
V_{OH}	Output HIGH Voltage I_{OH} = −25 mA TTL High	2.4			V
V_{OL}	Output LOW Voltage I_{OL} = 25 mA			0.4	V
V_{IH}	Input HIGH Voltage, CLK only (pin 1)	(V_{DD} / 2) + 1	V_{DD} / 2		V
V_{IL}	Input LOW Voltage, CLK only (pin 1)		V_{DD} / 2	(V_{DD} / 2) −1	V
V_{IH}	Input HIGH Voltage, S0, S1	V_{DD} – 0.5			V
V_{IL}	Input LOW Voltage, S0, S1			0.5	V
V_{IM}	Input level of S1 when open (Input Mid Point)		V_{DD} ÷ 2		V
C_{in}	Input Capacitance, S0, S1		4		pF
I_{SC}	Output Short Circuit Current		± 70		mA

2. Parameters are guaranteed by characterization and design, not tested in production.

Table 7. AC CHARACTERISTICS (V_{DD} = 3 V to 5.5 V unless otherwise noted, GND = 0 V, T_A = −40°C to +85°C) (Note 3)

Symbol	Characteristic	Min	Typ	Max	Unit
f_{Xtal}	Crystal Input Frequency	5		27	MHz
f_{CLK}	Clock Input Frequency	2		50	MHz
f_{OUT}	Output Frequency Range V_{DD} = 4.5 to 5.5 V (5.0 V ± 10%) V_{DD} = 3.0 to 3.6 V (3.3 V ± 10%)	 14 14		 190 120	 MHz MHz
DC	Clock Output Duty Cycle at 1.5 V up to 190 MHz	45	50	55	%
$t_{jitter\ (rms)}$	Period Jitter (RMS, 1 σ)		15		ps
$t_{jitter\ (pk-to-pk)}$	Total Period Jitter, (peak−to−peak)		±40		ps
t_r/t_f	Output rise/fall time (0.8 V to 2.0 V / 2.0 V to 0.8 V)		1		ns

3. Parameters are guaranteed by characterization and design, not tested in production.

APPLICATIONS INFORMATION

High Frequency CMOS/TTL Oscillators

The NB3N502, along with a low frequency fundamental mode crystal, can build a high frequency CMOS/TTL output oscillator. For example, a 20 MHz crystal connected to the NB3N502 with the 5X output selected (S1 = L, S0 = H) produces a 100 MHz CMOS/TTL output clock.

External Components

Decoupling Instructions

In order to isolate the NB3N502 from system power supply, noise de−coupling is required. The 0.01 μF decoupling capacitor has to be connected between V_{DD} and GND on pins 2 and 3. It is recommended to place de−coupling capacitors as close as possible to the NB3N502 device to minimize lead inductance. Control input pins can be connected to device pins V_{DD} or GND, or to the V_{DD} and GND planes on the board.

Series Termination Resistor Recommendation

A 33 Ω series terminating resistor can be used on the CLKOUT pin.

Crystal Load Capacitors Selection Guide

The total on−chip capacitance is approximately 12 pF per pin (C_{IN1} and C_{IN2}). A parallel resonant, fundamental mode crystal should be used.

The device crystal connections should include pads for small capacitors from X1/CLK to ground and from X2 to ground. These capacitors, C_{L1} and C_{L2}, are used to adjust the stray capacitance of the board to match the nominally required crystal load capacitance (C_{LOAD} (crystal)). Because load capacitance can only be increased in this trimming process, it is important to keep stray capacitance to a minimum by using very short PCB traces (and no vias) between the crystal and device. Crystal load capacitors, if needed, must be connected from each of the pins X1 and X2 to ground. The load capacitance of the crystal (C_{LOAD} (crystal)) must be matched by total load capacitance of the oscillator circuitry network, C_{INX}, C_{SX} and C_{LX}, as seen by the crystal (see Figure 3 and equations below).

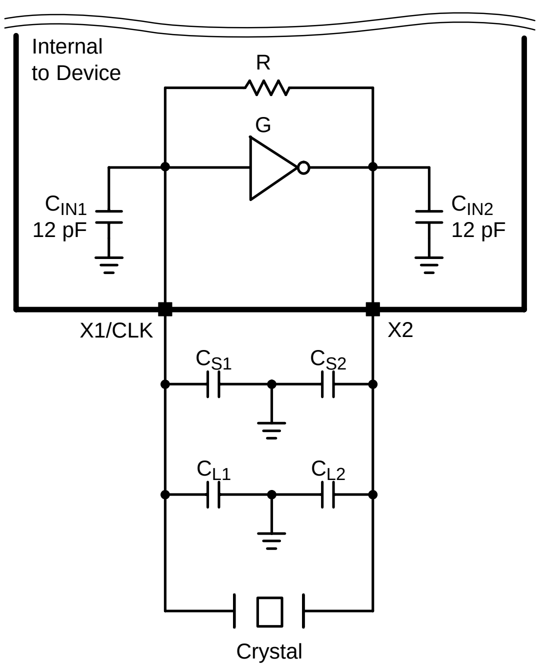


Figure 3. Using a Crystal as Reference Clock

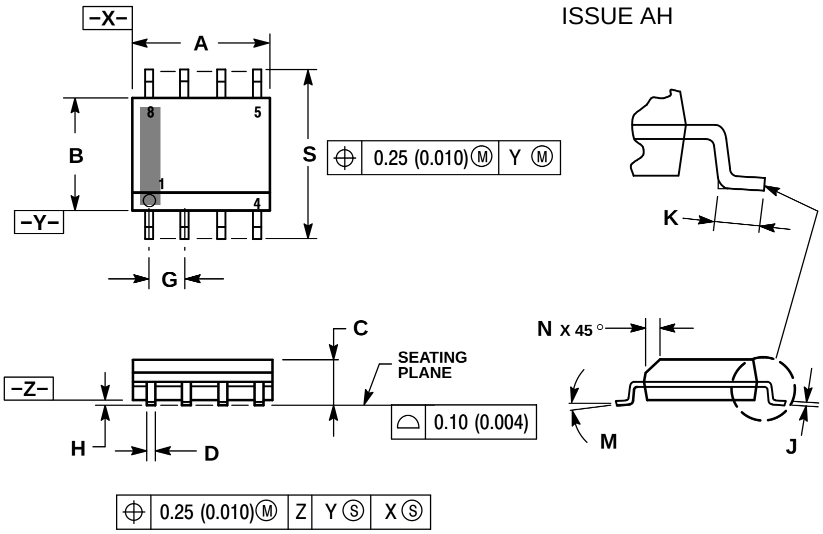
$C_{LOAD1} = C_{IN1} + C_{S1} + C_{L1}$ [Total capacitance on X1/CLK]
$C_{LOAD2} = C_{IN2} + C_{S2} + C_{L2}$ [Total capacitance on X2]
$C_{IN1} \approx C_{IN2} \approx 12$ pF (Typ) [Internal capacitance]
$C_{S1} \approx C_{S2} \approx 5$ pF (Typ) [External PCB stray capacitance]
$C_{LOAD1,2} = 2 \bullet C_{LOAD}$ (Crystal)
$C_{L2} = C_{LOAD2} - C_{IN2} - C_{S2}$ [External load capacitance on X2]
$C_{L1} = C_{LOAD1} - C_{IN1} - C_{S1}$ [External load capacitance on X1/CLK]

Example 1: Equal stray capacitance on PCB
C_{LOAD} (Crystal) = 18 pF (Specified by the crystal manufacturer)
$C_{LOAD1} = C_{LOAD2} = 36$ pF
$C_{IN1} = C_{IN2} = 12$ pF
$C_{S1} = C_{S2} = 6$ pF
$C_{L1} = 36 - 12 - 6 = 18$ pF
$C_{L2} = 36 - 12 - 6 = 18$ pF

Example 2: Different stray capacitance on PCB trace X1/CLK vs. X2
C_{LOAD} (Crystal) = 18 pF
$C_{LOAD1} = C_{LOAD2} = 36$ pF
$C_{IN1} = C_{IN2} = 12$ pF
$C_{S1} = 4$ pF & $C_{S2} = 8$ pF
$C_{L1} = 36 - 12 - 4 = 20$ pF
$C_{L2} = 36 - 12 - 8 = 16$ pF

PACKAGE DIMENSIONS

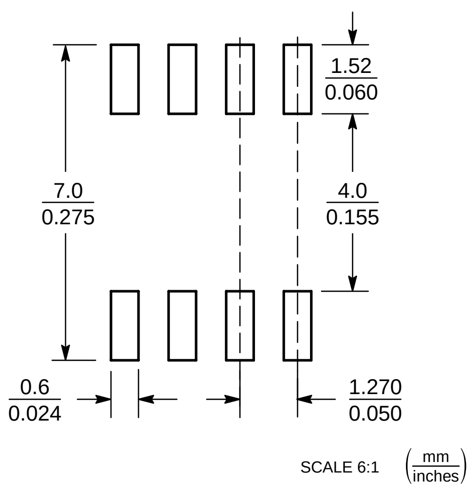
SOIC−8 NB
CASE 751−07
ISSUE AH



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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Тел: +7 (812) 336 43 04 (многоканальный)
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www.lifeelectronics.ru