# 128Kx16 LOW VOLTAGE, ULTRA LOW POWER CMOS STATIC RAM

**MAY 2016**

## KEY FEATURES

- High-speed access time: 45ns, 55ns
- CMOS low power operation
  - – Operating Current: 18 mA (max) at 85°C
  - – CMOS Standby Current: 5.4uA (typ) at 25°C
- TTL compatible interface levels
- Single power supply
  - –1.65V-2.2V VDD (IS62WV12816EALL)
  - – 2.2V-3.6V VDD (IS62/65WV12816EBLL)
- Three state outputs
- Industrial and Automotive temperature support
- Lead-free available

## DESCRIPTION

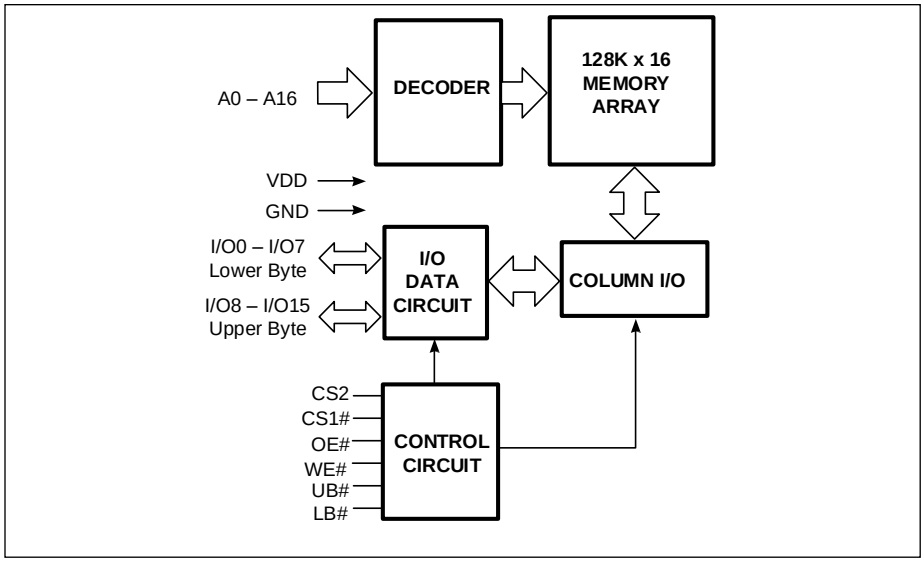
The *ISSI* IS62/65WV12816EALL/EBLL are high-speed, 2M bit static RAMs organized as 128K words by 16 bits. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields high-performance and low power consumption devices.

When CS1# is HIGH (deselected) or when CS2 is LOW (deselected) or when CS1# is LOW, CS2 is HIGH and both LB# and UB# are HIGH, the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs. The active LOW Write Enable (WE#) controls both writing and reading of the memory. A data byte allows Upper Byte (UB#) and Lower Byte (LB#) access.

The IS62/65WV12816EALL/EBLL are packaged in the JEDEC standard 48-pin mini BGA (6mm x 8mm) and 44-Pin TSOP (TYPE II)

## BLOCK DIAGRAM

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b.) the user assume all such risks; and
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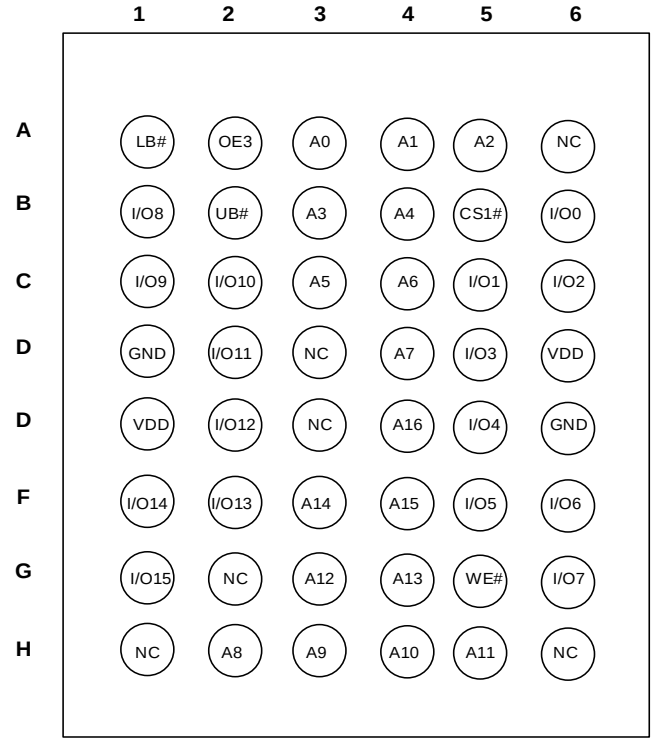
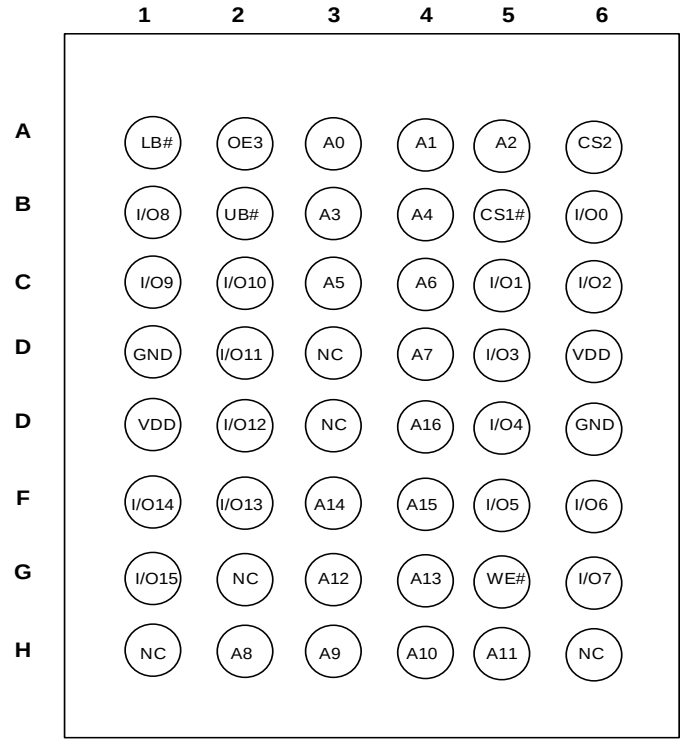
# PIN CONFIGURATIONS

### 48-Pin mini BGA (6mm x 8mm)
### (Package Code B)



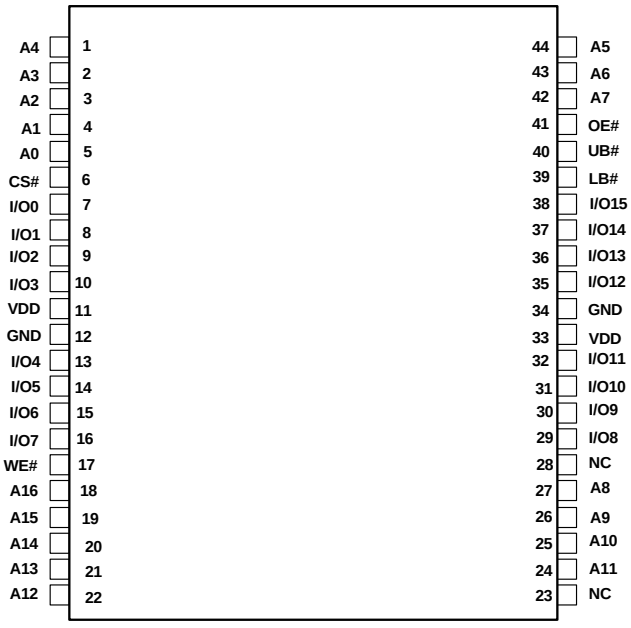

### 48-Pin mini BGA (6mm x 8mm)
### 2 CS Option (Package Code B2)




## PIN DESCRIPTIONS

| | |
|---|---|
| A0-A16 | Address Inputs |
| I/O0-I/O15 | Data Inputs/Outputs |
| CS1#, CS2 | Chip Enable Input |
| OE# | Output Enable Input |
| WE# | Write Enable Input |
| LB# | Lower-byte Control (I/O0-I/O7) |
| UB# | Upper-byte Control (I/O8-I/O15) |
| NC | No Connection |
| VDD | Power |
| GND | Ground |

### 44-Pin mini TSOP (Type II)
### (Package Code T)



# FUNCTION DESCRIPTION

SRAM is one of random access memories. Each byte or word has an address and can be accessed randomly. SRAM has three different modes supported. Each function is described below with Truth Table.

### STANDBY MODE

Device enters standby mode when deselected (CS1# HIGH or CS2 LOW or both UB# and LB# are HIGH). The input and output pins (I/O0-15) are placed in a high impedance state. The current consumption in this mode will be ISB1 or ISB2. CMOS input in this mode will maximize saving power.

### WRITE MODE

Write operation issues with Chip selected (CS1# LOW and CS2 HIGH) and Write Enable (WE#) input LOW. The input and output pins (I/O0-15) are in data input mode. Output buffers are closed during this time even if OE# is LOW. UB# and LB# enables a byte write feature. By enabling LB# LOW, data from I/O pins (I/O0 through I/O7) are written into the location specified on the address pins. And with UB# being LOW, data from I/O pins (I/O8 through I/O15) are written into the location.

### READ MODE

Read operation issues with Chip selected (CS1# LOW and CS2 HIGH) and Write Enable (WE#) input HIGH. When OE# is LOW, output buffer turns on to make data output. Any input to I/O pins during READ mode is not permitted. UB# and LB# enables a byte read feature. By enabling LB# LOW, data from memory appears on I/O0-7. And with UB# being LOW, data from memory appears on I/O8-15.

In the READ mode, output buffers can be turned off by pulling OE# HIGH. In this mode, internal device operates as READ but I/Os are in a high impedance state. Since device is in READ mode, active current is used.

### TRUTH TABLE

| Mode | CS1# | CS2 | WE# | OE# | LB# | UB# | I/O0-I/O7 | I/O8-I/O15 | VDD Current |
|---|---|---|---|---|---|---|---|---|---|
| Not Selected | H | X | X | X | X | X | High-Z | High-Z | ISB1,ISB2 |
| | X | L | X | X | X | X | High-Z | High-Z | |
| | X | X | X | X | H | H | High-Z | High-Z | |
| Output Disabled | L | H | H | H | L | X | High-Z | High-Z | ICC |
| | L | H | H | H | X | L | High-Z | High-Z | |
| Read | L | H | H | L | L | H | DOUT | High-Z | ICC |
| | L | H | H | L | H | L | High-Z | DOUT | |
| | L | H | H | L | L | L | DOUT | DOUT | |
| Write | L | H | L | X | L | H | DIN | High-Z | ICC |
| | L | H | L | X | H | L | High-Z | DIN | |
| | L | H | L | X | L | L | DIN | DIN | |

# ABSOLUTE MAXIMUM RATINGS AND OPERATING RANGE

## ABSOLUTE MAXIMUM RATINGS (1)

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| Vterm | Terminal Voltage with Respect to GND | –0.2 to +3.9($V_{DD}$+0.3V) | V |
| tBIAS | Temperature Under Bias | –55 to +125 | °C |
| $V_{DD}$ | $V_{DD}$ Related to GND | –0.2 to +3.9($V_{DD}$+0.3V) | V |
| tStg | Storage Temperature | –65 to +150 | °C |
| $I_{OUT}$ (2) | DC Output Current (LOW) | 20 | mA |

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. This condition is not per pin. Total current of all pins must meet this value.

## OPERATING RANGE (1)

| Range | Device Marking | Ambient Temperature | VDD |
|---|---|---|---|
| Commercial | IS62WV12816EALL | 0°C to +70°C | 1.65V-2.2V |
| Industrial | IS62WV12816EALL | -40°C to +85°C | 1.65V-2.2V |
| Commercial | IS62WV12816EBLL | 0°C to +70°C | 2.2V-3.6V |
| Industrial | IS62WV12816EBLL | -40°C to +85°C | 2.2V-3.6V |
| Automotive | IS65WV12816EBLL | -40°C to +125°C | 2.2V-3.6V |

Note:

1. Full device AC operation assumes a 100 µs ramp time from 0 to Vcc(min) and 200 µs wait time after Vcc stabilization.

## PIN CAPACITANCE (1)

| Parameter | Symbol | Test Condition | Max | Units |
|---|---|---|---|---|
| Input capacitance | $C_{IN}$ | $T_A$ = 25°C, f = 1 MHz, $V_{DD}$ = $V_{DD}$(typ) | 10 | pF |
| DQ capacitance (IO0–IO15) | $C_{I/O}$ | | 10 | pF |

Note:

1. These parameters are guaranteed by design and tested by a sample basis only.

## THERMAL CHARACTERISTICS (1)

| Parameter | Symbol | Rating | Units |
|---|---|---|---|
| Thermal resistance from junction to ambient (airflow = 1m/s) | $R_{\theta JA}$ | TBD | °C/W |
| Thermal resistance from junction to pins | $R_{\theta JB}$ | TBD | °C/W |
| Thermal resistance from junction to case | $R_{\theta JC}$ | TBD | °C/W |

Note:

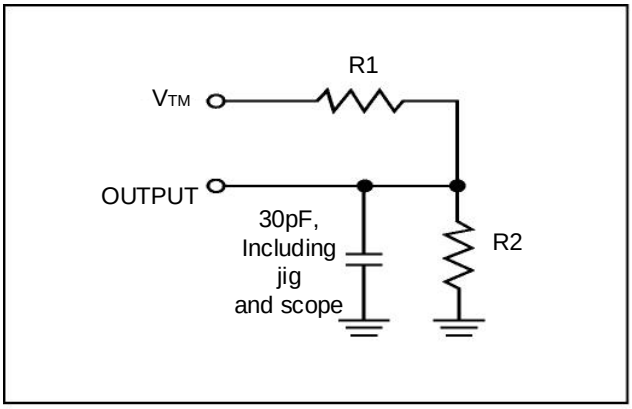
1. These parameters are guaranteed by design and tested by a sample basis only.

## AC TEST CONDITIONS (OVER THE OPERATING RANGE)

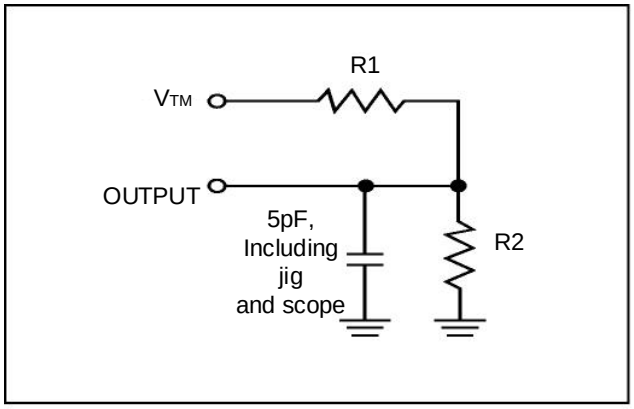
| Parameter | Unit (1.65V~2.2V) | Unit (2.2V~3.6V) |
|---|---|---|
| Input Pulse Level | 0V to $V_{DD}$ | 0V to $V_{DD}$ |
| Input Rise and Fall Time | 1V/ns | 1V/ns |
| Output Timing Reference Level | 0.9V | ½ $V_{DD}$ |
| R1 | 13500 | 1005 |
| R2 | 10800 | 820 |
| $V_{TM}$ | 1.8V | $V_{DD}$ |
| Output Load Conditions | Refer to Figure 1 and 2 | |

## OUTPUT LOAD CONDITIONS FIGURES

### FIGURE 1




### FIGURE 2



# ELECTRICAL CHARACTERISTICS

## IS62WV12816EALL DC ELECTRICAL CHARACTERISTICS-I (OVER THE OPERATING RANGE)

| Symbol | Parameter | Test Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = -0.1 mA | 1.4 | — | V |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 0.1 mA | — | 0.2 | V |
| $V_{IH}$ (1) | Input HIGH Voltage | | 1.4 | $V_{DD}$ + 0.2 | V |
| $V_{IL}$ (1) | Input LOW Voltage | | –0.2 | 0.4 | V |
| $I_{LI}$ | Input Leakage | GND < $V_{IN}$ < $V_{DD}$ | –1 | 1 | µA |
| $I_{LO}$ | Output Leakage | GND < $V_{IN}$ < $V_{DD}$, Output Disabled | –1 | 1 | µA |

Notes:
1. VILL(min) = -1.0V AC (pulse width < 10ns). Not 100% tested.
   VIHH (max) = VDD + 1.0V AC (pulse width < 10ns). Not 100% tested.

## IS62(5)WV12816EBLL DC ELECTRICAL CHARACTERISTICS-I (OVER THE OPERATING RANGE)

| Symbol | Parameter | Test Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | 2.2 ≤ $V_{DD}$ < 2.7, $I_{OH}$ = -0.1 mA | 2.0 | — | V |
| | | 2.7 ≤ $V_{DD}$ ≤ 3.6, $I_{OH}$ = -1.0 mA | 2.4 | — | V |
| $V_{OL}$ | Output LOW Voltage | 2.2 ≤ $V_{DD}$ < 2.7, $I_{OL}$ = 0.1 mA | — | 0.4 | V |
| | | 2.7 ≤ $V_{DD}$ ≤ 3.6, $I_{OL}$ = 2.1 mA | — | 0.4 | V |
| $V_{IH}$ (1) | Input HIGH Voltage | 2.2 ≤ $V_{DD}$ < 2.7 | 1.8 | $V_{DD}$ + 0.3 | V |
| | | 2.7 ≤ $V_{DD}$ ≤ 3.6 | 2.2 | $V_{DD}$ + 0.3 | V |
| $V_{IL}$ (1) | Input LOW Voltage | 2.2 ≤ $V_{DD}$ < 2.7 | –0.3 | 0.6 | V |
| | | 2.7 ≤ $V_{DD}$ ≤ 3.6 | –0.3 | 0.8 | V |
| $I_{LI}$ | Input Leakage | GND < $V_{IN}$ < $V_{DD}$ | –1 | 1 | µA |
| $I_{LO}$ | Output Leakage | GND < $V_{IN}$ < $V_{DD}$, Output Disabled | –1 | 1 | µA |

Notes:
1. VILL(min) = -2.0V AC (pulse width < 10ns). Not 100% tested.
   VIHH (max) = VDD + 2.0V AC (pulse width < 10ns). Not 100% tested.

## IS62WV12816EALL DC ELECTRICAL CHARACTERISTICS-II FOR POWER (OVER THE OPERATING RANGE)

| Symbol | Parameter | Test Conditions | Grade | | 55ns | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Typ (1) | Max | |
| ICC | $V_{DD}$ Dynamic Operating Supply Current | $V_{DD}=V_{DD}(max)$, $I_{OUT}$=0mA, f = $f_{max}$<br>CS1# = $V_{IL}$, CS2 = $V_{IH}$ | Com. | | 10 | 15 | mA |
| | | | Ind. | | - | 18 | |
| ICC1 | $V_{DD}$ Static Operating Supply Current | $V_{DD}=V_{DD}(max)$, $I_{OUT}$ = 0mA, f=0<br>CS1# = $V_{IL}$, CS2 = $V_{IH}$ | Com. | | 1 | 3 | mA |
| | | | Ind. | | - | 3 | |
| ISB2 | CMOS Standby Current (CMOS Inputs) | $V_{DD}$ = $V_{DD}(max)$, f = 0,<br>CS1# ≥ $V_{DD}$ - 0.2V or<br>0V ≤ CS2 ≤ 0.2V or<br>LB# and UB# ≥ $V_{DD}$ - 0.2V<br>VIN ≤ 0.2V or VIN ≥ $V_{DD}$ - 0.2V | Com. | 25°C | 5.4 | 10 | µA |
| | | | | 45°C | 5.6 | 11 | |
| | | | | 70°C | 7.0 | 13 | |
| | | | Ind. | 85°C | 7.6 | 16 | |

Note:
1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at VDD = 1.8V

## IS62(5)WV12816EBLL DC ELECTRICAL CHARACTERISTICS-II FOR POWER (OVER THE OPERATING RANGE)

| Symbol | Parameter | Test Conditions | Grade | | 45/55ns | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Typ(1) | Max | |
| ICC | $V_{DD}$ Dynamic Operating Supply Current | $V_{DD}=V_{DD}(max)$, $I_{OUT}$=0mA, f = $f_{max}$<br>CS1# = $V_{IL}$, CS2 = $V_{IH}$ | Com. | | 10 | 15 | mA |
| | | | Ind. | | - | 18 | |
| | | | Auto. | | - | 25 | |
| ICC1 | $V_{DD}$ Static Operating Supply Current | $V_{DD}=V_{DD}(max)$, $I_{OUT}$ = 0mA, f=0<br>CS1# = $V_{IL}$, CS2 = $V_{IH}$ | Com. | | 1 | 3 | mA |
| | | | Ind. | | - | 3 | |
| | | | Auto. | | - | 4 | |
| ISB2 | CMOS Standby Current (CMOS Inputs) | $V_{DD}$ = $V_{DD}(max)$, f = 0,<br>CS1# ≥ $V_{DD}$ - 0.2V or<br>0V ≤ CS2 ≤ 0.2V or<br>LB# and UB# ≥ $V_{DD}$ - 0.2V<br>VIN ≤ 0.2V or VIN ≥ $V_{DD}$ - 0.2V | Com. | 25°C | 5.4 | 10 | µA |
| | | | | 45°C | 5.6 | 11 | |
| | | | | 70°C | 7.0 | 13 | |
| | | | Ind. | 85°C | 7.6 | 16 | |
| | | | Auto. | 125°C | 12.6 | 32 | |

Note:
1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at VDD = 3.0V

# AC CHARACTERISTICS [6] (OVER OPERATING RANGE)

## READ CYCLE AC CHARACTERISTICS

| Parameter | Symbol | 45ns | | 55ns | | unit | notes |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | |
| Read Cycle Time | tRC | 45 | - | 55 | - | ns | 1,5 |
| Address Access Time | tAA | - | 45 | - | 55 | ns | 1 |
| Output Hold Time | tOHA | 8 | - | 8 | - | ns | 1 |
| CS1#, CS2 Access Time | tACS1/tACS2 | - | 45 | - | 55 | ns | 1 |
| OE# Access Time | tDOE | - | 22 | - | 25 | ns | 1 |
| OE# to High-Z Output | tHZOE | - | 18 | - | 18 | ns | 2 |
| OE# to Low-Z Output | tLZOE | 5 | - | 5 | - | ns | 2 |
| CS1#, CS2 to High-Z Output | tHZCS/tHZCS2 | - | 18 | - | 18 | ns | 2 |
| CS1#, CS2 to Low-Z Output | tLZCS/tLZCS2 | 10 | - | 10 | - | ns | 2 |
| UB#, LB# Access Time | tBA | 45 | | 55 | | ns | 1,7 |
| UB#, LB# to High-Z Output | tHZB | - | 18 | - | 18 | ns | 2 |
| UB#, LB# to Low-Z Output | tLZB | 10 | - | 10 | - | ns | 2 |

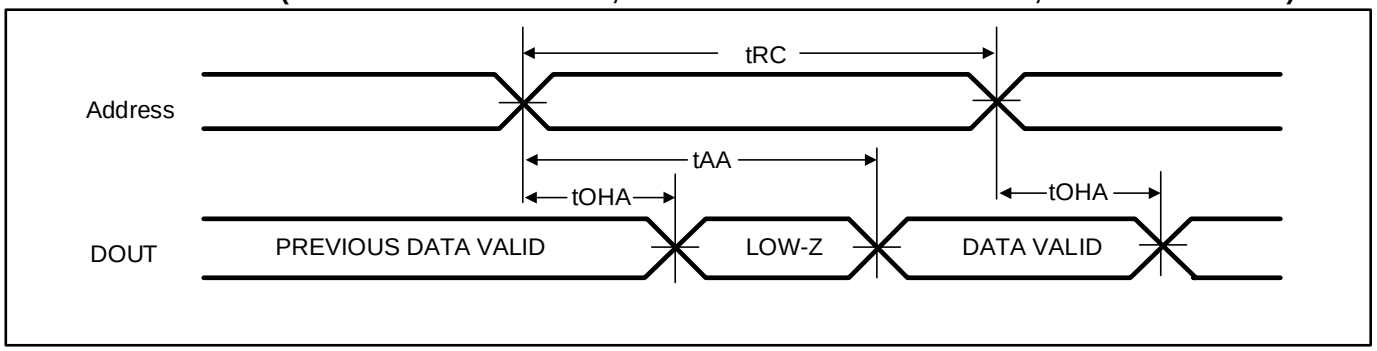
## WRITE CYCLE AC CHARACTERISTICS

| Parameter | Symbol | 45ns | | 55ns | | unit | notes |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | |
| Write Cycle Time | tWC | 45 | - | 55 | - | ns | 1,3,5 |
| CS1#, CS2 to Write End | tSCS1/tSCS2 | 35 | - | 40 | - | ns | 1,3 |
| Address Setup Time to Write End | tAW | 35 | - | 40 | - | ns | 1,3 |
| Address Hold from Write End | tHA | 0 | - | 0 | - | ns | 1,3 |
| Address Setup Time | tSA | 0 | - | 0 | - | ns | 1,3 |
| UB#,LB# to Write End | tPWB | 35 | - | 40 | - | ns | 1,3 |
| WE# Pulse Width | tPWE | 35 | - | 40 | - | ns | 1,3,4 |
| Data Setup to Write End | tSD | 28 | - | 28 | - | ns | 1,3 |
| Data Hold from Write End | tHD | 0 | - | 0 | - | ns | 1,3 |
| WE# LOW to High-Z Output | tHZWE | - | 18 | - | 18 | ns | 2,3 |
| WE# HIGH to Low-Z Output | tLZWE | 10 | - | 10 | - | ns | 2,3 |

Notes:
1. Tested with the load in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. tHZOE, tHZCS, tHZB, and tHZWE transitions are measured when the output enters a high impedance state. Not 100% tested.
3. The internal write time is defined by the overlap of CS1# = LOW, CS2=HIGH, UB# or LB# = LOW, and WE# = LOW. All four conditions must be in valid states to initiate a Write, but any condition can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
4. tPWE > tHZWE + tSD when OE# is LOW.
5. Address inputs must meet $V_{IH}$ and $V_{IL}$ SPEC during this period. Any glitch or unknown inputs are not permitted. Unknown input with standby mode is acceptable.
6. Data retention characteristics are defined later in DATA RETENTION CHARACTERISTICS.

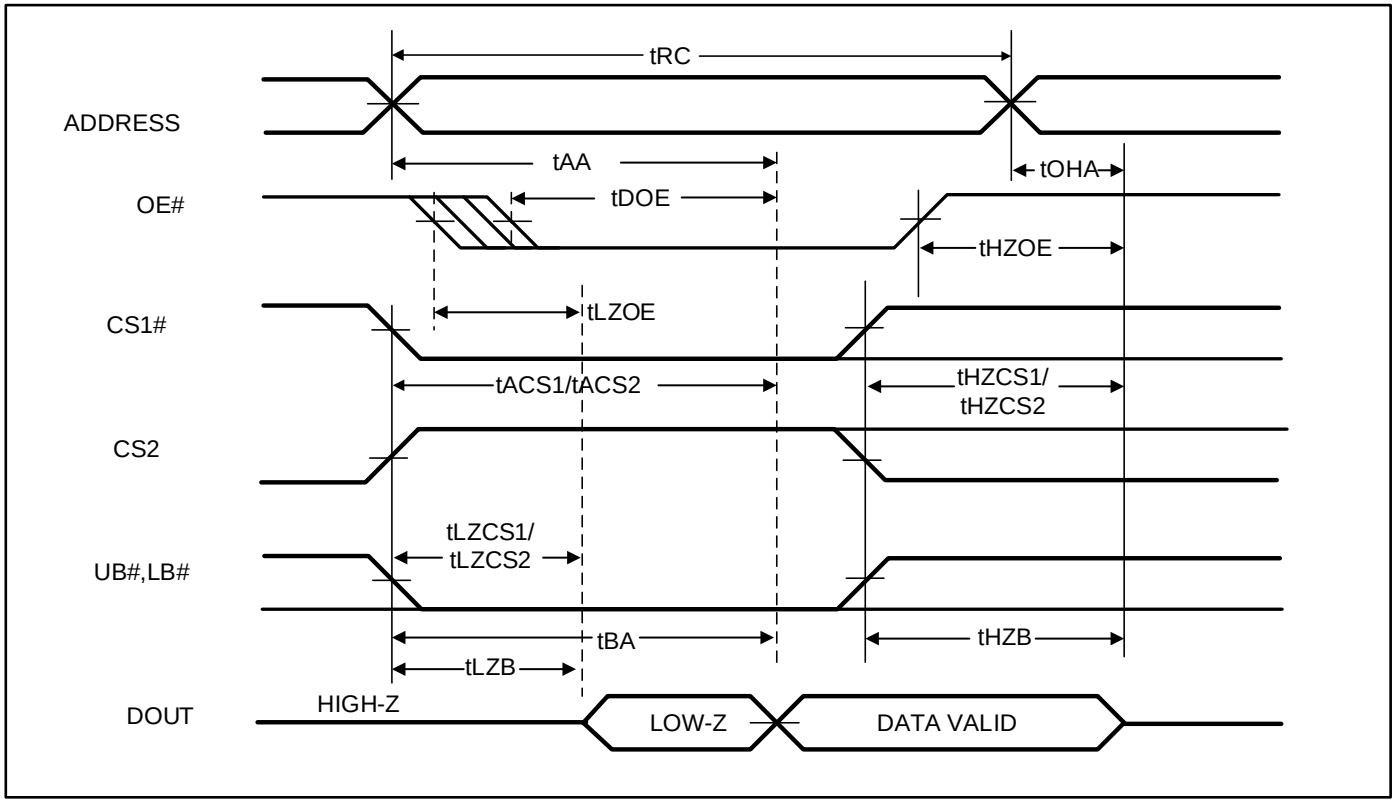
# TIMING DIAGRAM

### READ CYCLE NO. 1[1] (ADDRESS CONTROLLED, CS1# = OE# = UB# = LB# = LOW, CS2 = WE# = HIGH)



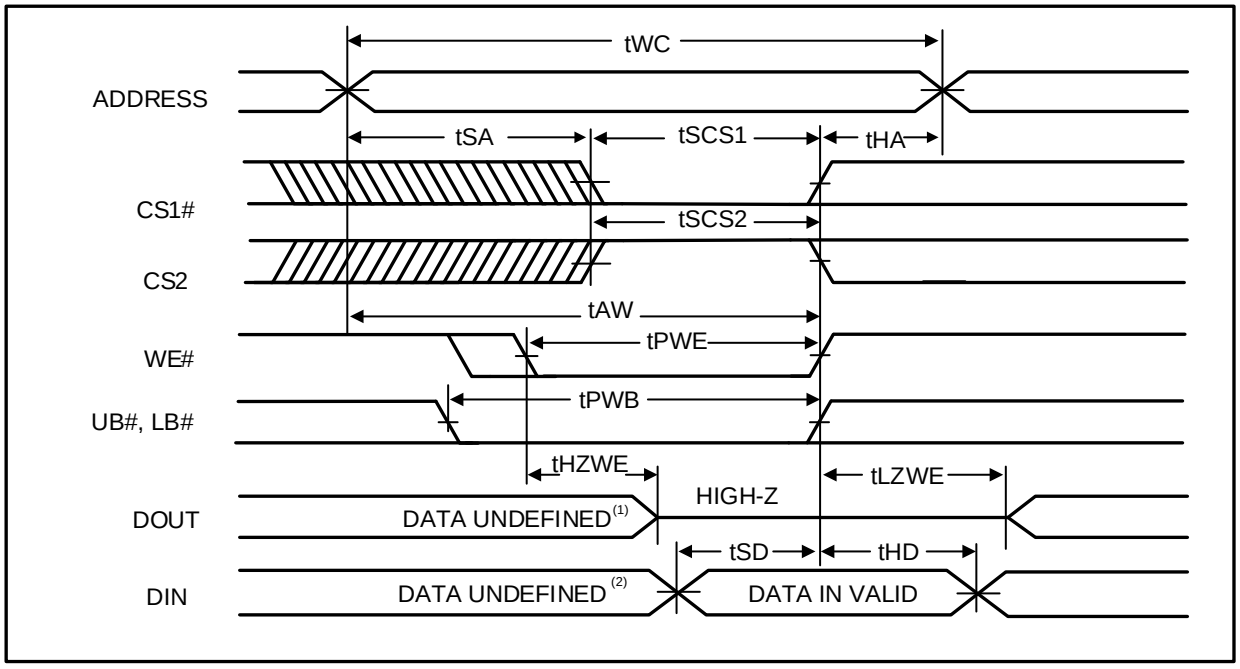

Note:
1. The device is continuously selected.

### READ CYCLE NO.2 [1] (OE# CONTROLLED)



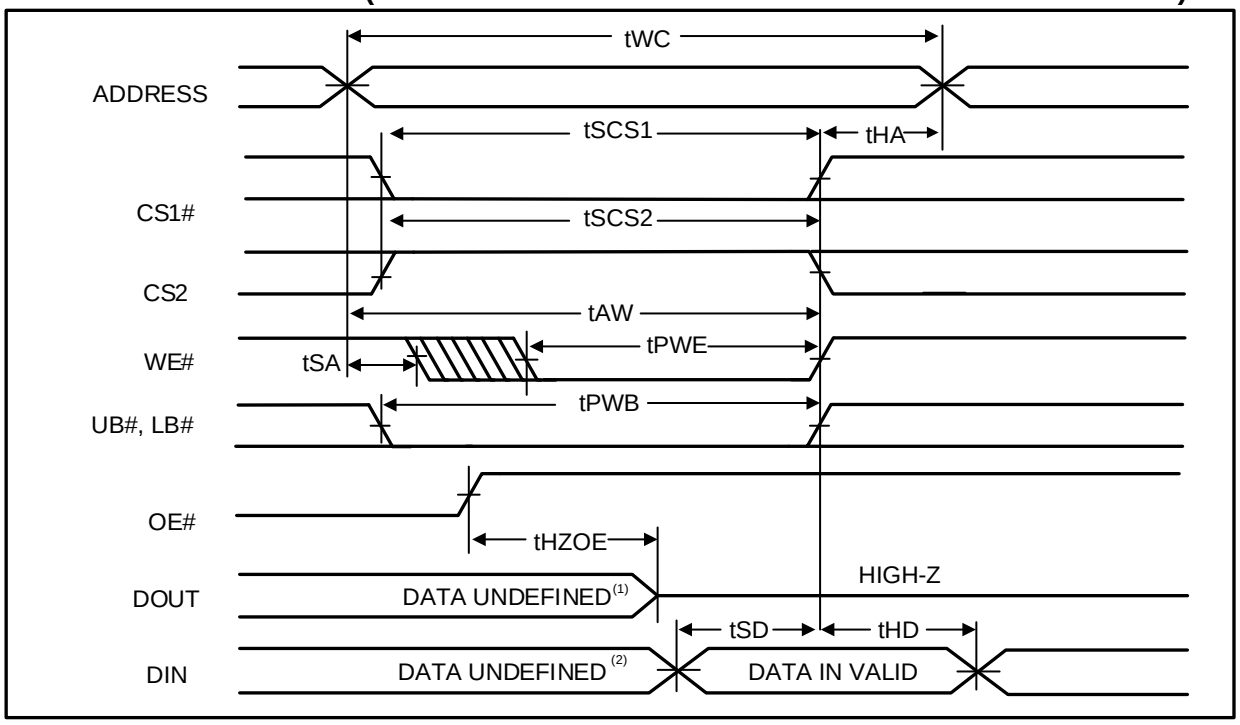

Note:
1. Address is valid prior to or coincident with CS1# LOW or CS2 HIGH transition.

## WRITE CYCLE NO.1 [1, 2] (CS1# , CS2 Controlled, OE# = HIGH or LOW)



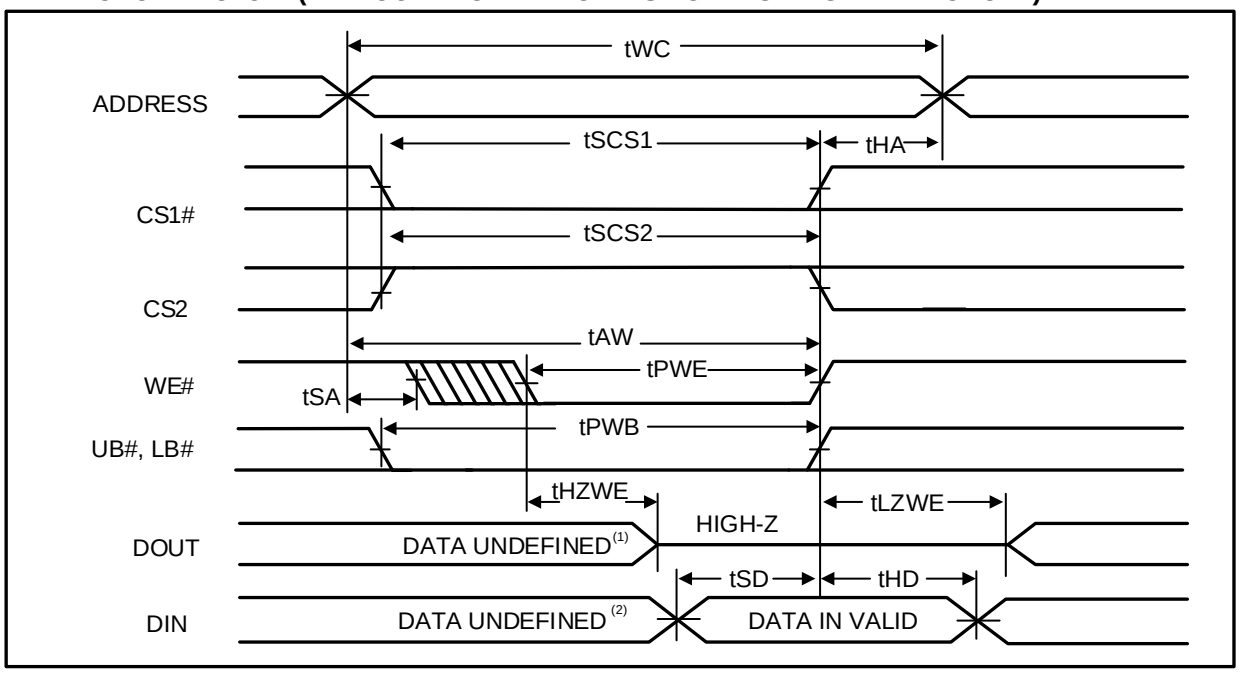

Notes:
1. tHZWE is based on the assumption when tSA=0nS after READ operation. Actual DOUT for tHZWE may not appear if OE# goes high before Write Cycle. tHZOE is the time DOUT goes to High-Z after OE# goes high.
2. During this period, the I/Os are in output state. Do not apply input signals.

## WRITE CYCLE NO. 2 [1, 2] (WE# CONTROLLED: OE# IS HIGH DURING WRITE CYCLE)



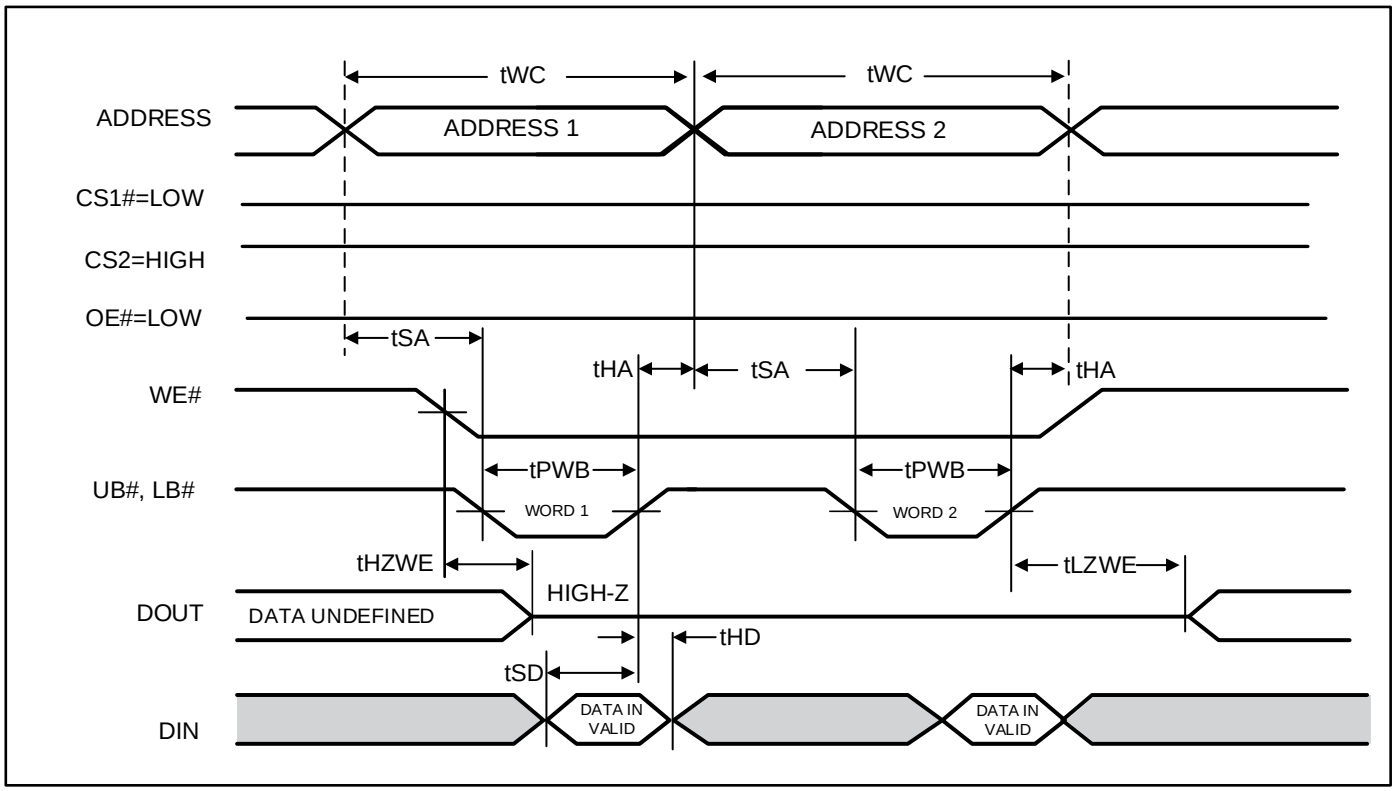

Notes:
1. tHZOE is the time DOUT goes to High-Z after OE# goes high.
2. During this period, the I/Os are in output state. Do not apply input signals.

## WRITE CYCLE NO. 3 [1] (WE# CONTROLLED: OE# IS LOW DURING WRITE CYCLE)




Notes:
3. If OE# is low during write cycle, tHZWE must be met in the application. Do not apply input signal during this period. Data output from the previous READ operation will drive IO BUS.

**WRITE CYCLE NO. 4 [1, 2, 3] (UB# & LB# Controlled, OE# = LOW)**



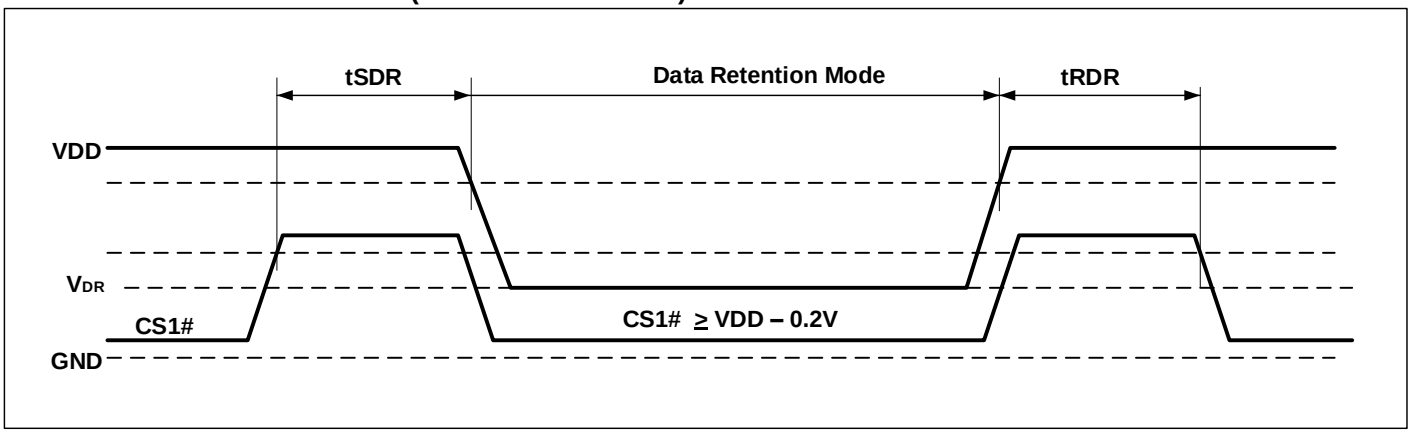

Notes:
1. If OE# is low during write cycle, tHZWE must be met in the application. Do not apply input signal during this period. Data output from the previous READ operation will drive IO BUS.
2. Due to the restriction of note1, OE# is recommended to be HIGH during write period.
3. WE# stays LOW in this example. If WE# toggles, tPWE and tHZWE must be considered.

## DATA RETENTION CHARACTERISTICS

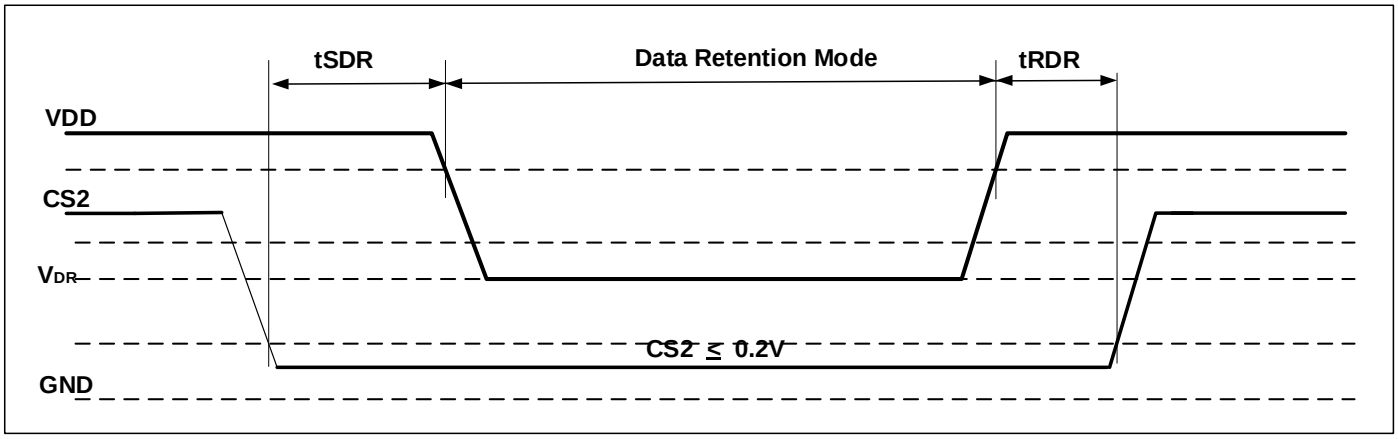
| Symbol | Parameter | Test Condition | OPTION | Min | Typ(2) | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DR}$ | $V_{DD}$ for Data Retention | See Data Retention Waveform | | 1.5 | - | 3.6 | V |
| $I_{DR}$ | Data Retention Current | $V_{DD}$= $V_{DR}$(min), CS1# ≥ $V_{DD}$ – 0.2V,(1) or 0V ≤ CS2 ≤ 0.2V, or LB# and UB# ≥ $V_{DD}$ -0.2V, VIN ≤ 0.2V or VIN ≥ $V_{DD}$ - 0.2V | Com. | - | 5.4 | 13 | uA |
| | | | Ind. | - | | 16 | |
| | | | Auto A3 | - | | 32 | |
| $t_{SDR}$ | Data Retention Setup Time | See Data Retention Waveform | | 0 | - | - | ns |
| $t_{RDR}$ | Recovery Time | See Data Retention Waveform | | tRC | - | - | ns |

Notes:
1. If CS1# >VDD–0.2V, all other inputs including CS2 and UB# and LB# must meet this condition.
2. Typical values are measured at VDD=1.8V or 3V, $T_A$ = 25°C, and not 100% tested.

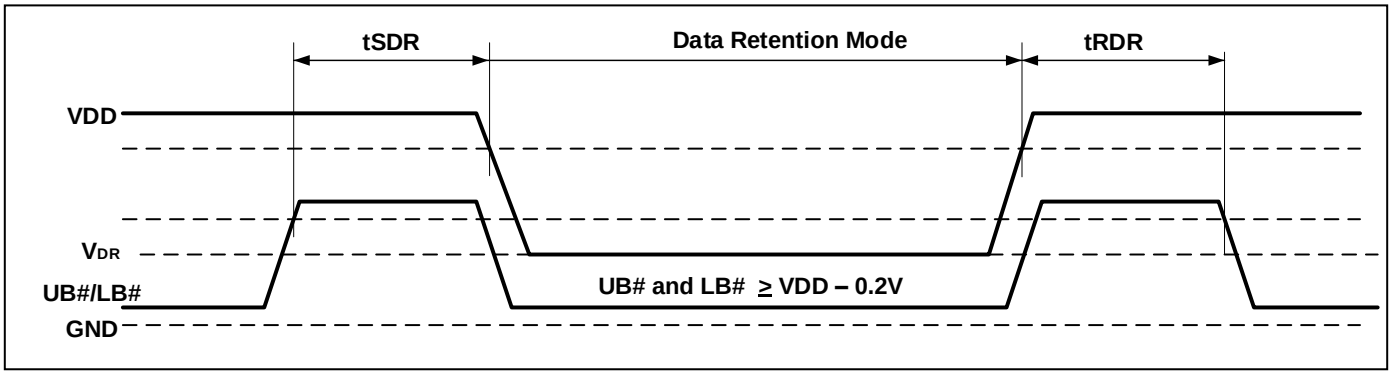
### DATA RETENTION WAVEFORM (CS1# CONTROLLED)




### DATA RETENTION WAVEFORM (CS2 CONTROLLED)



## DATA RETENTION WAVEFORM (UB# AND LB# CONTROLLED)




**Note:**
1. CS2 must satisfy either CS2 ≥ VDD -0.2V or CS2 ≤ 0.2V
2. CS1# must satisfy either CS1# ≥ VDD - 0.2V or CS1# ≤ 0.2V

# ORDERING INFORMATION

## IS62WV12816EALL (1.65V - 2.2V)
## Industrial Range: –40°C to +85°C

| Speed (ns) | Order Part No. | Package |
|---|---|---|
| 55 | IS62WV12816EALL-55TI | TSOP (Type II) |
| | IS62WV12816EALL-55BI | mini BGA (6mm x 8mm) |
| | IS62WV12816EALL-55B2I | mini BGA (6mm x 8mm), 2 CS Option |
| | IS62WV12816EALL-55BLI | mini BGA (6mm x 8mm), Lead-free |

## IS62WV12816EBLL (2.2V - 3.6V)

## Industrial Range: –40°C to +85°C

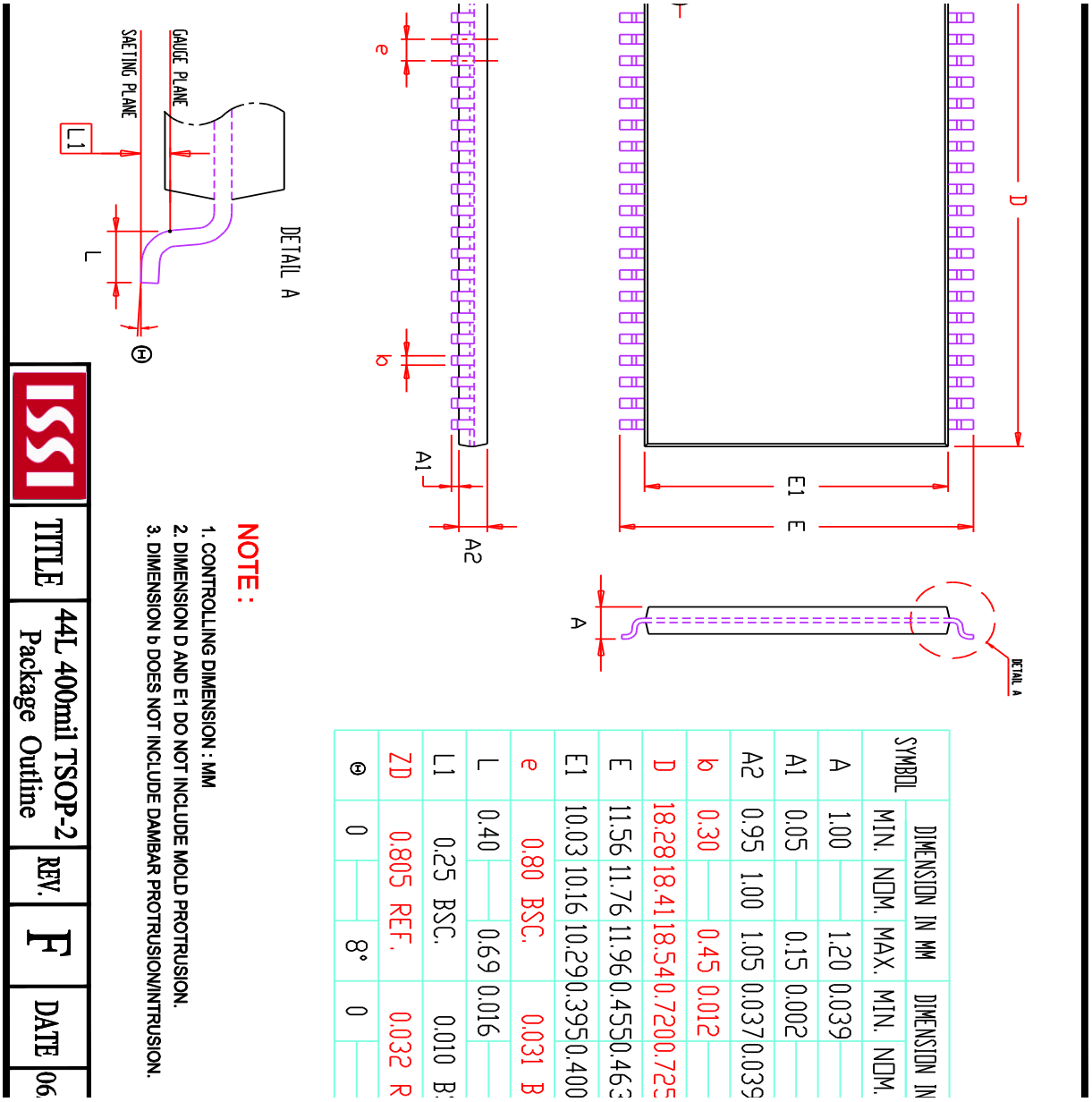
| Speed (ns) | Order Part No. | Package |
|---|---|---|
| 45 | IS62WV12816EBLL-45TLI | TSOP (Type II), Lead-free |
| | IS62WV12816EBLL-45BLI | mini BGA (6mm x 8mm), Lead-free |
| | IS62WV12816EBLL-45B2LI | mini BGA (6mm x 8mm), 2 CS Option, Lead-free |
| 55 | IS62WV12816EBLL-55TI | TSOP (Type II) |
| | IS62WV12816EBLL-55TLI | TSOP (Type II), Lead-free |
| | IS62WV12816EBLL-55BI | mini BGA (6mm x 8mm) |
| | IS62WV12816EBLL-55BLI | mini BGA (6mm x 8mm), Lead-free |
| | IS62WV12816EBLL-55B2I | mini BGA (6mm x 8mm), 2 CS Option |
| | IS62WV12816EBLL-55B2LI | mini BGA (6mm x 8mm), 2 CS Option, Lead-free |

## IS65WV12816EBLL (2.2V - 3.6V)

## Automotive Range (A3): –40°C to +125°C

| Speed (ns) | Order Part No. | Package |
|---|---|---|
| 55 | IS65WV12816EBLL-55CTLA3 | TSOP (Type II), Lead-free, Copper Leadframe |
| | IS65WV12816EBLL-55BLA3 | mini BGA (6mm x 8mm), Lead-free |

## PACKAGE INFORMATION

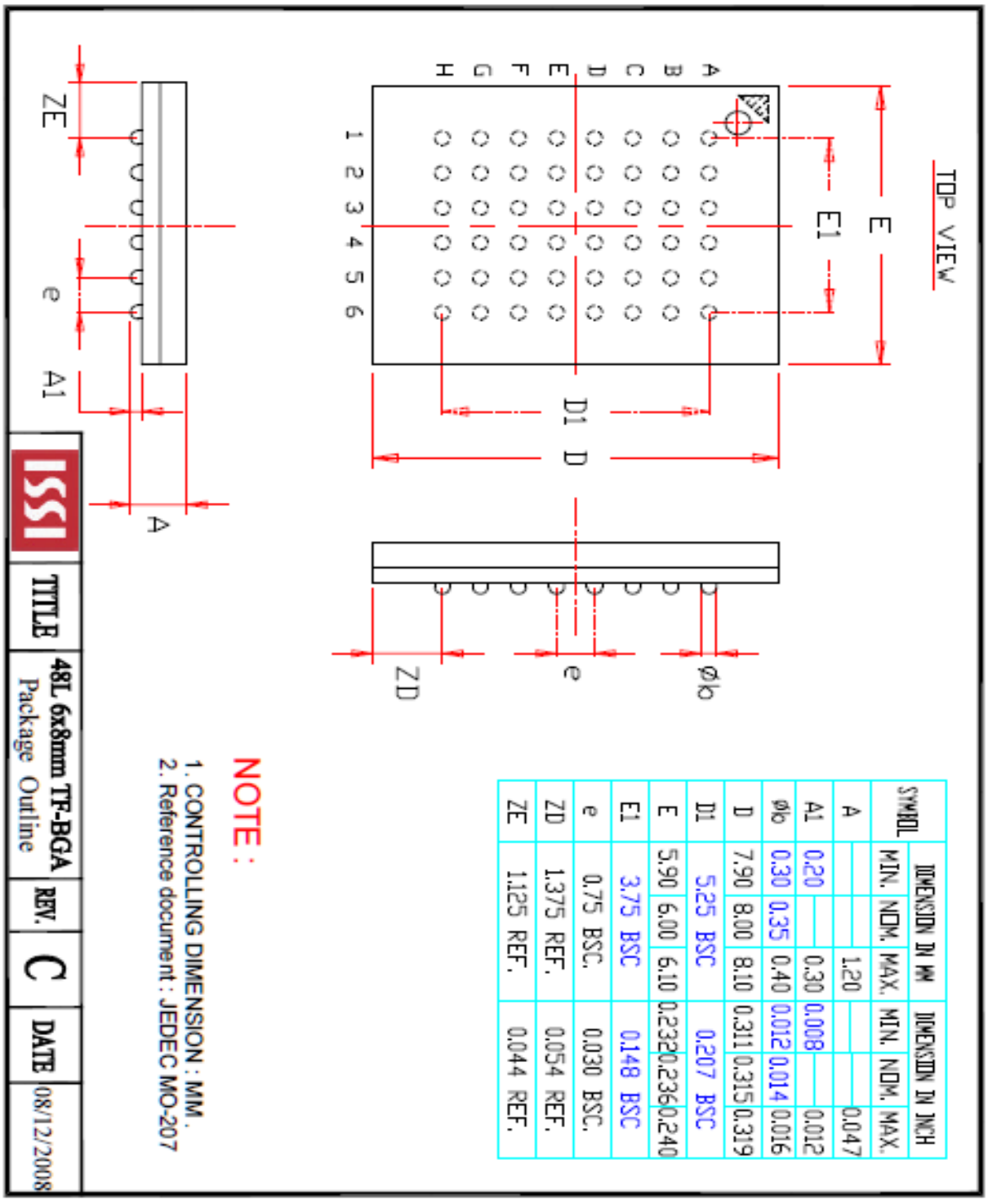



| SYMBOL | DIMENSION IN MM | | | DIMENSION IN |
|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. NOM. |
| A | 1.00 | — | 1.20 | 0.039 — — |
| A1 | 0.05 | — | 0.15 | 0.002 — — |
| A2 | 0.95 | 1.00 | 1.05 | 0.037 0.039 |
| b | 0.30 | — | 0.45 | 0.012 — — |
| D | 18.28 | 18.41 | 18.54 | 0.720 0.725 |
| E | 11.56 | 11.76 | 11.96 | 0.455 0.463 |
| E1 | 10.03 | 10.16 | 10.29 | 0.395 0.400 |
| e | 0.80 BSC. | | | 0.031 B |
| L | 0.40 | — | 0.69 | 0.016 — |
| L1 | 0.25 BSC. | | | 0.010 B |
| ZD | 0.805 REF. | | | 0.032 R |
| θ | 0 | — | 8° | 0 — |

**NOTE :**

1. CONTROLLING DIMENSION : MM
2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.

| | | | | |
|---|---|---|---|---|
| ISSI | TITLE | 44L 400mil TSOP-2 Package Outline | REV. F | DATE 06 |




| SYMBOL | DIMENSION IN MM | | | DIMENSION IN INCH | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | | | 1.20 | | | 0.047 |
| A1 | 0.20 | | 0.30 | 0.008 | | 0.012 |
| øb | 0.30 | 0.35 | 0.40 | 0.012 | 0.014 | 0.016 |
| D | 7.90 | 8.00 | 8.10 | 0.311 | 0.315 | 0.319 |
| D1 | | 5.25 BSC | | | 0.207 BSC | |
| E | 5.90 | 6.00 | 6.10 | 0.232 | 0.236 | 0.240 |
| E1 | | 3.75 BSC | | | 0.148 BSC | |
| e | | 0.75 BSC. | | | 0.030 BSC. | |
| ZD | | 1.375 REF. | | | 0.054 REF. | |
| ZE | | 1.125 REF. | | | 0.044 REF. | |

LifeElectronics
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