

### DESCRIPTION

The MP8051 is a high-efficiency, monolithic, switching bridge regulator with two self-driven integrated N-MOSFETs and two Schottky diodes. It provides 1A continuous output current over a wide input supply range.

The MP8051 is available in a very compact 3mmx3mm Flip-Chip QFN package that measures 0.45mm high.

### FEATURES

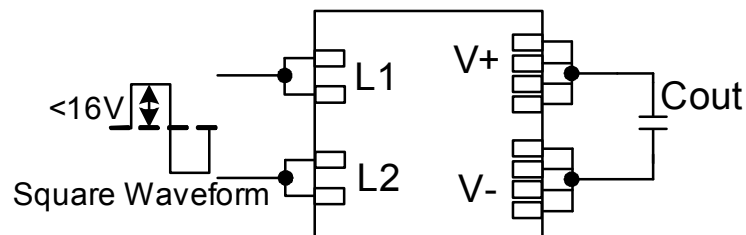
- 0.4V Low Forward-Voltage Drop
- 1A Output Current
- High Reliability
- Only 1 $\mu$ A Reverse Leakage Current
- Very Low Profile (0.45mm)
- Ideal for Printed Circuit Boards

### APPLICATIONS

- DC Transformer
- Wireless Charger
- Low Voltage AC and Industrial Systems

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### TYPICAL APPLICATION

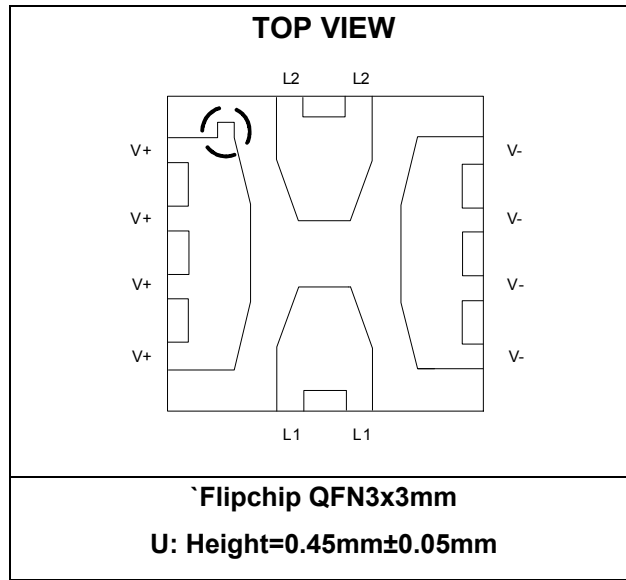


## ORDERING INFORMATION

Part Number*	Package	Top Marking	Junction Temperature (T <sub>J</sub> )
MP8051DQU	Flipchip QFN3x3	ABE	-40°C to +125°C

\* For Tape & Reel, add suffix -Z (e.g. MP8051DQU -Z);  
 For RoHS, compliant packaging, add suffix -LF (e.g. MP8051DQU-LF-Z).

## PACKAGE REFERENCE



### ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>

V <sub>L1, L2</sub> to V-	-1.0V to +23V
V+ to V-	-0.3V to +23V
Lead Temperature	260°C
Continuous Power Dissipation (T <sub>A</sub> = 25°C) <sup>(2)</sup>	0.75W
Storage Temperature	-55°C to +150°C

### ESD SUSCEPTIBILITY <sup>(3)</sup>

HBM (Human Body Mode)	2kV
MM (Machine Mode)	200V

### Recommended Operating Conditions <sup>(4)</sup>

Supply Voltage (V <sub>L1, L2</sub> )	4 to 16 V
Output Voltage (V+ to V-)	16 V
Maximum Junction Temp. (T <sub>J</sub> )	125°C

Thermal Resistance <sup>(5)</sup>	θ <sub>JA</sub>	θ <sub>JC</sub>
Flip-Chip QFN3x3	60	12... °C/W

**Notes:**

- 1) Exceeding these ratings may damage the device.
- 2) The maximum allowable power dissipation depends on the schottky's thermal run away point, the junction-to-ambient thermal resistance θ<sub>JA</sub>, and the ambient temperature T<sub>A</sub>. The maximum allowable continuous power dissipation is different at different ambient temperature. Exceeding the maximum allowable power dissipation will cause excessive die temperature and permanent damage. Please refer to the derating operation curve in TYPICAL PERFORMANCE CHARACTERISTICS.
- 3) Devices are ESD sensitive. Handling precaution recommended.
- 4) The device is not guaranteed to function outside of its operating conditions.
- 5) Measured on JESD51-7, 4-layer PCB.

## ELECTRICAL CHARACTERISTICS <sup>(6)</sup>

T<sub>A</sub> = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Total Reverse Leakage Current	I <sub>REVERSE</sub>	Short L1 and L2, V <sub>+</sub> - V <sub>-</sub> =6.5V		1		μA
<b>Diode Specification</b>						
Reverse Breakdown Voltage	V <sub>BR</sub>	L1=L2=V <sub>-</sub> , I <sub>V+</sub> = 1mA	-23			V
Reverse Leakage Current	I <sub>LEAKAGE</sub>	L1=L2=V <sub>-</sub> , V <sub>+</sub> - V <sub>-</sub> =16V		80		μA
Forward Voltage	V <sub>F</sub>	@ I <sub>F</sub> =1A		0.4	0.46	V
Diode Junction Capacitance <sup>(6)</sup>	C <sub>Diode</sub>	V <sub>+</sub> to L1/L2=2V, f=1MHz		455		pF
Reverse Recovery Time	t <sub>rr</sub>	V <sub>R</sub> =16V, I <sub>FM</sub> =1A		78.5		ns
<b>MOSFET Specification</b>						
Breakdown Voltage	V <sub>DS</sub>		23			V
Conduction Resistance	R <sub>ON</sub>	Voltage difference between L1 and L2 is 6.5V (V <sub>GS</sub> =5V)		45	70	mΩ
Turn On Time <sup>(6)</sup>	t <sub>Rise</sub>	L1, L2 to (V-) = 5V		25		ns
Turn Off Time <sup>(6)</sup>	t <sub>Fall</sub>	L1, L2 to (V-) = 5V		25		ns

**Notes:**

6) Guaranteed by design.

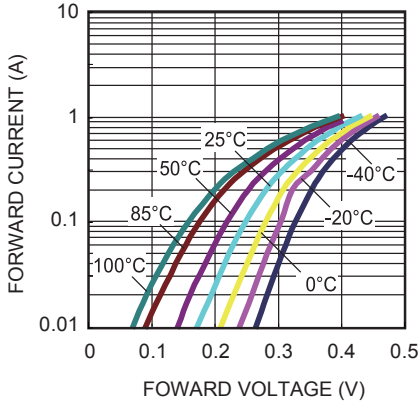
## PIN FUNCTIONS

Pin #	Name	Description
1,2,3,4	V+	Rectifier Positive Output
5,6	L1	Power Input
7,8,9,10	V-	Rectifier Negative Output
11,12	L2	Power Input

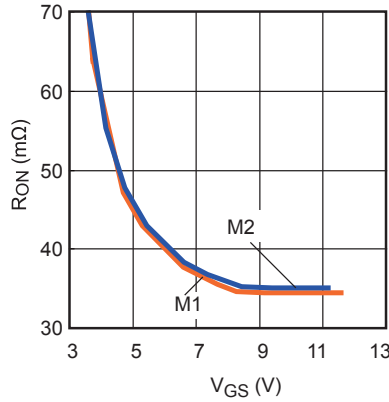
## TYPICAL PERFORMANCE CHARACTERISTICS

Square waveform input to L1 & L2,  $V_{L1, L2} = 5V$ ,  $C_{OUT} = 10\mu F$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

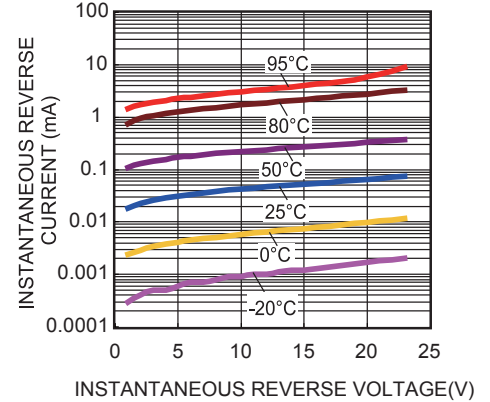
Diode - Conduction



MOSFET - Conduction



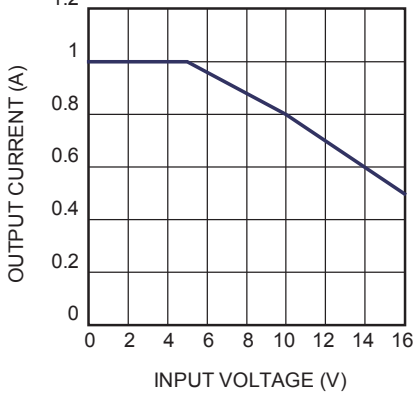
Schottky Reverse Voltage vs. Current



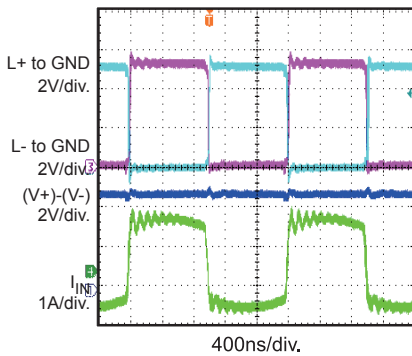
Derating Operation

$T_A = 85^\circ C$

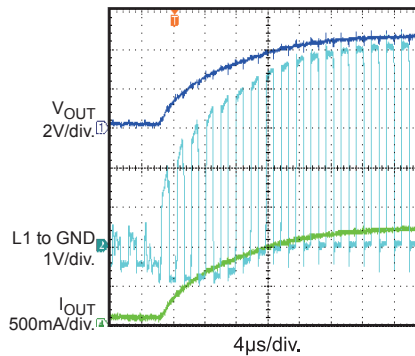
The input square waveform is  $>200kHz$



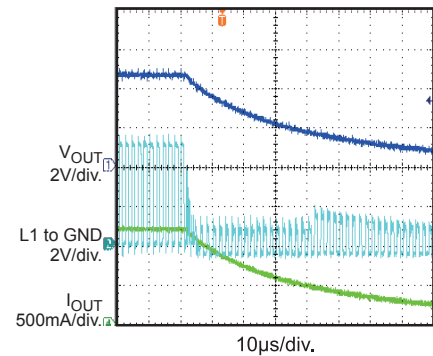
Steady State of Low Side MOSFET Operation at Load=1A



Startup at Load=1A



Shutdown at Load=1A



**FUNCTIONAL BLOCK DIAGRAM**

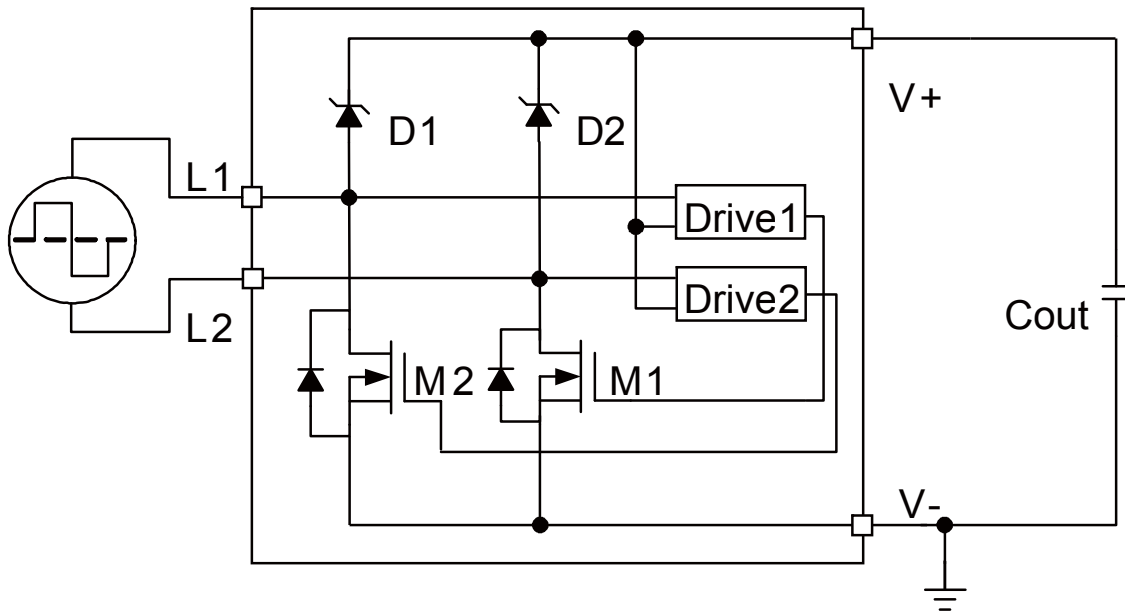


Figure 1—Functional Block Diagram

## OPERATION

The MP8051 is a monolithic switch bridge regulator to regulate the input square waveform to the DC output.

Compared against conventional 4-diode silicon bridge regulators, the two integrated MOSFETs reduce power loss by implementing soft switching. These two MOSFETs (M1 and M2) are driven from the input signals (refer to Figure1).

The MP8051 takes a square wave input. When L1 initially receives the positive input and L2 the negative input, current initially flows through the

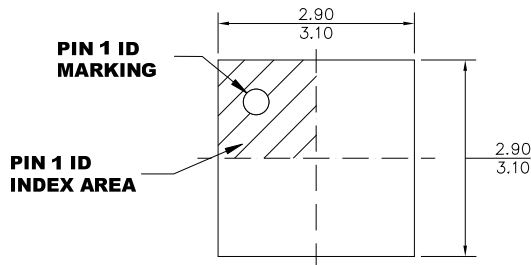
M1 parasitic diode, D1. Then Drive1 generates the turn on signal for the rest of the device.

When the square wave signal inverts, the Drive1 turns off M1 while D1 continues to conduct for soft switching. Then D2, M2, and Drive2 follow the same process.

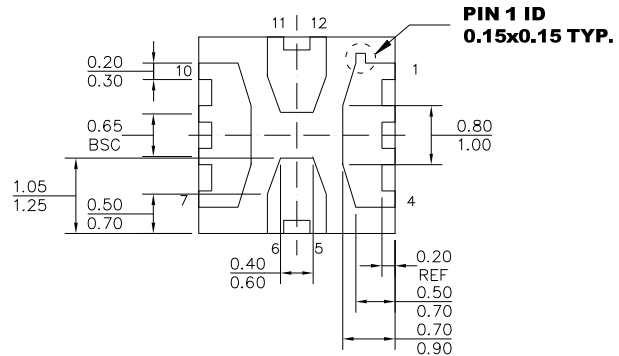
Both Drive1 and Drive2 clamp the driving signals of the two low-side MOSFETs below 6.5V when the voltage difference between L1 and L2 exceeds 6.5V.

## PACKAGE INFORMATION

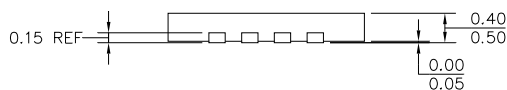
### THE 0.45mm HEIGHT 3X3 FLIP CHIP QFN



**TOP VIEW**



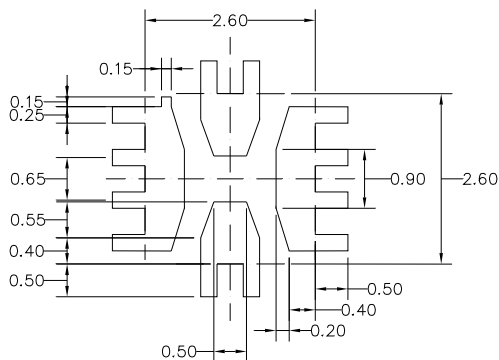
**BOTTOM VIEW**



**SIDE VIEW**

**NOTE:**

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
- 3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
- 4) JEDEC REFERENCE IS MO-220.
- 5) DRAWING IS NOT TO SCALE.



**RECOMMENDED LAND PATTERN**

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