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# FSA880 / FSA881 – USB Port 2:1 Switch with Accessory and Charger Detection

## Features

Switch Type	2:1 USB
Switch Mechanism	Automatic switching with Available Interrupt
Accessory Detection	USB Data Cable Chargers (CDP, DCP, Travel Adapter, Car Kit-CEA-936-A) Factory-Mode Cables
USB	FS and HS 2.0 Compliant
USB Charging	Battery Charging 1.1 Compliant Charger Detect, DCD, OVT (28 V)
UART	RxD and TxD
VBAT	3.0 to 4.4 V
Programmability	I <sup>2</sup> C
ESD	15kV IEC 61000-4-2 Air Gap
Operating Temperature	-40°C to 85°C
Package	16-Lead UMLP 1.8x2.6x0.55 mm, 0.4 mm Pitch
JIG Option	FSA880 – Active LOW FSA881 – Active HIGH
Ordering Information	FSA880UMX FSA881UMX

## Description

The FSA88x is a high-performance switch featuring automatic switching and accessory detection for a USB port. The FSA88x allows sharing of a common USB port to pass USB data, as well as factory programmability. In addition, the FSA88x integrates accessory detection of devices such as USB chargers and factory data cables. The FSA88x can be programmed for manual switching or automatic switching of data paths. VBUS\_IN has 28 V over-voltage tolerance.

The difference between the FSA880 and the FSA881 is that FSA880 JIG output is an open-drain, active-LOW output, while FSA881 JIG is an active-HIGH, CMOS output.

## Applications

- Cellular Phones, Smart Phones
- MP3 and PMP

## Related Resources

- FSA880 / FSA881 Demonstration Board

## Typical Application

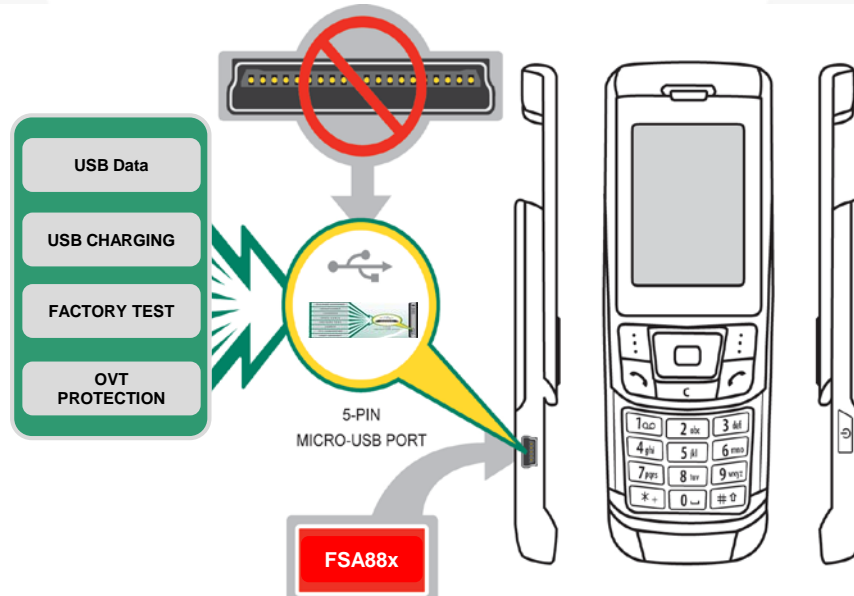


Figure 1. Mobile Phone Example

### Ordering Information

Part Number	Operating Temperature Range	Top Mark	Package
FSA880UMX	-40 to +85°C	KU	16-Lead, Ultrathin Molded Leadless Package (UMLP), 1.8 mm x 2.6 mm x 0.55 mm, 0.4 mm Pitch
FSA881UMX	-40 to +85°C	KX	16-Lead, Ultrathin Molded Leadless Package (UMLP), 1.8 mm x 2.6 mm x 0.55 mm, 0.4 mm Pitch

### Block Diagram

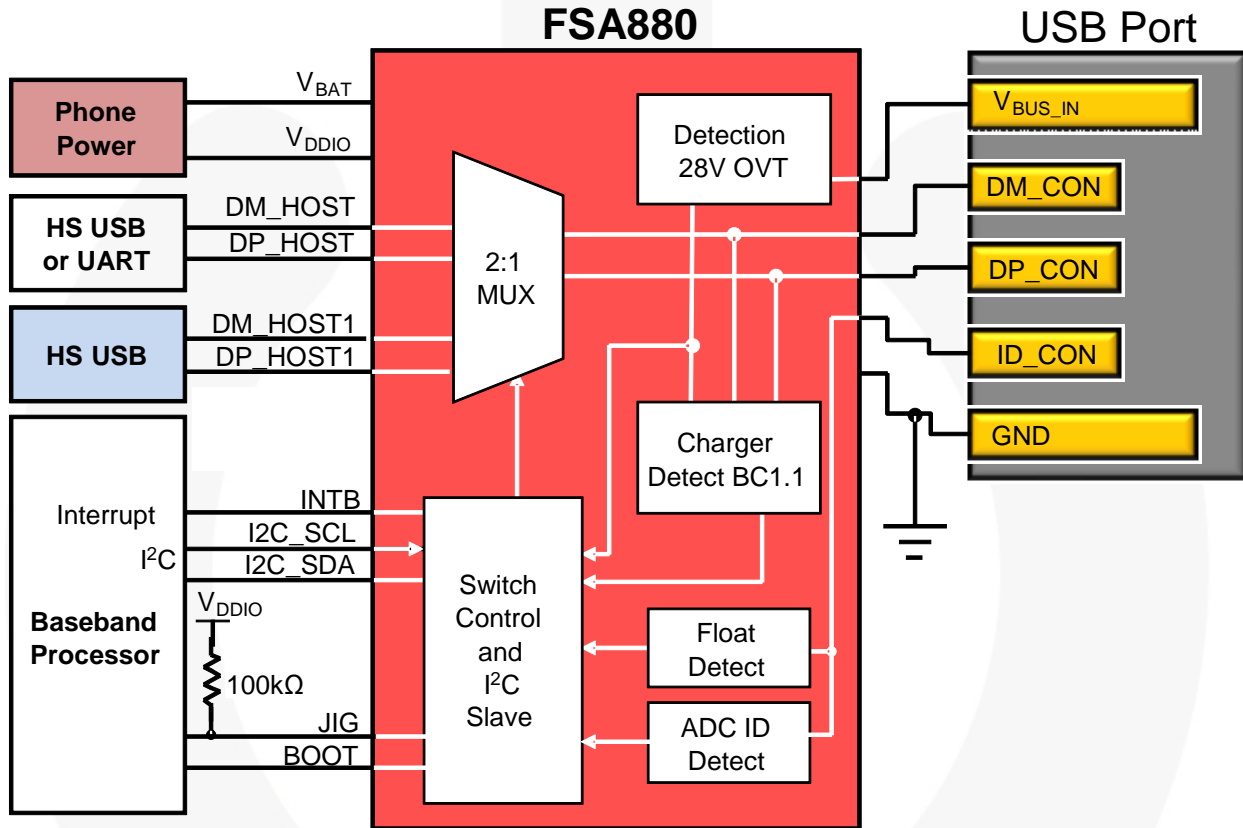


Figure 2. Block Diagram



## Pin Configuration

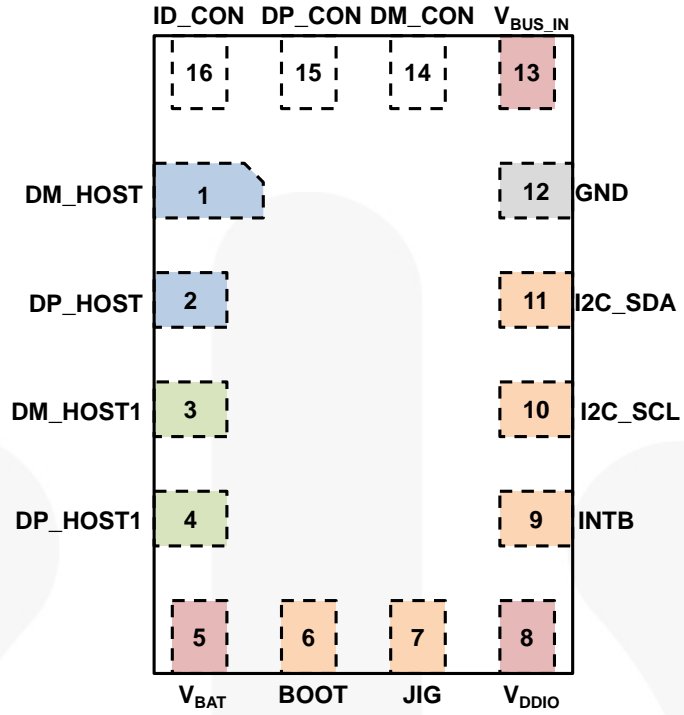


Figure 3. Pin Assignment (Through View)



## Pin Descriptions

Name	Pin #	Type	Default State	Description
<b>USB/UART Interface</b>				
DP_HOST	2	Signal Path	Open	D+ signal switch path, dedicated USB port to be connected to the resident USB / UART on the phone. Default port for all USB accessories and USB factory modes.
DM_HOST	1	Signal Path	Open	D- signal switch path, dedicated USB port to be connected to the resident USB / UART on the phone. Default port for all USB accessories and USB factory modes.
V <sub>BUS_IN</sub>	13	Input	N/A	Input voltage supply pin to be connected to the VBUS pin of the USB connector
<b>USB/UART Interface 1</b>				
DM_HOST1	3	Signal Path	Open	D- signal switch path, dedicated USB port to be connected to the secondary resident USB / UART on the phone. Default port for UART factory modes.
DP_HOST1	4	Signal Path	Open	D+ signal switch path, dedicated USB port to be connected to the secondary resident USB / UART on the phone. Default port for UART factory modes.
<b>Connector Interface</b>				
GND	12	Ground	N/A	Ground
ID_CON	16	Signal Path	Open	Connected to the USB connector ID pin and used for detecting accessories
DP_CON	15	Signal Path	Open	Connected to the USB connector D+ pin; depending on the signaling mode, this pin can be switched to DP_HOST or RxD_HOST pins.
DM_CON	14	Signal Path	Open	Connected to the USB connector D- pin; depending on the signaling mode, this pin can be switched to DM_HOST or TxD_HOST pins.
<b>Power Interface</b>				
V <sub>DDIO</sub>	8	Power	N/A	Input baseband interface I/O supply pin
V <sub>BAT</sub>	5	Power	N/A	Input voltage supply pin to be connected to the mobile phone battery output or to an internal regulator on the phone
<b>Factory Interface</b>				
JIG	7	FSA880: Open-Drain Output FSA881: CMOS Output	FSA880: Hi-Z FSA881: LOW	Output control signal and used by the processor for factory test modes FSA880: Active LOW open-drain output FSA881: Active HIGH CMOS output
BOOT	6	CMOS Output	LOW	Output control signal and used by the processor for factory test modes
<b>I<sup>2</sup>C Interface</b>				
I2C_SCL	10	Input	Hi-Z	I <sup>2</sup> C serial clock signal to be connected to the phone-based I <sup>2</sup> C master
I2C_SDA	11	Open-Drain I/O	Hi-Z	I <sup>2</sup> C serial data signal to be connected to the phone-based I <sup>2</sup> C master
INTB	9	CMOS Output	LOW	Interrupt active LOW output used to prompt the phone baseband processor to read the I <sup>2</sup> C register bits, indicate a change in ID_CON pin status or accessories' attach status

### Note:

1. LOW = V<sub>OL</sub> or V<sub>IL</sub>; HIGH = V<sub>OH</sub> or V<sub>IH</sub>.

# 1. Functionality

The FSA88x is USB port accessory detector and switch with integrated 28 V over-voltage tolerance. Fully controlled using I<sup>2</sup>C, FSA88x enables high-speed USB 2.0 Standard Downstream Port (SDP), USB Charging Downstream Port (CDP) battery charger, USB Dedicated Charging Port (DCP) charger data cables to use a common connector micro or mini USB 2.0 port. Factory-mode cables can be detected and switched to use either the UART or USB data path. The FSA88x can be programmed for manual switching or automatic switching of data paths.

The architecture uses ID pin detection for convenient factory testing. Figure 9 - Figure 13 show the FSA88x passing the USB eye compliance test with ample margin.

## 1.1. Functional Overview

The FSA88x is designed for minimal software requirements for proper operation. The flow diagram in Figure 4 walks through the fundamental steps of operation and contains references to more detailed information.

Flow Diagram	State	Datasheet Section	Description
<pre> graph TD     A[Power-up &amp; Reset] --&gt; B[I2C]     B --&gt; C[Configuration]     C --&gt; D[Accessory Plug-in]     D --&gt; E[Detection]     E --&gt; F[Processor Communication]     F --&gt; G[Switch Configuration]     G --&gt; H[Active Signals]     H --&gt; I[Accessory Detached]     I --&gt; D                     </pre>	<b>Power-Up &amp; Reset</b>	<i>Section 2</i>	Applies power to the device and resets state of the device
	<b>I<sup>2</sup>C</b>	<i>Section 3</i>	Communication with device through I <sup>2</sup> C
	<b>Configuration</b>	<i>Section 4</i>	Configures the device using I <sup>2</sup> C and the internal registers (which can be bypassed during power-up)
	<b>Detection</b>	<i>Section 5</i>	Manages accessory detection, including attachment and detachment
	<b>Processor Communication</b>	<i>Section 6</i>	How the detection of the accessory is indicated to the processor
	<b>Switch Configuration</b>	<i>Section 7</i>	Configuration of switches based on detection
	<b>Active Signal</b>	<i>Section 8</i>	Signal performance of selected configuration

Figure 4. Basic Operation Flow

## 2. Power-Up & Reset

The FSA88x does not need special power sequencing for correct operation. The main power is provided by  $V_{BAT}$  only.  $V_{DDIO}$  is only used for I<sup>2</sup>C interface and interrupt processing.

Table 1 summarizes the enabled features of each power state. The valid voltages levels for each power supply can be found in Section 9.

**Table 1. Power States Summary**

Valid $V_{BUS\_IN}$	Valid $V_{BAT}$	Valid $V_{DDIO}^{(1)}$	Power State	Enabled Functionality	
				Processor Communication (I <sup>2</sup> C & Interrupts)	Detection
X	N	N	Power Down	NO	
X	N	Y <sup>(2)</sup>	Not Typical	Illegal State	
X	Y	N	Powered from $V_{BAT}$	NO	YES
X	Y	Y	Powered from $V_{BAT}$	YES	YES

**Notes:**

1.  $V_{DDIO}$  is expected to be the same supply used by the baseband I/Os.
2. Typically  $V_{DDIO}$  is only present when  $V_{BAT}$  is valid.
3. X = Don't care.

### 2.1. Reset

When the device is reset, all the registers are initialized to the default values shown in Section 9.9 and all switch paths are open. After reset or power up, FSA88x enters Standby Mode and is ready to detect accessories sensed on its  $V_{BUS\_IN}$  and / or ID\_CON pins.

#### 2.1.1. Hardware Reset

Power-on reset is caused by the initial rising edge of  $V_{BAT}$

#### 2.1.2. Software Reset

The device can be reset through software by writing to the Reset bit in the Register (1BH).



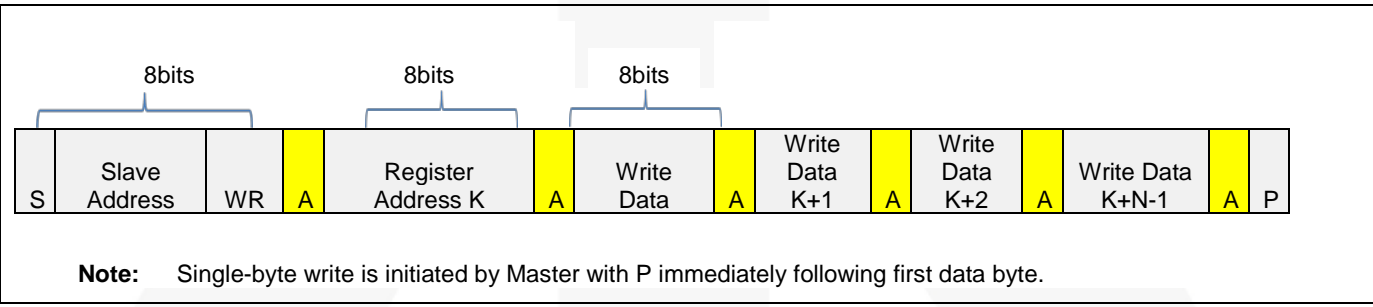
### 3. I<sup>2</sup>C

The FSA88x integrates a full fast-mode I<sup>2</sup>C slave controller compliant with the I<sup>2</sup>C specification version 2.1. The FSA88x I<sup>2</sup>C interface runs up to 400 kHz.

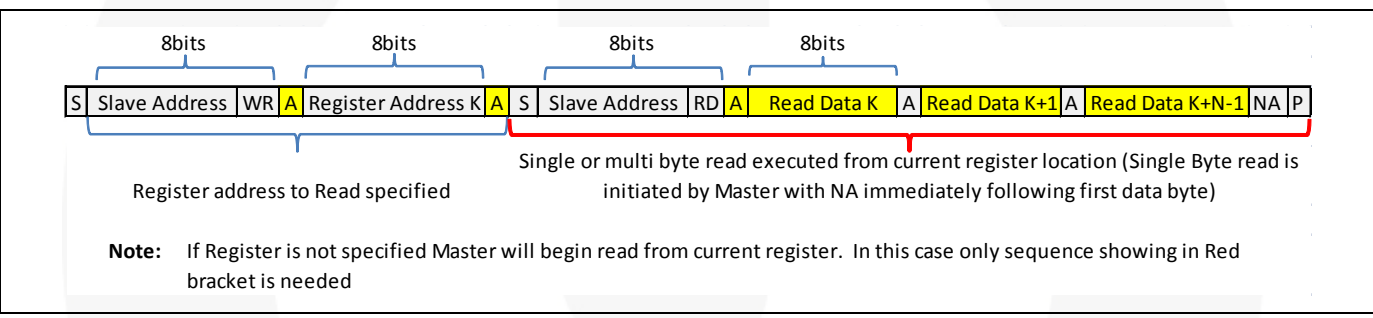
The slave address is shown in Table 2. Status information and configuration occurs via the I<sup>2</sup>C interface. *Please see Table 7 for more information.*

**Table 2. I<sup>2</sup>C Slave Address**

Name	Size (Bits)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Slave Address	8	0	1	0	0	1	0	1	Read / Write



**Figure 5. I<sup>2</sup>C Write Sequence**



**Figure 6. I<sup>2</sup>C Read Sequence**

□	From Master to Slave	<b>S</b>	Start Condition	<b>NA</b>	NOT Acknowledge (SDA High)	<b>RD</b>	Read =1
□	From Slave to Master	<b>A</b>	Acknowledge (SDA Low)	<b>WR</b>	Write=0	<b>P</b>	Stop Condition

### 4. Configuration

FSA88x requires minimal configuration for proper detection and reporting. The following steps provide full configuration.

1. Write Control register (02h) to configure manual or automatic switching modes.
- a. If using manual switching modes, write Manual SW 1 register (13h) to configure switches.
2. Write Control register (02h) to clear INT Mask bit. This enables interrupts to the baseband.



## 5. Detection

The FSA88x monitors both  $V_{BUS\_IN}$  and ID\_CON to detect accessories. The ID\_CON detection is a “resistive detection” that reads the resistance to GND on the ID\_CON pin to determine the accessory attached. Table 3 shows the assignment of accessories based on resistor values.

FSA88x can also detect accessories with ID resistances outside the specified ranges. The FSA88x detects these unknown accessories in the same manner as the defined accessories and interrupts the baseband processor and provides the correct ADC value, as shown in Table 3.

**Table 3. ID\_CON Accessory Detection**

ADC Code					Equivalent R <sub>ID</sub>			Description
4	3	2	1	0	Min.	Target	Max.	
1	0	1	0	1	117.4 kΩ	121 kΩ	124.6 kΩ	Unknown Accessory
1	0	1	1	0	145.5 kΩ	150 kΩ	154.5 kΩ	Unknown Accessory
1	0	1	1	1	176.4 kΩ	200 kΩ <sup>(4)</sup>	206 kΩ	Travel Adapter (TA) or Car Kit Type 1 Charger
1	1	0	0	0	247.3 kΩ	255 kΩ	262.7 kΩ	Factory Mode Boot OFF-USB
1	1	0	0	1	291.9 kΩ	301 kΩ	310.1 kΩ	Factory Mode Boot ON-USB
1	1	0	1	0	354 kΩ	365 kΩ	375.9 kΩ	Unknown Accessory
1	1	0	1	1	428.7 kΩ	442 kΩ <sup>(4)</sup>	455.3 kΩ	Unknown Accessory
1	1	1	0	0	507.3 kΩ	523 kΩ	538.7 kΩ	Factory Mode Boot OFF-UART
1	1	1	0	1	600.4 kΩ	619 kΩ	637.6 kΩ	Factory Mode Boot ON-UART
1	1	1	1	0	750 kΩ	1000 kΩ	1030 kΩ	Unknown Accessory
Not 'h1F or any code above					3 MΩ	None of the above ranges		Unknown Accessory

**Note:**

4. These accessories need VBUS to be valid in order to be detected since they are charger accessories.

### 5.1. Factory Cable Detection

Factory modes are initiated with the attachment of special test hardware, called a “JIG box” for factory testing. The FSA88x automatically configures switch paths to any of the factory-mode accessories when the appropriate resistor is sensed on the ID\_CON pin. A change of resistor on the ID\_CON pin dynamically switches between factory modes and auto-configures the appropriate switch paths without detaching and attaching the cable.

The different factory mode accessories with the associated resistor values (1% standard resistors) on the ID\_CON pin

and the JIG and BOOT logic states are listed in Table 4. The FSA88x allows both HS USB and FS USB in addition to UART signals to be passed on both ports with matched performance. This allows greater flexibility when designing with the FSA88x.

JIG output signals when a factory mode accessory is plugged in and BOOT output signals the mobile phone to boot up. The switch paths for factory modes are shown in Table 4.

**Table 4. ID\_CON Factory Cable Detection**

Configuration Type		DP_CON	DM_CON	ID_CON			BOOT	FSA880 JIG	FSA881 JIG
<b>Factory Mode Jig: UART</b>	Boot_On	DP_HOST1	DM_HOST1	600kΩ	619kΩ	637kΩ	HIGH	LOW	HIGH
	Boot_Off	DP_HOST1	DM_HOST1	507kΩ	523kΩ	538kΩ	LOW	LOW	HIGH
<b>Factory Mode Jig: USB</b>	Boot_On	DP_Host	DM_Host	292kΩ	301kΩ	310kΩ	HIGH	LOW	HIGH
	Boot_Off	DP_Host	DM_Host	247kΩ	255kΩ	262kΩ	LOW	LOW	HIGH

The FSA88x detection algorithms monitor both the  $V_{BUS}$  and ID pins of the USB interface. Based on the detection results, multiple registers are updated and the INTB pin is asserted to indicate to the baseband processor that an accessory was detected and to read the registers for the complete

information. The detection algorithm allows the application to control the timing of the detection algorithm and the configuration of the internal switches. The flow diagram in Figure 7 shows the operation of the detection algorithm.

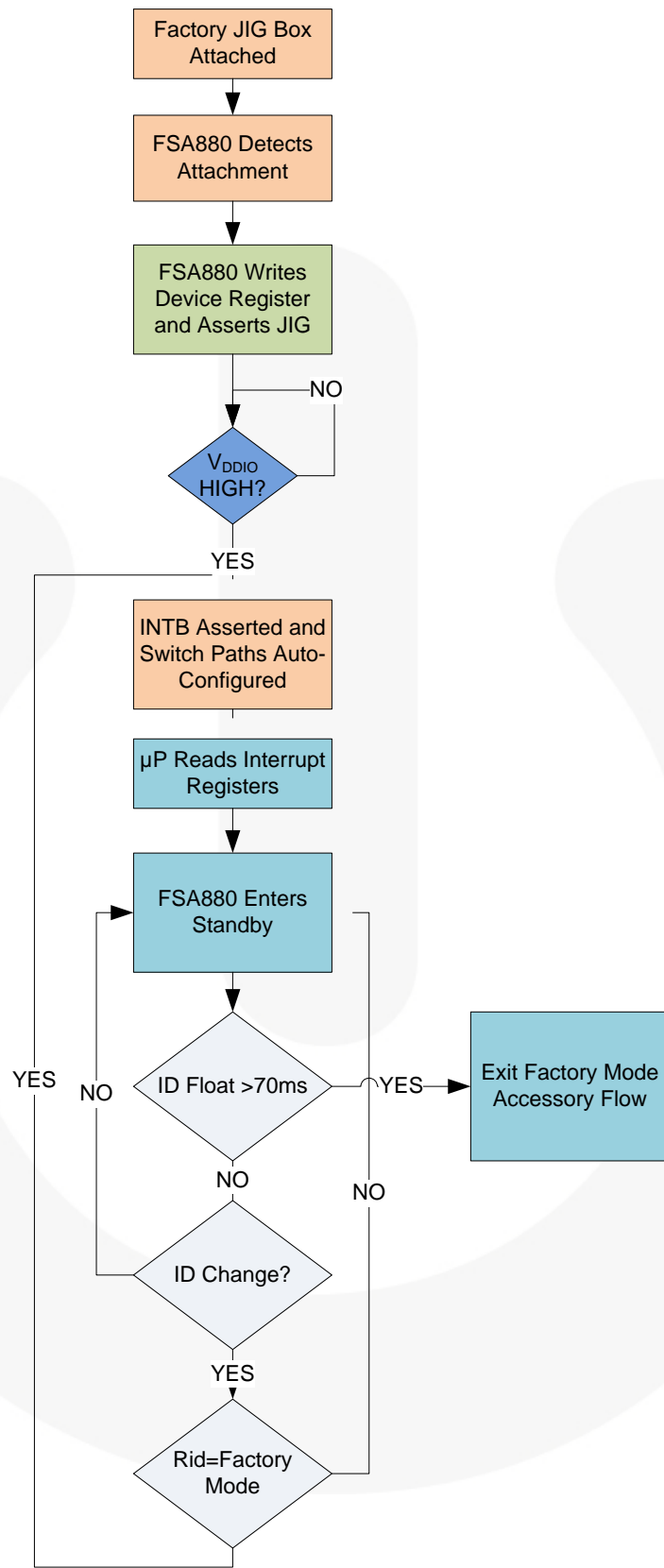


Figure 7. Factory Cable Detection Flow Chart (FSA880)

## 5.2. USB Port Detection

The multiple types of USB 2.0 ports the FSA88x can detect are summarized in Table 5.

**Table 5. ID\_CON and VBUS Detection Table for USB Devices**

V <sub>BUS_IN</sub>	DP_CON	DM_CON	ID_CON resistance to GND			Accessory Detected <sup>(5)</sup>
			Min.	Typ.	Max.	
5V	Not Checked	Not Checked	174.6 kΩ	200 kΩ	206 kΩ	TA (travel adapter) Charger (180 kΩ) and Car Kit Charger Type 1 only (200 kΩ) <sup>(6)</sup>
5V	Shorted to DM_CON	Shorted to DP_CON	3 MΩ	Open	Open	USB Dedicated Charging Port, Travel Adapter or Dedicated Charger (DCP) <sup>(6)</sup>
5V	DP_HOST	DM_HOST	3 MΩ	Open	Open	USB Charging Downstream Port (CDP) <sup>(6)</sup>
5V	DP_HOST	DM_HOST	3 MΩ	Open	Open	USB Standard Downstream Port (SDP) <sup>(6)</sup>

### Notes:

5. The accessory type is reported in the Device Type 1 (0Ah) register for each valid accessory detected.
6. The FSA88x follows the Battery Charging 1.1 specification, which uses DP\_CON and DM\_CON to determine the USB accessory attached. Refer to *Battery Charging 1.1 specification* for further details.

For SDP and CDP USB accessories, the following pin mapping is automatically configured:

- DP\_HOST = DP\_CON
- DM\_HOST = DM\_CON

For DCP charger, the DP\_HOST and DM\_HOST switches are open. For all USB accessories V<sub>BUS\_IN</sub> is Over-Voltage Tolerance (OVT) up to 28 V.

## 6. Processor Communication

Typical communication steps between the processor and the FSA88x during accessory detection are:

1. INTB is asserted LOW, indicating change in accessory detection.
2. Processor reads Interrupt 1 (03h) register to determine if an attach or detach event was detected.
3. Processor reads Status registers to determine the exact accessory detected.
  - a. Device Type 1 (0Ah): Indicates which USB, Car Kit CDP, or DCP accessory was detected.
  - b. Device Type 2 (0Bh): Indicates which factory mode or unknown accessory was detected.

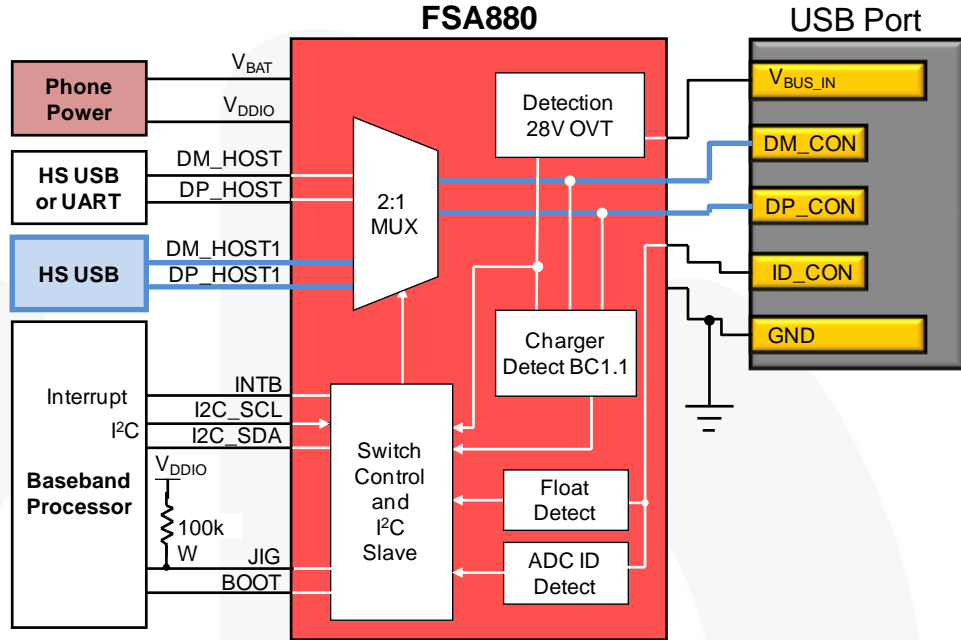
## 7. Switch Configuration

FSA88x devices have two modes of operation when configuring the internal switches. The FSA88x can auto-configure the switches or the switches can be configured

manually by the processor. Typical applications use Auto-Configuration Mode and do not require interaction with the baseband to configure the switches correctly.

### 7.1. Configurations

**USB Accessories and Factory Cables:**  
**DP\_CON=DP\_HOST**  
**DM\_CON=DM\_HOST**



**UART Factory Cables:**  
**DP\_CON=DP\_HOST1**  
**DM\_CON=DM\_HOST1**

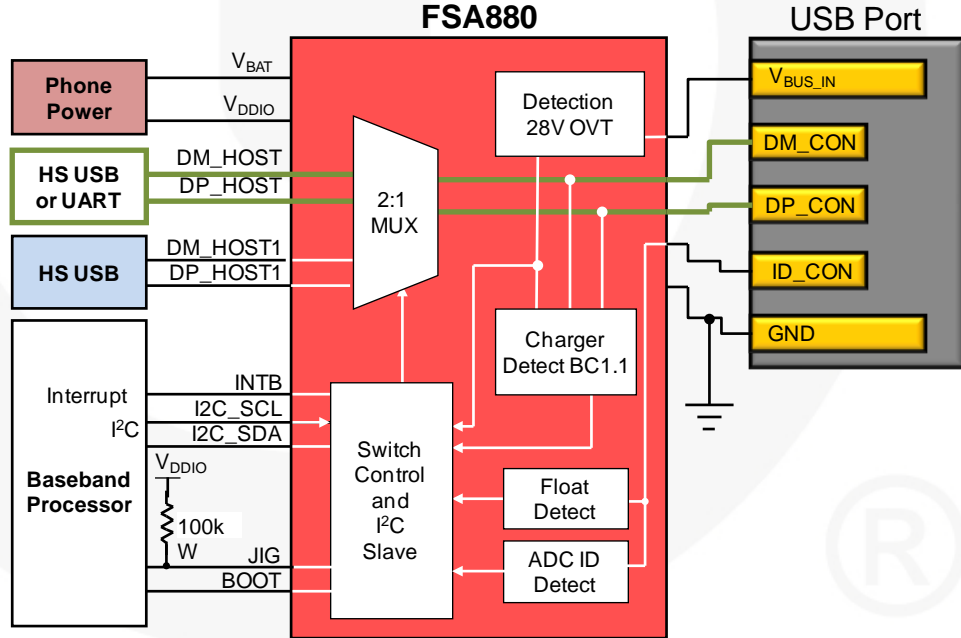


Figure 8. Switch Configurations

### 7.2. Manual Switching

Manual switching is enabled by writing the following registers:

- Manual Switch 1 (13h): Configures the switches for DM\_CON, and DP\_CON.
- Manual Switch 2 (14h): Configures the BOOT, and JIG pins.

## 8. Active Signal Performance

### 8.1. HS USB Data

#### 8.1.1. DP\_HOST/DM\_HOST

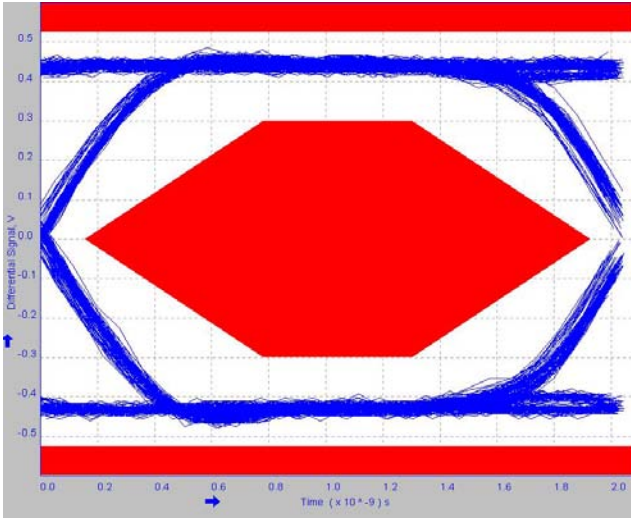


Figure 9. Pass Through Eye Compliance Testing Input Signal

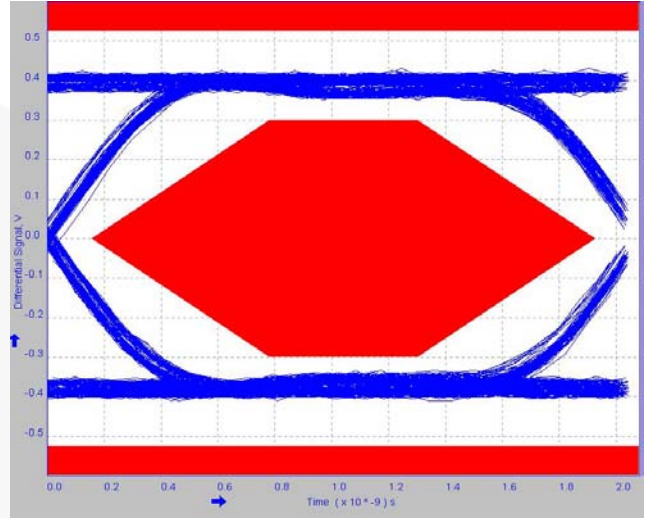


Figure 10. USB 2.0 Eye Compliance Test Results at Output

#### 8.1.2. DP\_HOST1/DM\_HOST1

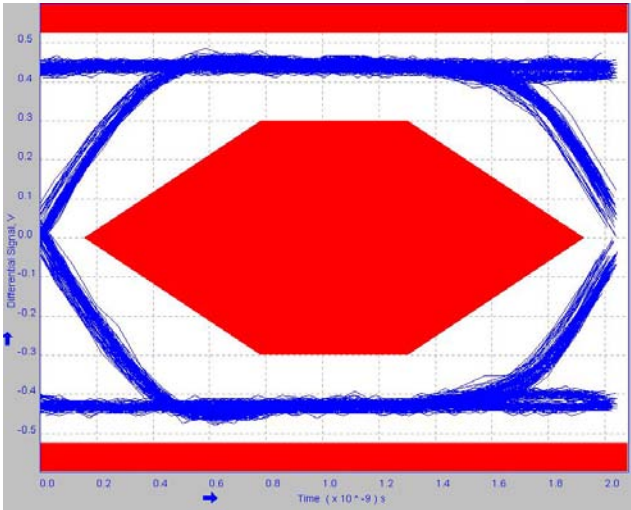


Figure 11. Pass-Through Eye Compliance Testing Input Signal

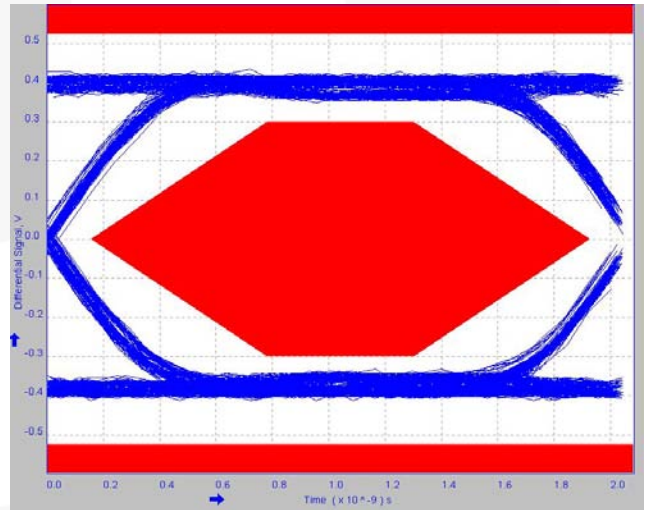


Figure 12. USB 2.0 Eye Compliance Test Results at Output



8.2. Full-Speed USB  
 8.2.1. DP\_HOST/DM\_HOST

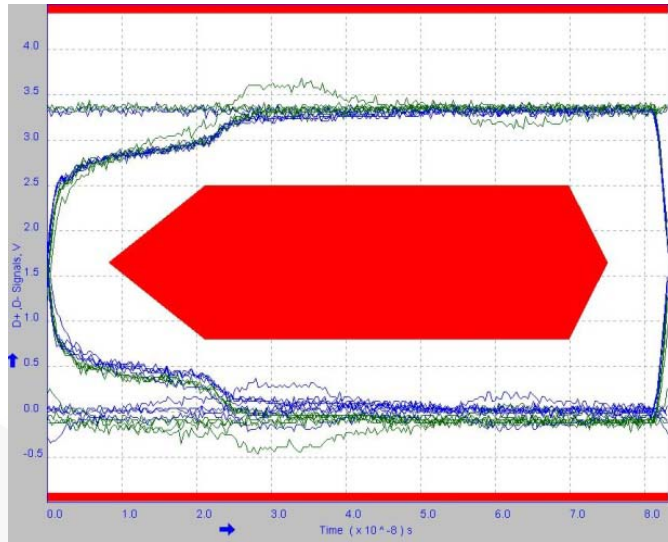


Figure 13. USB FS Eye Compliance Testing

8.2.2. DP\_HOST1/DM\_HOST1

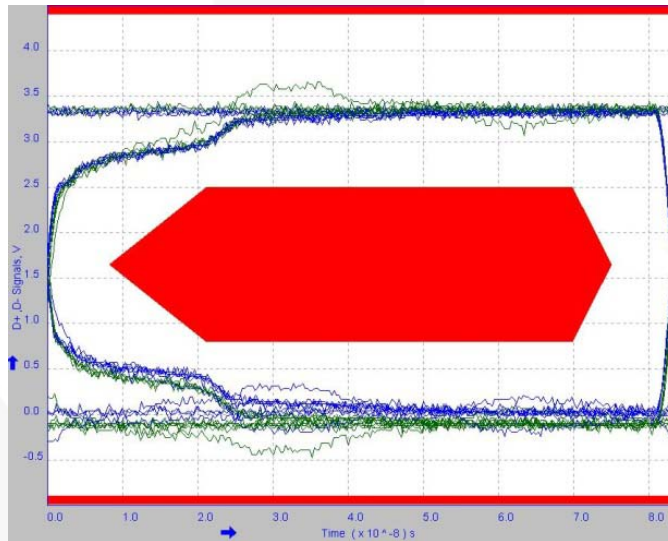


Figure 14. USB FS Eye Compliance Testing



## 9. Product Specifications

### 9.1. Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V <sub>BAT</sub>	Supply Voltage from Battery		-0.5	6.0	V
V <sub>BUS_IN</sub>	Supply Voltage from USB Connector		-0.5	28.0	V
V <sub>SW</sub>	Switch I/O Voltage	USB	-1.0	6.0	V
		UART	-1.0	6.0	
I <sub>IK</sub>	Input Clamp Diode Current		-50		mA
I <sub>SW</sub>	Switch I/O Current (Continuous)	USB at T <sub>A</sub> =85°C		25	mA
		UART at T <sub>A</sub> =85°C		12	
I <sub>SWPEAK</sub>	Peak Switch Current (Pulsed at 1ms Duration, <10% Duty Cycle)			150	mA
T <sub>STG</sub>	Storage Temperature Range		-65	+150	°C
T <sub>J</sub>	Maximum Junction Temperature			+150	°C
T <sub>L</sub>	Lead Temperature (Soldering, 10 Seconds)			+260	°C
ESD	IEC 61000-4-2 System ESD	USB Connector Pins (DP_CON, DM_CON, V <sub>BUS_IN</sub> , ID_CON) to GND	Air Gap	15	kV
			Contact	8	
	Human Body Model, JEDEC JESD22-A114		All Pins	4	
	Charged Device Model, JEDEC JESD22-C101		All Pins	2	

### 9.2. Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter		Min.	Typ.	Max.	Unit
V <sub>BAT</sub>	Battery Supply Voltage		3.0		4.4	V
V <sub>BUSIN</sub>	V <sub>BUS_IN</sub> Voltage		4.0		5.5	V
V <sub>DDIO</sub>	Processor Supply Voltage		1.8		3.6	V
V <sub>SW</sub>	Switch I/O Voltage	USB Path Active	0		3.6	V
		UART Path Active	0		3.6	
ID <sub>CAP</sub>	Capacitive Load on ID_CON Pin for Reliable Accessory Detection				1.0	nF
T <sub>A</sub>	Operating Temperature		-40		+85	°C

### 9.3. Switch Path DC Electrical Characteristics

All typical values are at  $T_A=25^\circ\text{C}$  unless otherwise specified.

Symbol	Parameter	$V_{BAT}$ (V)	Conditions	$T_A = -40$ to $+85^\circ\text{C}$			Unit
				Min.	Typ.	Max.	
<b>Host Interface Pins (BOOT, JIG, INTB)</b>							
$V_{OH}$	Output High Voltage (FSA881 JIG Output)	3.0 to 4.4	$I_{OH}=-2$ mA	$0.8 \cdot V_{BAT}$			V
$V_{OH}$	Output High Voltage (just BOOT & INTB Outputs) <sup>(7)</sup>	3.0 to 4.4	$I_{OH}=-2$ mA	$0.7 \cdot V_{DDIO}$			V
$V_{OL}$	Output Low Voltage (INTB, JIG & BOOT Outputs)	3.0 to 4.4	$I_{OL}=3$ mA			0.4	V
<b>I<sup>2</sup>C Interface Pins – Fast Mode (I2C_SDA, I2C_SCL)</b>							
$V_{IL}$	Low-Level Input Voltage	3.0 to 4.4				$0.3 \cdot V_{DDIO}$	V
$V_{IH}$	High-Level Input Voltage	3.0 to 4.4		$0.7 \cdot V_{DDIO}$			V
$V_{HYS}$	Hysteresis of Schmitt Trigger Inputs	3.0 to 4.4		$V_{DDIO}>2$ V	$0.05 V_{DDIO}$		V
				$V_{DDIO}<2$ V	$0.1 V_{DDIO}$		V
$V_{OL1}$	Low-Level Output Voltage at 3 mA Sink Current (Open-Drain)	3.0 to 4.4		$V_{DDIO}>2$ V		0.4	
				$V_{DDIO}<2$ V		$0.2 \cdot V_{DDIO}$	V
$I_{I2C}$	Input Current of I2C_SDA and I2C_SCL Pins	3.0 to 4.4	Input Voltage 0.26 V to 2.34 V	-10		10	$\mu\text{A}$
<b>Switch OFF Characteristics</b>							
$I_{OFF}$	Power-Off Leakage Current	0	All Data Ports $V_{SW}=0$ V to 4.4 V			10	$\mu\text{A}$
$I_{NO(OFF)}$	Off Leakage Current	3.0 to 4.4	$V_{BAT}=4.4$ V; I/O Pins=0.3 V, 4.1 V, or Floating	-0.100	0.001	0.100	$\mu\text{A}$
$I_{IDSHRT}$	Short-Circuit Current	3.0 to 4.4	Current Limit if ID_CON=0 V		1		mA
<b>USB Switch ON Path</b>							
$R_{ONUSB}$	USB Switch On Resistance <sup>(8)</sup>	3.0 to 4.4	$V_{D+/D-}=0$ V, 0.4 V; $I_{ON}=8$ mA		8	10	$\Omega$
			$V_{SW}=0$ V, 3.6 V; $I_{ON}=30$ mA		25	30	$\Omega$
<b>VBUS Path</b>							
$V_{BUSIN}$	$V_{BUS\_IN}$ Valid Threshold			0.8		4.0	V
$R_{BUS}$	$V_{BUS\_IN}$ Resistance to GND				3		M $\Omega$
<b>UART Switch ON Paths</b>							
$V_{ASR\_UART}$	Analog Signal Range	3.0 to 4.4		0		3.6	V
$R_{ONUART}$	UART Switch On Resistance	3.0 to 4.4	$V_{D+/D-}=0$ V, 0.4 V; $I_{ON}=8$ mA		8	10	$\Omega$
			$V_{SW}=0$ V, 3.6 V; $I_{ON}=30$ mA		25	30	
<b>Total Current Consumption</b>							
$I_{CCSL}$	Battery Supply Standby Mode Current (No Accessory Attached)	3.0 to 4.4	No Accessory, Static Current During Standby Mode		15	25	$\mu\text{A}$
$I_{CCSLWA}$	Battery Supply Standby Mode Current with Accessory Attached <sup>(7)</sup>	3.0 to 4.4	With non-Factory Mode Accessories Attached		30	40	$\mu\text{A}$
			With Factory Mode Accessories Attached <sup>(9)</sup>		100	120	$\mu\text{A}$

**Notes:**

7. Limits based on electrical characterization data.
8. On resistance is the voltage drop between the two terminals at the indicated current through the switch.
9. Factory mode accessories leave the detection circuitry active after attach to allow detection of ID changes without an attach.



#### 9.4. Capacitance

Symbol	Parameter	V <sub>BAT</sub> (V)	Conditions	T <sub>A</sub> = -40 to +85°C			Unit
				Min.	Typ.	Max.	
C <sub>ON</sub>	DP_CON, DM_CON On Capacitance	3.8	V <sub>BIAS</sub> =0.2 V, f=1 MHz		6		pF
C <sub>I</sub>	Capacitance for Each I/O Pin	3.8			5		pF

#### 9.5. I<sup>2</sup>C DC Electrical Characteristics

Symbol	Parameter	V <sub>BAT</sub> (V)	Conditions	T <sub>A</sub> = -40 to +85°C		Unit
				Min.	Max.	
<b>Fast Mode (I2C_SDA, I2C_SCL)</b>						
V <sub>IL</sub>	Low-Level Input Voltage	3.0 to 4.4			0.3•V <sub>DDIO</sub>	V
V <sub>IH</sub>	High-Level Input Voltage	3.0 to 4.4		0.7•V <sub>DDIO</sub>		V
V <sub>hys</sub>	Hysteresis of Schmitt Trigger Inputs	3.0 to 4.4	V <sub>DDIO</sub> >2 V	0.05 V <sub>DDIO</sub>		V
			V <sub>DDIO</sub> <2 V	0.1 V <sub>DDIO</sub>		V
V <sub>OL1</sub>	Low-Level Output Voltage at 3 mA Sink Current (Open-Drain)	3.0 to 4.4	V <sub>DDIO</sub> >2 V		0.4	
			V <sub>DDIO</sub> <2 V		0.2•V <sub>DDIO</sub>	V
I <sub>I2C</sub>	Input Current of I2C_SDA and I2C_SCL Pins	3.0 to 4.4	Input Voltage 0.26 V to 2.34 V	-10	10	μA

#### 9.6. I<sup>2</sup>C AC Electrical Characteristics

Symbol	Parameter	Fast Mode		Unit
		Min.	Max.	
f <sub>SCL</sub>	I2C_SCL Clock Frequency	0	400	kHz
t <sub>HD;STA</sub>	Hold Time (Repeated) START Condition	0.6		μs
t <sub>LOW</sub>	LOW Period of I2C_SCL Clock	1.3		μs
t <sub>HIGH</sub>	HIGH Period of I2C_SCL Clock	0.6		μs
t <sub>SU;STA</sub>	Set-up Time for Repeated START Condition	0.6		μs
t <sub>HD;DAT</sub>	Data Hold Time	0	0.9	μs
t <sub>SU;DAT</sub>	Data Set-up Time <sup>(10)</sup>	100		ns
t <sub>r</sub>	Rise Time of I2C_SDA and I2C_SCL Signals <sup>(10,11)</sup>	20+0.1C <sub>b</sub>	300	ns
t <sub>f</sub>	Fall Time of I2C_SDA and I2C_SCL Signals <sup>(10,11)</sup>	20+0.1C <sub>b</sub>	300	ns
t <sub>SU;STO</sub>	Set-up Time for STOP Condition	0.6		μs
t <sub>BUF</sub>	BUS-Free Time between STOP and START Conditions	1.3		μs
t <sub>SP</sub>	Pulse Width of Spikes that Must Be Suppressed by the Input Filter	0	50	ns

**Notes:**

10. A fast-mode I<sup>2</sup>C Bus<sup>®</sup> device can be used in a Standard-Mode I<sup>2</sup>C Bus system, but the requirement t<sub>SU;DAT</sub> ≥ 250 ns must be met. This is automatically the case if the device does not stretch the LOW period of the I2C\_SCL signal. If a device does stretch the LOW period of the I2C\_SCL signal, it must output the next data bit to the I2C\_SDA line t<sub>r,max</sub> + t<sub>SU;DAT</sub> = 1000 + 250 = 1250 ns (according to the Standard-Mode I<sup>2</sup>C bus specification) before the I2C\_SCL line is released.
11. C<sub>b</sub> equals the total capacitance of one bus line in pF. If mixed with high-speed devices, faster fall times are allowed by the I<sup>2</sup>C specification.

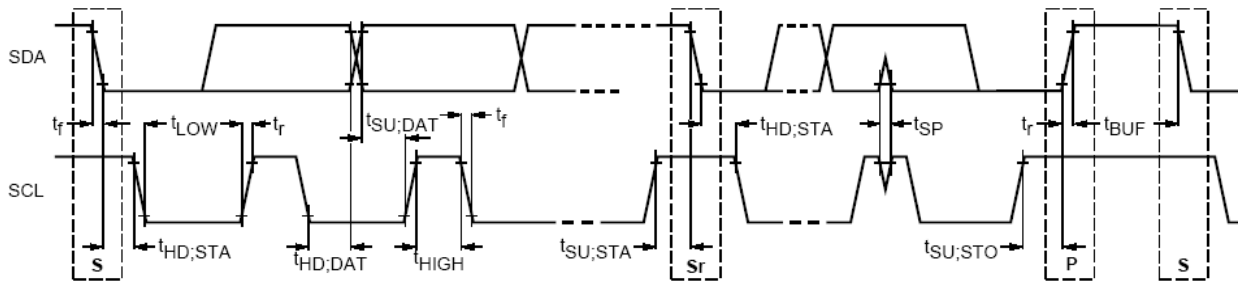


Figure 15. Definition of Timing for Full-Speed Mode Devices on the I<sup>2</sup>C Bus®

Table 6. I<sup>2</sup>C Slave Address

Name	Size (Bits)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Slave Address	8	0	1	0	0	1	0	1	R/W

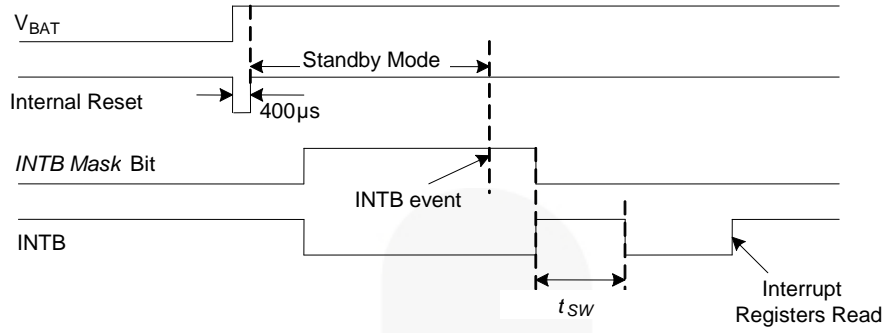
### 9.7. Switch Path AC Electrical Characteristics

All typical values are for  $V_{BAT}=3.8\text{ V}$  at  $T_A=25^\circ\text{C}$  unless otherwise specified.

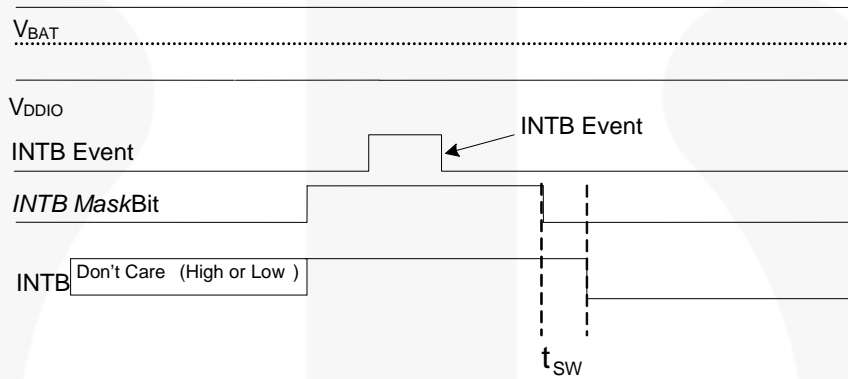
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Xtalk	Active Channel Crosstalk DP_CON to DM_CON	USB Mode $f=1\text{ MHz}, R_T=50\ \Omega, C_L=0\text{ pF}$		-60		dB
		$f=240\text{ MHz}, R_T=50\ \Omega, C_L=0\text{ pF}$		-30		
O <sub>IRR</sub>	Off Isolation	USB Mode $f=1\text{ MHz}, R_T=50\ \Omega, C_L=0\text{ pF}$		-60		dB
t <sub>SK(P)</sub>	Skew of Opposite Transitions of the Same Output (USB Mode)	$t_r=t_f=750\text{ ps}$ (10-90%) at 240 MHz, $C_L=0\text{ pF}, R_L=50\ \Omega$		35		ps
t <sub>sw</sub>	Time after <i>INT Mask</i> Cleared to “0” until INTB Goes LOW to Signal the Interrupt after Interruptible Event while <i>INT Mask</i> Bit Set to “1”	See Figure 16 and Figure 17		10		ms
t <sub>SDPDET</sub>	Time from $V_{BUS\_IN}$ Valid to USB Switches Closed for USB Standard Downstream Port	See Figure 17		130		ms
t <sub>CHGOUT</sub>	Time from $V_{BUS\_IN}$ Valid to USB Switches Closed for USB Charging Downstream Port (CDP)	See Figure 18		170		ms
t <sub>JIGVBUS</sub>	Time from $V_{BUS\_IN}$ Valid to JIG LOW for Factory Mode Operation with $V_{BUS\_IN}$ Present	See Figure 20		200		ms
t <sub>JIGVBUS</sub>	Time from $V_{BUS\_IN}$ Valid to JIG LOW for Factory Mode Operation without $V_{BUS\_IN}$ Present	See Figure 21		200		ms



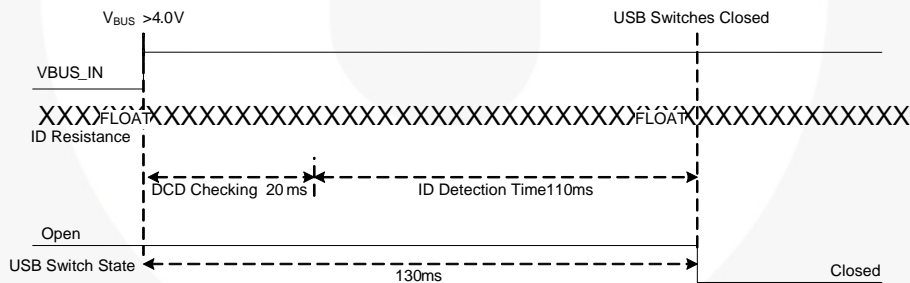
## 9.8. Timing Diagrams



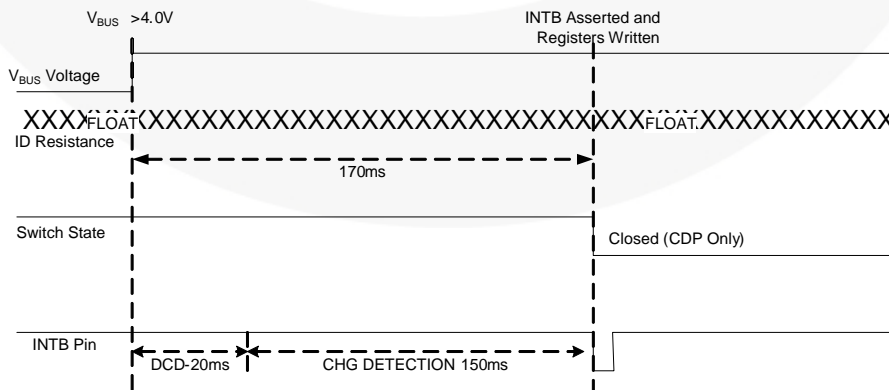
**Figure 16. INT Mask to INTB Interrupt at Power-Up Timing Diagram**



**Figure 17. INT Mask to INTB Interrupt During Operation Timing Diagram**



**Figure 18. USB Standard Downstream Port Attach Timing**



**Figure 19. USB Charging Ports (DCP & CDP) Attach Timing**



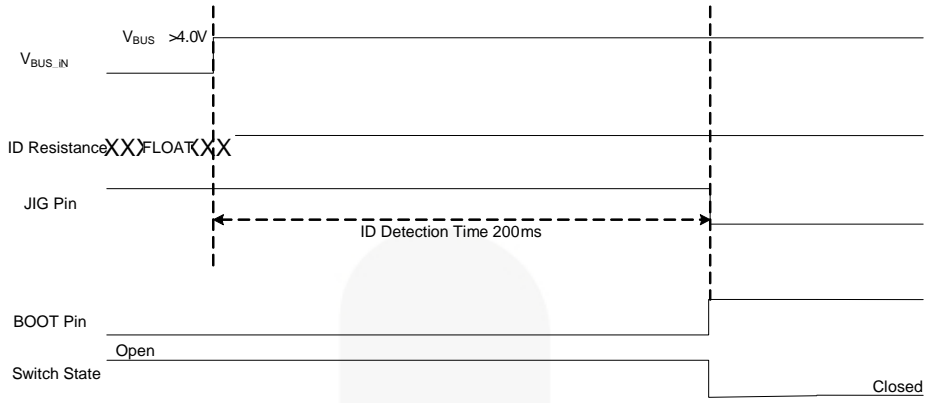


Figure 20. Jig Box Attach Timing ( $V_{BUS\_IN}$  Valid)

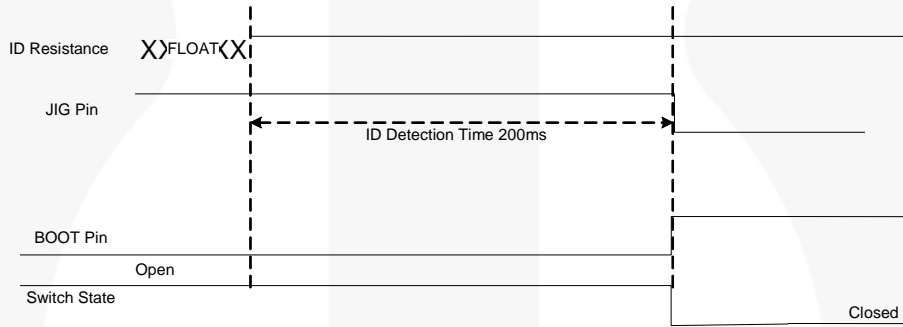


Figure 21. JIG Box Attach Timing without  $V_{BUS\_IN}$



## 9.9. Programmability Tables

**Table 7. I<sup>2</sup>C Register Map**

Address	Register	Type	Reset Value <sup>(12,13)</sup>	Bit 7 <sup>(14)</sup>	Bit 6 <sup>(14)</sup>	Bit 5 <sup>(14)</sup>	Bit 4 <sup>(14)</sup>	Bit 3 <sup>(14)</sup>	Bit 2 <sup>(14)</sup>	Bit 1 <sup>(14)</sup>	Bit 0 <sup>(14)</sup>
01H	Device ID	R	N/A	Revision Number					Vendor ID		
02H	Control	R/W	xxx0x1x1				Switch Open		Auto Config		INT Mask
03H	Interrupt	R/C	xxxxxx00							Detach	Attach
07H	ADC	R	xxx11111	ADC Value							
0AH	Device Type 1	R	x000x0xx		Dedicated Charger (DCP)	USB Charger (CDP)	Car Kit Type 1 & TA Charger		Standard USB (SDP)		
0BH	Device Type 2	R	0xxx0000	Unknown Accessory				Jig UART Off	Jig UART On	Jig USB Off	Jig USB On
13H	Manual SW 1	R/W	000000xx	D- Switching			D+ Switching				
14H	Manual SW 2	R/W	xxxx00xx					BOOT SW	JIG ON		
1BH	Reset	R/W	xxxxxxx0								Reset

**Notes:**

- 12. Write “0” to undefined register bits.
- 13. Values read from undefined register bits are not defined and invalid.
- 14. Do not use undefined register locations.

**Table 8. Device ID**

Address: 01h

Type: Read

Bit #	Name	Size (Bits)	Description
7:3	Revision Number	5	Rev 0.0 = 00000
2:0	Vendor ID	3	000: Fairchild Semiconductor

**Table 9. Control**

Address: 02h

Reset Value: xxx0x1x1

Type: Read/Write

Bit #	Name	Size (Bits)	Description
7:5	DoNotUse	3	N/A
4	Switch Open	1	1: Open all switches 0: Automatic switching by accessory status
3	DoNotUse	1	N/A
2	Auto Config	1	1: Automatic switching (also called auto-configuration) 0: Manual switching
1	DoNotUse	1	N/A
0	INT Mask	1	1: Mask interrupt – do not interrupt baseband processor 0: Unmask interrupt – interrupt baseband processor on change of state in Interrupt register

**Table 10. Interrupt**

Address: 03h

Reset Value: xxxxxx00

Type: Read/Clear

Bit #	Name	Size (Bits)	Description
7:2	DoNotUse	6	N/A
1	Detach	1	1: Accessory detached 0: Accessory not detached
0	Attach	1	1: Accessory attached 0: Accessory not attached

**Table 11. Device Type 1**

Address: 07h

Reset Value: xxx11111

Type: Read

Bit #	Name	Size (Bits)	Description
7:5	Reserved	3	NA
4:0	ADC Value	5	ADC value read from ID

**Table 12. Device Type 1**

Address: 0Ah

Reset Value: x00x00xx

Type: Read

Bit #	Name	Size (Bits)	Description
7	DoNotUse	1	N/A
6	Dedicated Charger (DCP)	1	1: USB dedicated charging port (DCP) charger detected 0: USB dedicated charging port (DCP) charger not detected
5	USB Charger (CDP)	1	1: USB charging downstream port (CDP) charger detected 0: USB charging downstream port (CDP) charger not detected
4	Car Kit Type 1 & TA Charger	1	1: Car Kit Type 1 or Travel Adapter (TA) detected 0: Car Kit Type 1 or Travel Adapter (TA) not detected
3	DoNotUse	1	N/A
2	Standard USB (SDP)	1	1: USB standard downstream port (SDP) detected 0: USB standard downstream port (SDP) not detected
1:0	DoNotUse	2	N/A

**Table 13. Device Type 2**

Address: 0Bh

Reset Value: 0xxx0000

Type: Read

Bit #	Name	Size (Bits)	Description
7	Unknown Accessory	1	1: Any accessory detected as unknown or an accessory that cannot be detected as being valid even though ID_CON is not floating 0: Unknown accessory not detected
6:4	DoNotUse	4	N/A
3	JIG_UART_OFF	1	1: Factory mode BOOT-OFF-UART detected 0: Factory mode BOOT-OFF-UART not detected

Bit #	Name	Size (Bits)	Description
2	JIG_UART_ON	1	1: Factory mode cable UART path with BOOT ON detected 0: Factory mode cable UART path with BOOT ON not detected
1	JIG_USB_OFF	1	1: Factory mode cable USB path with BOOT OFF detected 0: Factory mode cable USB path with BOOT OFF not detected
0	JIG_USB_ON	1	1: Factory mode cable USB path with BOOT ON detected 0: Factory mode cable USB path with BOOT ON not detected

**Table 14. Manual S/W 1** <sup>(15)</sup>

Address: 13h

Reset Value: 000000xx

Type: Read/Write

Bit #	Name	Size (Bits)	Description
7:5	DM_CON Switching	3	000: Open switch 001: DM_CON connected to DM_HOST of USB port 011: DM_CON connected to DM_HOST1 of UART port All other values: DoNotUse
4:2	DP_CON Switching	3	000: Open switch 001: DP_CON connected to DP_HOST of USB port 011: DP_CON connected to DP_HOST1 of UART port All other values: DoNotUse
1:0	DoNotUse	2	N/A

**Note:**

15. When switching between manual switch configurations on a single attach, the accessory must pass through an “000: Open Switch” state between configurations. Manual Modes must have an accessory attached prior to operation. The FSA88x does not configure per the Manual Modes register if an accessory has not been previously attached.

**Table 15. Manual S/W 2**

Address: 14h

Reset Value: xxxx00xx

Type: Read/Write

Bit #	Name	Size (Bits)	Description
7:4	DoNotUse	4	N/A
3	BOOT_SW	1	1: HIGH 0: LOW
2	JIG_ON	1	1: JIG output=GND (FSA880) or JIG output=HIGH (FSA881) 0: JIG output=High impedance (FSA880) or JIG output=LOW (FSA881)
1:0	DoNotUse	2	N/A

**Table 16. Reset**

Address: 1Bh

Reset Value: xxxxxx0

Type: Read/Write

Bit #	Name	Size (Bits)	Description
7:1	DoNotUse	6	N/A
0	Reset	1	1: Resets the FSA88x 0: Does not reset the FSA88x

## 10. Layout Guidelines

### 10.1. PCB Layout Guidelines for High-Speed USB Signal Integrity

1. Place FSA88x as close to the USB controller as possible. Shorter traces mean less loss, less chance of picking up stray noise, and less radiated EMI.
  - a) Keep the distance between the USB controller and the device less than 25 mm (< one inch).
  - b) For best results, this distance should be <18mm. This keeps it less than one quarter ( $\frac{1}{4}$ ) of the transmission electrical length.
2. Use an impedance calculator to ensure 90  $\Omega$  differential impedance for DP\_CON and DM\_CON lines.
3. Select the best transmission line for the application.
  - a) For example, for a densely populated board, select an edge-coupled differential stripline.
4. Minimize the use of vias and keep HS USB lines on same plane in the stack.
  - a) Vias are an interruption in the impedance of the transmission line and should be avoided.
  - b) Try to avoid routing schemes that generally force the use of at least two vias: one on each end to get the signal to and from the surface.
5. Cross lines, only if necessary, orthogonally to avoid noise coupling (traces running in parallel couple).
6. If possible, separate HS USB lines with GND to improve isolation.
  - a) Routing GND, power, or components close to the transmission lines can create impedance discontinuities.
7. Match transmission line pairs as much as possible to improve skew performance.
8. Avoid sharp bends in PCB traces; a chamfer or rounding is generally preferred.
9. Place decoupling for power pins as close to the device as possible.
  - a) Use low-ESR capacitors for decoupling if possible.
  - b) A tuned PI filter should be used to negate the effects of switching power supplies and other noise sources if needed.

### 10.2. Layout for GSM / TDMA Buzz Reduction

There are two possible mechanisms for TDMA / GSM noise to negatively impact FSA88x performance. The first is the result of large current draw by the phone transmitter during active signaling when the transmitter is at full or almost-full power. With the phone transmitter dumping large amounts of current in the phone GND plane; it is possible for there to be temporary voltage excursions in the GND plane if not properly designed. This noise can be coupled back through the GND plane into the FSA88x device and, although the FSA88x has very good isolation; if the GND noise amplitude is large enough, it can result in noise coupling to the FSA88x. The second path for GSM noise is through electromagnetic coupling onto the signal lines themselves.

In most cases, the noise introduced as a result is on the  $V_{BAT}$  and / or GND supply rails. Following are recommendations for PCB board design that help address these two sources of TDMA / GSM noise.

1. Provide a wide, low-impedance GND return path to both the FSA88x and to the power amplifier that sources the phone transmit block.
2. Provide separate GND connections to PCB GND plane for each device. Do not share GND return paths among devices.
3. Add as large a decoupling capacitor as possible ( $\geq 1\mu\text{F}$ ) between the  $V_{BAT}$  pin and GND to shunt any power supply noise away from the FSA88x. Also add decoupling capacitance at the PA (*see the reference application schematic in Figure 22 for recommended decoupling capacitor values*).
4. Add 33 pF shunt capacitors on any PCB nodes with the potential to collect radiated energy from the phone transmitter.
5. Add a series  $R_{BAT}$  resistor prior to the decoupling capacitor on the  $V_{BAT}$  pin to attenuate noise prior to reaching the FSA88x.



### 11. Reference Schematic

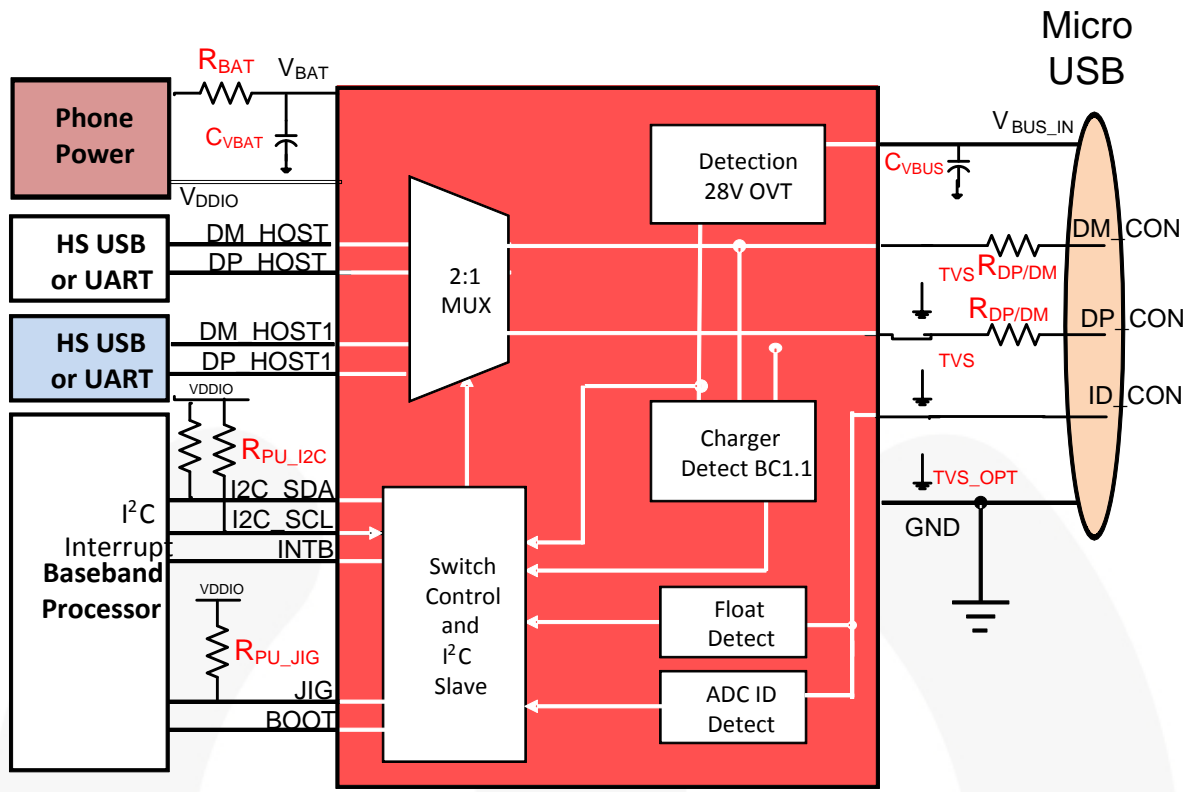
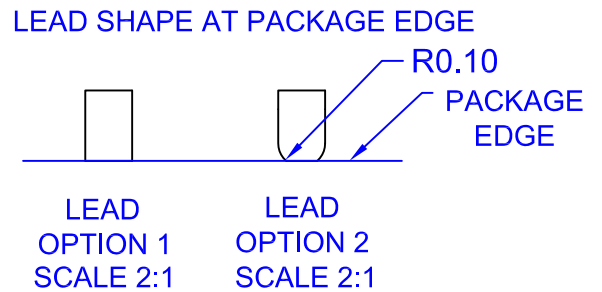
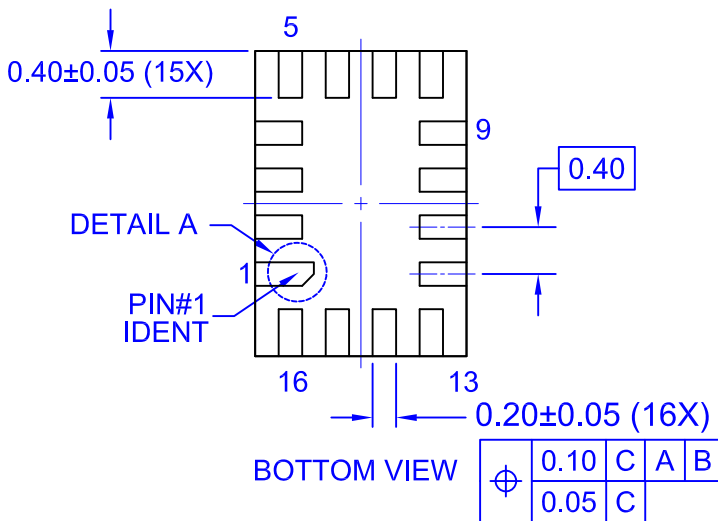
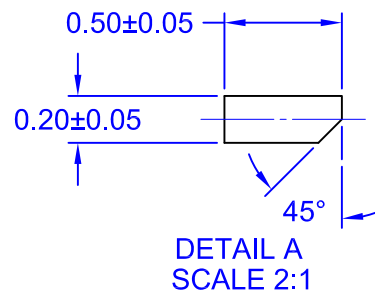
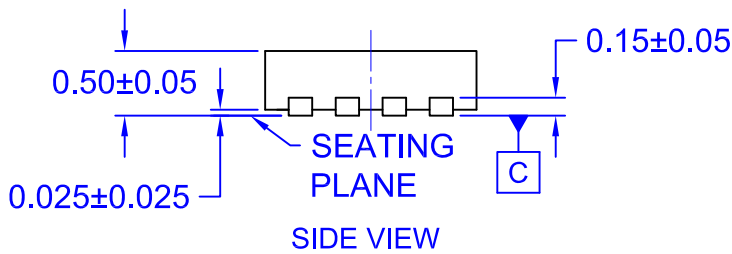
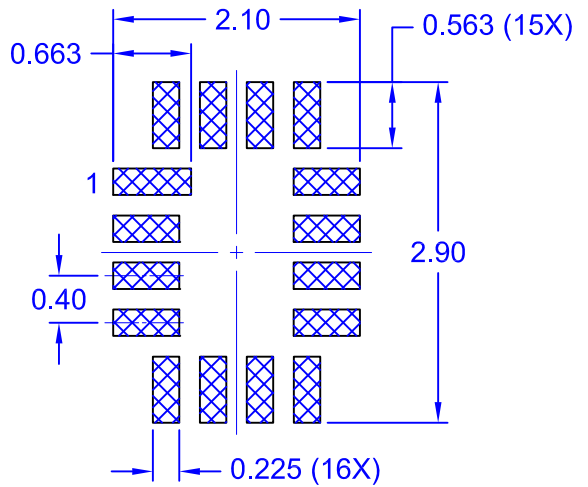
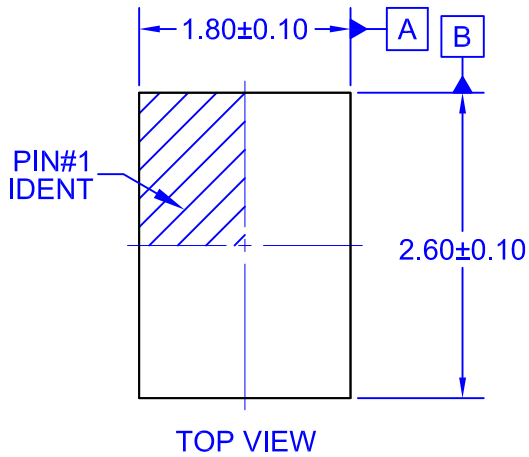


Figure 22. Reference Schematic

Table 17. Reference Schematic Component Values

Symbol	Parameter	Recommended Value			Unit	Notes
		Min.	Typ.	Max.		
C <sub>VBUS</sub>	V <sub>BUS_IN</sub> Decoupling	1.0	4.7	10.0	μF	This is the recommended capacitance in the USB standard (for the downstream port V <sub>BUS</sub> capacitance specification).
C <sub>VBAT</sub>	V <sub>BAT</sub> Decoupling Capacitance		1	10	μF	Increasing this capacitance can help reduce GSM / TDMA noise.
R <sub>BAT</sub>	V <sub>BAT</sub> Series Resistance		50	100	Ω	Adding series resistance can help reduce GSM / TDMA noise. Ensure that resistance is small enough to not reduce V <sub>BAT</sub> levels under normal operation.
R <sub>PU_I2C</sub>	I <sup>2</sup> C Pull-up Resistance		4.7		kΩ	The actual value used must allow compliance to I <sup>2</sup> C specification based on V <sub>DDIO</sub> and bus capacitance.
R <sub>PU_JIG</sub>	JIG Pull-up Resistance (FSA880 ONLY)		100		kΩ	Pull-up resistance for open-drain JIG pin.
R <sub>DP/DM</sub>	DP_CON/DM_CON Series Resistance		2.2		Ω	Series resistance to improve surge performance of high-speed USB path.
TVS	High-Speed TVS Diodes		1		pF	Recommended high-speed TVS diodes to improve ESD performance.
TVS <sub>OPT</sub>	Optional High-Speed TVS Diodes		1		pF	Optional high-speed TVS diodes to improve ESD performance.



NOTES:

- A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC STANDARD.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.
- D. DRAWING FILENAME: MKT-UMLP16ArevG.
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