FAIRCHILD SEMICONDUCTOR®

October 2006

FIN24C
µSerDes™ Low-Voltage 24-Bit Bi-Directional Serializer/Deserializer

Features

- Low power for minimum impact on battery life
  - Multiple power-down modes
  - AC coupling with DC balance
- 100nA in standby mode, 5mA typical operating conditions
- Cable reduction: 25:4 or greater
- Bi-directional operation 50:7 reduction or greater
- Up to 24 bits in either direction
- Up to 20MHz parallel interface operation
- Voltage translation from 1.65V to 3.6V
- Ultra-small and cost-effective packaging
- High ESD protection: >7.5kV HBM
- Parallel I/O power supply (V_{DDP}) range between 1.65V to 3.6V

Applications

- Micro-controller or pixel interfaces
- Image sensors
- Small displays
  - LCD, cell phone, digital camera, portable gaming, printer, PDA, video camera, automotive

General Description

The FIN24C µSerDes™ is a low-power Serializer/Deserializer (SerDes) that can help minimize the cost and power of transferring wide signal paths. Through the use of serialization, the number of signals transferred from one point to another can be significantly reduced. Typical reduction is 4:1 to 6:1 for unidirectional paths. For bi-directional operation, using half duplex for multiple sources, it is possible to increase the signal reduction to close to 10:1. Through the use of differential signaling, shielding and EMI filters can also be minimized, further reducing the cost of serialization. The differential signaling is also important for providing a noise-insensitive signal that can withstand radio and electrical noise sources. Major reduction in power consumption allows minimal impact on battery life in ultra-portable applications. A unique word boundary technique assures that the actual word boundary is identified when the data is deserialized. This guarantees that each word is correctly aligned at the deserializer on a word-by-word basis through a unique sequence of clock and data that is not repeated except at the word boundary. A single PLL is adequate for most applications, including bi-directional operation.

Ordering Information

Order Number	Package Number	Pb-Free	Package Description
FIN24CGFX	BGA042	Yes	42-Ball Ultra Small Scale Ball Grid Array (USS-BGA), JEDEC MO-195, 3.5mm Wide
FIN24CMLX	MLP040	Yes	40-Terminal Molded Leadless Package (MLP), Quad, JEDEC MO-220, 6mm Square

Pb-Free package per JEDEC J-STD-020B. BGA and MLP packages available in tape and reel only.

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Functional Block Diagram

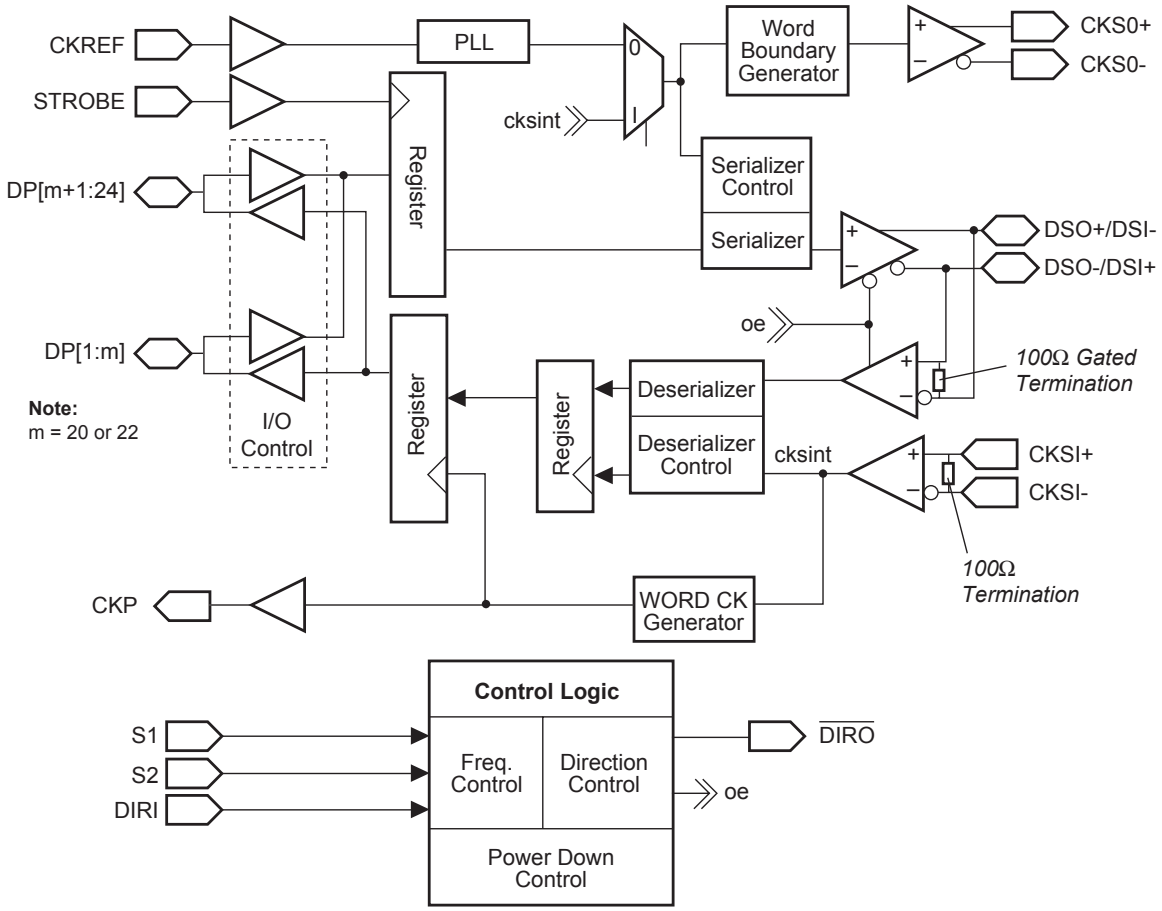


Figure 1. Block Diagram

Terminal Description

Terminal Name	I/O Type	Number of Terminals	Description of Signals
DP[1:20]	I/O	20	LVCMOS Parallel I/O, direction controlled by DIRI Terminal
DP[21:24]	I or O	4	LVCMOS Parallel Unidirectional Inputs or Outputs Dependent on State of S1, S2 Terminals
CKREF	IN	1	LVCMOS Clock Input and PLL Reference
STROBE	IN	1	LVCMOS Strobe Signal for Latching Data into the Serializer
CKP	OUT	1	LVCMOS Word Clock Output
DSO+ / DSI– DSO– / DSI+	DIFF-I/O	2	CTL Differential Serial I/O Data Signals(1) DSO: Refers to output signal pair DSI: Refers to input signal pair DSO(I)+: Positive signal of DSO(I) pair DSO(I)–: Negative signal of DSO(I) pair
CKSI+, CKSI–	DIFF-IN	2	CTL Differential Deserializer Input Bit Clock CKSI: Refers to signal pair CKSI+: Positive signal of CKSI pair CKSI–: Negative signal of CKSI pair
CKSO+, CKSO–	DIFF-OUT	2	CTL Differential Serializer Output Bit Clock CKSO: Refers to signal pair CKSO+: Positive signal of CKSO pair CKSO–: Negative signal of CKSO pair
S1	IN	1	LVCMOS Mode Selection Pins used to define mode of operation for some terminals. The control terminals, DP[21:24] can be set as 4 terminals in the same direction or two in each direction.
S2	IN	1	
DIRI	IN	1	LVCMOS Control Input Used to control direction of Data Flow
$\overline{\text{DIRO}}$	OUT	1	LVCMOS Control Output Inversion of DIRI
V_{DDP}	Supply	1	Power Supply for Parallel I/O and Translation Circuitry
V_{DDS}	Supply	1	Power supply for core circuitry and serial I/O
V_{DDA}	Supply	1	Power Supply for Analog PLL Circuitry
GND	Supply	0	Use Bottom Ground Plane for Ground Signals

Note:

1. The DSO/DSI serial port terminals have been arranged such that when one device is rotated 180° to the other device, the serial connections properly align without the need for any traces or cable signals to cross. Other layout orientations may require that traces or cables cross.

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Connection Diagrams

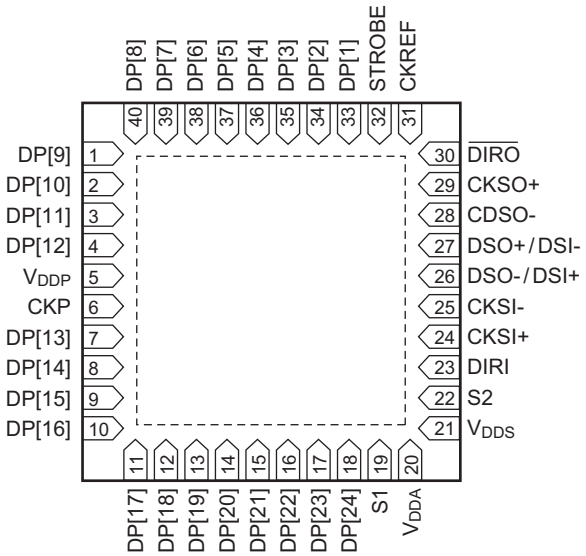
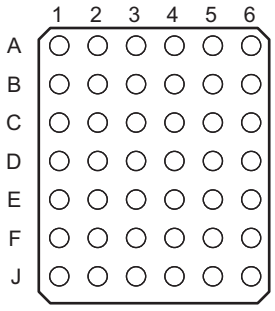


Figure 2. Terminal Assignments for MLP (Top View)



(Top View)

Pin Assignments

	1	2	3	4	5	6
A	DP[9]	DP[7]	DP[5]	DP[3]	DP[1]	CKREF
B	DP[11]	DP[10]	DP[6]	DP[2]	STROBE	$\overline{\text{DIRO}}$
C	CKP	DP[12]	DP[8]	DP[4]	CKSO+	CKSO-
D	DP[13]	DP[14]	V_{DDP}	GND	DSO- / DSI+	DSO+ / DSI-
E	DP[15]	DP[16]	GND	V_{DDS}	CKSI+	CKSI-
F	DP[17]	DP[18]	DP[21]	V_{DDA}	S2	DIRI
J	DP[19]	DP[20]	DP[22]	DP[23]	DP[24]	S1

Figure 3. Terminal Assignments for µBGA

Control Logic Circuitry

The FIN24C has four signals that are selectable as two unidirectional inputs and two unidirectional outputs, or as four unidirectional inputs or four unidirectional outputs. These are often used by applications for control signals. The mode signals S1 and S2 determine the direction of the DP[21:24] data signals. The 00 state provides for a power-down state where all functionality of the device is disabled or reset. The DIRI terminal controls the direction of the device in Modes 1 and 3. When in Mode 2, the direction is controlled by both the DIRI and STROBE signals. Table 1 provides a complete description of the various modes of operation. For unidirectional operation, the DIRI terminal should be hardwired to a valid logic level and the $\overline{\text{DIRO}}$ terminal should be left floating. For bi-directional operation, the $\overline{\text{DIRO}}$ of the master device should be connected to the DIRI of the slave device.

When operating in a bi-directional mode, the turn-around functionality is dependent on the mode of the device. For Modes 1 and 3, the device asynchronously passes and inverts the DIRI signal through the device to the $\overline{\text{DIRO}}$ signal. Care must be taken during design to ensure that no contention occurs between the deserializer outputs and the other devices on this port. Optimally the peripheral device driving the serializer should be in a HIGH-impedance state prior to the DIRI signal being asserted.

When a device with dedicated data outputs turns from a deserializer to a serializer, the dedicated outputs remain at the last logical value asserted. This value only changes if the device is once again turned around into a deserializer and the values are overwritten.

When the device is in Mode 2 (S2 = 1, S1 = 0), the direction of operation is dependent upon both the STROBE signal and the DIRI signal. At power-up, the mode select signals are both LOW and the $\overline{\text{DIRO}}$ signal is the inversion of the DIRI signal. After power-up, the DIRI and STROBE signal should initially both be HIGH. When STROBE goes LOW the device is configured as a serializer and $\overline{\text{DIRO}}$ will be forced LOW. The device remains a serializer until the DIRI signal goes LOW. When DIRI goes LOW, the device is re-configured as a deserializer and the $\overline{\text{DIRO}}$ signal is asserted HIGH.

When operating the SerDes in pairs, not all operating modes are compatible. Regardless of the mode of operation, the serializer is always sending 24 bits of data and two word boundary bits. The deserializer is always receiving 24 bits of data and two word boundary bits. For some modes of operation, not all of the data bits are valid because some pins are dedicated inputs or outputs. A value of “0” is sent in the serial stream for all invalid data bits.

Table 1. Control Logic Circuitry

Mode Number	Inputs				Output	Device State	Description
	S2	S1	STROBE	DIRI	$\overline{\text{DIRO}}$		
0	0	0	x	0	1	na	Power-Down State. The device is powered down and disabled regardless of all other signals.
			x	1	0	na	
1	0	1	x	0	1	Des	4-Bit Unidirectional Control Mode DP[21:24] are outputs
			x	1	0	Ser	
2	1	0	0	0	1	Des	4-Bit Unidirectional Control Mode DP[21:24] are inputs STROBE and DIRI operate as an RS-Latch to change the state of operation. In general, DIRI and Strobe should not be LOW at the same time.
			0	1	0	Ser	
			1	0	1	Des	
			1	1	DIRO (n-1)	Previous	
3	1	1	x	0	1	Des	2-Bit Unidirectional Control Mode DP[21:22] are Inputs DP[23:24] Outputs
	1	1	x	1	0	Ser	2-Bit Unidirectional Control Mode DP[21:22] are Inputs DP[23:24] Outputs

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4-Bit Control Mode

When operating in 4-bit control mode, the master device must be configured as MODE 2 (S2 = 1, S1 = 0) and the slave device must be configured as MODE 1 (S2 = 0, S1 = 1). When operating in this mode, 24 data and control bits can be sent from the master to the slave and 20 data bits can be sent from the slave to the master. Unidirectional control signals should be connected to DP[21:24].

2-Bit Control Mode

When operating in 2-bit control mode, both devices must be configured in MODE 3 (S2 = S1 = "1"). In this mode, 22 bits can be sent in either direction. When operating in a 2-bit control mode, serialized bits 21 and 22 appear on outputs 23 and 24 of the deserializer.

Power-Down Mode: (Mode 0)

Mode 0 is used for powering down and resetting the device. When both of the mode signals are driven to a LOW state, the PLL and references are disabled, differential input buffers are shut off, differential output buffers are placed into a HIGH-impedance state, LVCMOS outputs are placed into a HIGH-impedance state, LVCMOS inputs are driven to a valid level internally, and all internal circuitry is reset. The loss of CKREF state is also enabled to ensure that the PLL only powers up if there is a valid CKREF signal.

In a typical application, the device only changes between the power-down mode and the selected mode of operation. This allows for system-level power-down functionality to be implemented via a single wire for a SerDes pair. The S1 and S2 selection signals that have their operating mode driven to a "logic 0" should be hardwired to GND. The S1 and S2 signals that have their operating mode driven to a "logic 1" should be connected to a system level power-down signal.

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Serializer Operation Mode

The serializer configuration is described in the following sections. The basic serialization circuitry works essentially the same in these modes, but the actual data and clock streams differ depending on if CKREF is the same as the STROBE signal or not. When CKREF equals STROBE, the CKREF and STROBE signals are hardwired together as one signal. When CKREF does not equal STROBE, each signal is distinct and CKREF must be running at a frequency high enough to avoid any loss of data condition. CKREF must never be a lower frequency than STROBE.

Serializer Operation: (Figure 4)
DIRI = 1,
CKREF = STROBE

The Phase-Locked Loop (PLL) must receive a stable CKREF signal to achieve lock prior to any valid data being sent. The CKREF signal can be used as the data STROBE signal, provided that data can be ignored during the PLL lock phase.

Once the PLL is stable and locked, the device can begin to capture and serialize data. Data is captured on the rising edge of the STROBE signal and then serialized. The serialized data stream is synchronized and sent source synchronously with a bit clock with an embedded word boundary. Serialized data is sent at 26 times the CKREF clock rate. Two additional data bits are sent that define the word boundary. When in this mode, the internal deserializer circuitry is disabled; including the serial clock, serial data input buffers, the bidirectional parallel outputs, and the CKP word clock. The CKP word clock is driven HIGH.

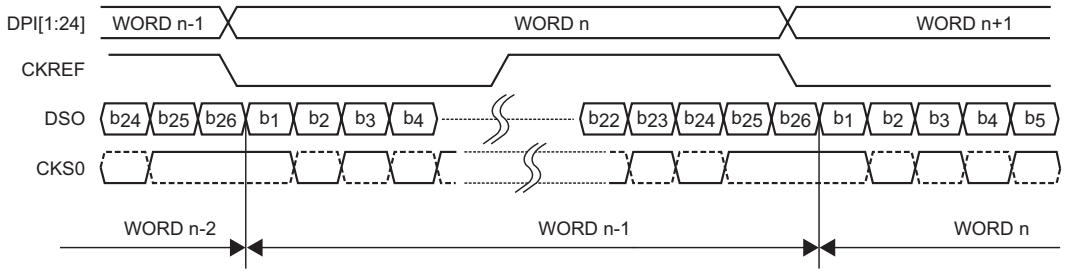


Figure 4. Serializer Timing Diagram (CKREF equals STROBE)

Serializer Operation: (Figure 5),
DIRI = 1,
CKREF does not = STROBE

If the same signal is not used for CKREF and STROBE, the CKREF signal must be run at a higher frequency than the STROBE rate to serialize the data correctly. The actual serial transfer rate remains at 26 times the CKREF frequency. A data bit value of zero is sent when no valid data is present in the serial bit stream. The operation of the serializer otherwise remains the same.

The exact frequency that the reference clock needs is dependent upon the stability of the CKREF and STROBE signal. If the source of the CKREF signal implements spread spectrum technology, the maximum frequency of this spread spectrum clock should be used in calculating the ratio of STROBE frequency to the CKREF frequency. Similarly if the STROBE signal has significant cycle-to-cycle variation, the maximum cycle-to-cycle time needs to be factored into the selection of the CKREF frequency.

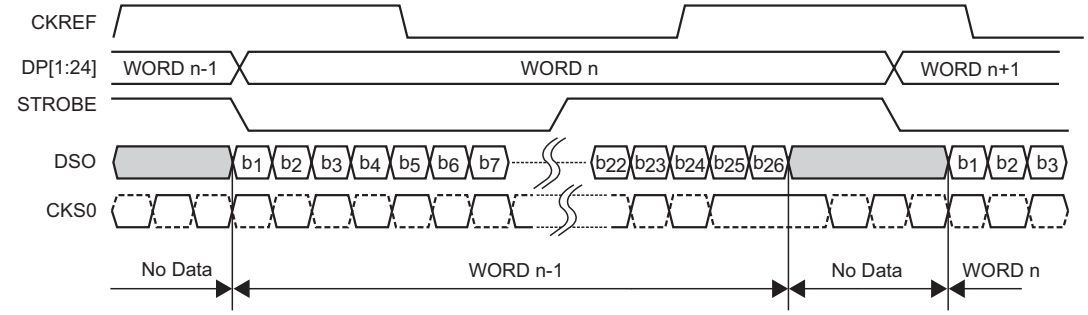


Figure 5. Serializer Timing Diagram (CKREF does not equal STROBE)

Serializer Operation Mode (Continued)

Serializer Operation: (Figure 6), DIRI = 1, No CKREF

A third method of serialization can be accomplished with a free running bit clock on the CKSI signal. This mode is enabled by grounding the CKREF signal and driving the DIRI signal HIGH.

At power-up, the device is configured to accept a serialization clock from CKSI. If a CKREF is received, the device enables the CKREF serialization mode. The device remains in this mode even if CKREF is stopped. To re-enable this mode, the device must be powered down and powered back up with “logic 0” on CKREF.

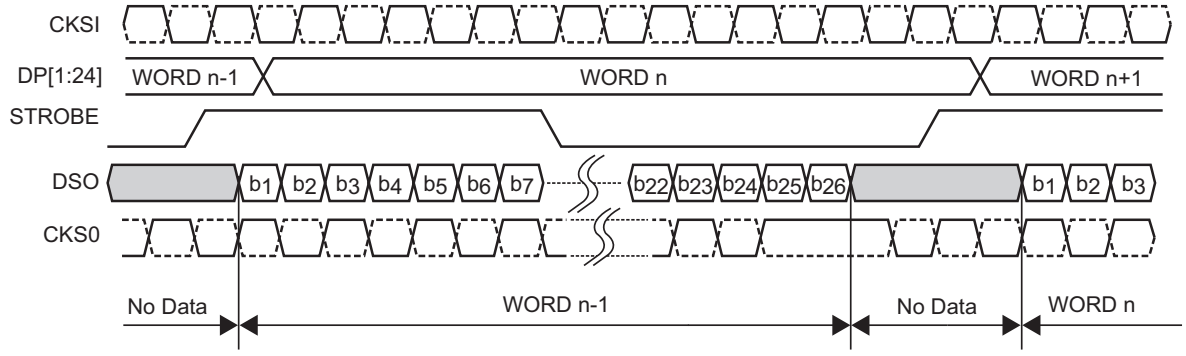


Figure 6. Serializer Timing Diagram Using Provided Bit Clock (No CKREF)

Deserializer Operation Mode

The operation of the deserializer is only dependent upon the data received on the DSI data signal pair and the CKSI clock signal pair. The following two sections describe the operation of the deserializer under two distinct serializer source conditions. References to the CKREF and STROBE signals refer to the signals associated with the serializer device used in generating the serial data and clock signals that are inputs to the deserializer.

When operating in this mode, the internal serializer circuitry is disabled, including the parallel data input buffers. If there is a CKREF signal provided, the CKSO serial clock continues to transmit bit clocks. Upon device power-up (S1 or S2 = 1), all deserializer output data pins are driven LOW until valid data is passed through the deserializer.

Deserializer Operation: DIRI = 0 (Serializer Source: CKREF = STROBE)

When the DIRI signal is asserted LOW, the device is configured as a deserializer. Data is captured on the serial port and deserialized through use of the bit clock sent with the data. The word boundary is defined in the actual clock and data signal. Parallel data is generated at the time the word boundary is detected. The falling edge of CKP occurs approximately six bit times after the next falling edge of CKSI. The rising edge of CKP goes HIGH approximately 13 bit times after CKP goes LOW. When no embedded word boundary occurs, no pulse is generated on CKP and CKP remains HIGH.

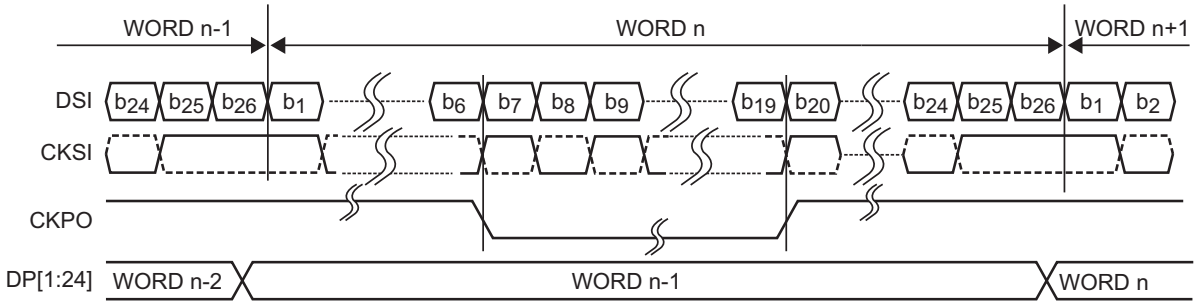


Figure 7. Deserializer Timing Diagram (Serializer Source: CKREF equals STROBE)

Deserializer Operation: DIRI = 0 (Serializer Source: CKREF does not = STROBE)

The logical operation of the deserializer remains the same if the CKREF is equal in frequency to the STROBE or at a higher frequency than the STROBE. The actual serial data stream presented to the deserializer, however, differs because it has non-valid data bits sent between words. The duty cycle of CKP varies based on the ratio of the frequency of the CKREF signal to the STROBE signal. The frequency of the CKP signal is equal to the STROBE frequency. The falling edge of CKP occurs six bit times after the data transition. The LOW time of the CKP signal is equal to half (13 bit times) of the CKREF period. The CKP HIGH time is equal to STROBE period – half of the CKREF period. Figure 8 is representative of a waveform that could be seen when CKREF is not equal to STROBE. If CKREF is significantly faster, additional non-valid data bits occur between data words.

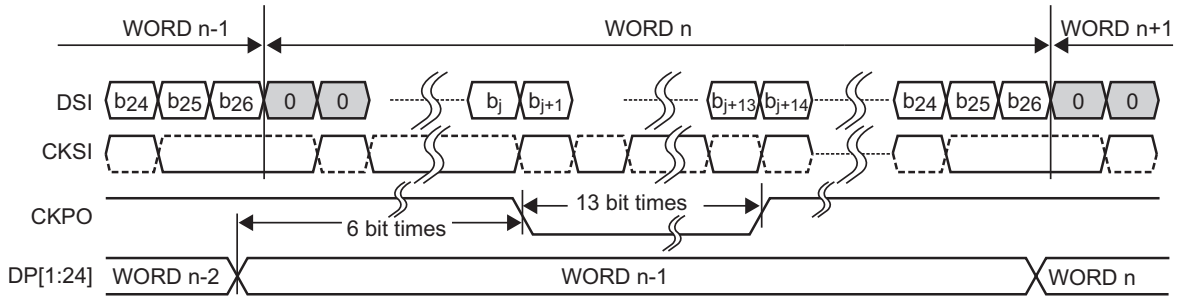


Figure 8. Deserializer Timing Diagram (Serializer Source: CKREF does not equal STROBE)

Embedded Word Clock Operation

The FIN24C sends and receives serial data source synchronously with a bit clock. The bit clock has been modified to create a word boundary at the end of each data word. The word boundary has been implemented by skipping a LOW clock pulse. This appears in the serial clock stream as three consecutive bit times where signal CKSO remains HIGH.

To implement this sort of scheme, two extra data bits are required. During the word boundary phase, the data toggles either HIGH-then-LOW or LOW-then-HIGH dependent upon the last bit of the actual data word. Table 2 provides some examples of the actual data word and the data word with the word boundary bits added. Note that a 24-bit word is extended to 26 bits during serial transmission. Bit 25 and Bit 26 are defined with-respect-to Bit 24. Bit 25 is always the inverse of Bit 24 and Bit 26 is always the same as Bit 24. This ensures that a "0" → "1" and a "1" → "0" transition always occurs during the embedded word phase where CKSO is HIGH.

The serializer generates the word boundary data bits and the boundary clock condition and embeds them into the serial data stream. The deserializer looks for the end of the word boundary condition to capture and transfer the data to the parallel port. The deserializer only uses the embedded word boundary information to find and capture the data. These boundary bits are stripped prior to the word being sent out the parallel port.

LVCMOS Data I/O

The LVCMOS input buffers have a nominal threshold value equal to half V_{DDP}. The input buffers are only operational when the device is operating as a serializer. When the device is operating as a deserializer, the inputs are gated off to conserve power.

The LVCMOS 3-STATE output buffers are rated for a source/sink current of 2mAs at 1.8V. The outputs are active when the DIRI signal is asserted LOW. When the DIRI signal is asserted HIGH, the bi-directional LVCMOS I/Os are in a HIGH-Z state. Under purely capacitive load conditions, the output swings between GND and V_{DDP}.

Unused LVCMOS input buffers must be tied off to either a valid logic LOW or a valid logic HIGH level to prevent static current draw due to a floating input. Unused LVCMOS outputs should be left floating. Unused bidirectional pins should be connected to GND through a high-value resistor. If a FIN24C devices is configured as an unidirectional serializer, unused data I/O can be treated as unused inputs. If the FIN24C is hardwired as a deserializer, unused date I/O can be treated as unused outputs.

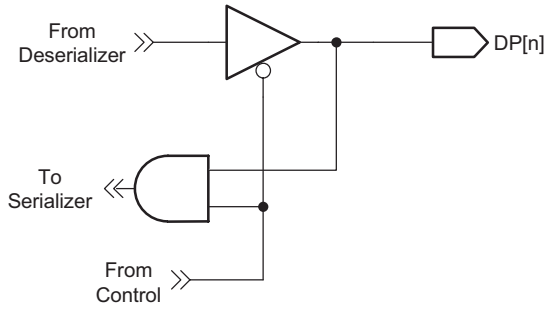


Figure 9. LVCMOS I/O

Differential I/O Circuitry

The FIN24C employs FSC proprietary CTL I/O technology. CTL is a low-power, low-EMI differential swing I/O technology. The CTL output driver generates a constant output source and sink current. The CTL input receiver senses the current difference and direction from the output buffer to which it is connected. This differs from LVDS, which uses a constant current source output, but a voltage sense receiver. Like LVDS, an input source termination resistor is required to properly terminate the transmission line. The FIN24C device incorporates an internal termination resistor on the CKSI receiver and a gated internal termination resistor on the DS input receiver. The gated termination resistor ensures proper termination regardless of direction of data flow. The relatively greater sensitivity of the current sense receiver of CTL allows it to work at much lower current drive and a much lower voltage.

During power-down mode, the differential inputs are disabled and powered down and the differential outputs are placed in a HIGH-Z state. CTL inputs have an inherent fail-safe capability that supports floating inputs. When the CKSI input pair of the serializer is unused, it can reliably be left floating. Alternately both of the inputs can be connected to ground. CTL inputs should never be connected to V_{DD}. When the CKSO output of the deserializer is unused, it should be allowed to float.

Table 2. Word Boundary Data Bits

24-Bit Data Words		24-Bit Data Word with Word Boundary	
Hex	**Binary**	**Hex**	**Binary**
FFFFFFh	1111 1111 1111 1111 1111 1111b	2FFFFFFh	10 1111 1111 1111 1111 1111 1111b
555555h	0101 0101 0101 0101 01010 0101b	1555555h	01 0101 0101 0101 0101 0101 0101b
xxxxxxh	0xxx xxxx xxxx xxxx xxxx xxxxb	1xxxxxxh	01 0xxx xxxx xxxx xxxx xxxx xxxxb
xxxxxxh	1xxx xxxx xxxx xxxx xxxx xxxxb	2xxxxxxh	10 1xxx xxxx xxxx xxxx xxxx xxxxb

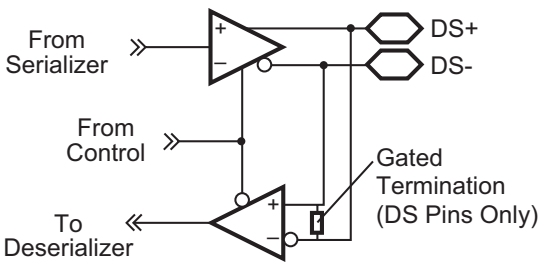


Figure 10. Bi-Directional Differential I/O Circuitry

PLL Circuitry

The CKREF input signal is used to provide a reference to the PLL. The PLL generates internal timing signals capable of transferring data at 26 times the incoming CKREF signal. The output of the PLL is a bit clock sent with the serial data stream.

There are two ways to disable the PLL: by entering the Mode 0 state (S1 = S2 = 0) or upon detecting a LOW on both the S1 and S2 signals. Any of the other modes are entered by asserting either S1 or S2 HIGH and by providing a CKREF signal. The PLL powers up and goes through a lock sequence. Wait the specified number of clock cycles prior to capturing valid data into the parallel port. When the µSerDes chipset transitions from a power-down state (S1, S2 = 0, 0) to a powered state (example S1, S2 = 1, 1), CKP on the deserializer transitions LOW for a short duration, then returns HIGH. Following this, the signal level of the deserializer at CKP corresponds to the serializer signal levels.

An alternate way of powering down the PLL is by stopping the CKREF signal either HIGH or LOW. Internal circuitry detects the lack of transitions and shuts the PLL and serial I/O down. Internal references, however, are not disabled, allowing the PLL to power-up and re-lock in a lesser number of clock cycles than when exiting Mode 0. When a transition is seen on the CKREF signal, the PLL is reactivated.

Application Mode Diagrams MODE = 3: Unidirectional Data Transfer

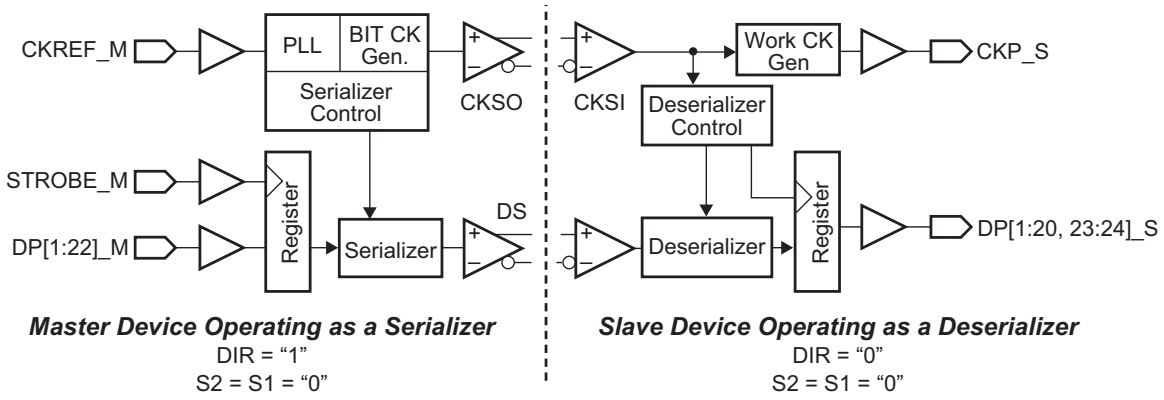


Figure 11. Simplified Block Diagram for Unidirectional Serializer and Deserializer

Figure 11 shows basic operation when a pair of SerDes is configured in an unidirectional operation mode.

In Master Operation, the device:

1. Is configured as a serializer at power-up based on the value of the DIRI signal.
2. Accepts CKREF_M word clock and generate a bit clock with embedded word boundary. This bit clock is sent to the slave device through the CKSO port.
3. Receives parallel data on the rising edge of STROBE_M.
4. Generates and transmits serialized data on the DS signals source synchronous with CKSO.
5. Generates an embedded word clock for each strobe signal.

In Slave Operation, the device:

1. Is configured as a deserializer at power-up based on the value of the DIRI signal.
2. Accepts an embedded word boundary bit clock on CKSI.
3. Deserializes the DS data stream using the CKSI input clock.
4. Writes parallel data onto the DP_S port and generates the CKP_S. CKP_S is only generated when a valid data word occurs.

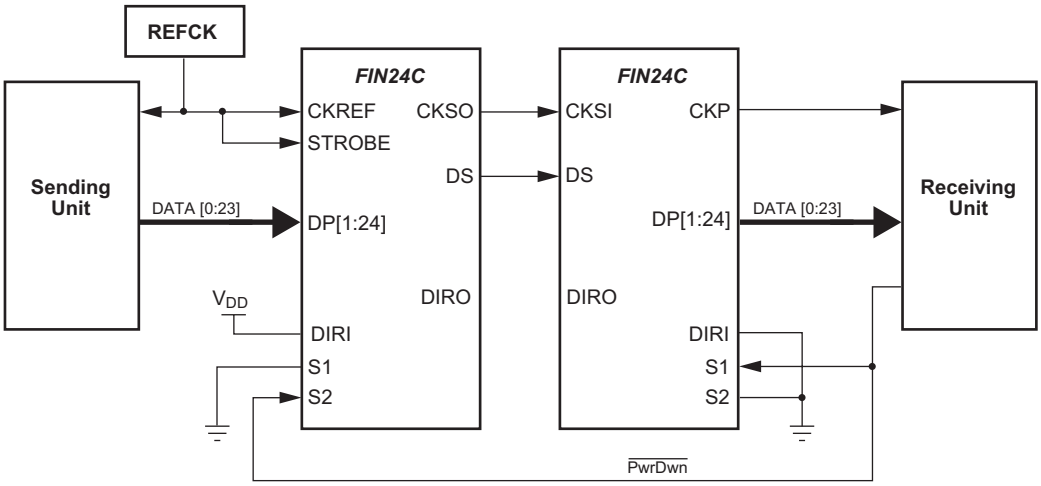


Figure 12. 24-Bit Unidirectional Serializer and Deserializer

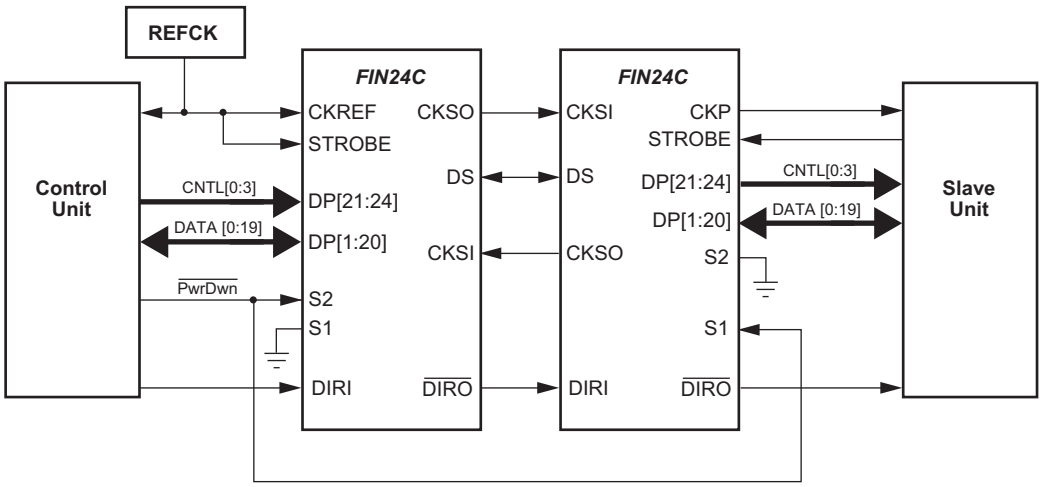


Figure 13. Unidirectional Control, Bi-directional Data Interface

Flex Circuit Design Guidelines

The serial I/O information is transmitted at a high serial rate. Care must be taken implementing this serial I/O flex cable. The following best practices should be used when developing the flex cabling or Flex PCB:

- Keep all four differential wires the same length.
- Allow no noisy signals over or near differential serial wires. Example: No LVCMOS traces over differential wires.
- Use only one ground plane or wire over the differential serial wires. Do not run ground over top and bottom.
- Do not place test points on differential serial wires.
- Use differential serial wires a minimum of 2cm away from the antenna.

Absolute Maximum Ratings

The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table defines the conditions for actual device operation.

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Supply Voltage	-0.5	+4.6	V
	All Input/Output Voltage	-0.5	+4.6	V
	LVDS Output Short-Circuit Duration	Continuous		
T_{STG}	Storage Temperature Range	-65	+150	°C
T_J	Maximum Junction Temperature		+150	°C
T_L	Lead Temperature (Soldering, 4 seconds)		+260	°C
	ESD Rating Human Body Model, 1.5k¾, 100pF All Pins CKSO, CKSI, DSO to GND	 > 2 > 7.5		 kV kV

Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Unit
V_{DDA}, V_{DDS}	Supply Voltage	2.5	2.9	V
V_{DDP}	Supply Voltage	1.65	3.6	V
T_A	Operating Temperature	-30	+70	°C
V_{DDA-PP}	Supply Noise Voltage		100	mVp-p

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DC Electrical Characteristics

Values are provided for over-supply voltage and operating temperature ranges, unless otherwise specified.

Symbol	Parameter	Test Conditions		Min.	Typ.(2)	Max.	Unit
LVCMOS I/O							
V_{IH}	Input High Voltage			0.65 x V_{DDP}		V_{DDP}	V
V_{IL}	Input Low Voltage			GND		0.35 x V_{DDP}	V
V_{OH}	Output High Voltage	I_{OH} = –2.0 mA	V_{DDP} = 3.3 ± 0.3	0.75 x V_{DDP}			V
			V_{DDP} = 2.5 ± 0.2				
			V_{DDP} = 1.8 ± 0.15				
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA	V_{DDP} = 3.3 ± 0.3			0.25 x V_{DDP}	V
			V_{DDP} = 2.5 ± 0.2				
			V_{DDP} = 1.8 ± 0.15				
I_{IN}	Input Current	V_{IN} = 0V to 3.6V		–5.0		5.0	µA
DIFFERENTIAL I/O							
I_{ODH}	Output High Source Current	V_{OS} = 1.0V, Figure 14			1.75		mA
I_{ODL}	Output Low Sink Current	V_{OS} = 1.0V, Figure 14			0.95		mA
I_{OZ}	Disabled Output Leakage Current	CKSO, DSO = 0V to V_{DDS}, S2 = S1 = 0V			±0.1	±5.0	µA
I_{IZ}	Disabled Input Leakage Current	CKSI, DSI = 0V to V_{DDS}, S2 = S1 = 0V			±0.1	±5.0	µA
V_{ICM}	Input Common Mode Range	V_{DDS} = 2.775 ± 5%			V_{GO} + 0.80		V
V_{GO}	Input Voltage Ground Off-set Relative to Driver(3)	See Figure 15			0		V
R_{TRM}	CKSI Internal Receiver Termination Resistor	V_{ID} = 50mV, V_{IC} = 925mV, DIRI = 0, | CKSI+ – CKSI- | = V_{ID}		80.0	100	120	¾
R_{TRM}	DSI Internal Receiver, Termination Resistor	V_{ID} = 50mV, V_{IC} = 925mV, DIRI = 0, | DSI+ – DSI- | = V_{ID}		80.0	100	120	¾

Notes:

2. Typical Values are given for V_{DD} = 2.775V and T_A = 25°C. Positive current values refer to the current flowing into device and negative values means current flowing out of pins. Voltage is referenced to GROUND unless otherwise specified (except ΔV_{OD} and V_{OD}).
3. V_{GO} is the difference in device ground levels between the CTL driver and the CTL receiver.

Power Supply Currents

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Units
I_{DDA1}	V_{DDA} Serializer Static Supply Current	All DPI and Control Inputs at 0V or V_{DDP}, NO CKREF, S2 = 0, S1 = 1, DIRI = 1			450		µA
I_{DDA2}	V_{DDA} Deserializer Static Supply Current	All DPI and Control Inputs at 0 or V_{DDP}, NO CKREF, S2 = 0, S1 = 1, DIRI = 1			550		µA
I_{DDS1}	V_{DDS} Serializer Static Supply Current	All DPI and Control Inputs at 0V or V_{DDP}, NO CKREF, S2 = 0, S1 = 1, DIRI = 1			4.0		mA
	V_{DDS} Deserializer Static Supply Current	All DPI and Control Inputs at 0V or V_{DDP}, NO CKREF, S2 = 0, S1 = 1, DIRI = 0			4.5		
I_{DD_PD}	V_{DD} Power-Down Supply Current $I_{DD_PD} = I_{DDA} + I_{DDS} + I_{DDP}$	S1 = S2 = 0, All Inputs at GND or V_{DDP}			0.1		µA
I_{DD_SER1}	26:1 Dynamic Serializer Power Supply Current $I_{DD_SER1} = I_{DDA} + I_{DDS} + I_{DDP}$	CKREF = STROBE DIRI = H See Figure 16	10MHz		11.0		mA
			20MHz		16.0		
I_{DD_DES1}	1:26 Dynamic Deserializer Power Supply Current $I_{DD_DES1} = I_{DDA} + I_{DDS} + I_{DDP}$	CKREF = STROBE DIRI = L See Figure 16	10MHz		7.5		mA
			20MHz		10.0		
I_{DD_SER2}	26:1 Dynamic Serializer Power Supply Current $I_{DD_SER2} = I_{DDA} + I_{DDS} + I_{DDP}$	NO CKREF, STROBE Active CKSI = 15X Strobe DIRI = H, See Figure 16	10 MHz		10.0		mA
			15 MHz		12.0		

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AC Electrical Characteristics

Values are provided for over-supply voltage and operating temperature ranges, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.[4]	Max.	Units
SERIALIZER INPUT OPERATING CONDITIONS						
t_{TCP}	CKREF Clock Period (10 MHz–20 MHz)	See Figure 20	50.0	T	100	ns
f_{REF}	CKREF Frequency Relative to Strobe Frequency	CKREF does not equal STROBE	1.1 x f_{ST}		20.0	MHz
t_{CPWH}	CKREF Clock High Time		0.2	0.5		T
t_{CPWL}	CKREF Clock Low Time		0.2	0.5		T
t_{CLKT}	LVCMOS Input Transition Time	See Figure 20			90.0	ns
t_{SPWH}	STROBE Pulse Width HIGH/LOW	See Figure 20	(T x 4) / 26		(T x 22) / 26	ns
f_{MAX}	Maximum Serial Data Rate	CKREF x 26	260		520	Mb/s
t_{STC}	$DP_{(n)}$ Setup to STROBE	DIRI = 1, See Figure 9 (f = 5MHz)	2.5			ns
t_{HTC}	$DP_{(n)}$ Hold to STROBE		2.0			ns
f_{REF}	CKREF Frequency Relative to Strobe Frequency	CKREF Does Not Equal STROBE	1.1 x f_{STROBE}		20.0	MHz
SERIALIZER AC ELECTRICAL CHARACTERISTICS						
t_{TCCD}	Transmitter Clock Input to Clock Output Delay	See Figure 23, DIRI = 1, CKREF = STROBE	33a + 1.5		35a + 6.5	ns
t_{SPOS}	CKSO Position Relative to DS	See Figure 27[5]	–50.0		250	ps
PLL AC ELECTRICAL CHARACTERISTICS						
t_{TPLLS0}	Serializer PLL Stabilization Time	See Figure 22			200	µs
t_{TPLLD0}	PLL Disable Time Loss of Clock	See Figure 27			30.0	µs
t_{TPLLD1}	PLL Power-Down Time	See Figure 28[6]			20.0	ns
DESERIALIZER INPUT OPERATION CONDITIONS						
t_{S_DS}	Serial Port Setup Time, DS-to-CKSI	See Figure 25[7]	1.4			ns
t_{H_DS}	Serial Port Hold Time, DS-to-CKS	See Figure 25[7]	–250			ps
DESERIALIZER AC ELECTRICAL CHARACTERISTICS						
t_{RCOP}	Deserializer Clock Output (CKP OUT) Period	See Figure 21	50.0	T	500	ns
t_{RCOL}	CKP OUT Low Time	See Figure 21 (Rising Edge Strobe) Serializer Source STROBE = CKREF Where a = (1 / f) / 26[8]	13a-3		13a+3	ns
t_{RCOH}	CKP OUT High Time		13a-3		13a+3	ns
t_{PDV}	Data Valid to CKP LOW	See Figure 21 (Rising Edge Strobe) Where a = (1 / f) / 26[8]	8a-6		8a+1	ns
t_{ROLH}	Output Rise Time (20% to 80%)	C_L = 5pF		2.5		ns
t_{ROHL}	Output Fall Time (80% to 20%)	See Figure 18		2.5		ns

Notes:

4. Typical Values are given for V_{DD} = 2.775V and T_A = 25°C. Positive current values refer to the current flowing into device and negative values refer to current flowing out of pins. Voltage is referenced to GROUND unless otherwise specified (except ΔV_{OD} and V_{OD}).
5. Skew is measured from either the rising or falling edge of CKSO clock to the rising or falling edge of data (DSO). Signals are edge aligned. Both outputs should have identical load conditions for this test to be valid.
6. The power-down time is a function of the CKREF frequency prior to CKREF being stopped HIGH or LOW and the state of the S1/S2 mode pins. The specific number of clock cycles required for the PLL to be disabled varies based on the operating mode of the device.
7. Signals are transmitted from the serializer source synchronously. In some cases, data is transmitted when the clock remains at a high state. Skew should only be measured when data and clock are transitioning at the same time. Total measured input skew is a combination of output skew from the serializer, load variations, and ISI and jitter effects.
8. Rising edge of CKP appears approximately 13 bit times after the falling edge of the CKP output. Falling edge of CKP occurs approximately eight bit times after a data transition or six bit times after the first falling edge of CSKO. Variation of the data with respect to the CKP signal is due to internal propagation delay differences of the data and CKP path and propagation delay differences on the various data pins. If the CKREF is not equal to STROBE for the serializer, the CKP signal does not maintain a 50% duty cycle. The low time of the CKP remains 13 bit times.

Control Logic Timing Controls

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
t_{PHL_DIR}, t_{PLH_DIR}	Propagation Delay DIRI-to-$\overline{DIRO}$	DIRI LOW-to-HIGH or HIGH-to-LOW			17.0	ns
t_{PLZ}, t_{PHZ}	Propagation Delay DIRI-to-DP	DIRI LOW-to-HIGH			25.0	ns
t_{PZL}, t_{PZH}	Propagation Delay DIRI-to-DP	DIRI HIGH-to-LOW			25.0	ns
t_{PLZ}, t_{PHZ}	Deserializer Disable Time: S0 or S1 to DP	DIRI = 0, S1(2) = 0 and S2(1) = LOW-to-HIGH, Figure 30			25.0	ns
t_{PZL}, t_{PZH}	Deserializer Enable Time: S0 or S1 to DP	DIRI = 0,(10) S1(2) = 0 and S2(1) = LOW-to-HIGH, Figure 30			2.0	µs
t_{PLZ}, t_{PHZ}	Serializer Disable Time: S0 or S1 to CKSO, DS	DIRI = 1, S1(2) = 0 and S2(1) = HIGH-to-LOW, Figure 28			25.0	ns
t_{PZL}, t_{PZH}	Serializer Enable Time: S0 or S1 to CKSO, DS	DIRI = 1, S1(2) and S2(1) = LOW-to-HIGH, Figure 28			65.0	ns

Note:

9. Deserializer enable time includes the amount of time required for internal voltage and current references to stabilize. This time is significantly less than the PLL lock time and does not impact overall system startup time.

Capacitance

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
C_{IN}	Capacitance of Input Only Signals, CKREF, STROBE, S1, S2, DIRI	DIRI = 1, S1 = S2 = 0, V_{DDP} = 2.5V		2.0		pF
C_{IO}	Capacitance of Parallel Port Pins DP[1:12]	DIRI = 1, S1 = S2 = 0, V_{DDP} = 2.5V		2.0		pF
$C_{IO-DIFF}$	Capacitance of Differential I/O Signals	DIRI = 0, S1 = S2 = 0, V_{DDP} = 2.775V		2.0		pF

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AC Loading and Waveforms

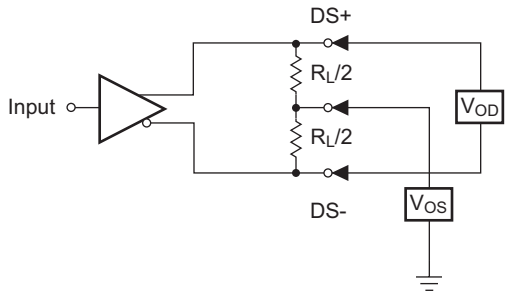


Figure 14. Differential CTL Output DC Test Circuit

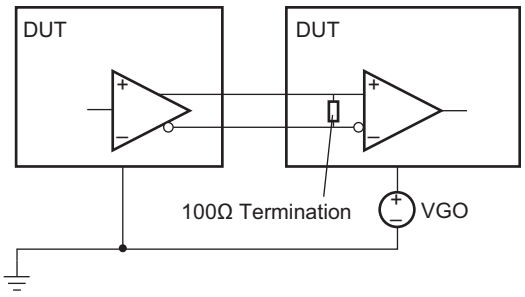
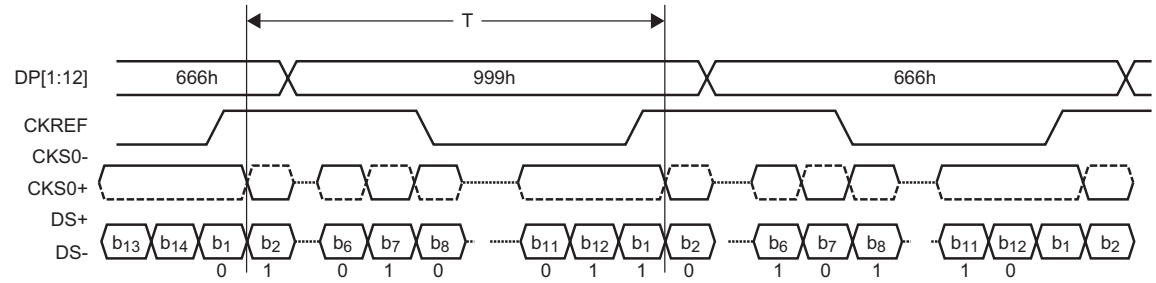


Figure 15. CTL Input Common Mode Test Circuit



Note:
The "worst-case" test pattern produces a maximum toggling of internal digital circuits, CTL I/O and LVCMOS I/O with the PLL operating at the reference frequency, unless otherwise specified. Maximum power is measured at the maximum V_{DD} values. Minimum values are measured at the minimum V_{DD} values. Typical values are measured at V_{DD} = 2.775V.

Figure 16. "Worst Case" Serializer Test Pattern

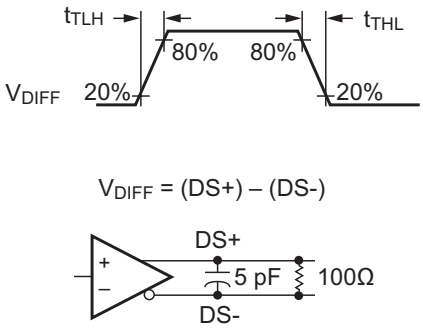


Figure 17. CTL Output Load and Transition Times

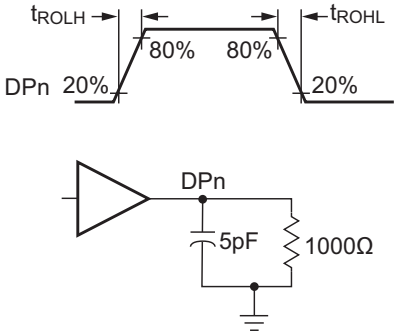
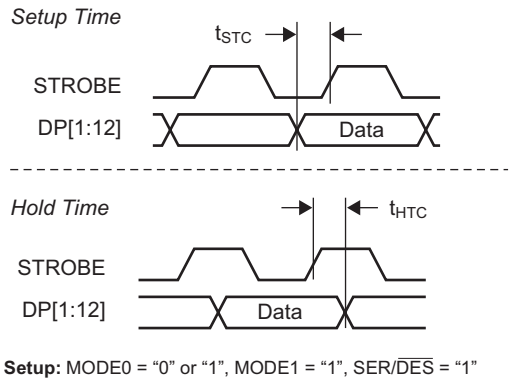


Figure 18. LVCMOS Output Load and Transition Times

AC Loading and Waveforms (Continued)



Setup: MODE0 = "0" or "1", MODE1 = "1", SER/$\overline{DES}$ = "1"

Figure 19. Serial Setup and Hold Time

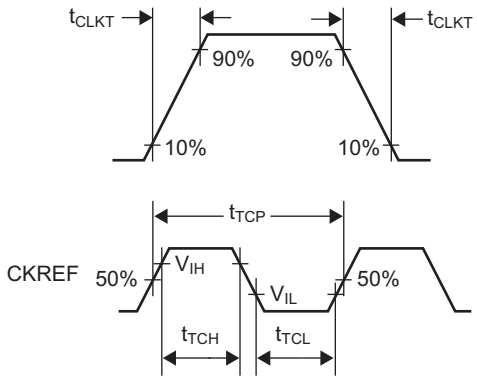
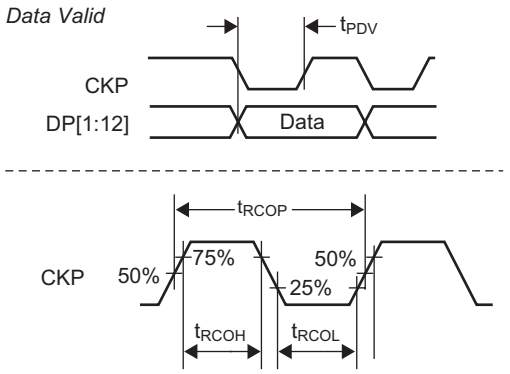
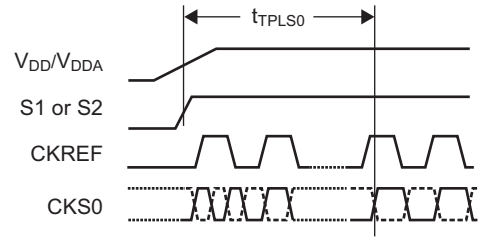


Figure 20. LVCMOS Clock Parameters



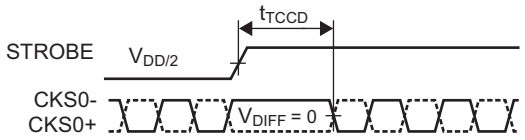
Setup: EN_DES = "1", CKSI, and DSI are valid signals.

Figure 21. Deserializer Data Valid Window Time and Clock Output Parameters



Note: CKREF signal is free running.

Figure 22. Serializer PLL Lock Time



Note: STROBE = CKREF

Figure 23. Serializer Clock Propagation Delay

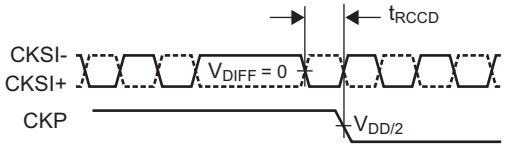


Figure 24. Deserializer Clock Propagation Delay

AC Loading and Waveforms (Continued)

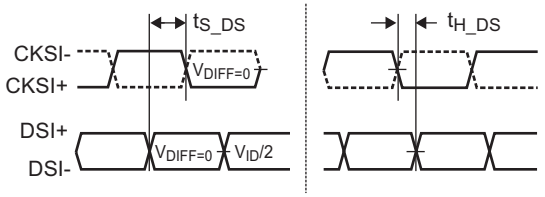
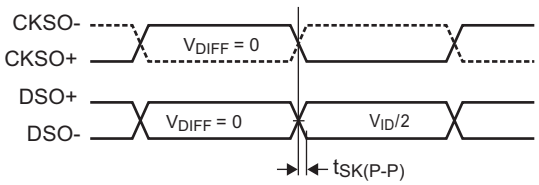
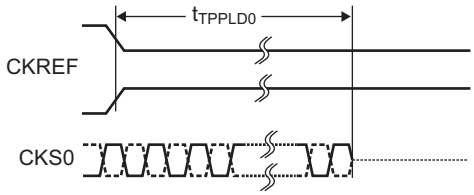


Figure 25. Differential Input Setup and Hold Times



Note: Data is typically edge aligned with the clock.

Figure 26. Differential Output Signal Skew



Note: CKREF Signal can be stopped either HIGH or LOW.

Figure 27. PLL Loss of Clock Disable Time

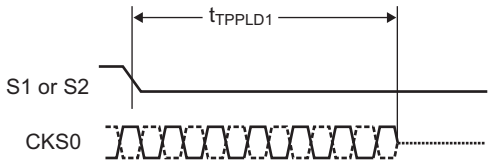
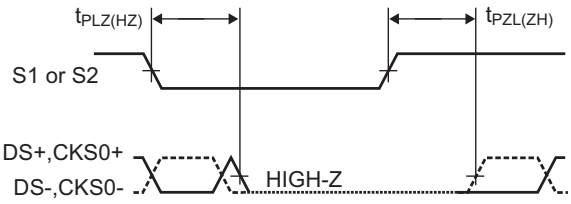
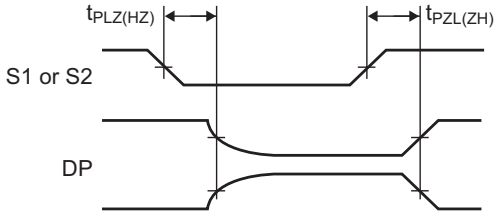


Figure 28. PLL Power-Down Time



Note: CKREF must be active and PLL must be stable.

Figure 29. Serializer Enable and Disable Time



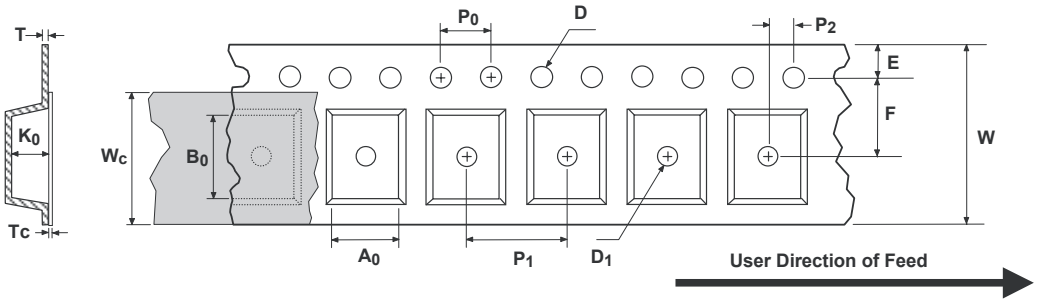
Note: If S1(2) transitioning, S2(1) must = 0 for test to be valid.

Figure 30. Deserializer Enable and Disable Times

Tape and Reel Specification

Dimensions are in millimeters unless otherwise noted.

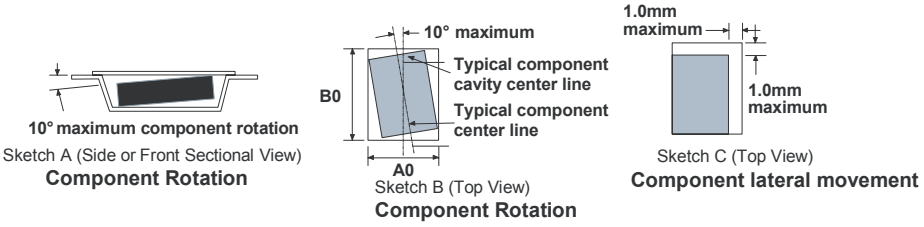
BGA Embossed Tape Dimension



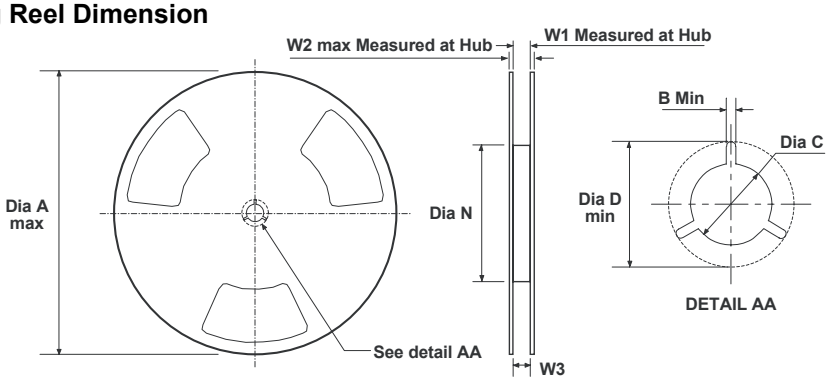
Package	A_0 ±0.1	B_0 ±0.1	D ±0.05	D_1 Min.	E ±0.1	F ±0.1	K_0 ±0.1	P_1 Typ.	P_0 Typ.	P_2 ±0/05	T Typ.	T_C ±0.005	W ±0.3	W_C Typ.
3.5 x 4.5	TBD	TBD	1.55	1.5	1.75	5.5	1.1	8.0	4.0	2.0	0.3	0.07	12.0	9.3

Note:

10. A0, B0, and K0 dimensions are determined with respect to the EIA/JEDEC RS-481 rotational and lateral movement requirements (see sketches A, B, and C).



Shipping Reel Dimension

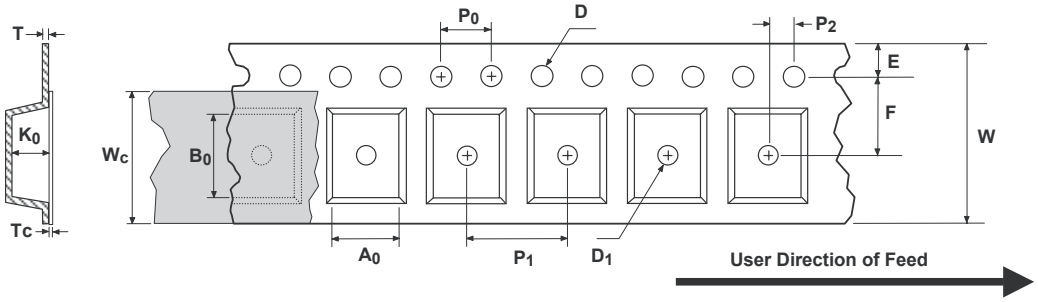


Tape Width	Dia A Max.	Dim B Min.	Dia C +0.5/–0.2	Dia D Min.	Dim N Min.	Dim W1 +2.0/–0	Dim W2 Max.	Dim W3 (LSL–USL)
8	330	1.5	13.0	20.2	178	8.4	14.4	7.9 ~ 10.4
12	330	1.5	13.0	20.2	178	12.4	18.4	11.9 ~ 15.4
16	330	1.5	13.0	20.2	178	16.4	22.4	15.9 ~ 19.4

Tape and Reel Specification (Continued)

Dimensions are in millimeters unless otherwise noted.

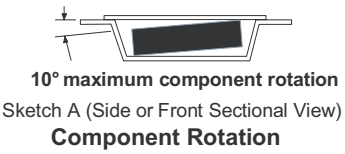
MLP Embossed Tape Dimension



Package	A_0 ±0.1	B_0 ±0.1	D ±0.05	D_1 Min.	E ±0.1	F ±0.1	K_0 ±0.1	P_1 Typ.	P_0 Typ.	P_2 ±0/05	T Typ.	T_C ±0.005	W ±0.3	W_C Typ.
5 x 5	5.35	5.35	1.55	1.5	1.75	5.5	1.4	8	4	2.0	0.3	0.07	12	9.3
6 x 6	6.30	6.30	1.55	1.5	1.75	5.5	1.4	8	4	2.0	0.3	0.07	12	9.3

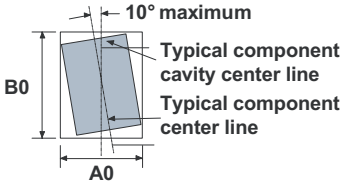
Note:

11. Ao, Bo, and Ko dimensions are determined with respect to the EIA/JEDEC RS-481 rotational and lateral movement requirements (see sketches A, B, and C).



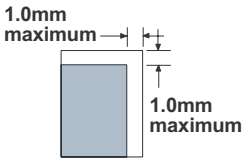
Sketch A (Side or Front Sectional View)

Component Rotation



Sketch B (Top View)

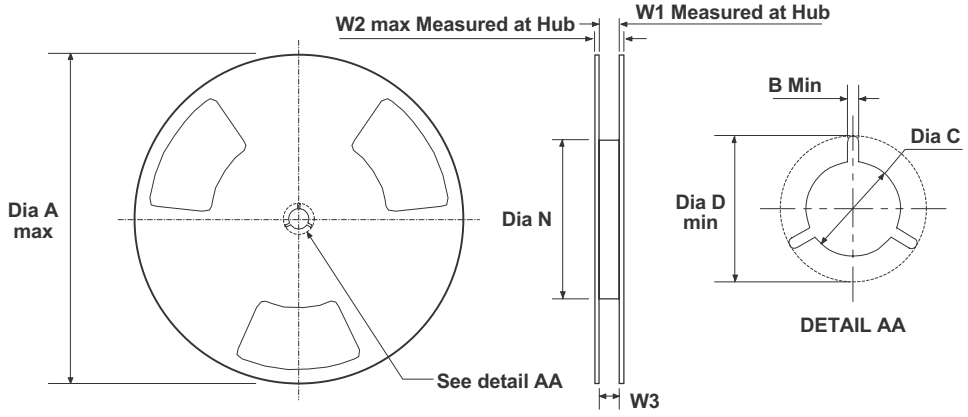
Component Rotation



Sketch C (Top View)

Component lateral movement

Shipping Reel Dimension

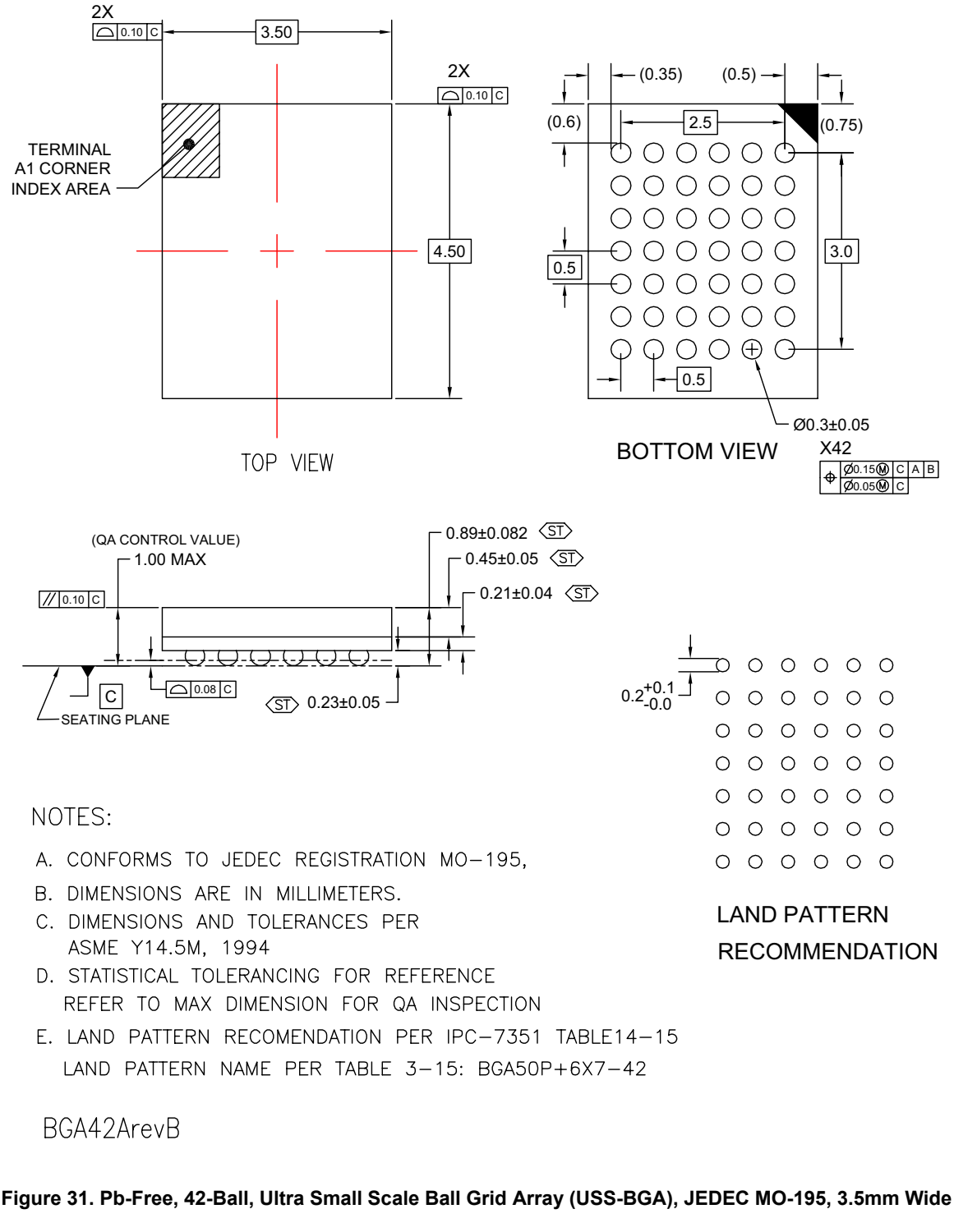


Tape Width	Dia A Max.	Dim B Min.	Dia C +0.5/–0.2	Dia D Min.	Dim N Min.	Dim W1 +2.0/–0	Dim W2 Max.	Dim W3 (LSL–USL)
8	330	1.5	13	20.2	178	8.4	14.4	7.9 ~ 10.4
12	330	1.5	13	20.2	178	12.4	18.4	11.9 ~ 15.4
16	330	1.5	13	20.2	178	16.4	22.4	15.9 ~ 19.4

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Physical Dimensions

Dimensions are in millimeters unless otherwise noted.



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO−195,

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

D. STATISTICAL TOLERANCING FOR REFERENCE REFER TO MAX DIMENSION FOR QA INSPECTION

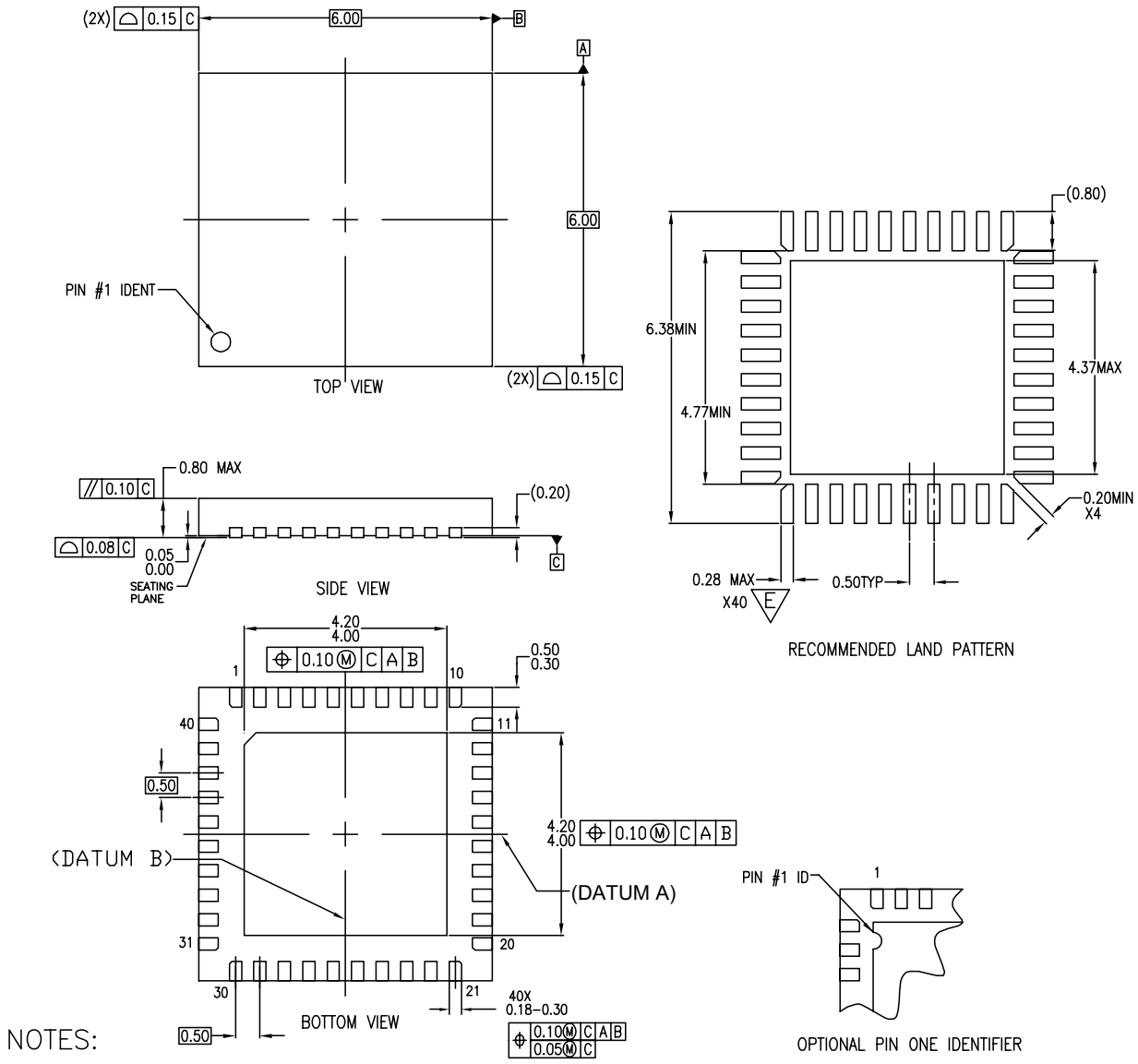
E. LAND PATTERN RECOMENDATION PER IPC−7351 TABLE14−15 LAND PATTERN NAME PER TABLE 3−15: BGA50P+6X7−42

BGA42ArevB

Figure 31. Pb-Free, 42-Ball, Ultra Small Scale Ball Grid Array (USS-BGA), JEDEC MO-195, 3.5mm Wide

Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-220, VARIATION WJJD-2 WITH EXCEPTION THIS IS A SAWN VERSION.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER

D. LAND PATTERN PER IPC SM-782 FABRICATION AND ASSEMBLY TOLERANCES OF 0.1 MM APPLIED

E. WIDTH REDUCED TO AVOID SOLDER BRIDGING.

G. DIMENSIONS ARE NOT INCLUSIVE OF BURRS, MOLD FLASH, NOR TIE BAR PROTRUSIONS.

MLP40Arev2

Figure 32. Pb-Free, 40-Terminal, Molded Leadless Package (MLP), Quad, JEDEC MO-220, 6mm Square

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CROSSVOLT™	*i-Lo*™	POP™	SuperSOT™-3	
DOME™	ImpliedDisconnect™	Power247™	SuperSOT™-6	
EcoSPARK™	IntelliMAX™	PowerEdge™	SuperSOT™-8	
E^2CMOS™	ISOPLANAR™	PowerSaver™	SyncFET™	
EnSigna™	LittleFET™	PowerTrench®	TCM™	
FACT™	MICROCOUPLER™	QFET®	TinyBoost™	
FAST®	MicroFET™	QS™	TinyBuck™	
FASTr™	MicroPak™	QT Optoelectronics™	TinyPWM™	
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FRFET™	MSX™	RapidConfigure™	TinyLogic®	
	MSXPro™	RapidConnect™	TINYOPTO™	
Across the board. Around the world.™		µSerDes™	TruTranslation™	
The Power Franchise®		ScalarPump™	UHC™	
Programmable Active Droop™				

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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Rev. I20

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